219th ECS Meeting

Resistive switching behaviors of ReRAM having W/CeO_2/Si/TiN structure

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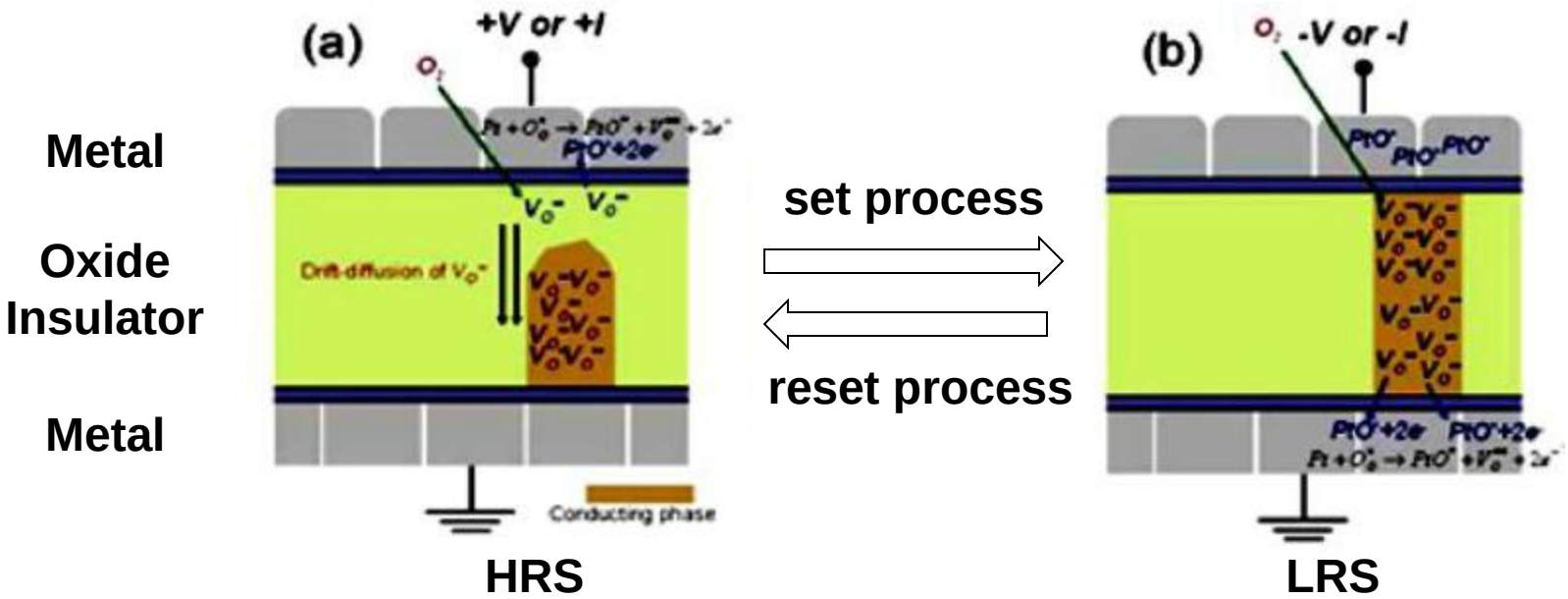
Introduction of Resistive RAM (ReRAM)

- Resistive switching behaviors & conductive filament model



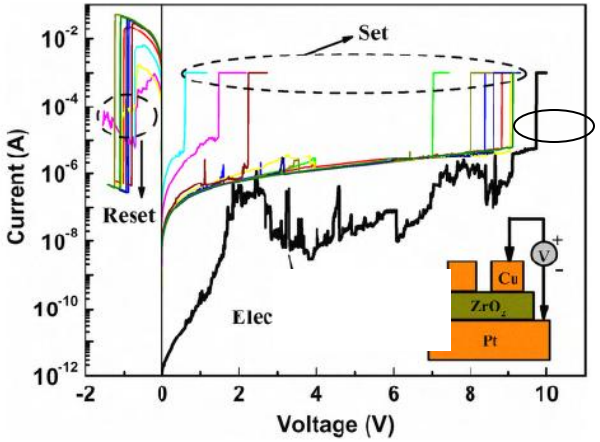
Example: Pt/TiO$_2$/Pt [1]

- Advantages of ReRAM
  - ➢Non-volatility
  - ➢Low consumption
  - ➢High speed
  - ➢Simple MIM structure
  - ➢Compatibility with CMOS process
  - ➢Great potential of scaling

ReRAM is a promising candidate for the next generation non-volatile memory

Challenges faced by ReRAM

- Elimination of electrical forming process with high voltage



Resistive switching of $Cu/ZrO_2/Pt$ ReRAM device[2]

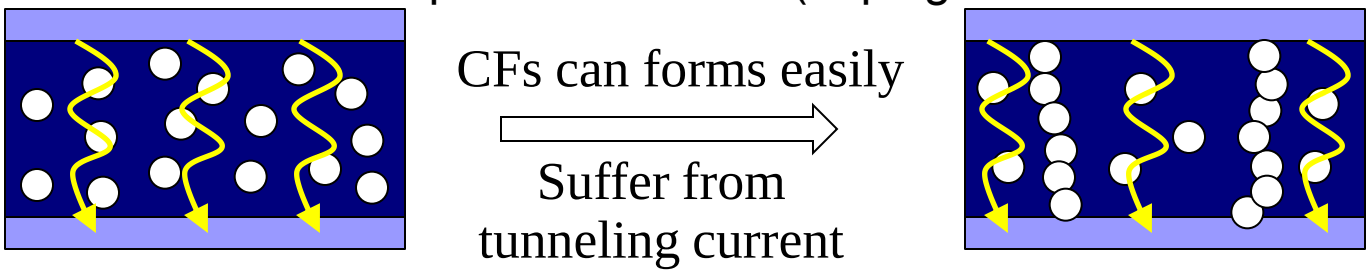
Forming process:

1) Increase external circuit complexity

2) Degrade stability of the device

- Reported proposals for eliminating forming process

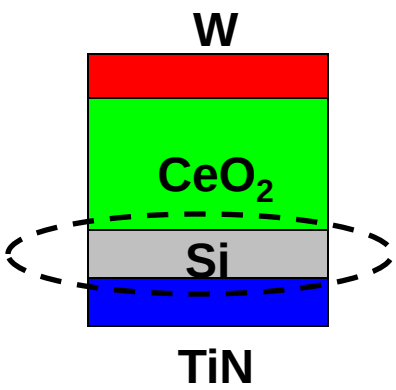
→ Introduction of vacancies/traps into materials (doping[3] or nonstoichiometric materials[4])



ReRAM still calls for new materials technology for eliminating forming process

Purpose of this study

1. Instead of fundamental change of material properties, modulate forming process by interface engineering



Changeable valence number (Ce^{3+} and Ce^{4+})
→ easily generate and eliminate oxygen vacancies [5]

Fluorite structure
→ High conductivity of oxygen ions

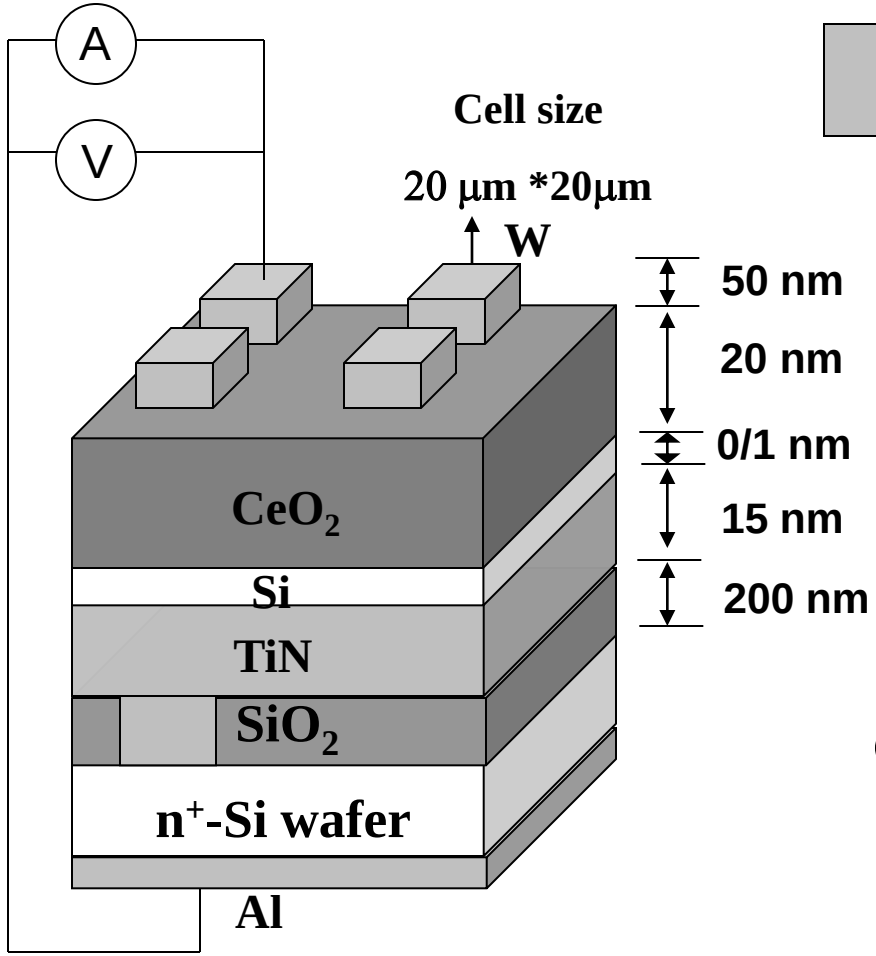
Reactivity with Si to form amorphous Ce-silicate[6]
→ Source of oxygen vacancies

2. By modeling resistive switching behaviors (reset process) of the device, provide a guideline for controlling operation parameter.

Part I: Modulation of forming process of CeO_2 ReRAM by incoporating Si buffer layer

1. Device structure and fabrication
2. Resistive switching properties
3. The effect of Si buffer layer
4. Proposed model for Si buffer layer

Device structure and fabrication

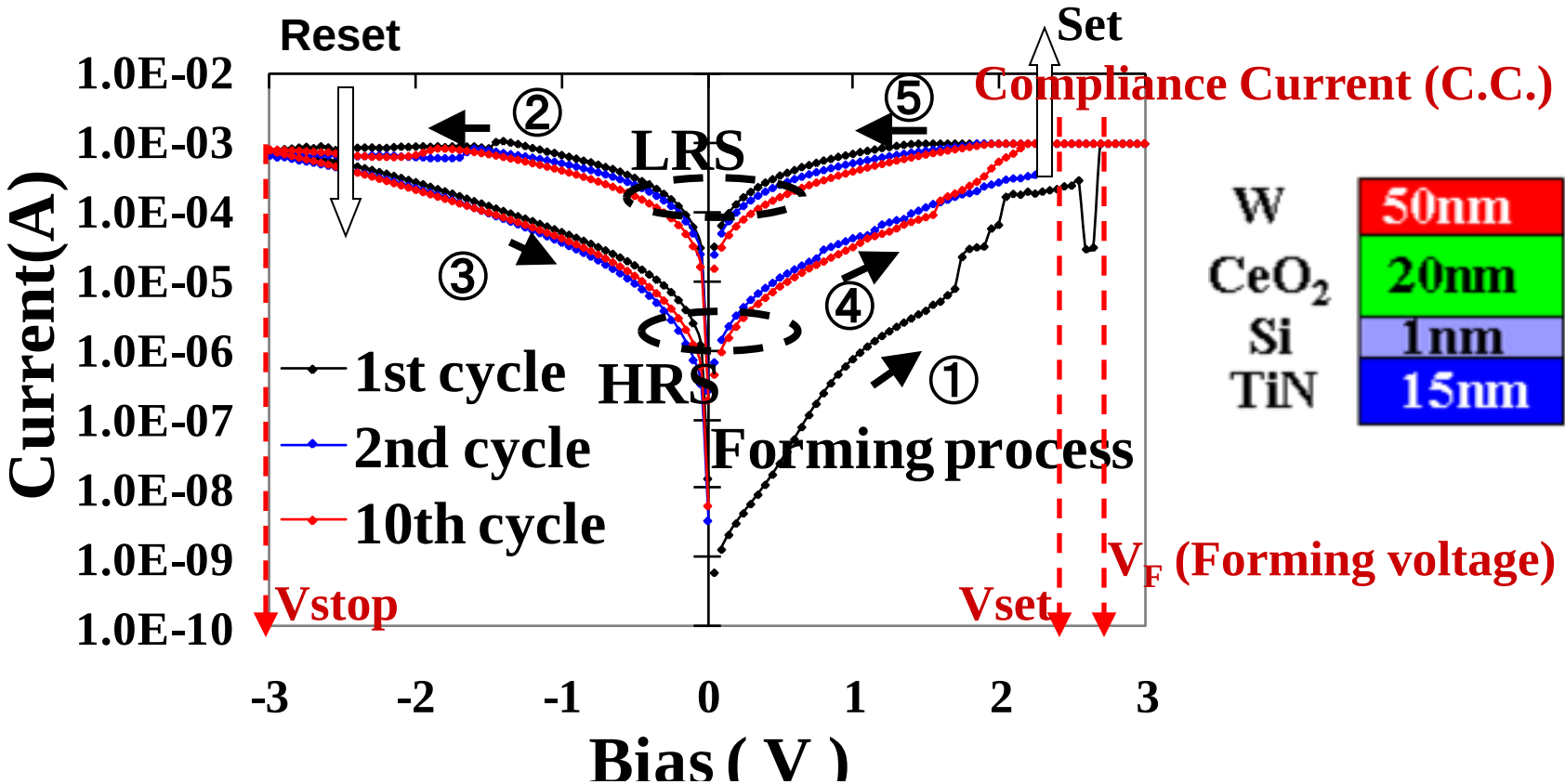


Materials and structure are suitable for practical application

n^+-Si wafer (0.02 < W cm)

- Cleaning (SPM + DHF)
- Growth of SiO_2 insulator (thermal oxidation)
- Patterning contact window
- Deposition of TiN bottom electrode (RF sputter)
- Deposition of Si buffer layer (RF sputter)
- Deposition of CeO_2 switching layer (electron beam)
- Deposition of W top electrode (RF sputter)
- Electrode patterning process
- Evaporation of Al back contact
- Annealing 400°C, 30s, N_2

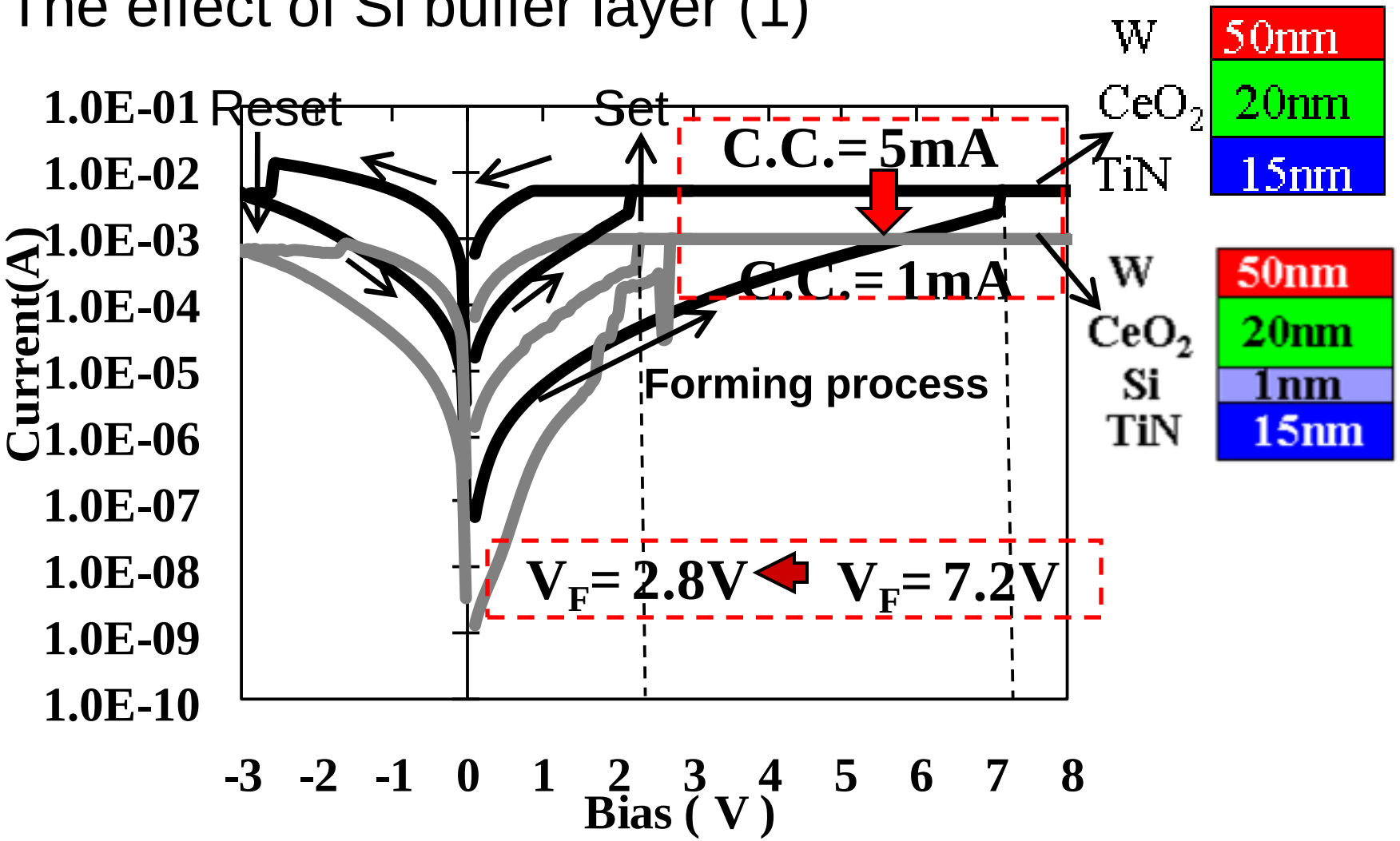
Typical resistive switching behavior of the device



I-V characteristics of W/CeO_2/Si/TiN under sweeping voltage

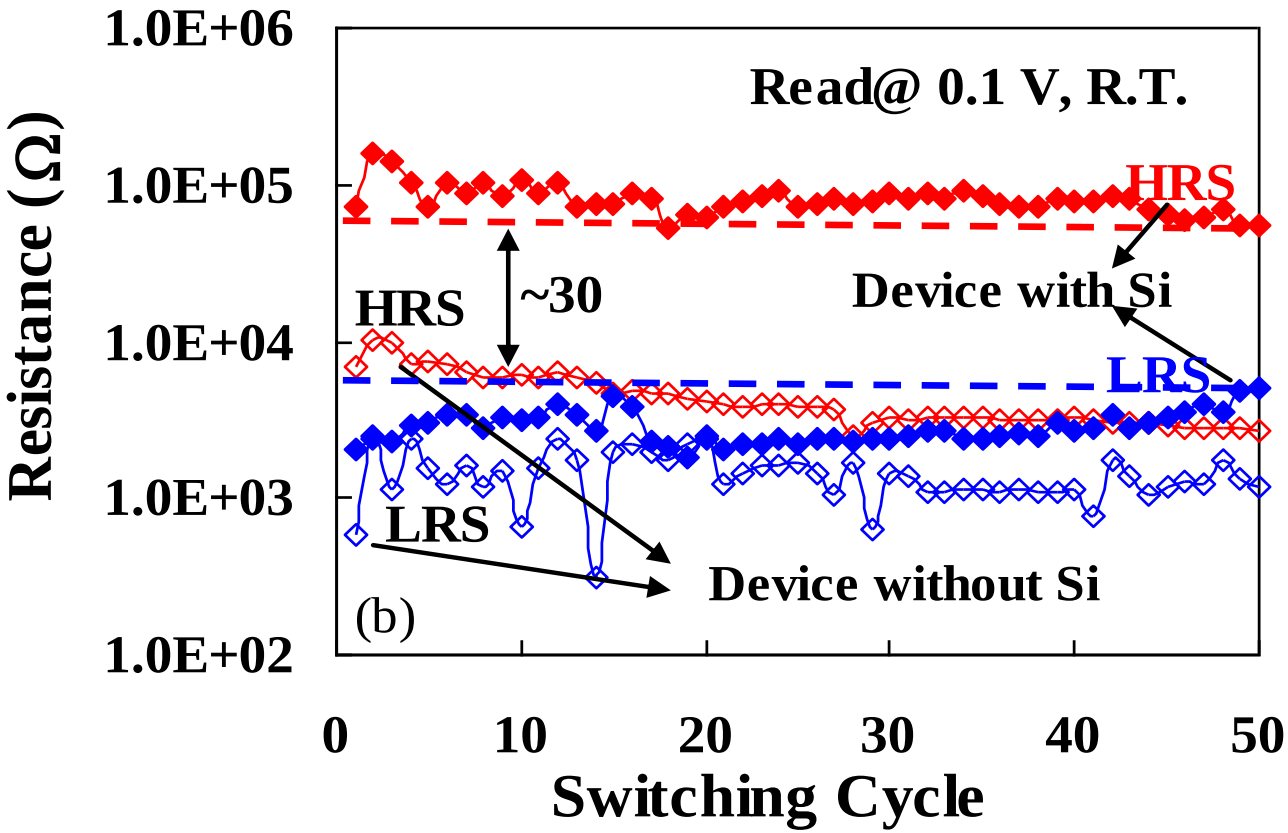
W/CeO_2/Si/TiN shows bipolar resistive switching behaviors without requiring a high forming voltage

The effect of Si buffer layer (1)



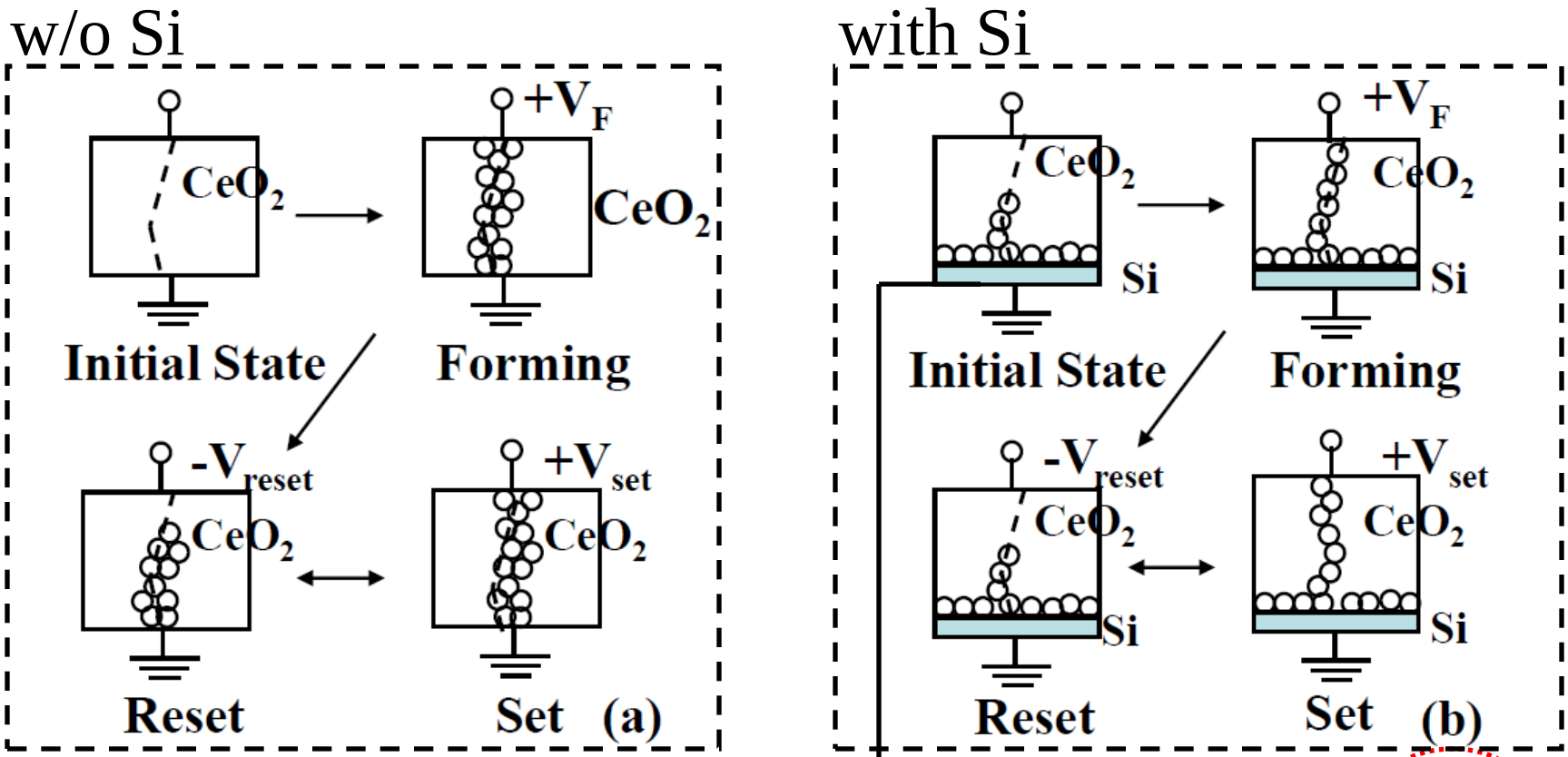
The device with Si buffer layer can finish forming process at lower voltage, and thus work under lower C.C.

The effect of Si buffer layer (2)



The device with the Si layer shows larger memory window, better endurance characteristic and also has been better protected from hard breakdown.

Proposed model for Si buffer layer



$CeO_2 + Si \rightarrow CeSiO_4 + 2Vo^{\cdot\cdot}$

$Ce_2O_3 + Si \rightarrow Ce_2SiO_5 + 2Vo^{\cdot}$

By formation of Ce-silicate, the Si buffer layer induces additional oxygen vacancies into the CeO_2 film, which help CFs form more easily

Summary of the effect of Si buffer layer

Si buffer layer

forming Ce-silicate

& introducing o.v.

⇨

Effectively decrease the forming voltage

Protect device from hard breakdown

Decrease Compliance Current

Formation weaker filament easily to fracture

⇨

1)Enlarged window

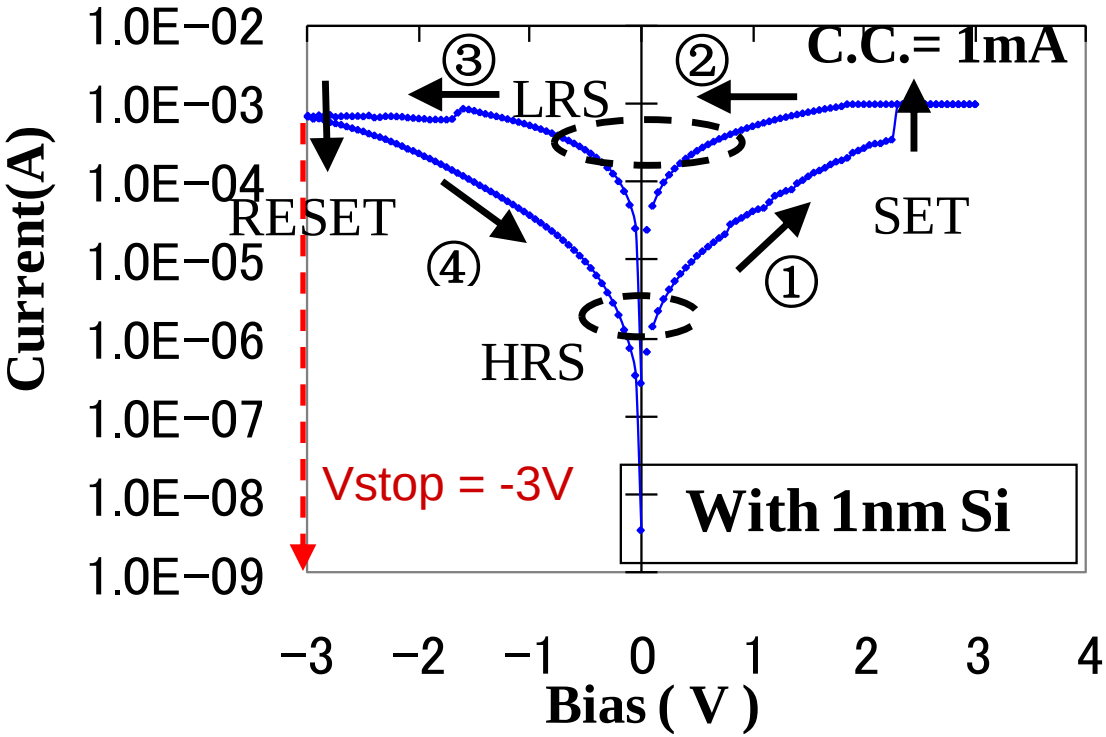
2) improved endurance characteristics

3) decrease power consumption

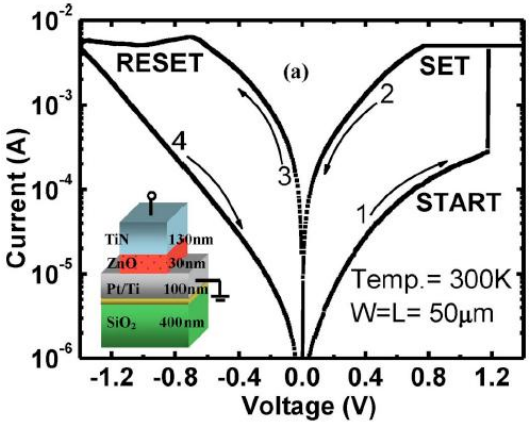
Part II: Modeling resistive switching behaviors of the device (reset process)

1. Influence of Vstop on resistive switching of the device
2. Modeling the reset process

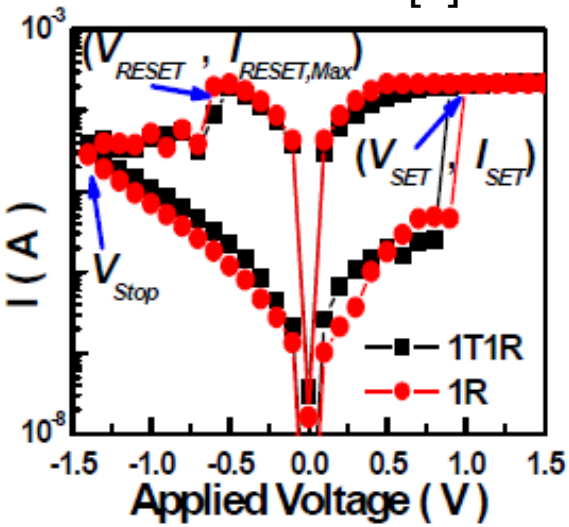
The motivation for modeling reset process



Typical resistive switching of W/CeO_2/Si/TiN



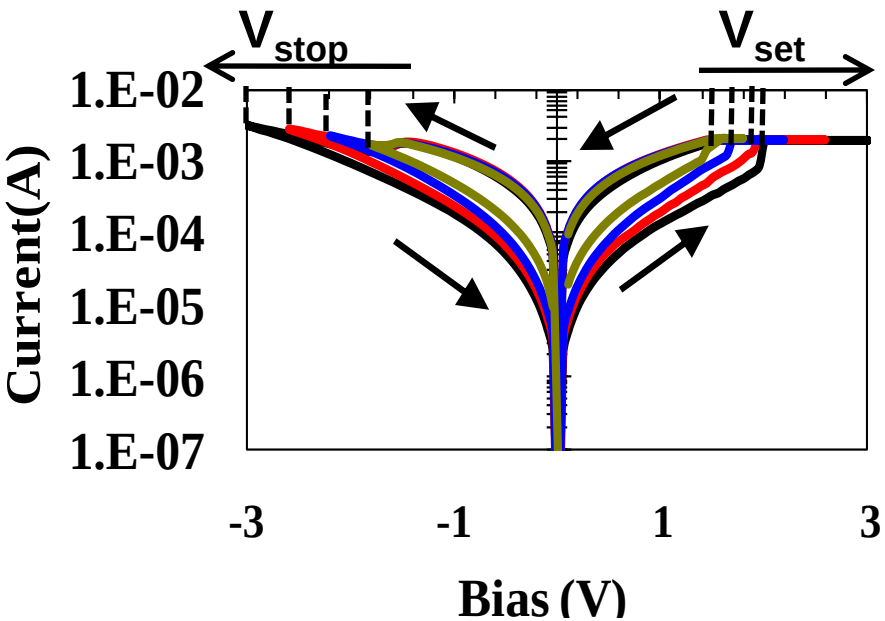
TiN/ZnO/Pt [7]

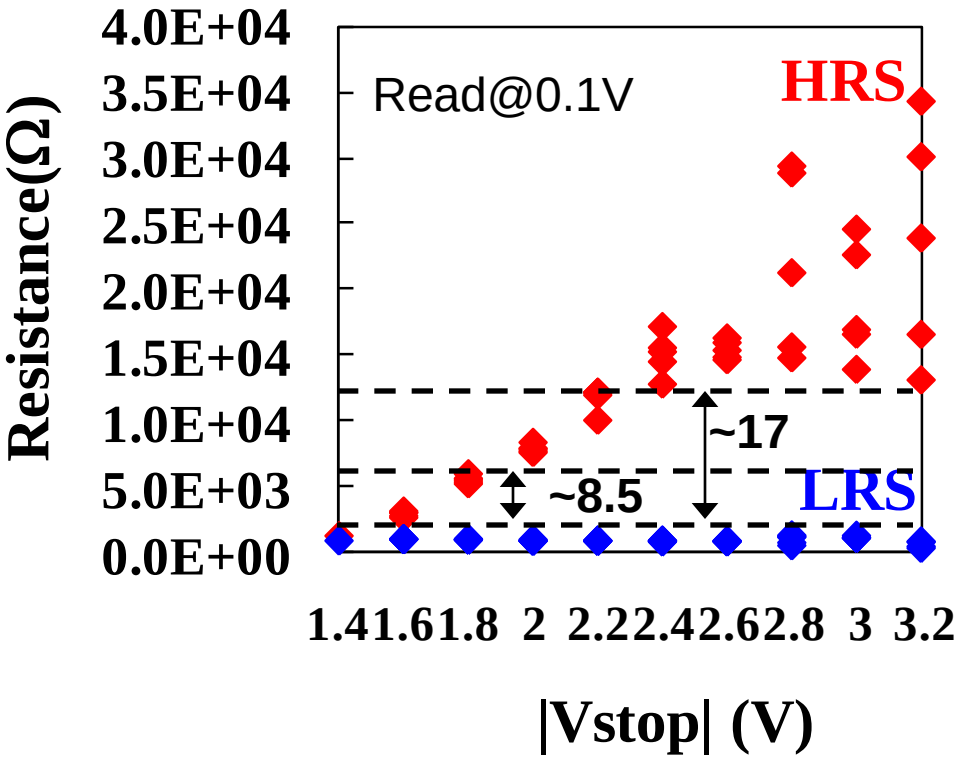


TiN/TiOx/HfO_2/TiN [8]

The device shows a gradual reset process that depends on V_{stop}, which is still lack of in-depth understanding.

Vstop dependent resistive switching of W/CeO_2/Si/TiN

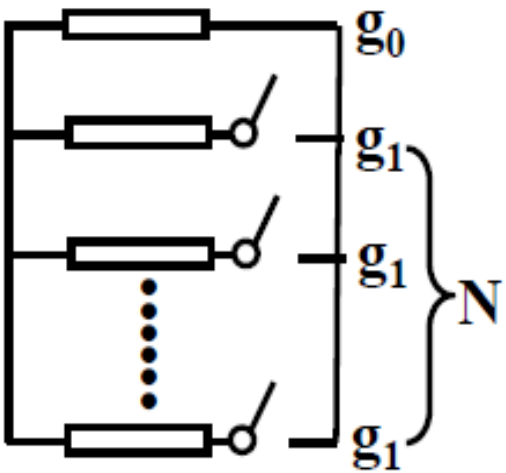




1. **Larger V_{stop} can reset the device to higher HRS. However, performance instability also increases.**
2. **The device has the potential of multi-level storage by controlling V_{stop}.**

Modeling the ratio of ruptured filaments on reset process

Parallel resistors model for ReRAM devices based on multiple CFs mechanism



g_0: the conductance of the CeO_2 thin film before resistive switching

g_1: the conductance of the each filament.

$g_0 << g_1$

Conductance of ON state:

$$G_{ON} = g_0 + N \times g_1 \approx N \times g_1$$

Number of filaments ruptured at certain V_{stop} : $n(V_{stop})$

Conductance of OFF state

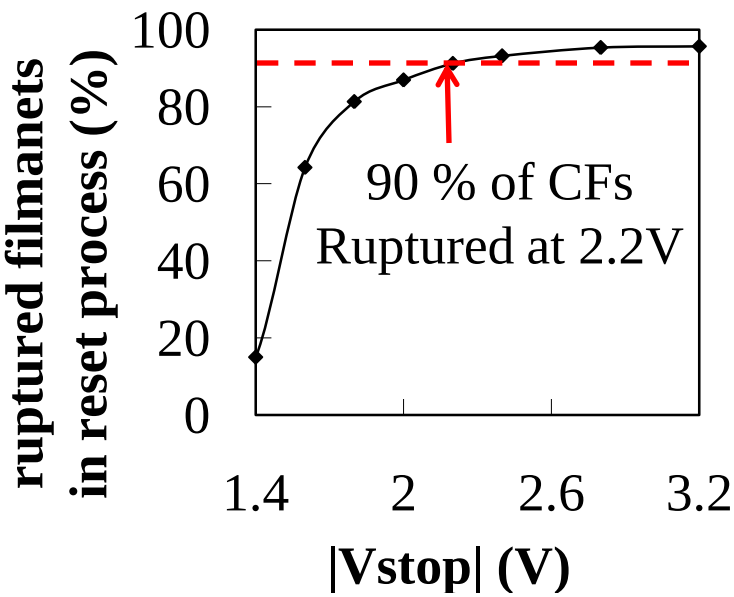
$$G_{OFF} = g_0 + (N - n(V_{stop})) \times g1$$

$$\approx (N - n(V_{stop})) \times g1$$

The ratio of ruptured filaments in reset process:

$$n(V_{stop})/N = 1 - G_{OFF}/ G_{ON}$$

Ratio of ruptured CFs on reset process:



Vstop ↑ → Enlarging window

Vstop ↓ → Decrease power consumption & increase device stability

⇨ The device performance can be further optimized by controlling Vstop

1. Once the reset process begins, most part of filaments facture rapidly in a short range of voltage.
2. Providing a guideline for maximum of device performance by controlling V_{stop}.

Summary

1. Successful improvement of performance CeO_2 ReRAM by incorporating a Si buffer layer at bottom interface. (forming voltage, window, endurance and power consumption)

2. The effect of the Si buffer layer is attributed to the formation of silicate, which serves as a source of oxygen vacancies.

3. V_{stop} dependent reset process of the device is investigated, and a guideline for V_{stop} control is provided.

Reference

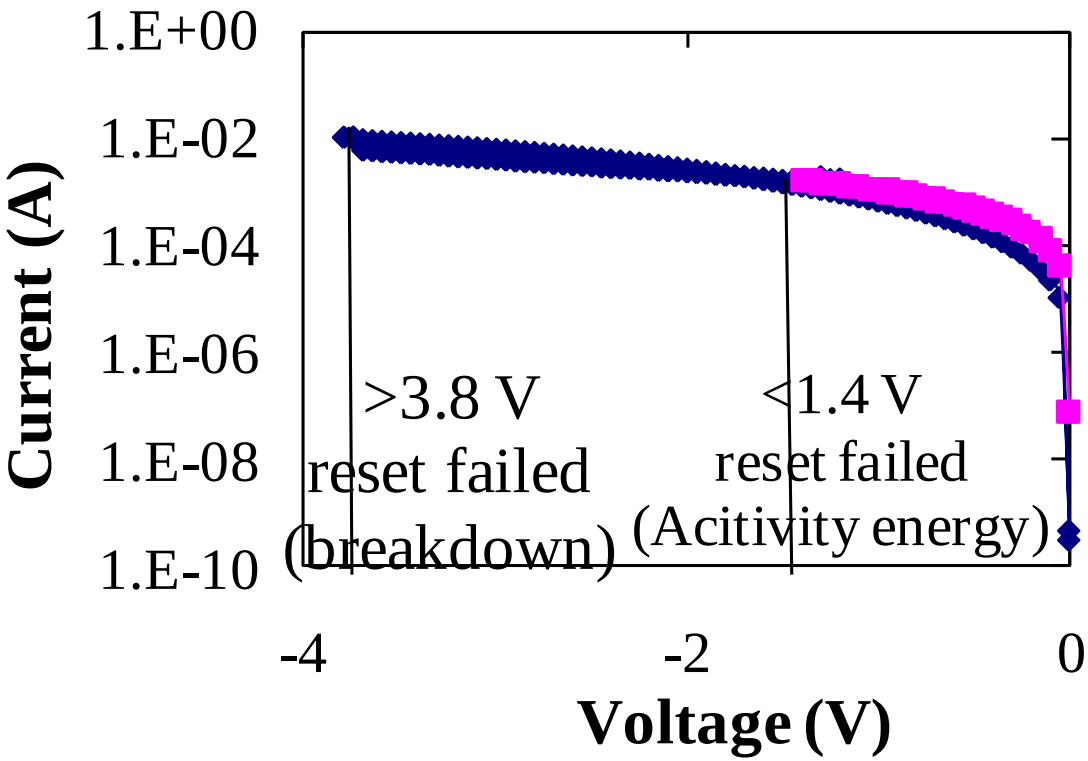
1. R. Waser and M. Aonom, Nature Materials. **6**, 833 (2007)
2. Q. liu, et, al. , 2009. **ESSDERC**
3. Q. Liu, W.Guan, S.Long, R.Jia, and M.Liu, Appl. Phys. Lett. 92, 012117 (2008)
4. X. Sun, B. Sun, L. Liu, N. Xu, X. Liu, R. Han, J. Kang, G. Xiong and T, P. Ma, IEEE Electron Device Lett. **30**, 4 (2009)
5. F. Esch, et. al, Science, **309**, 752-755 (2005)
6. K.Shubhakar, et. al, APL, **98**, 072902 (2011)
7. N. Xun, et. al, APPLIED PHYSICS LETTERS **92, 232112 2008**
8. L. Goux, et. al, APPLIED PHYSICS LETTERS **97, 243509 2010**

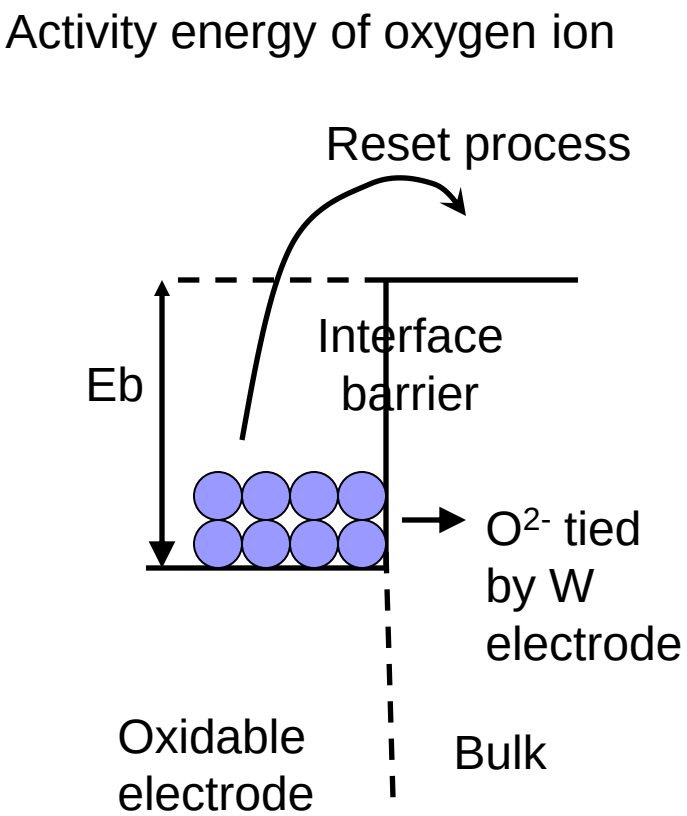
Thank you very much!

Welcome for comments and questions

Back up materials

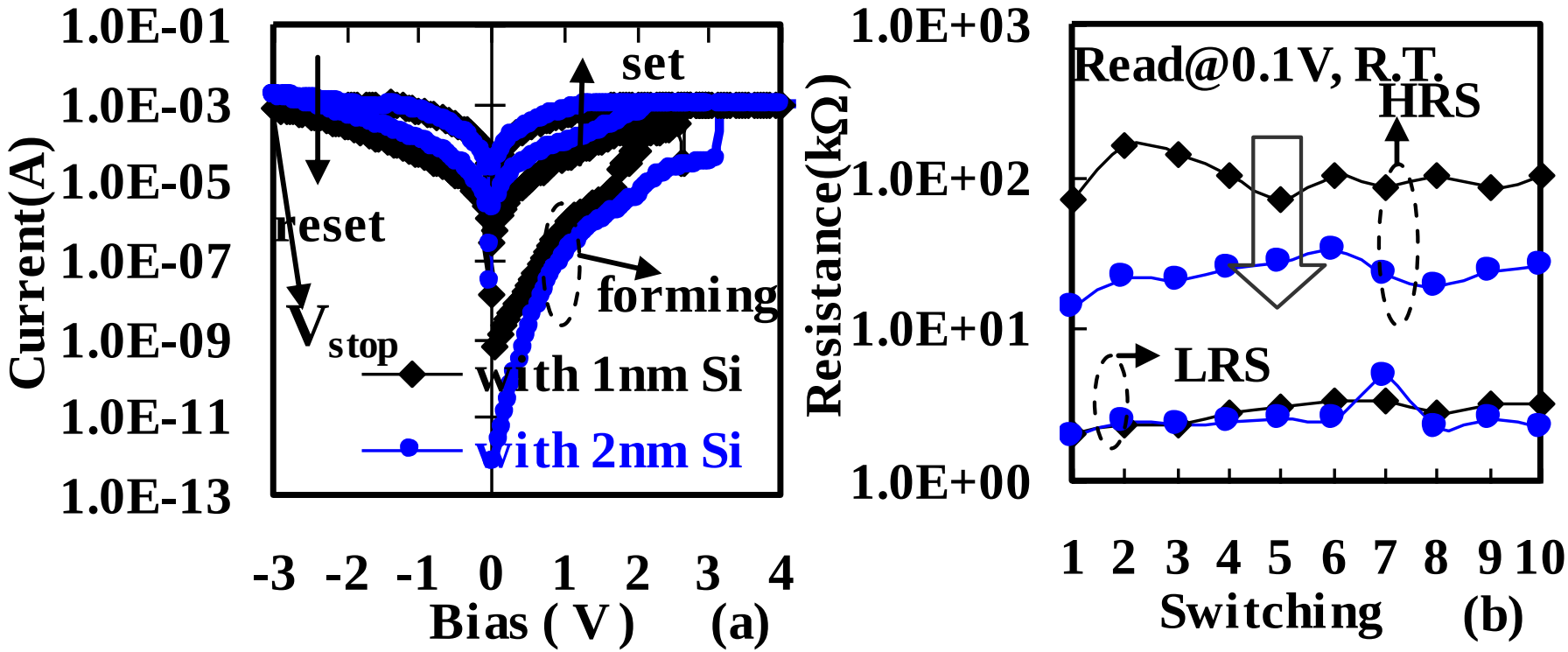
The range of Vstop for effective reset process

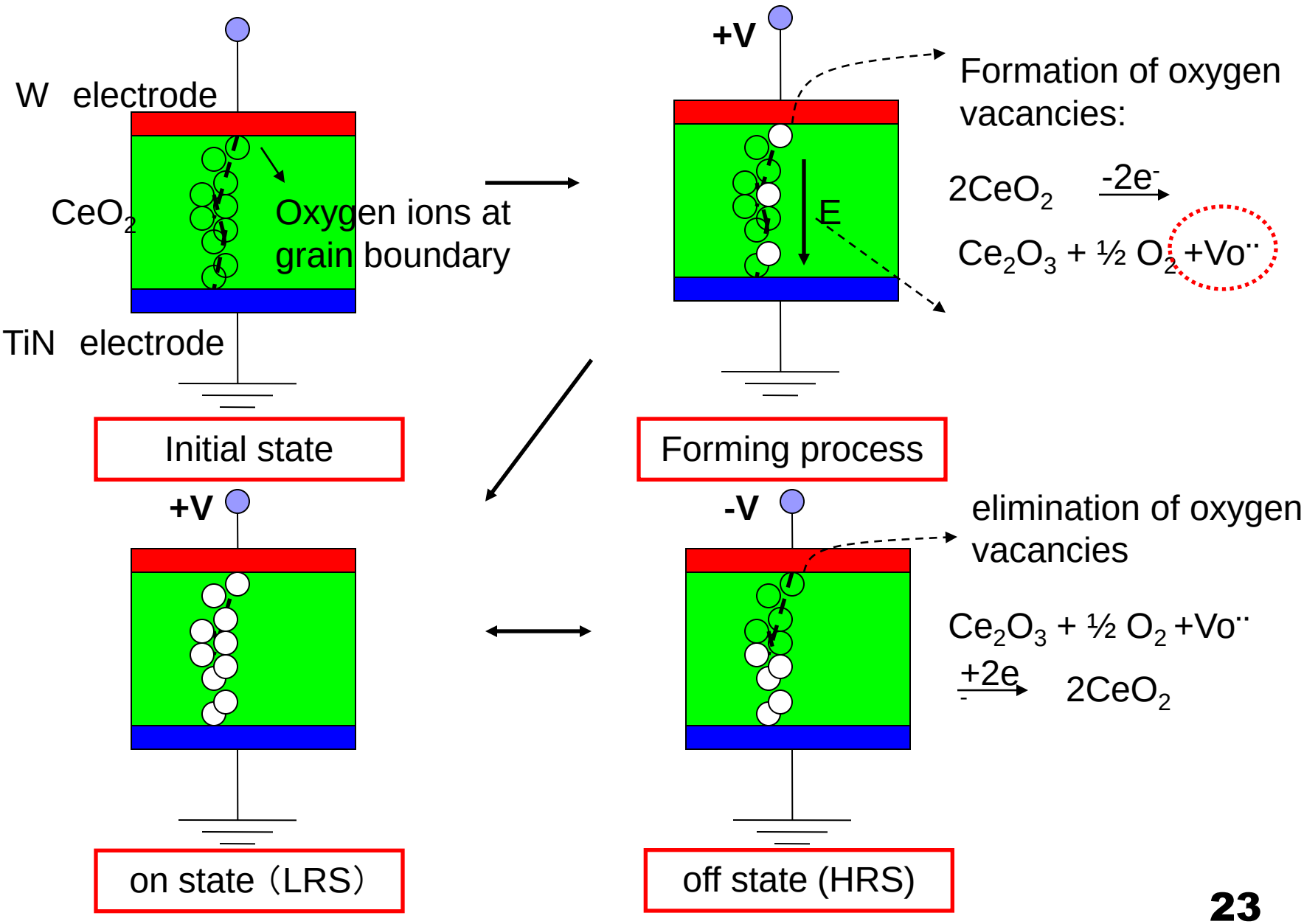




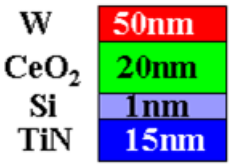
The maximum of |Vstop| is limited by breakdown while the minimum possibly comes from activity energy of oxygen ion.

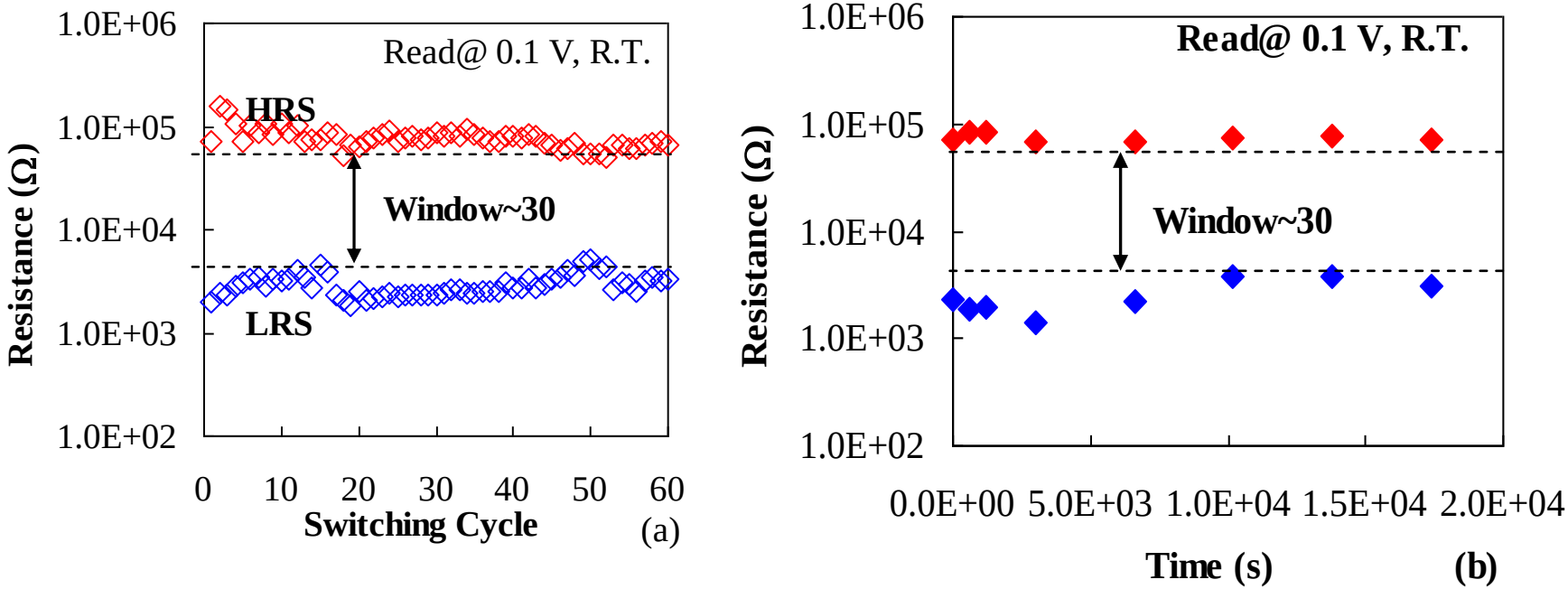
Thickness effect of the Si buffer layer




W electrode
CeO_2
Oxygen ions at grain boundary
TiN electrode
Initial state
+V
E
Formation of oxygen vacancies:
$2CeO_2 \xrightarrow{-2e^-} Ce_2O_3 + ½ O_2 + Vo^{\cdot\cdot}$
Forming process
+V
on state（LRS）
-V
elimination of oxygen vacancies
$Ce_2O_3 + ½ O_2 + Vo^{\cdot\cdot} \xrightarrow{+2e^-} 2CeO_2$
off state (HRS)

Endurance and Retention characteristics

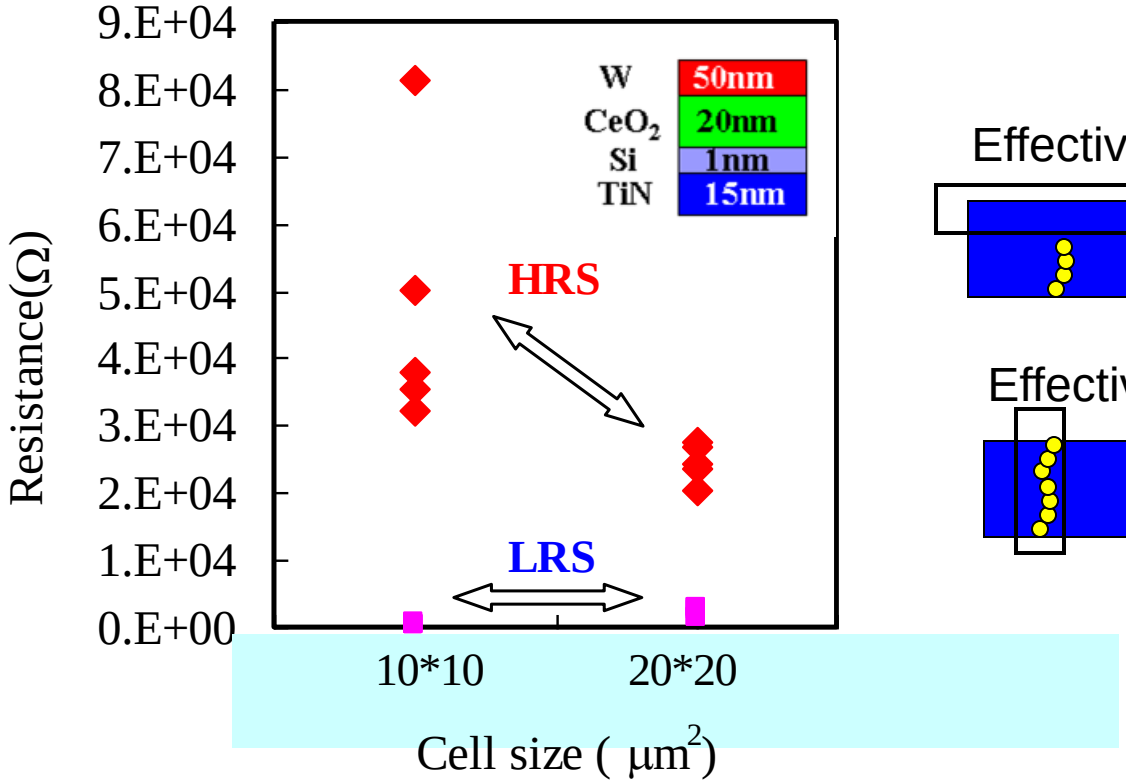


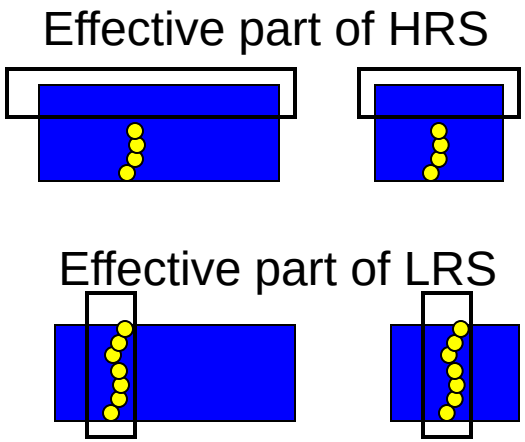


(a) Endurance and (b) retention characteristics of the device

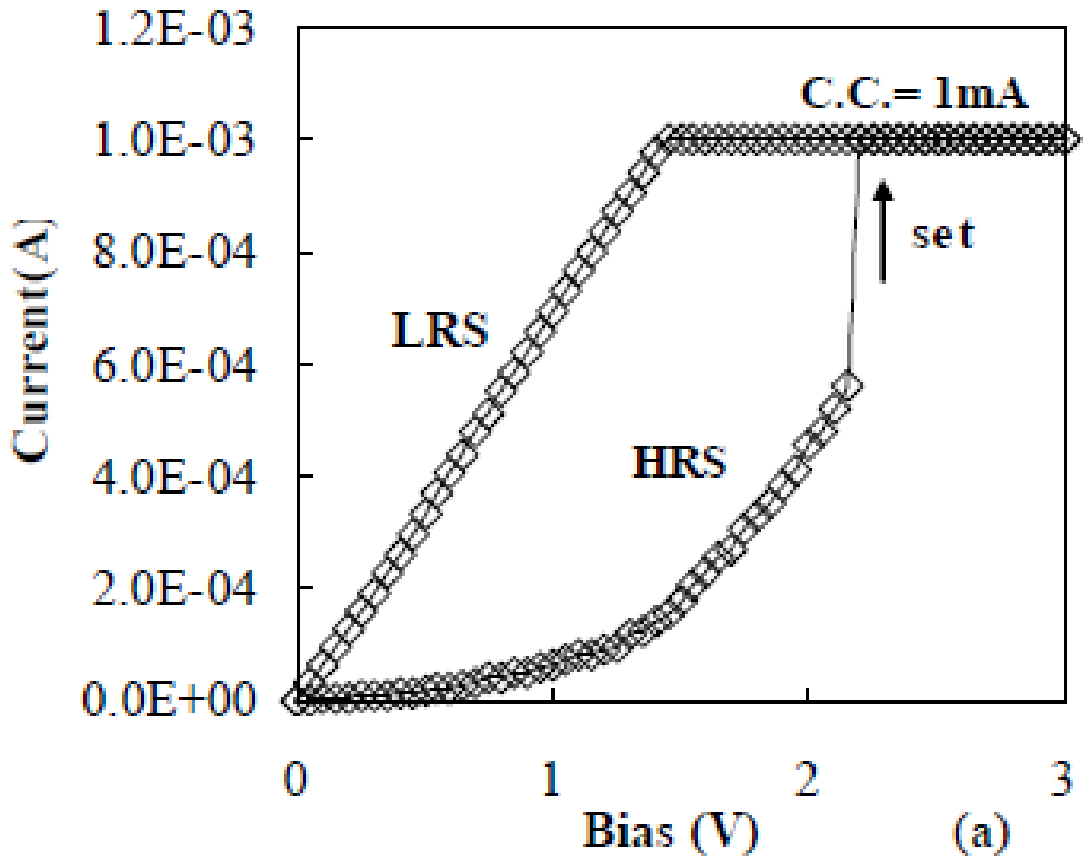
1) HRS and LRS has a ratio (window) of 30 even after 60 times cycling
2) The ration doesn't degrade after 5hrs.

Size dependence effect in resistive switching



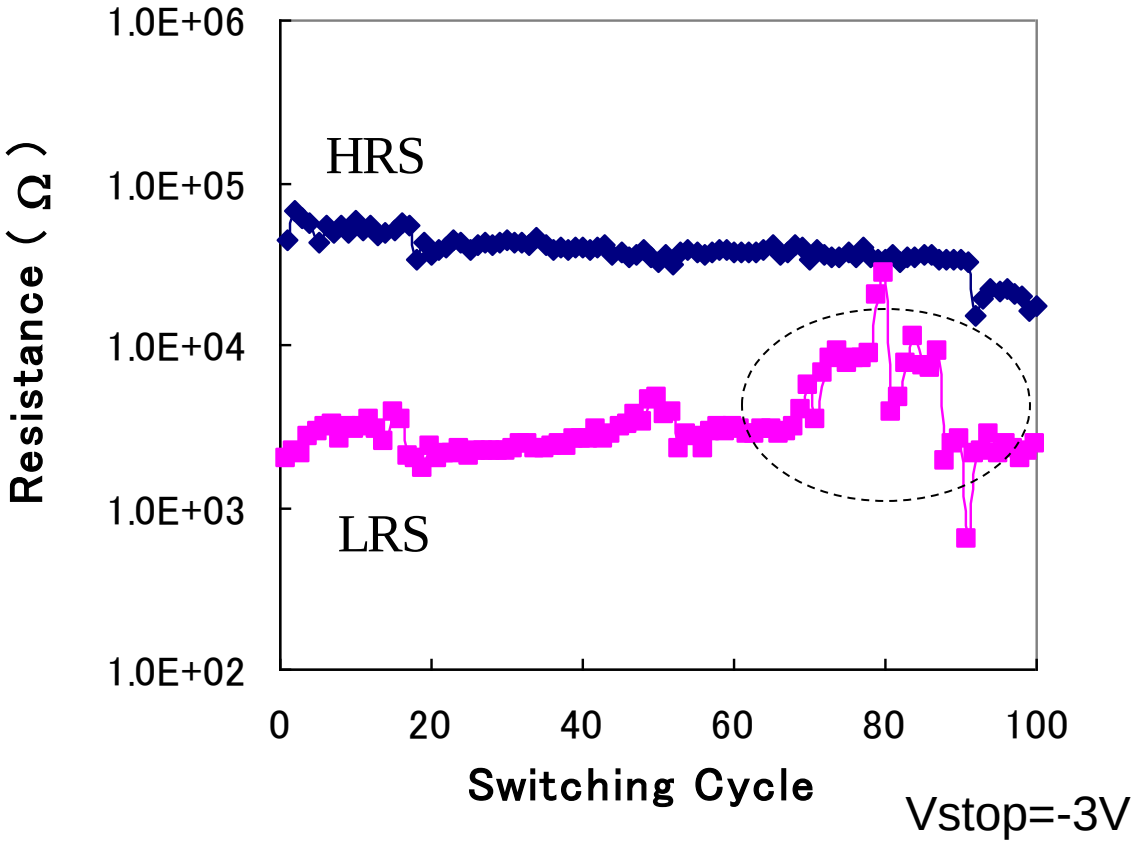


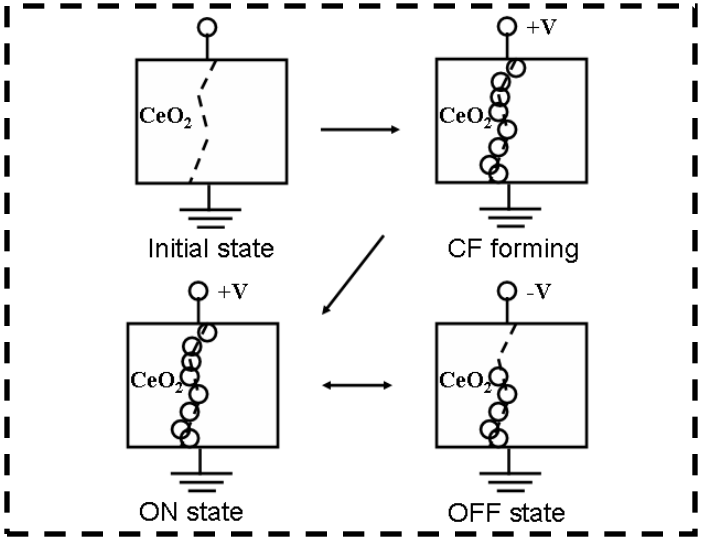
1. Weaker dependence on size of LRS matches filament mechanism
2. Potential for further scaling

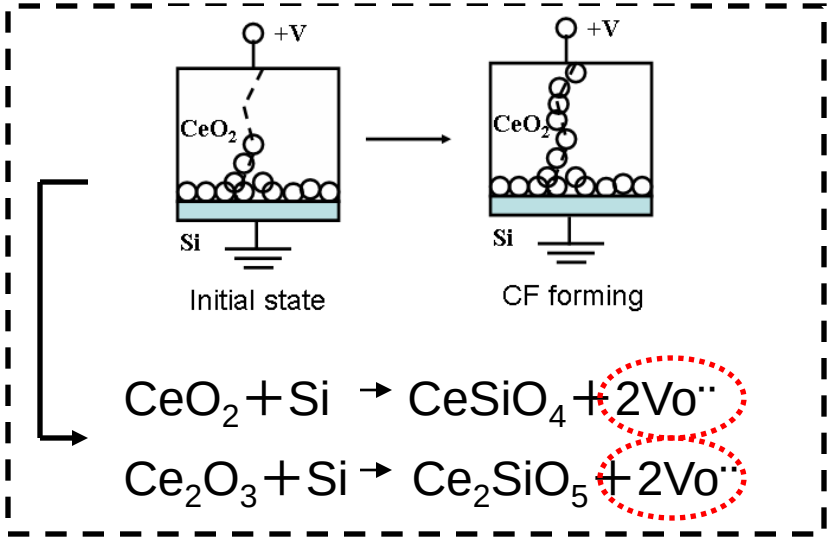


I-V curve of set process in linear scale

Adjustment of device performance by control of Vstop



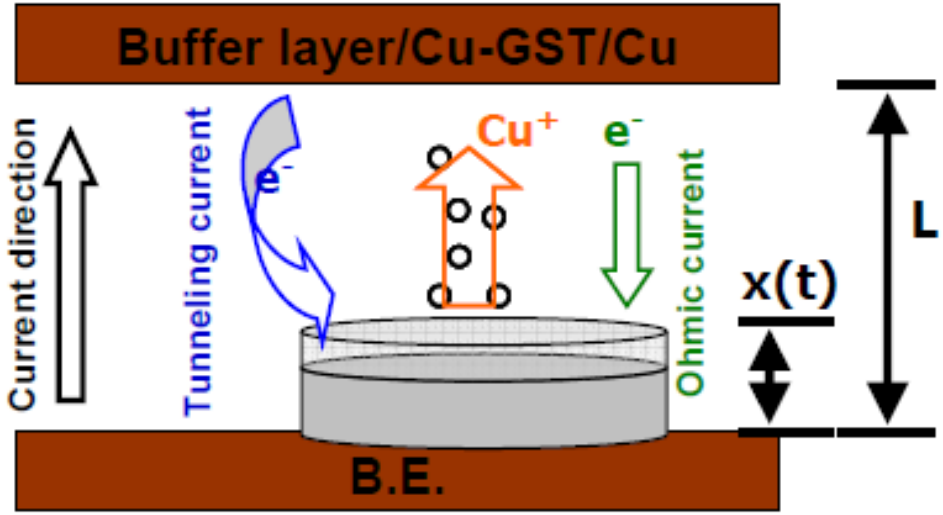


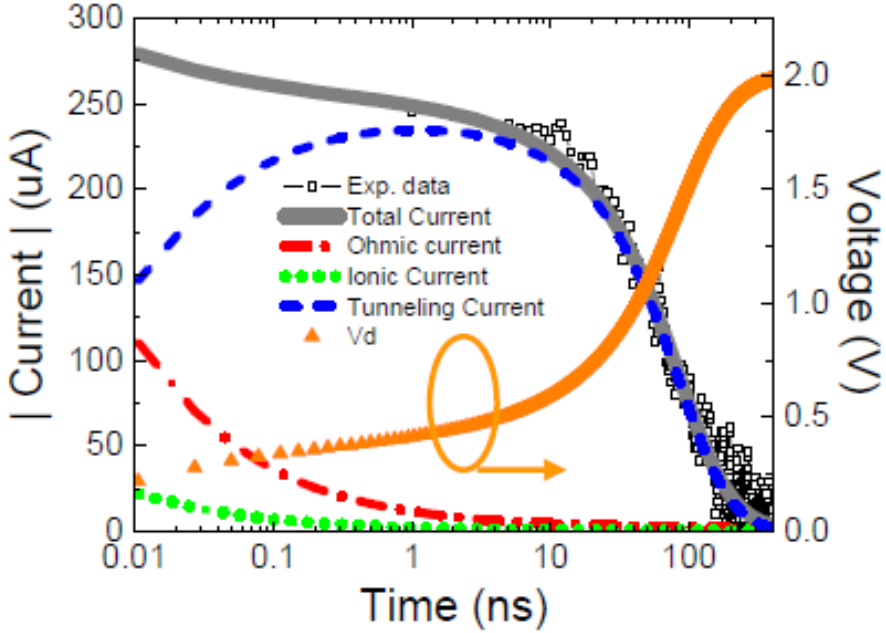


1. Mars and van Krevelen (MvK) mechanism: When an adsorbate is oxidized at the surface, the oxidant is often a surface lattice oxygen atom, thus creating a surface oxygen vacancy. *
2. Surface oxygen vacancies of ceria may tend to rearrange to chain configuration at high temperature.*
3. More defects generate at HK/silicon interface. **

* F. Esch, et. al, Science, **309**, 752-755 (2005)

** D.S. Ang, et, al, Appl. Phys. Lett. 92, 192904 (2008)





Yu-Yu Lin, et.al IEDM 2010

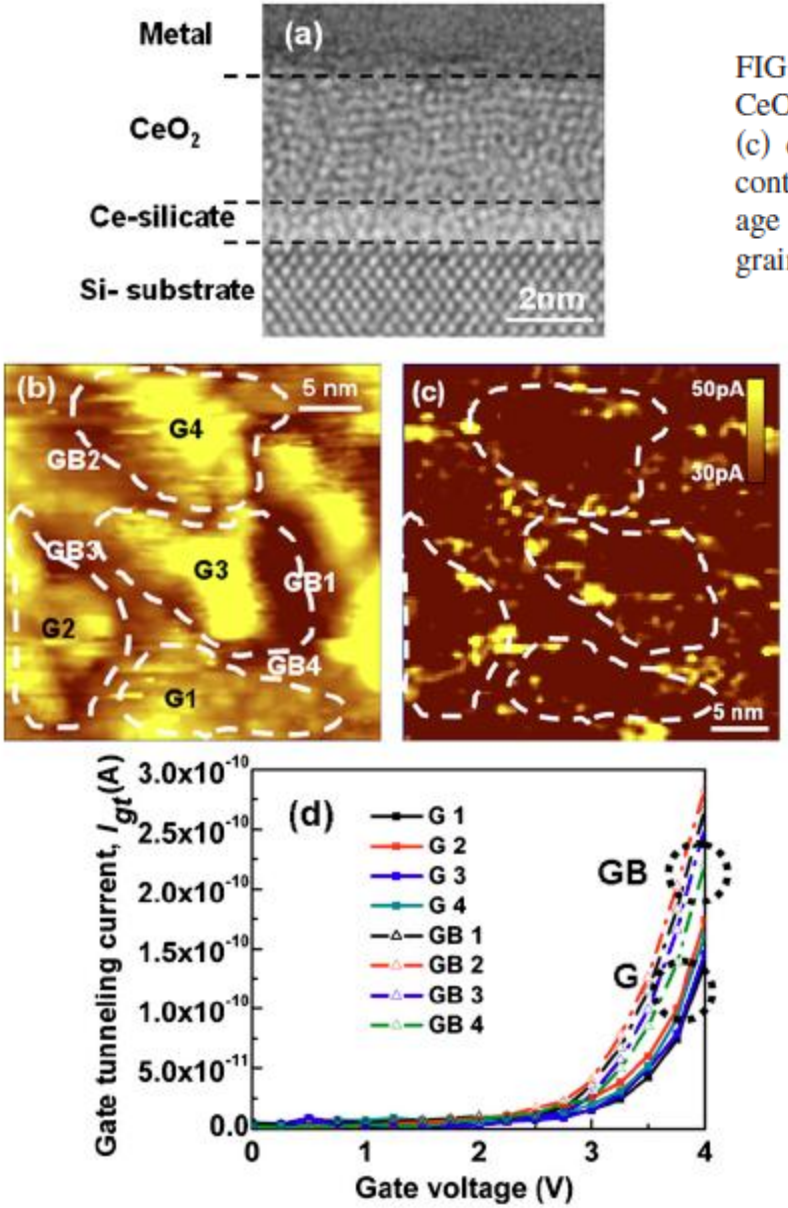


FIG. 1. (Color online) (a) Cross-sectional TEM micrograph of ~4 nm CeO_2/Ce-silicate/Si structure. (b) STM topography (at +3 V, 30 pA) and (c) corresponding CITS image at +3.5 V, indicating the grain boundary contours. (d) *I-V* characteristics at grain and GB locations. More gate leakage current is observed at GB locations (GB1–GB4) compared to that of grain (G) locations (G1–G4).

K.Shubhakar, et. al, APL, 98, 072902 (2011)