Observation of Tunneling FET operation in MOSFET with NiSi/Si Schottky source/channel interface

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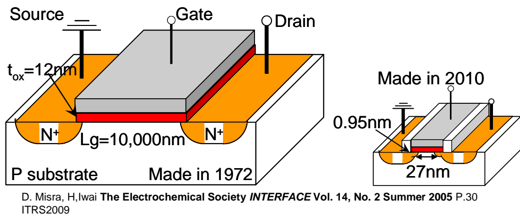

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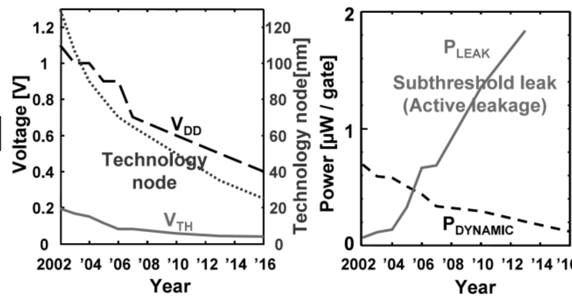
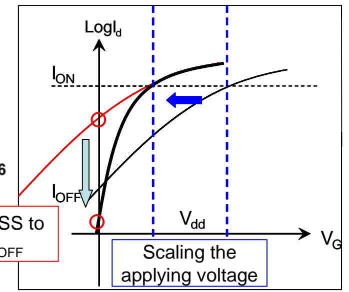
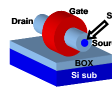
Scale (t_{ox}, L, W)	V, I, Delay	Power
1/K	1/K	1/K²



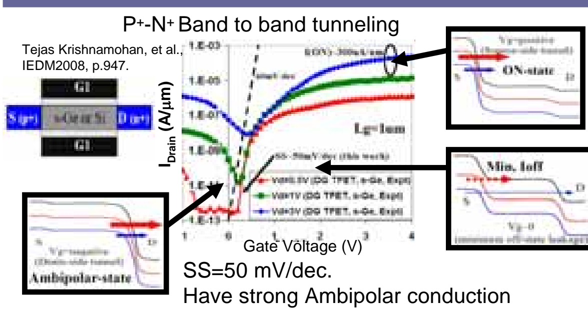




・UTSOI & high-k Technology
・GAA, Nanowire architecture } Subthreshold slope≧60 [mV/dec] (@RT)

・new process or new principle

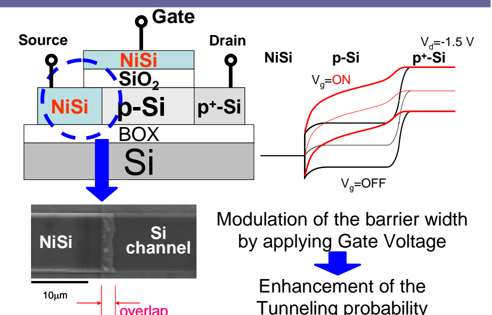
P+-N+ Band to band tunneling



SS=50 mV/dec.
Have strong Ambipolar conduction

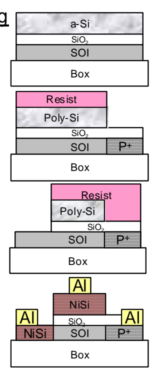
Tunneling Current
silicide
Si
silicide
Source
channel
Drain

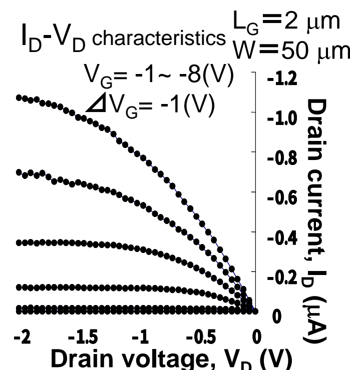
✓Lowering parasitic resistance
→ Larger ON Current
✓Can modulate Schottky Barrier
→ Device design is flexible
✓Metal/Si Source/Drain contact
→ Smaller short channel effect

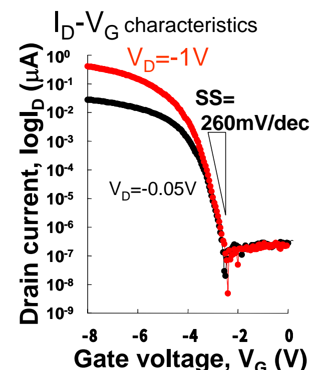


Modulation of the barrier width by applying Gate Voltage
Enhancement of the Tunneling probability

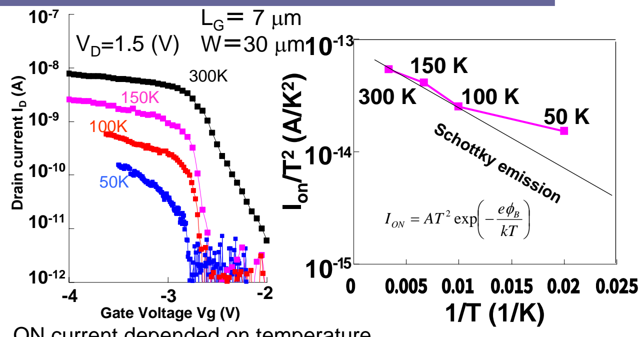
- p-SOI Active area pattering
- Gate oxide growth
- a-Si deposition
- Gate Etching1 (Drain)
- P+Area formation
  ion-implantation
- Gate Etching2(Souce)
- NiSi formation
  Ni sputtering annealing
- Formation of Al electrode



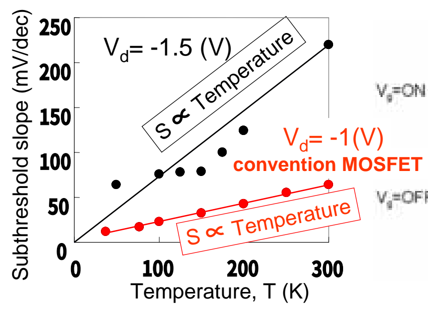


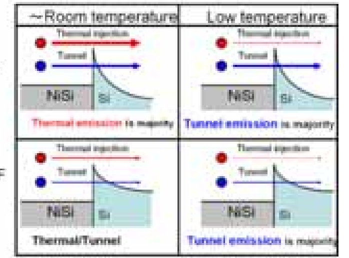


Good p-type transistor operation confirmed



ON current depended on temperature
→Thermal emission current was suppressed at low temperature (<~100K)





Subthreshold slope independence on temperature at <150K
→majority conduction mechanism is tunneling

Expression of schottky barrier tunneling current:

$$J = Jo\exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E_S}\right]$$

Decrease of
・ϕ_B : Schottky barrier heights (by silicide selection, impurity interface segregation)
・m* : effective mass (by strain, use other substrate types)
Increase of
・Es : electrical field at source edge (by larger dopant concentration)

Schottky barrier p-type transistor with NiSi source having appreciable encroachment under the gate region was successfully fabricated.

Tunneling component was confirmed through Low temperature operation of the transistor characteristics at around 150K.

Increase in On tunnel current is pursued through Schottky barrier modification, m* decrease or electric field increase at source edge region.