Characterization of carrier transport in vertically-stacked Si nanowire FETs

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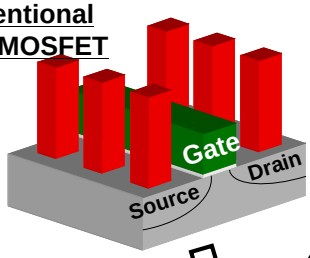
Motivation

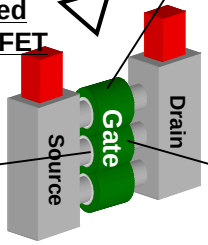
Performance of CMOS circuits

Circuit parameters		Device parameters
■ Power dissipation	→	■ Leakage current
■ Integration density	→	■ Device area
■ Switching speed	→	■ Drive current density

Conventional planer MOSFET



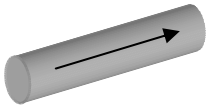
Vertically-stacked Si nanowire MOSFET



Gate-all-around

✓ Gate electrostatic control
✓ Short channel effect immunity

Nanowire channel



Carrier transport properties have been remained unclear...

Stacked channel

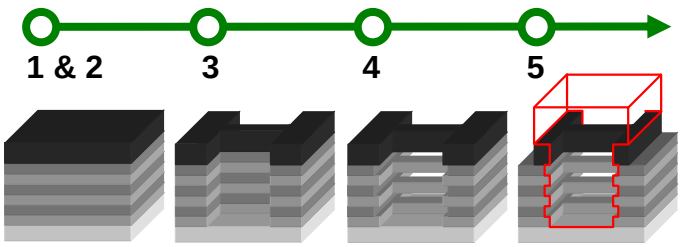
✓ Small device area
✓ High integration density

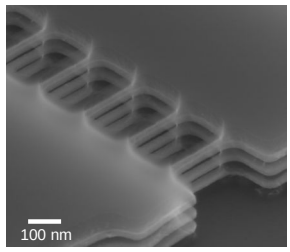
Purpose

To understand carrier transport properties in vertically-stacked Silicon Nanowire Transistors (SNWTs)

Device fabrication

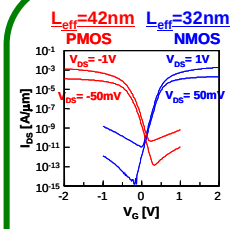
1. Si/SiGe superlattice selective epitaxy
2. Hard mask SiN deposition
3. Anisotropic etching of Si/SiGe layers
4. Isotropic etching of SiGe
5. Gate stack deposition
6. Gate patterning
7. Implantation
8. Nitride spacers

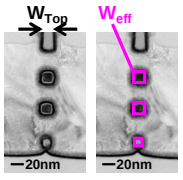




Results

Basic characteristics





W_{eff} ~ 8.5 x W_{Top}

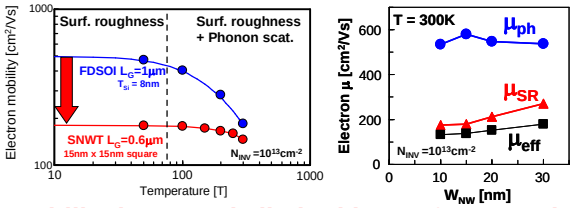
	NMOS	PMOS
NW cross-section	3-level-stacking	
NW dimensions	15 nm x 15 nm	
L_{eff} [nm]	32	42
EOT [nm]	1.7	1.7
V_{DD} [V]	1	1
I_{ON}/W_{eff}	840 μA/μm	540 μA/μm
I_{ON}/W_{Top}	7.2 mA/μm	4.7 mA/μm
I_{ON}/I_{OFF}	~2x10⁵	~6x10³
DIBL [mV/V]	32	63
SS [mV/dec]	64	73

I_{ON}: V_D=1V, V_G-V_T=0.7V
I_{OFF} : V_D=1V, V_G-V_T=-0.3V

Large effective surface for given layout

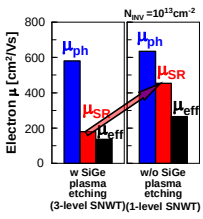
Excellent electrostatic control
High on-current density

Mobility in nanowires



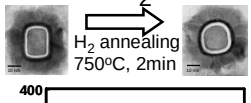
Mobility is strongly limited by surface roughness.

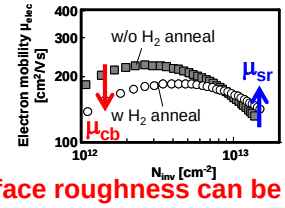
Impact on SiGe plasma etching



SiGe plasma etching causes surface degradation.

Effect of H_2 annealing





Surface roughness can be improved, while coulomb scattering increases.

Conclusion

Vertically-stacked SNWTs can achieve low leakage current and high integration density. However, the SiGe plasma etching to form the stacked channel causes the mobility degradation. Additional surface treatments are needed to cure the damaged Si surface.

References K. Tachi *et al.*, *IEDM 2009*, pp. 313-316
K. Tachi *et al.*, *IEDM 2010*, pp. 784-787

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