Estimation of Interface and Oxide Defects in Direct Contact High-k/Si Structure by Conductance Method

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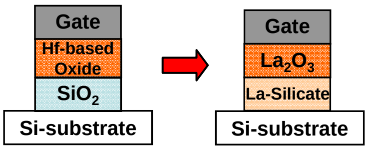
Background



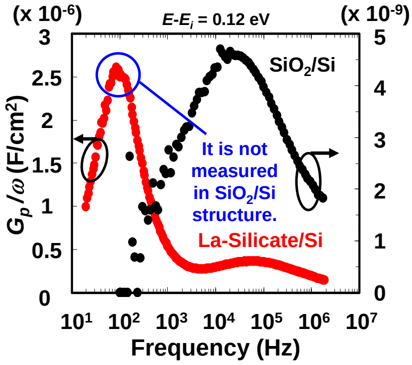
It is difficult for high-k/SiO_2 structure to progress scaling.
↓
We need the high-k dielectric that is possible to contact Si substrate directly.

Characteristics of La_2O_3
- Forming La-Silicate at the interface after heat treatment.
- High permittivity (ε_r = 23.4)
- Broad bang gap (E_g = 5.6eV)

➡ It is expected La_2O_3 is the gate dielectric of next generation.

We need to study interface properties without the SiO_2 layer.

Purpose



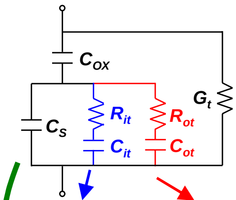
In La-Silicate/Si structure, different peak that is seemed to be oxide traps is found.

Purpose of this study

Modeling and quantifying interface and oxide traps in La-Silicate/Si structure

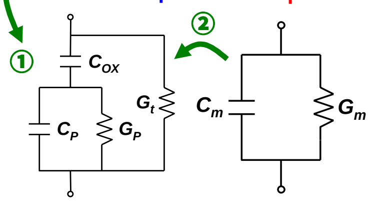
Method of Analysis

■ Conductance method



Equivalent circuit model of MOSCAP

Interface trap　Oxide trap



① Simulation

$$\frac{G_P}{\omega}=\frac{qD_{it}\omega\tau_{it}}{1+(\omega\tau_{it})^2}+\frac{qD_{ot}\omega\tau_{ot}}{1+(\omega\tau_{ot})^2}$$

Single level

$C_{it} = qD_{it}$　$C_{ot} = qD_{ot}$
$\tau_{it} = C_{it}R_{it}$　$\tau_{ot} = C_{ot}R_{ot}$

Actually, interface traps are measured as continuum level.

$$\frac{G_P}{\omega}=\frac{qD_{it}}{2\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right]+\frac{q\omega D_{ot}\tau_{ot}}{1+(\omega\tau_{ot})^2}$$

Continuum level

Consider surface potential fluctuations

$$\frac{G_P}{\omega}=\frac{q}{2}\int_{-\infty}^{\infty}\frac{D_{it}}{\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right]P(\psi_S)d\psi_S+\frac{q\omega D_{ot}\tau_{ot}}{1+(\omega\tau_{ot})^2}$$

Statistical model

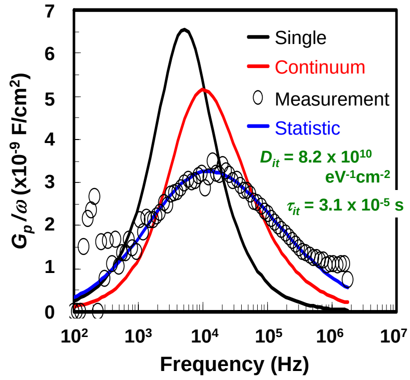
$$P(\psi_S)=\frac{1}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{(\psi_S-\bar{\psi}_S)^2}{2\sigma^2}\right)$$

Assume normal distribution

② Measurement

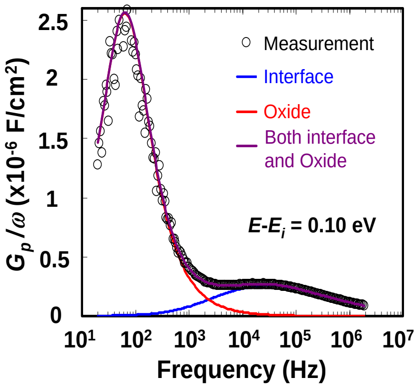
$$\frac{G_P}{\omega}=\frac{\omega(G_m-G_t)C_{OX}^2}{(G_m-G_t)^2+\omega^2(C_{OX}-C_m)^2}$$

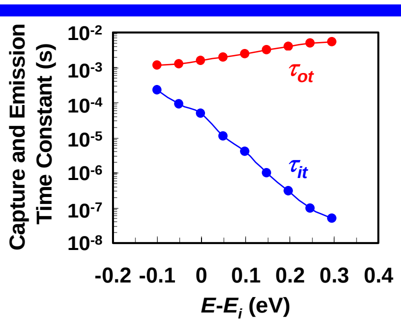
Include both interface and oxide traps

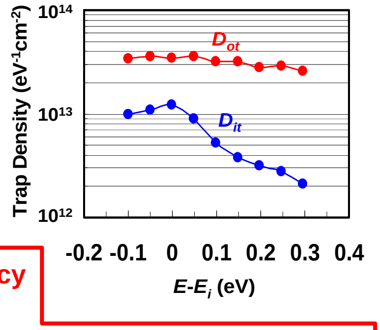


Simulation and measurement of only interface traps as a reference in SiO_2/Si structure

Results







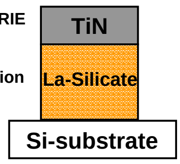
Reasons the signal in low frequency region means oxide traps

- Capture and emission time constant is long.
 ➔It is considered electrons are trapped away from the interface.
- Capture and emission time does not change compared with interface.
 ➔Because dependence of the surface potential is small, it is considered there are defects inside the oxide.

Fabrication Process

n & p-Si (100) substrate
- SPM cleaning HF treatment
- Deposition of La_2O_3 (3nm) by MBE } in-situ
- Deposition of Si (1.5nm) by RF sputtering } in-situ
- PDA in F.G. at 800°C for 2sec
- Deposition of TiN (60nm) by RF sputtering
- Photo lithography
- Gate electrode and resist etching by RIE
- PMA in F.G. at 420°C for 30min
- Deposition of Al by vacuum evaporation

Measurement



Conclusion

Oxide traps measured in La-Silicate/Si structure are modeled by equivalent circuit and it is agreed with measurement.

➡ Interface and oxide defects can be quantified.