

# Lateral encroachment of Ni silicide into Si nanowire

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### Introduction

Quasi-one-dimensional electron transport  
Gate-all-around (GAA) structure  
**High  $I_{ON}/I_{OFF}$  ratio**

A promising device to replace planer MOSFET

In terms of increase  $I_{ON}$  in Si nanowire FET, reduction of S/D resistance is effective.

### Objective

Characterizing the mechanism of Ni silicide encroachment  
Controlling and suppressing the encroachment length of Ni silicide into Si nanowire

Applying the Ni silicidation of S/D to Si nanowire FET

### Encroachment of Ni silicide into Si nanowire

Applying to fabrication of Si nanowire FET

Adverse Problem

- Increase of parasitic resistance
- Short between S/D
- Uncontrollable effective gate length

Controlling method of Ni silicide encroachment is necessary

### Fabrication Process

- Si Fin patterning: 30 nm (100) SOI, Si Fins directed <110>
- Thermal oxidation (Dry O<sub>2</sub>): (1000°C, 45min) Si nanowires with core width of 10-25 nm are fabricated
- Partially oxide removal: Partially removal of SiO<sub>2</sub> cover by buffered HF
- Ni deposition: 6nm Ni film is deposited in Ar ambient
- RTA (Rapid Thermal Annealing): Ni silicidation of Si nanowires in F.G. (N<sub>2</sub>+H<sub>2</sub>) ambient
- Unreacted Ni removal: Residual Ni is removed by SPM (H<sub>2</sub>SO<sub>4</sub>+H<sub>2</sub>O<sub>2</sub>)
- Observation by SEM (Scanning Electron Microscope)

### Results

#### Annealing Time Dependence

Diffusion equation

$$\lambda \propto A\sqrt{t}$$

$\lambda$ : Length of Ni silicide [nm]  
 $t$ : Annealing time[sec]

Ni silicide encroachment governed by the Ni diffusion.

### AES (Auger Electron Spectroscopy) Analysis

Uniform formation of Ni<sub>2</sub>Si was confirmed by AES analysis.  
With high temperature (600°C) annealing, Ni rich phase was formed. (in case of bulk, NiSi was formed)

### Suppression method of Ni silicide encroachment

2 Steps Annealing

Phase control in nano-scale structure is possible

**2 Steps Annealing**

**First Step**: Low Temperature : 300°C To suppress Ni diffusion To form Ni rich silicide

**Second Step**: High Temperature : 400°C-600°C To accomplish Ni silicidation

Unreacted Ni removal

### Annealing Temperature Dependence

Activation energy			
$W_{nw}$ [nm]	10	17	23
$E_a$ [eV]	1.48	1.52	1.60

Activation energy on bulk Si			
	Ni silicide	NiSi	Ni <sub>2</sub> Si
Activation energy [eV]		1.4	1.5

S. P. Murarka: SILICIDES FOR VLSI APPLICATIONS (Academic Press, New York, 1983) Chap.5

Experimental data fits to the activation energy for Ni<sub>2</sub>Si

### SEM Images after 1<sup>st</sup> and 2<sup>nd</sup> Annealing Step

After 1<sup>st</sup> RTA: Annealing condition : 300°C, 30sec

After 2<sup>nd</sup> RTA: Annealing condition : 300°C, 30sec + 400°C, 30sec

### Comparison of Annealing Conditions

400°C, 30 sec

300°C, 30 sec

400°C, 30 sec

2 step annealing method is very effective to suppress the encroachment by removing residual Ni after 1<sup>st</sup> step.

### Annealing Time Dependence

1 step

2 step

Although the encroachment was observed during first 150 sec, further annealing hardly increased.

### Conclusions

#### Mechanism of the encroachment of Ni silicide

- The encroachment governed by Ni diffusion.
- Activation energy indicates that Ni<sub>2</sub>Si was formed by annealing for 30 sec between 350-600°C.
- AES analysis indicates that Ni<sub>2</sub>Si was formed by annealing for 30 sec at 600 °C.

#### Suppression of the encroachment into Si nanowire

- 2 step annealing method dramatically suppressed the encroachment of Ni silicide into Si nanowire.
- In 2<sup>nd</sup> annealing of 2 step annealing, the encroachment occurred during 150 sec at 400 °C by phase change of ahead formed Ni rich silicide at 1<sup>st</sup> step.