# III-V MOSFETs for Next Generation

## - Fabrication of III-V MOS Capacitors

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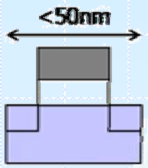
# Importance of CMOS devices

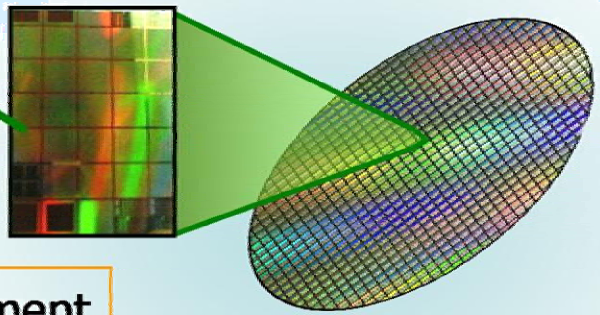
## Green Nanoelectronics

**Information**


Money transfer
Data center
Peta FLOPS computer




$10^8$ of transistors



**Home electronics**

Ubiquitous network
Digital broadcast
Smart image sensor

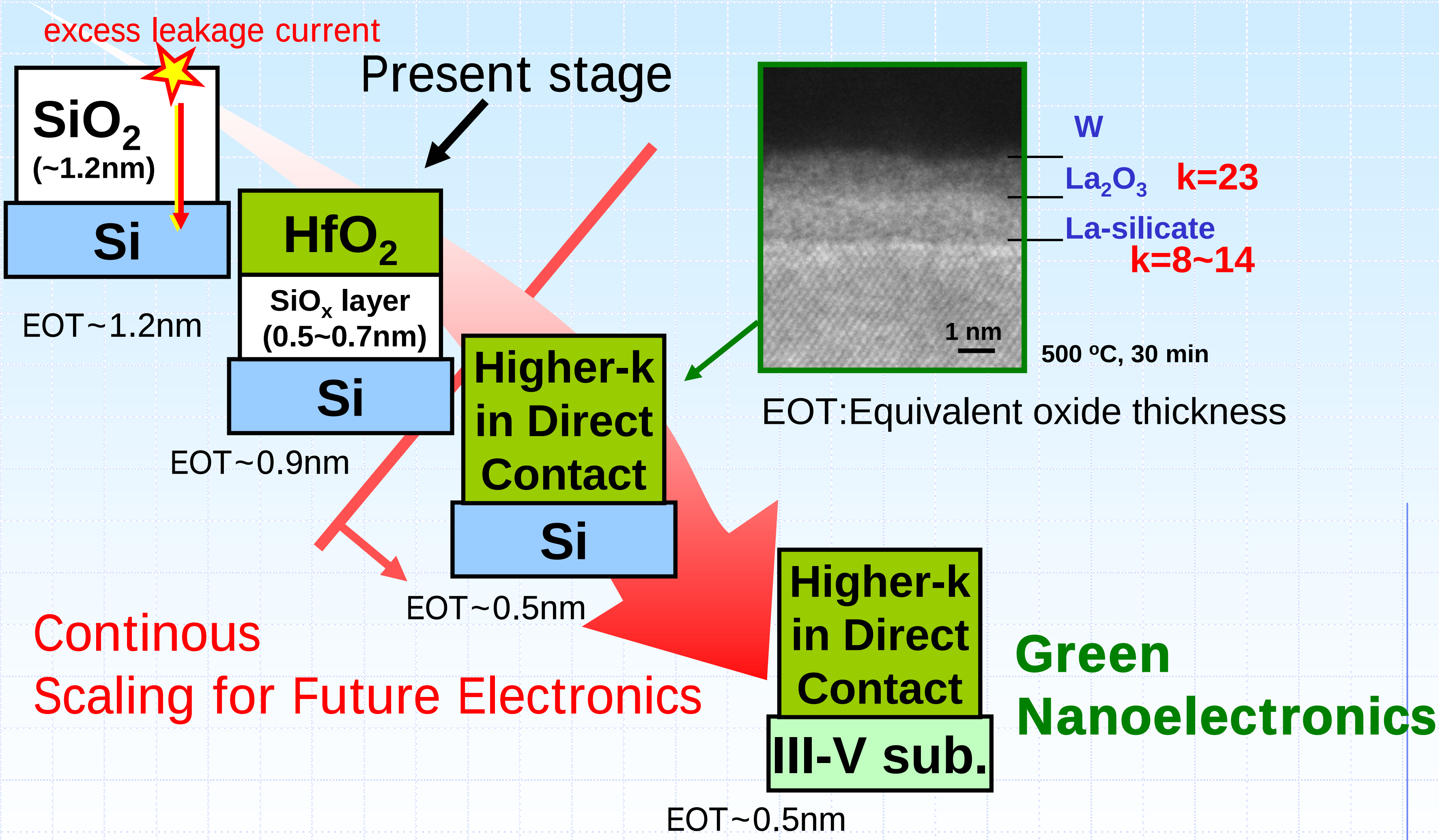
**System management**

Energy management in Builidings
Power supply

**Motion control**

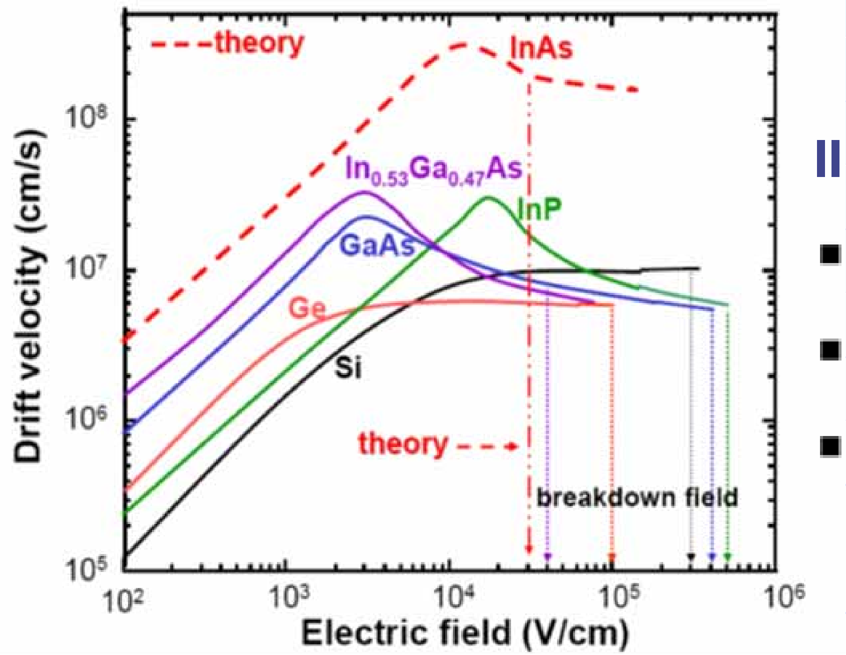
Speed control
Position control
Fuel/energy control

# CMOS device scaling



# Advantages of high-k/ III-V integration

| | Si | GaAs | $In_{0.53}Ga_{0.47}As$ | $In_{0.7}Ga_{0.3}As$ | InAs |
|---|---|---|---|---|---|
| $E_g$ (eV) | 1.12 | 1.42 | 0.74 | 0.59 | 0.35 |
| Bulk e mobility cm² /V s | 1400 | 8500 | 12000 | 20 000 | 40000 |
| Bulk hole mobility cm² /V s | 450 | 400 | 300 | 300~ 400 | 500 |




**III-V materials have:**

- High electron mobility
- High-low field drift velocity
- Good for low power logic application

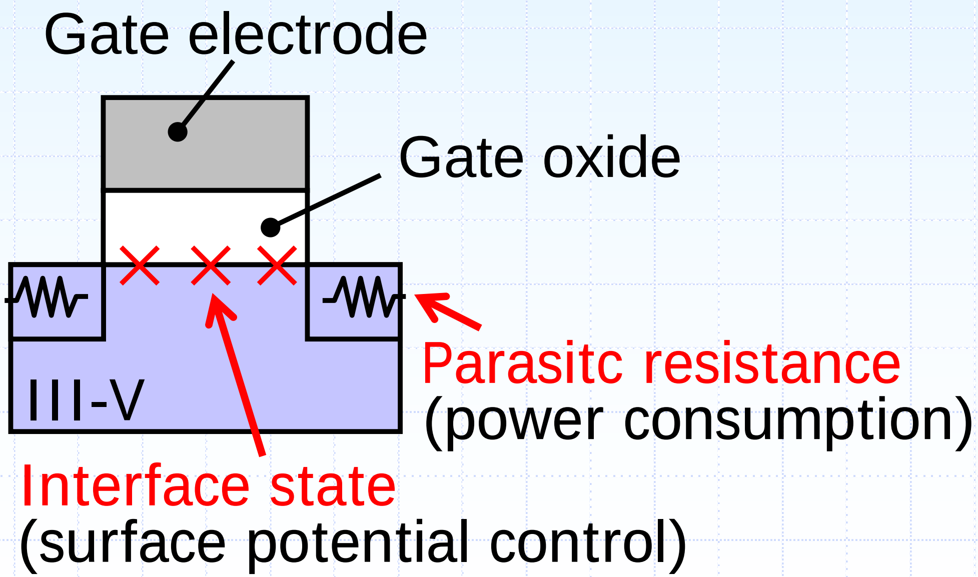
# Issues in high-k/ III-V technology

## 1. Redution of interface state density

- Selection of high-k material
- Proper surface treatments
- Optimization in the annealing process

## 2. Reduction of parasitic resistance

- Alloy process, etc..



# Selection of high-k material for III-V

- High interface density $D_{it}$: High $D_{it}$ results in Fermi level pinning, instability, carrier scattering.
- Oxides with high dielectric constant and large band gap are required.

| Oxide | $Al_2O_3$ | $HfO_2$ | $La_2O_3$ | $CeO_2$ |
|---|---|---|---|---|
| k | 8~11.5 | 25 | 30 | 38 |
| Eg (eV) | 6.65 | 5.7 | 4.3 | 3.2 |

# Our collaborative mission

National Chiao Tung University CSD Lab.

- High-k on verious III-V substrates

$In_xGa_{1-x}As$ (x=0.53, 0.70, 1.00)

Tokyo Institute of Technology Iwai Lab.

- Verious high-k for $In_{0.53}Ga_{0.47}As$ substrates

$HfO_2$, $La_2O_3$, $CeO_2$, $Pr_6O_{11}$

Establish a material selection guidline for future high-k/III-V technology

- Process engineering
- Interface reaction upon process
- Electrical characterization

# Content

1. ALD $Al_2O_3$ on InAs substrarte
2. ALD $Al_2O_3$ on InGaAs substrate
3. Surface treatment for $La_2O_3$/InGaAs
4. Enhanced deposition for $HfO_2$/InGaAs

# 1. ALD $Al_2O_3$ on InAs substrarte

# Experimental procedure

**Starting InAs surface**

↓

**Surface treatments**

ACE, IPA clean

↓

TMA treatment only: 10 TMA/$N_2$ pluses, 300°C

Or:

HCl treatment: HCl for 1min → TMA pretreatment

Or:

Sulfide treatment: HCl for 1min, $(NH_4)_2S$ for 20min → TMA pretreatment

→

1.5nm $Al_2O_3$, 300°C

**ALD $Al_2O_3$**

18nm $Al_2O_3$, 300°C

→ **XPS measurement**

→ **Surface treatments**

PDA: 400°C, $N_2$, 30s

↓

Ti/Pt/Au gate metal, lift-off

↓

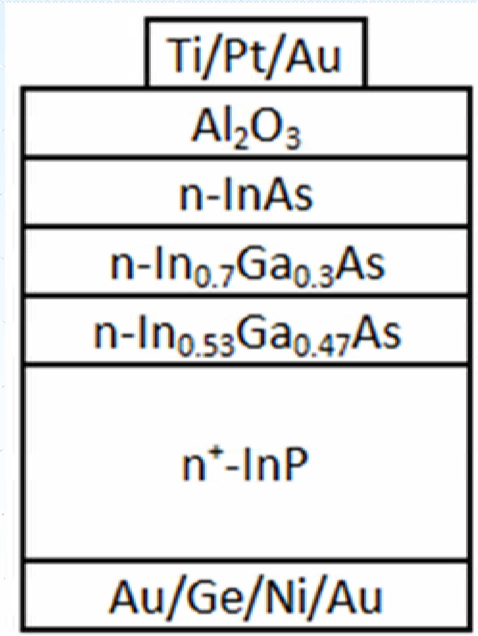
Au/Ge/Ni/Au ohmic metal

↓

PMA: 400°C, $N_2$, 30s

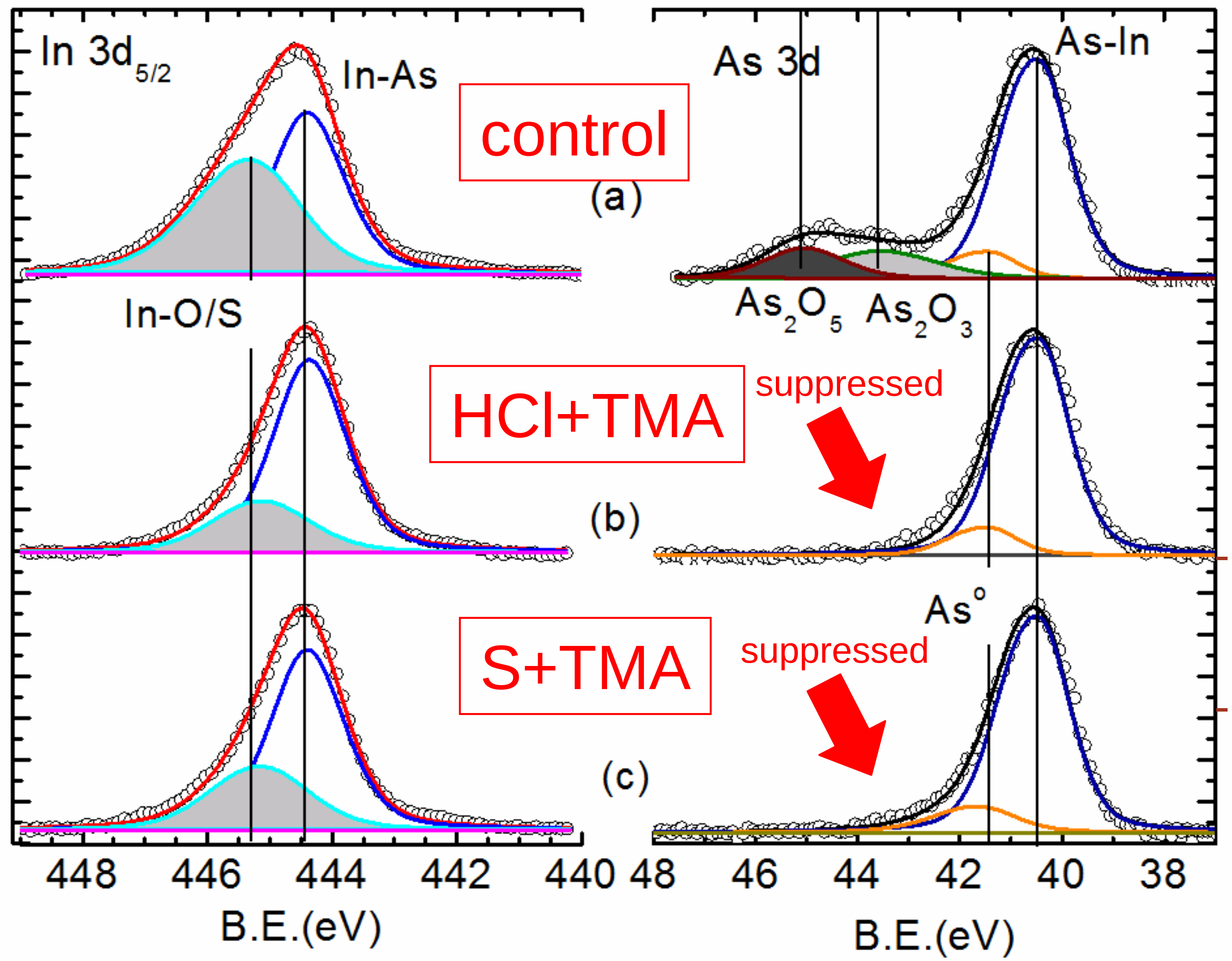
↓

**J-V, C-V, QSCV measurements**



# X-ray photoelectron spectroscopy (XPS) analysis

## $Al_2O_3$/InAs




*(a) Native oxide coverred InAs surface*

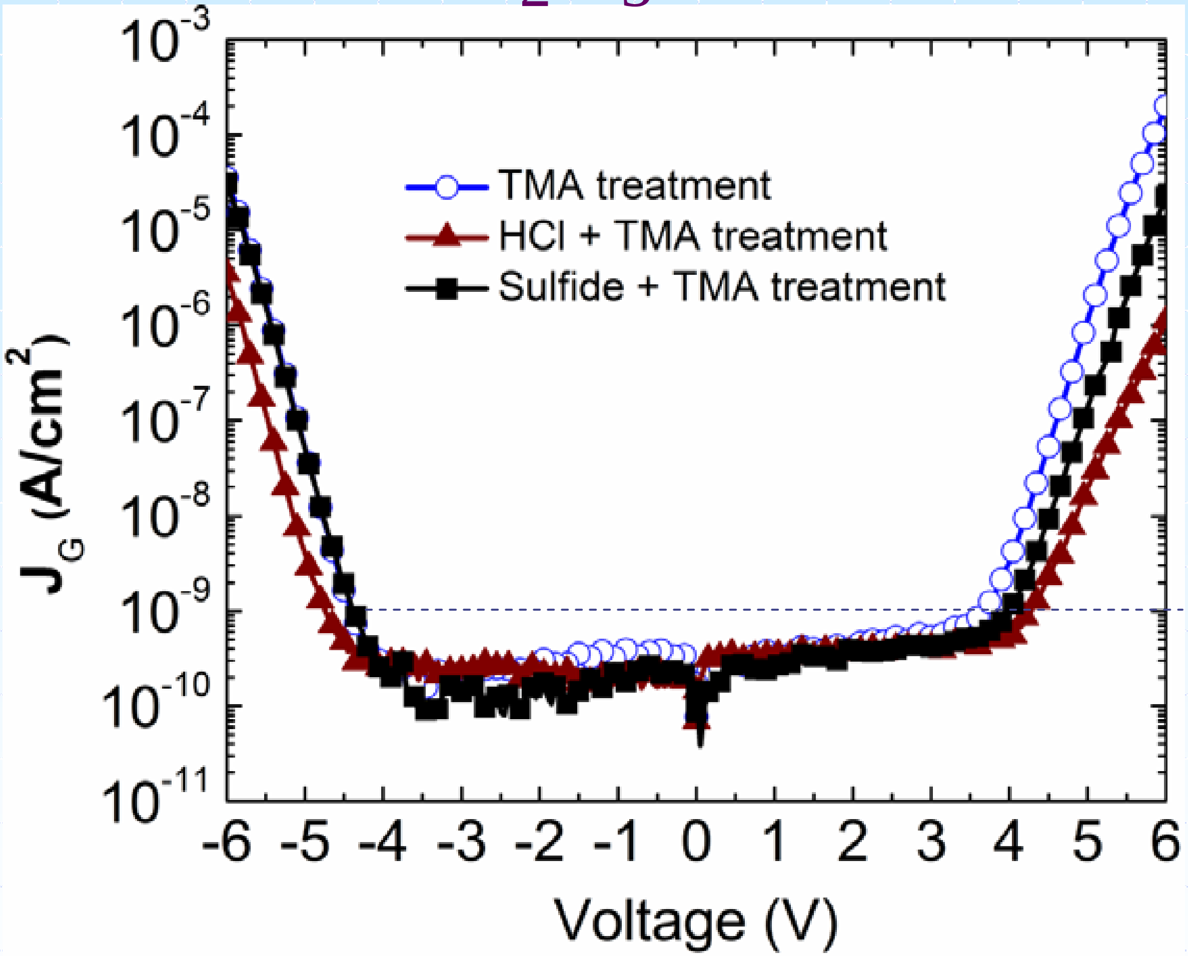
*(b) $Al_2O_3$/HCl+TMA-treated InAs interface.*

*(c) $Al_2O_3$/sulfide+TMA treated interface.*

- As-related oxides are reduced to below level of XPS detection
- In-O(S) bonds are also reduce after surface treatments, HCl+TMA treatment seems be more effective

# J-V analysis

## $Al_2O_3$/InAs

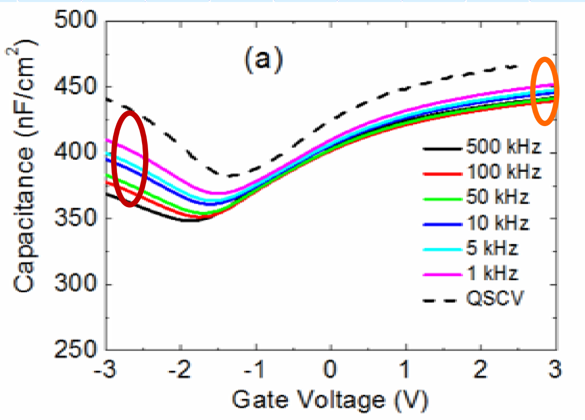



- $J_G < 10^{-9}$ A/cm², with -4 V < $V_G$ < 3.5 V, ensure that it is not affect C-V measurement

# Multi frequency C-V analysis

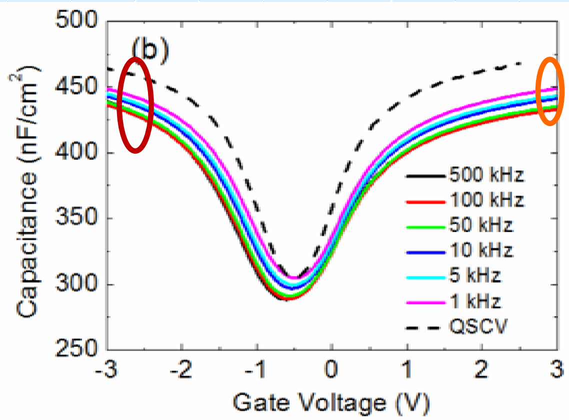
## $Al_2O_3$/InAs

TMA only (control)



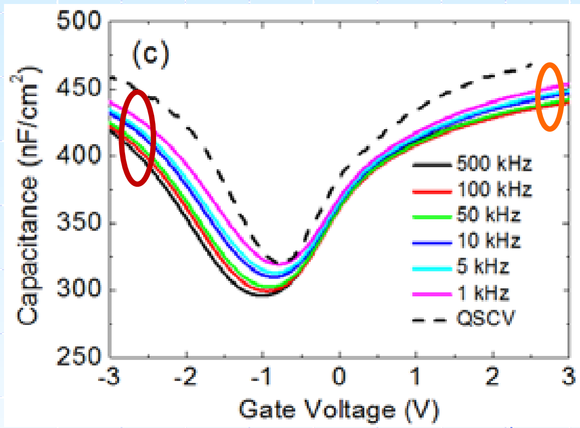

10 cycle TMA, 300°C

HCl + TMA treatment




HCl, 1 min
10 cycle TMA, 300°C

Sulfide + TMA treatment

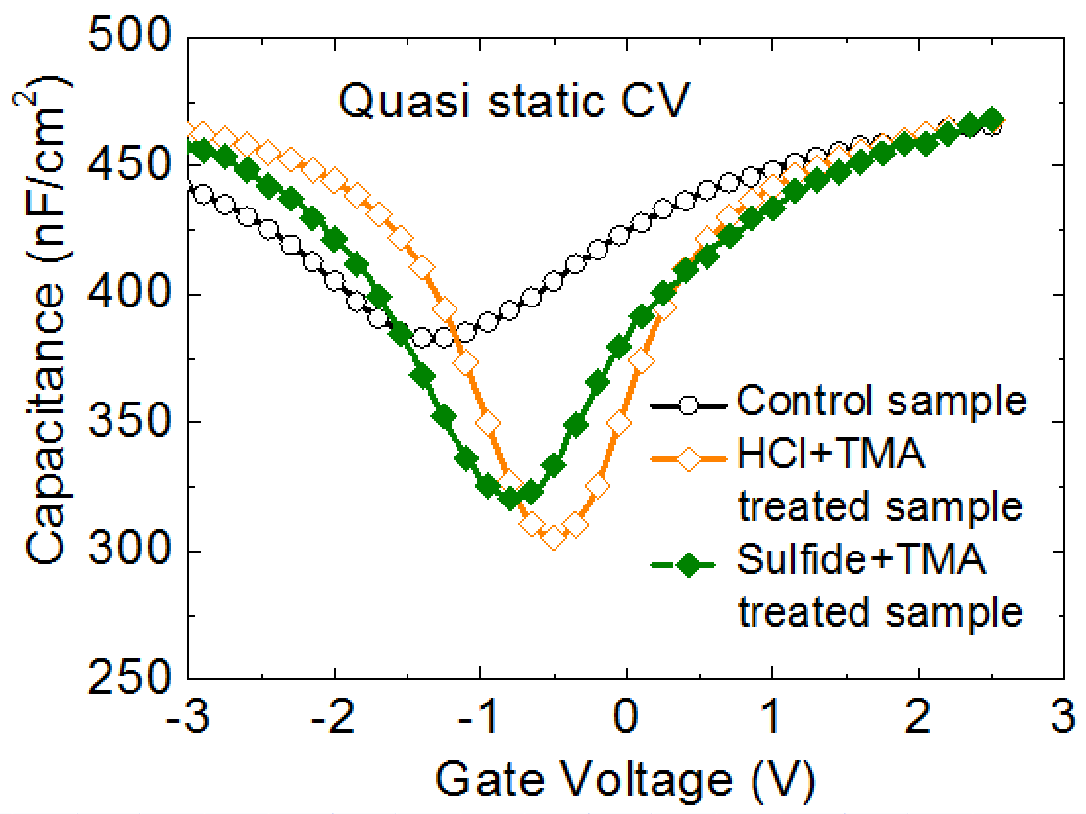



HCl, 1 min; $(NH_4)_2S$, 20min
10 cycle TMA, 300°C

- "Low frequency" C-V behavior: Short minority carrier response
- Accumulation regime: ΔC is small and does not seem to be affected significantly by the different surface treatments
- Inversion regime: ΔC (control) > ΔC (sulfide+TMA) > ΔC (HCl+TMA)

# Quasi static C-V (QSCV) analysis

$Al_2O_3/InAs$




- Depletion capacitance ($C_{dep}$): HCl + TMA → Sulfide + TMA → TMA only (control)
- C-V stretch-out: HCl + TMA → Sulfide + TMA → TMA only (control)

Large

# C-V simulation with $D_{it}$ profiles

- Using full numerical solution of the Poisson equation:

$$\frac{d^2V(x)}{dx^2} = -\frac{e\left(N_d - N_a + p(x) - n(x)\right)}{\varepsilon_s}$$

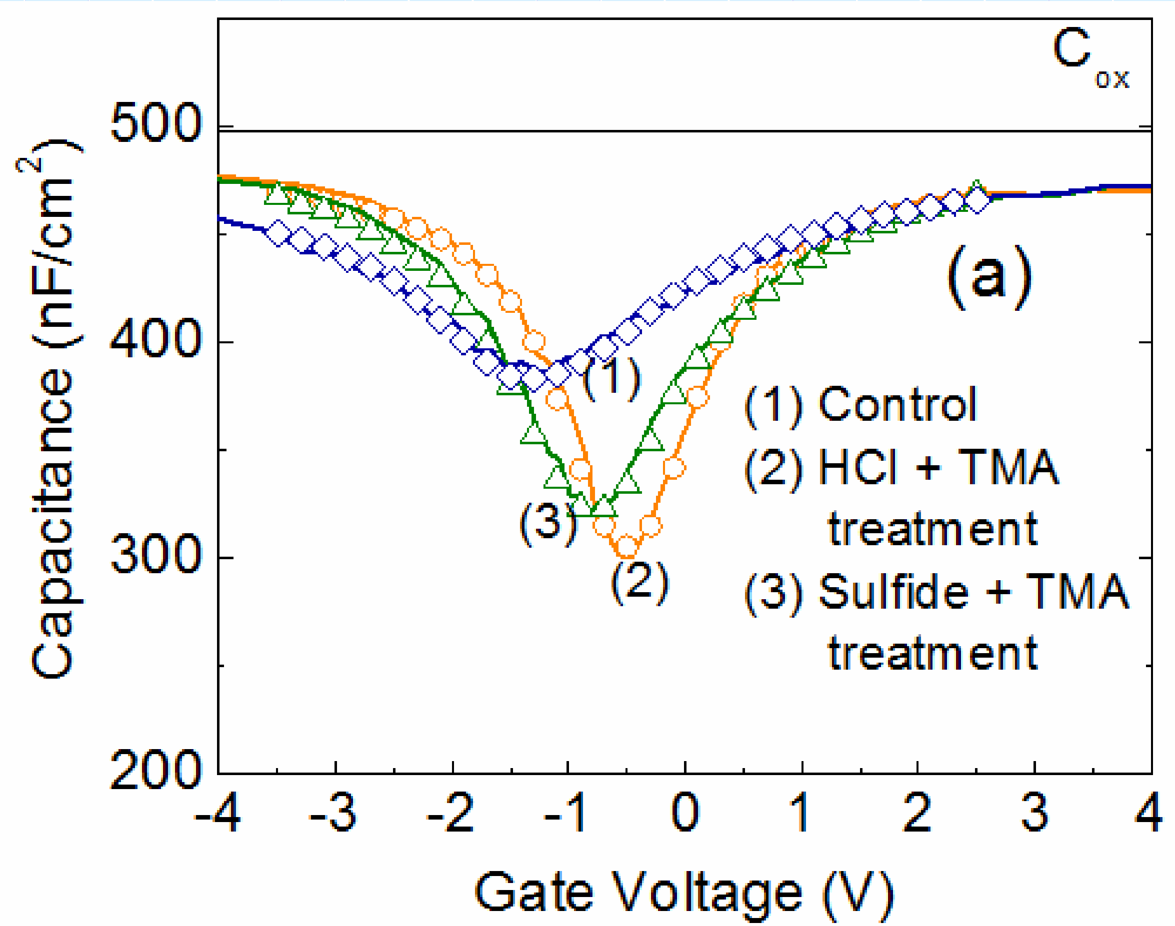
- $N_d$ and $N_a$: are the donor and acceptor concentrations in the semiconductor
- n(x) and p(x): are the electron and hole density
- $\varepsilon_s$ is the dielectric constant of the semiconductor

- The $D_{it}$ at the InGaAs, InAs/high-k interface was varied, until a good fit to the experimental data was obtained

- Charge quantization effects and non-parabolicity in the conduction band is not included in simulation

# C-V simulation results

$Al_2O_3/InAs$

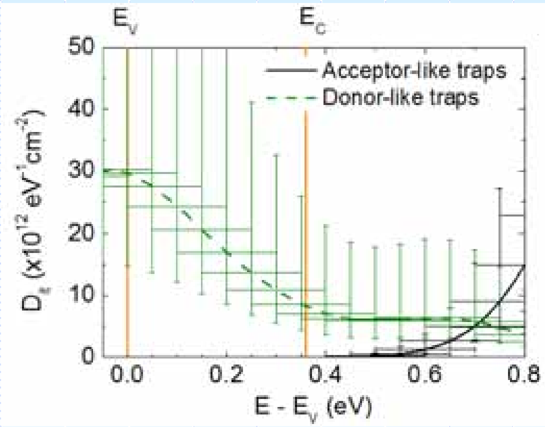



QSCV curves were well fitted by the simulations

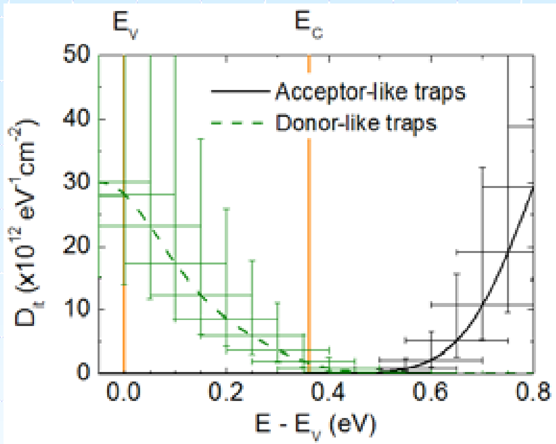
# Extracted $D_{it}$ profiles

## $Al_2O_3/InAs$

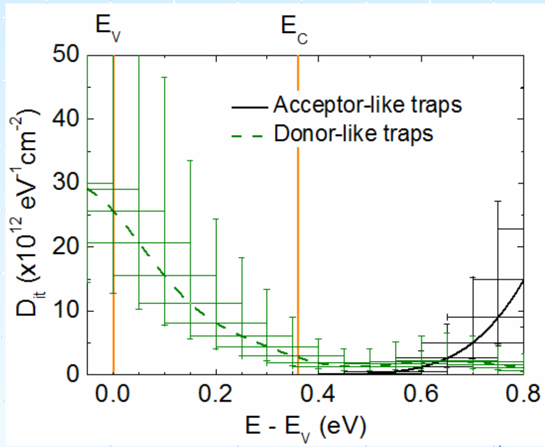
TMA only (control)




HCl + TMA treatment




Sulfide + TMA treatment

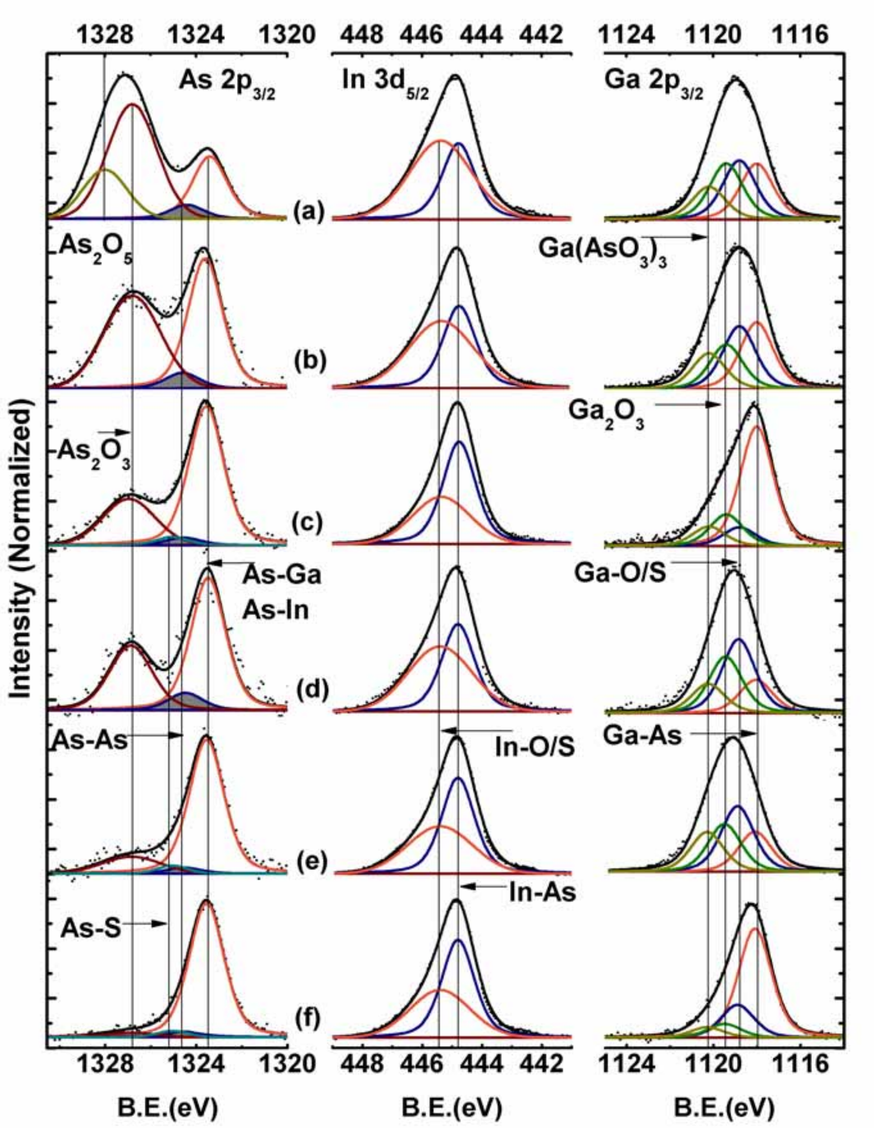



- U-shape profile, very similar to $Al_2O_3/In_{0.53}Ga_{0.47}As$ case (APL 95, 202109)
- Chemical + TMA surface treatments significantly reduce the donor-like traps
- HCl + TMA treated sample shows lower donor like-traps than that of sulfide + TMA treated sample

# 2. ALD $Al_2O_3$ on InGaAs substrarte

# $Al_2O_3/In_{0.53}Ga_{0.47}As$

X-ray photoelectron spectroscopy (XPS) analysis




(a) Native surface

(b) After TMA treatment

(c) Sulfide + TMA treatment

(d) TMA treatment, PDA: 500C in $N_2$

(e) Sulfide + TMA treatment, PDA: 500C in $N_2$

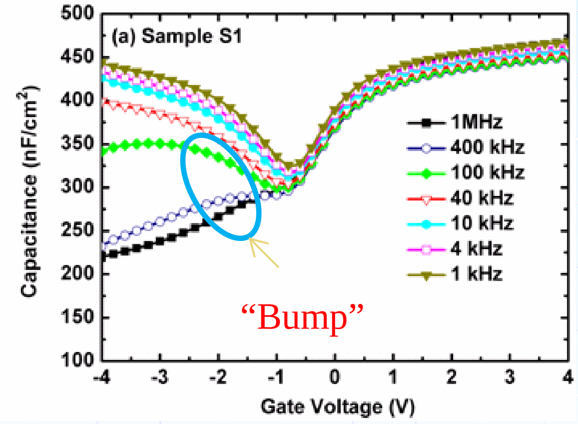
(f) Sulfide + TMA treatment, PDA: 500C in $H_2$

- ✓ Sulfide + TMA treatment, PDA: 500C in $H_2$: strong effect in reducing native oxides

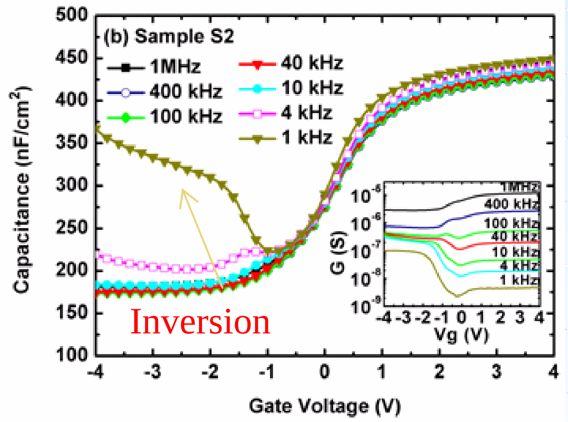
# Multi-frequency C-V characterization

## $Al_2O_3/In_{0.53}Ga_{0.47}As$

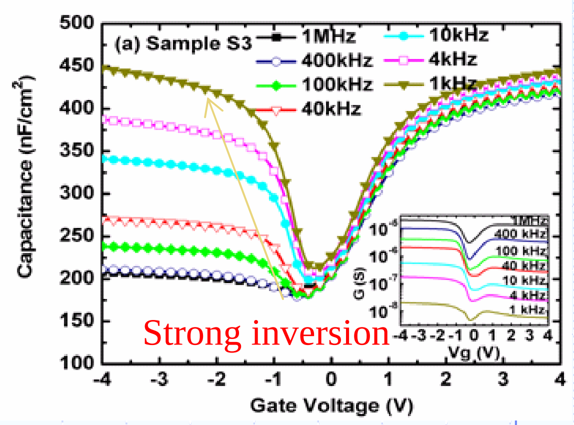
TMA treatment only, $N_2$ PDA




Sulfide + TMA treatment $N_2$ PDA




Sulfide + TMA treatment, $H_2$ PDA



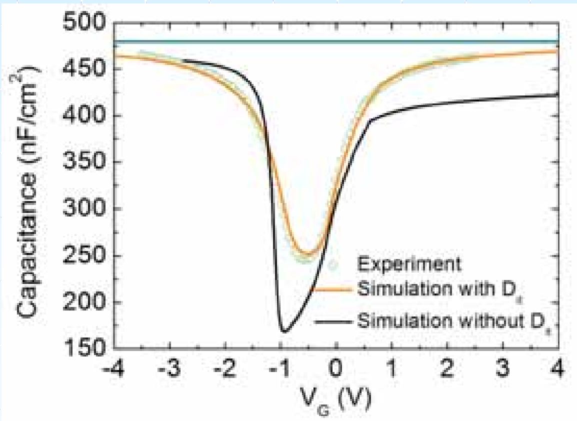

- ✓ True inversion response at high frequency of 1 MHz

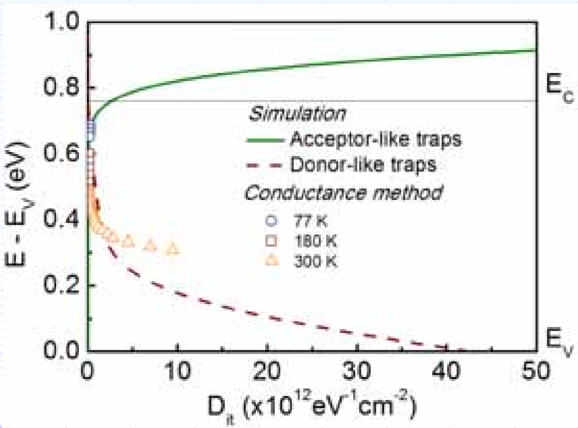
# C-V simulation results

## $Al_2O_3/In_{0.53}Ga_{0.47}As$

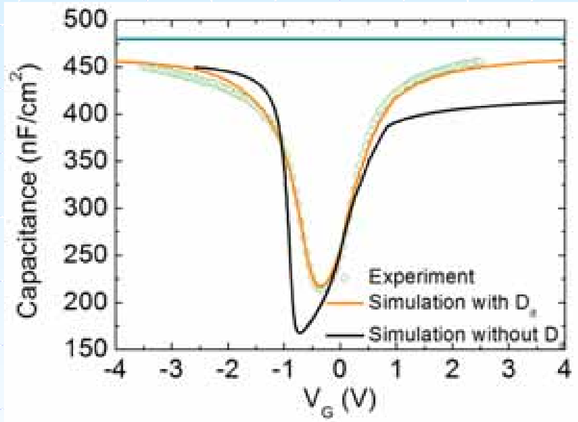
### $D_{it}$ extracted by conductance method and simulation

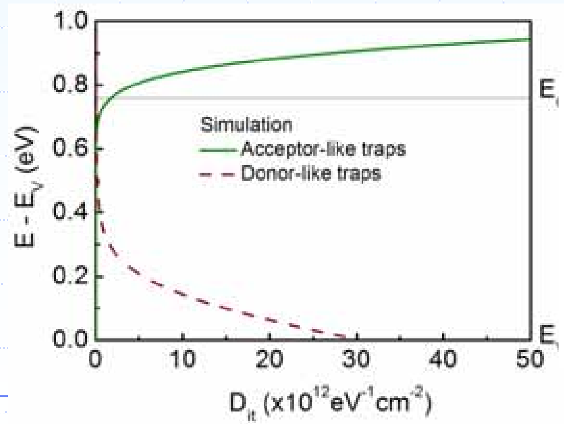
HCl + TMA treatment, $N_2$ PDA




Sulfide + TMA treatment, $H_2$ PDA



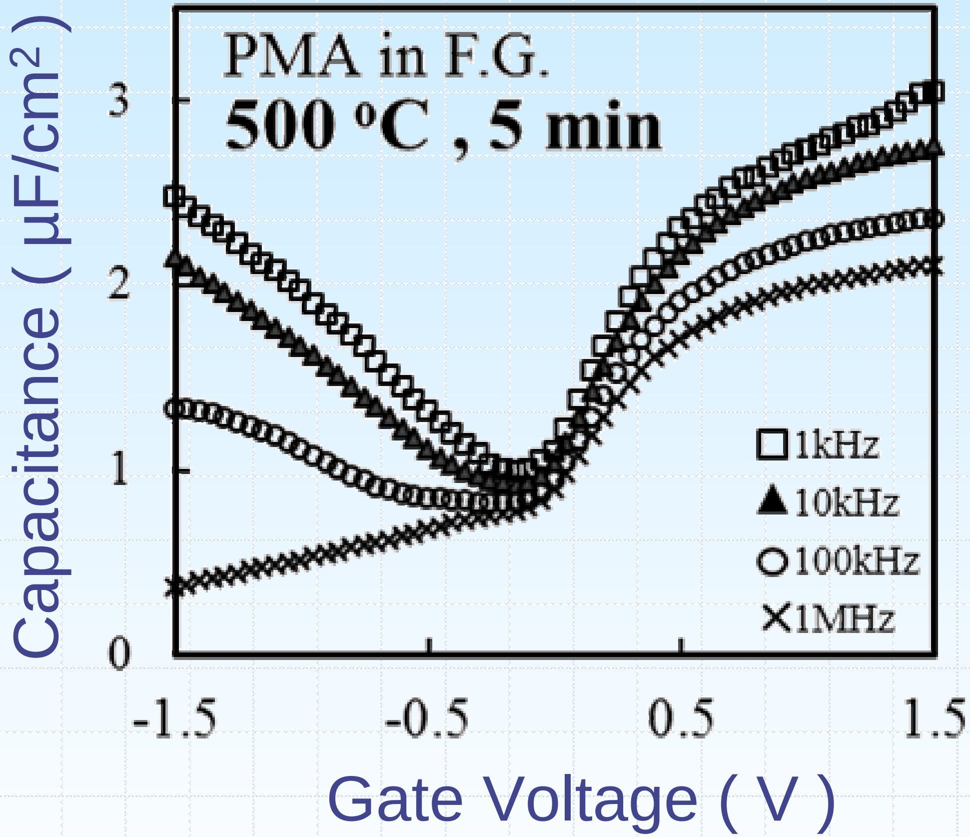



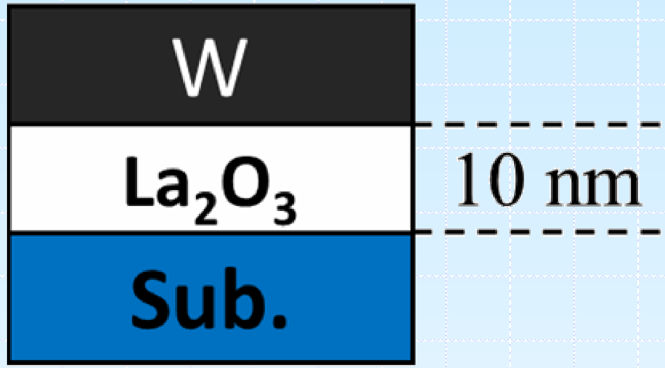

- ✓ Simulation is well fitted with experimental data

- ✓ U-shape profiles
- ✓ Low $D_{it} < 2 \times 10^{11}$ $eV^{-1}cm^{-2}$ at 0.5-0.6 eV above valence maximum

# 3. Surface treatment for $La_2O_3$/InGaAs

# CV characteristics of $La_2O_3$/InGaAs MOS capacitor



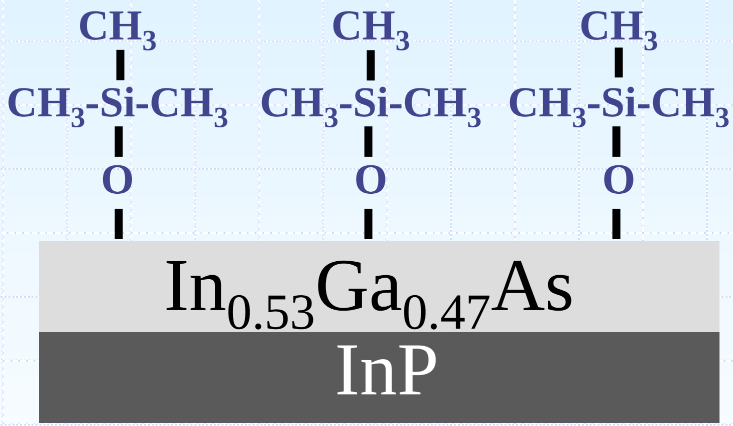

EB deposited $La_2O_3$

Sputter deposited W gate

Large frequency dispersion at accumulation

# Novel interface engineering process

Surface Si passivation using a self-assembled monolayer
HMDS (Hexamethyldisilazane )




HMDS coating

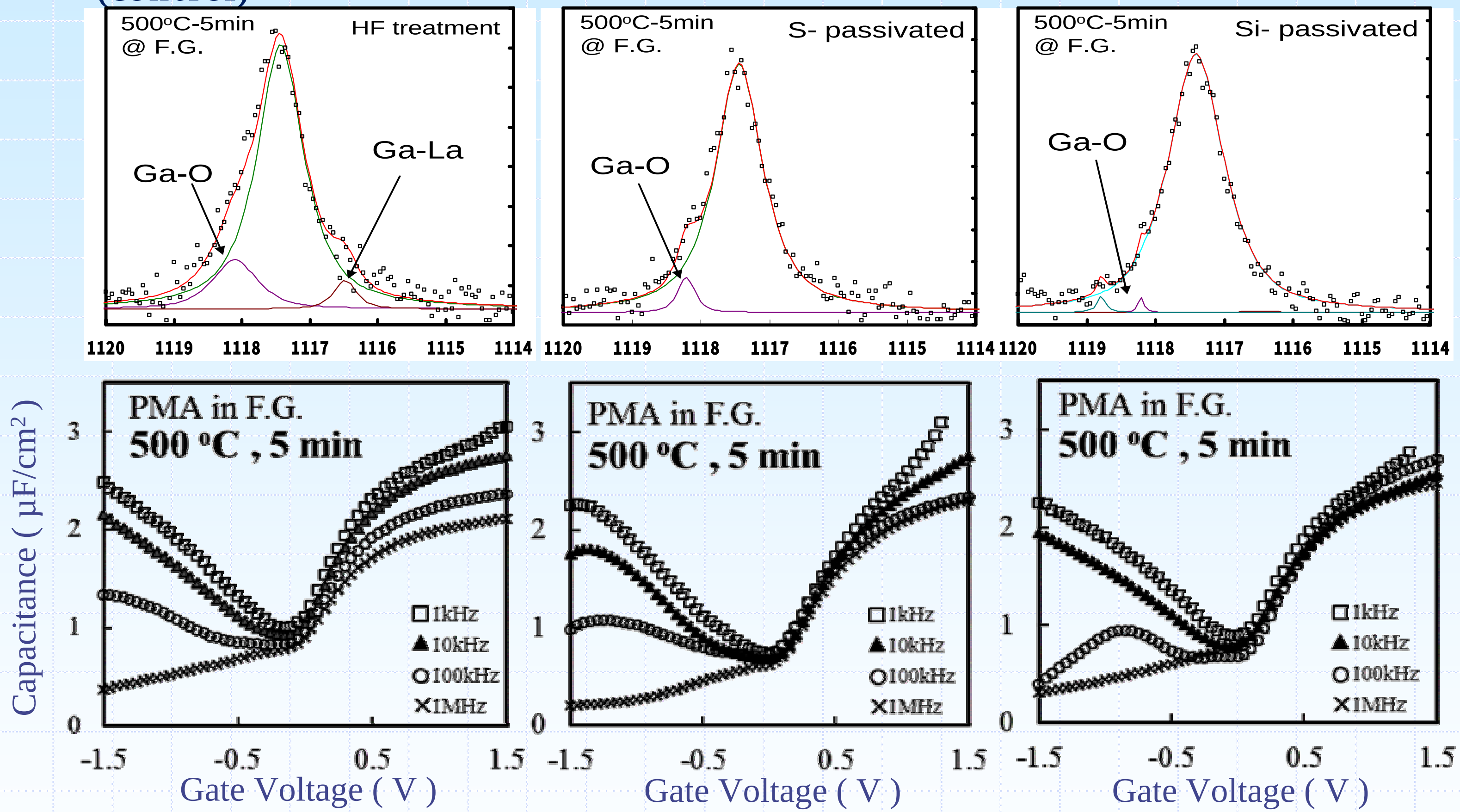
The impact to the CV curves are characterized

# Impact of Si monolayer insertion to the CV curves

HF treatment (control)

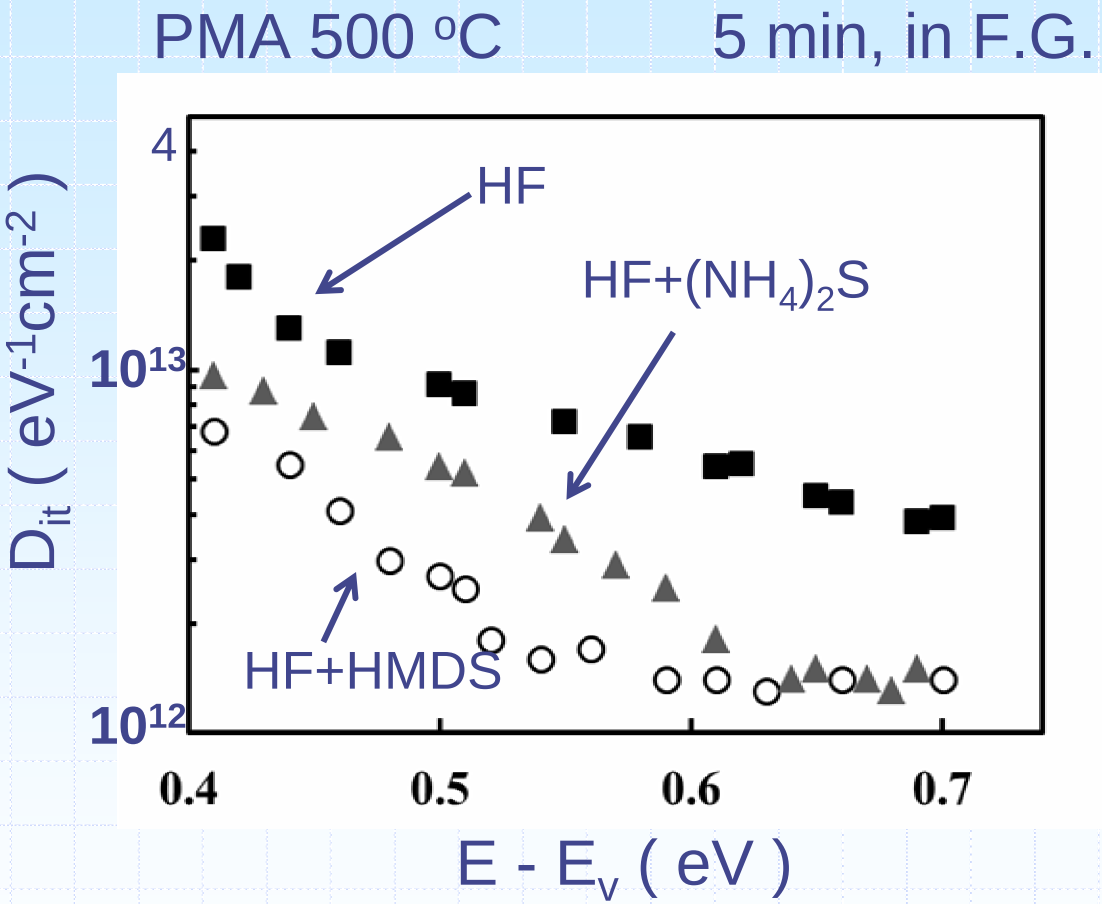
$(NH_4)_2S$ treatment

HMDS vapor coating




Less $GaO_x$ foramtion with less frequency disperssion

# Impact on the interface state density ($D_{it}$)




HMDS treatment→Lower $D_{it}$ especially at $E_c$ edge

# 4. Enhanced deposition for $HfO_2$/InGaAs

# The effect of $HfO_2$ deposition temperature

(Preparation: HF cleaning → Vacuum anneal 450°C for 30min)

Deposition at 100 °C

Frequency disspersion + Large $D_{it}$

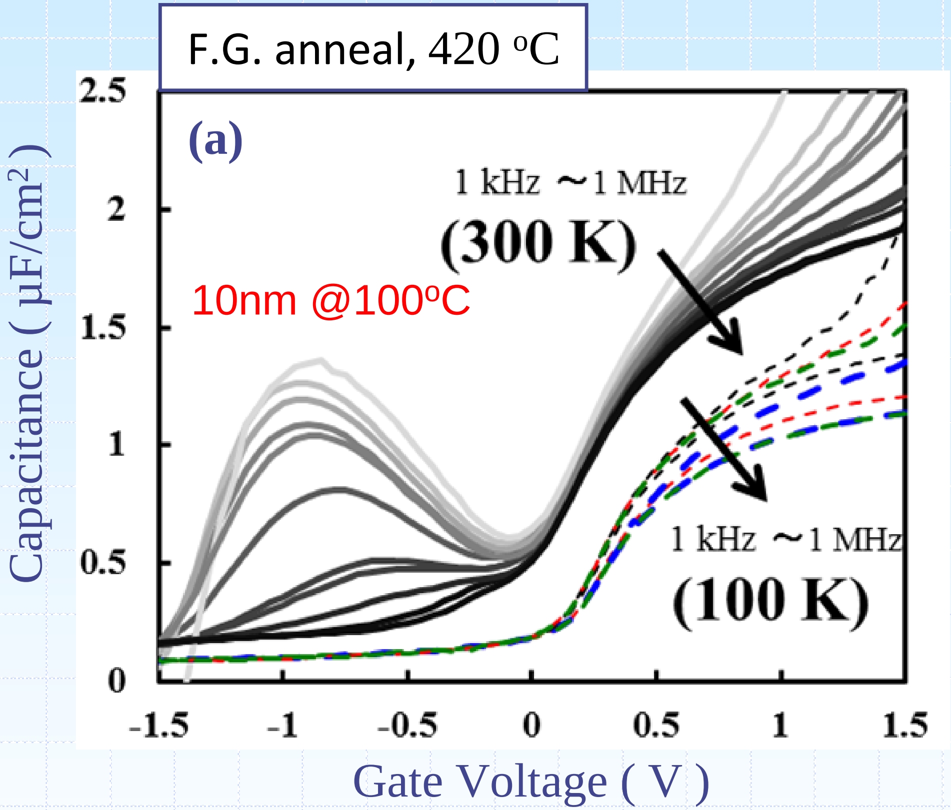
Deposition at 300 °C

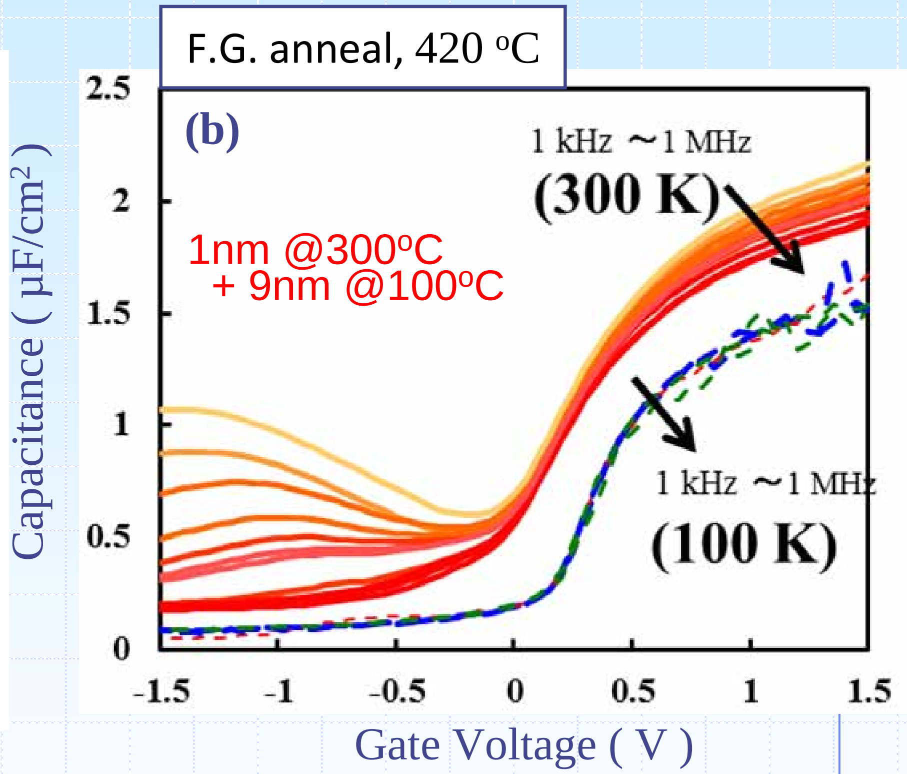
High leakage current, (hard to measure)
but seems less $D_{it}$

→ Combination of 100 and 300 °C deposition

1nm deposition at 300 °C and the rest at 100 °C

# CV curves measured at RT and 100K with enhanced $HfO_2$ deposition

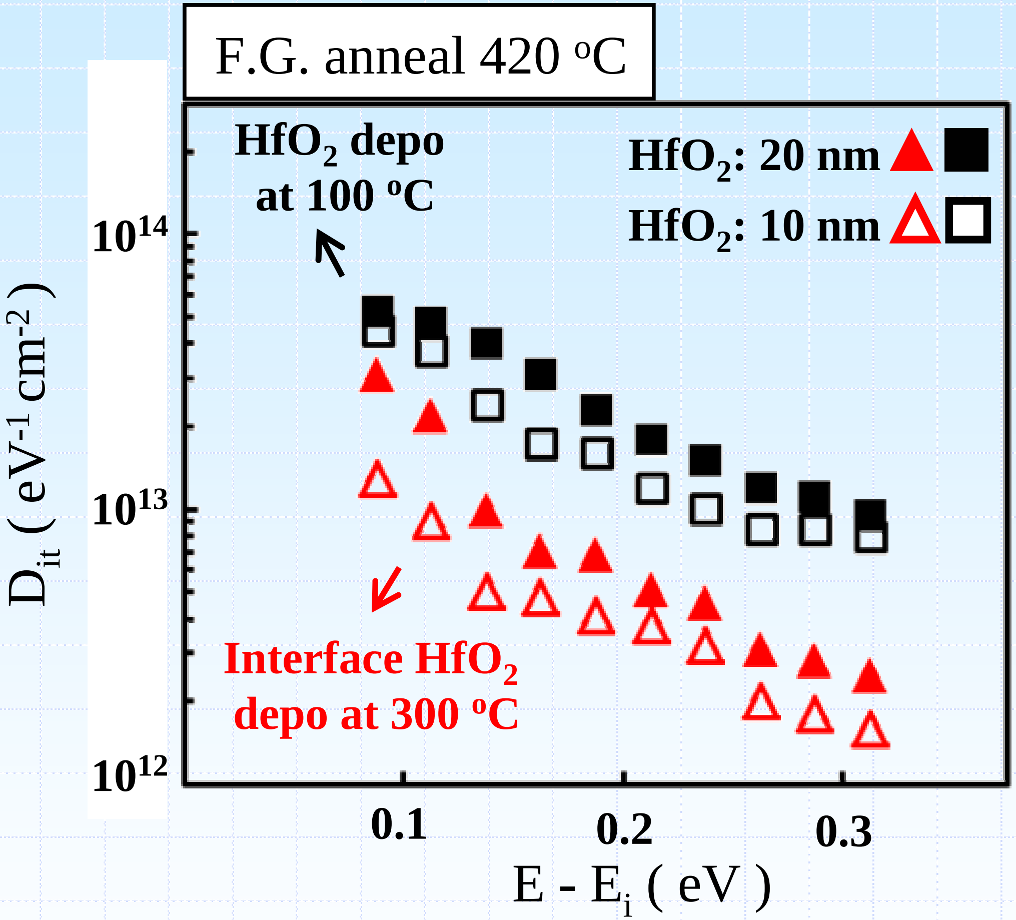



Large frequency disperssion still observed at 100K

Almost ideal CV curve obtained At 100K with enhanced deposition

# $D_{it}$ distribution with enhanced $HfO_2$ deposition




Smaller $D_{it}$ with interface $HfO_2$ deposited at 300 °C

# Conclusions

Surface treatment of InAs and InGaAs substrate with TMA is effective in removing the native oxide at the interface

With $H_2$ annealing, a $D_{it}$ below $2x10^{11}$ $cm^{-2}/eV$ can be achieved

Si insertion at $La_2O_3$/InGaAs by self-assembled monolayer can reduce the frequency disperssion at accumulation

Controling the temperature during the deposition is effective to change the interface properties to reduce the $D_{it}$