Feasibility study of Ce oxide for resistive RAM application

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Background and Motivation — 1

- RRAM: Resistance Switching Random Access Memory

Write voltage
High resistance — Off state
Low resistance — On state
Erase voltage

- nonvolatile
- High speed
- Compatibility with CMOS
- Simple MIM structure
- Low consumption
- Great potential of scaling

Promising candidate for next-generation memory

- CeO_2: potential for high-performance RRAM device
  - Changeable valence number (Ce^{3+} and Ce^{4+})
  - Fluorite structure ⇒ high conductivity of oxygen ions [1]
  - Reactivity with Si to form amorphous Ce-silicate [2]

Ce O

High performance RRAM based on Cerium oxide and Si buffer layer

Model for switching mechanism — 4

W electrode
CeO_2
TiN electrode
Oxygen ions at grain boundary
Initial state

+V
Formation of oxygen vacancies:
$2CeO_2 \xrightarrow{-2e} Ce_2O_3 + ½ O_2 + Vo^{..}$
oxygen vacancies drift under electric field
Forming process

-V
elimination of oxygen vacancies
$Ce_2O_3 + ½ O_2 + Vo^{..} \xrightarrow{+2e} 2CeO_2$

+V
on state
off state

Device design — 2

A
V
50 μm
20 μm
10 μm
W
CeO_2
Si
TiN
SiO_2
n^+-Si wafer
Al

50 nm
20 nm
0/1 nm
15 nm
200 nm

n^+-Si wafer (0.02 < W cm)

- Cleaning (SPM + DHF)
- Growth of SiO_2 insulator (thermal oxidation)
- Patterning contact window
- Deposition of TiN bottom electrode (RF sputter)
- Deposition of Si buffer layer (RF sputter)
- Deposition of CeO_2 switching layer (electron beam)
- Deposition of W top electrode (RF sputter)
- Electrode patterning process
- Evaporation of Al back contact

Materials and structure are suitable for practical application

Results of W/CeO_2/Si/TiN structure — 5

C.C. = 5mA
C.C. = 1mA
Forming Voltage decrease dramatically
w/o Si
with Si
Bias (V)

Read@ 0.1 V, R.T.
HRS
LRS
Device with Si
Device without Si
Resistance (Ω)
Switching Cycle

Formation of Ce-silicate
Introduce oxygen vacancies
$CeO_2 + Si \rightarrow CeSiO_4 + 2Vo^{..}$
$Ce_2O_3 + Si \rightarrow Ce_2SiO_5 + 2Vo^{..}$

By inserting Si buffer layer:

1. Forming process can be finished at lower voltage, results in protect devices from break down
2. A stable window (AVG~18) in 50times switching is achieved

Results of W/CeO_2/TiN structure — 3

C.C = 1mA
LRS
HRS
Forming process
CeO_2 20nm
20μm*20μm
Current (A)
Bias (V)

Read@0.5V, R.T.
HRS:LRS ~ 9.5
HRS:20 LRS:20 ~ 1.5
HRS
LRS
20μm*20μm
Resistance (Ω)
Switching Cycle

HRS
LRS
Resistance (Ω)
Electrode Area
10um*10um 20um*20um 50um*50um

For resistance change of W/CeO_2/TiN:

1. Forming process is necessary
2. Bipolar switching behaviors
3. As electrode areas scales, window gets large
4. Endurance characteristics is bad

Modeling of Reset process — 6

Vstop
Current (A)
Bias (V)

HRS
LRS
Resistance (kΩ)
|Vstop| (a)

R_{OFF} As $R_{OFF} = R_{CF1} = \cdots = R_{CFN} = R_{CF}$
$R_{ON} = R_{CF}/N$
$R_{OFF}(Vstop) = R_{CF}/[N - n(Vstop)]$
where, n (Vstop) is # of the ruptured CFs.
Ratio of ruptured CFs to all CFs = n(Vstop)/N (c)

90% filaments rupture
ruptured filaments in reset process (%)
|Vstop| (V) (b)

It is possible to decrease power consumption without losing too much window by properly decrease Vstop

Summary:

1. The resistive switching behaviors of CeO_2 based ReRAM have been confirmed.
2. Si buffer layer is able to improve CeO_2 based ReRAM device by forming Ce-silicate at interface.
3. A guideline for reset process control of the W/CeO_2/Si/TiN device is provided..