

# 超薄い High-k ゲートスタック MOSFET における電子移動度の劣化



## Electron mobility degradation in ultrathin high-k gate stacked MOSFETs

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**【Introduction】** The mobility degradation is one of the main concerns in high-k gate stacked MOSFETs. For high-k/Si-substrate direct contacted ultrathin high-k gate stacked MOSFETs, remote scattering mechanisms (remote Coulomb, remote surface roughness, and also remote phonon) may also contribute to mobility degradation. In this report, we studied remote surface roughness (RSR) scattering limited electron mobility in CeO<sub>2</sub> capped La<sub>2</sub>O<sub>3</sub> high-k MOSFETs.

**【Experiment】** Fabrication of nMOSFET started from a source/drain pre-formed p-Si (100) substrate. The high-κ dielectric thin films (La<sub>2</sub>O<sub>3</sub> and CeO<sub>2</sub>) were deposited by electron-beam evaporation system in an ultra-high vacuum at a temperature of 300 °C. Then a metal W (thickness of 50 nm) was sputtered in the radio frequency (RF)-sputtering chamber. After defining the gate area, annealing in the forming gas (N<sub>2</sub>:H<sub>2</sub> = 97:3) was performed at a temperature of 500 °C for 30 min. Then after patterning the source/drain by lithography and RI etching, a metal Al was evaporated to the source/drain, and backside electrode contact. The effective mobility of the fabricated nMOSFETs is experimentally measured by I-V, and the split C-V method at 1 MHz.

**【Results and discussion】** Figure shows measured electron mobility for La<sub>2</sub>O<sub>3</sub> single layer and CeO<sub>x</sub>/La<sub>2</sub>O<sub>3</sub> gate stacked nMOSFETs. The total physical thicknesses of the high-k layers in all samples are same. The distance from the interface of CeO<sub>x</sub>/La<sub>2</sub>O<sub>3</sub> to surface of the Si substrate is intentionally decreased. The mobility of the CeO<sub>x</sub>(1.3nm)/La<sub>2</sub>O<sub>3</sub>(2.2nm) gate stacked MOSFET is increased compare to the mobility of the La<sub>2</sub>O<sub>3</sub>(3.5nm) gate stacked MOSFETs. This can be understood that the amount of fixed charges in the gate stack is decreased by CeO<sub>x</sub> capping on the La<sub>2</sub>O<sub>3</sub> layer. While the thickness of the La<sub>2</sub>O<sub>3</sub> is decreasing and the thickness of the CeO<sub>x</sub> is increasing, the interface of CeO<sub>x</sub>/La<sub>2</sub>O<sub>3</sub> is more close to the Si substrate. This might strength the effect of remote surface roughness scattering on the mobility of the channel electrons. As a result, the mobility is decreased in the CeO<sub>x</sub>(1.7nm)/La<sub>2</sub>O<sub>3</sub>(1.9nm) gate stacked MOSFET.

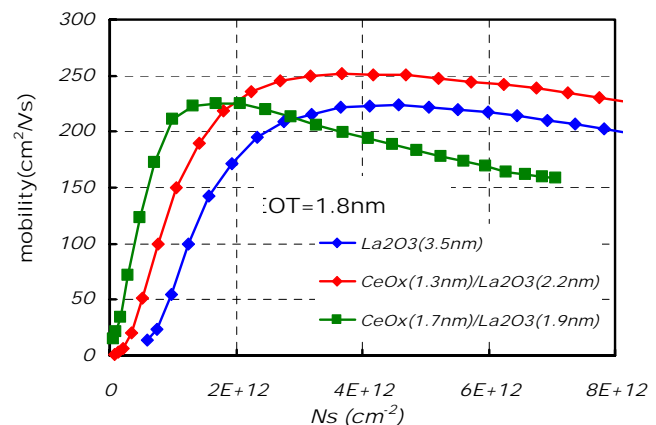


Fig. Measured electron mobility

**Acknowledgement:** This work was supported by NEDO, NEC C&C, and G-COE PICE of TIT.