CeO_2 を用いた抵抗変化型メモリーへの Si バッファー層の効果検討

Investigation of the effect of Si buffer layer in CeO_2 based RRAM Devices

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【**Introduction**】Resistive RAM (ReRAM), which is a strong candidate for the next generation of nonvolatile memory, still calls for new material technology because its problems in efficiency and reliability. Cerium oxide is promising for ReRAM application since it can be used as solid electrolyte having high dielectric constant and high ion conductivity [1]. In addition, cerium oxide is easy to react with Si to form silicate [2], which modifies structure and concentration of vacancies in cerium oxide film. This work proposes a new method to improve the performance of CeO_2 based RRAM by utilizing Si buffer layer and investigate its effects in details.

【 **Experiment** 】 The structure of the devices is schematically shown in Fig.1. Fabrication started from growing a SiO_2 layer on highly doped Si wafers by thermal oxidation, followed by formation of contact windows through SiO_2 layer. After that, a TiN bottom electrode layer, a Si buffer layer, a CeO_2 switching layer and a W bottom electrode layer were deposited in succession. Finally, Al was evaporated as a back contact followed by RTA in N_2 ambient for 30 s at 400 °C. Device without Si buffer layer was also fabricated for comparison.

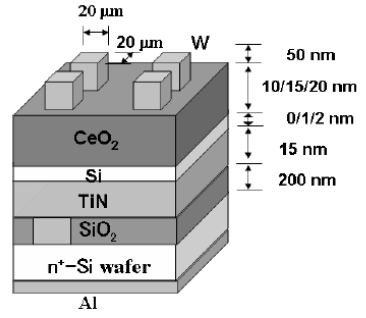

Fig.1. Schematic illustration of the RRAM device having W/CeO_2/Si/TiN structure.

【**Result**】W/CeO_2 (20 nm)/Si (1 nm)/TiN device shows the bipolar resistance switching behaviors. As shown in Fig.2, the ratio of high resistance state to low resistance state of this device takes an average value of about 20. Furthermore, it is also clearly shown in Fig.2 that by incorporating Si layer, the device exhibits enlarged window and better endurance characteristics. After 60 times cycles, devices incorporating Si layer still has a window of about 15 while the window of the device without incorporating Si layer degraded to 1.5.

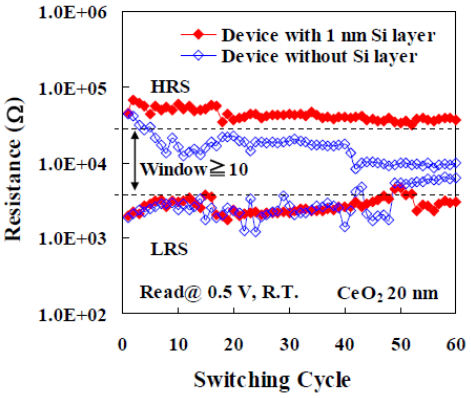

Fig.2 Endurance characteristics of the device with and without Si buffer layer

[1] C. Lin, et al., Surface & Coating Technology 203, p.480-483, (2008)

[2] K. Kakushima, et al., VLSI Tech. Dig. p.69-70(2010).