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Ni Silicide Schottky barrier tunnel FET for Low power device applications

(低消費電力動作に向けたニッケルシリサイドバリアトンネルFET)

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Abstract

To solve this problem that the supply voltage and the threshold voltage should be scaled but induction of the leakage would increase current at the zero gate voltage. The Subthreshold slope (SS) cannot be scaled down below 60mV/decade at Room temperature in principle and this fact hinders the applied voltage scaling. The tunnel FET is one of the promising candidates to decrease SS. Schottky barrier Tunneling FET (SBTT), which uses schottky tunnel junction, has many advantages to ordinary PN junction Tunnel FETs: low parasitic resistance, better short channel effect immunity and high controllability of output characteristics by the silicide material selection. The tunnel FET with NiSi/Si schottky barrier at the source/channel interface was fabricated and the characteristics were analyzed in terms of the drive current mechanism at low and high voltage. For that purpose, temperature dependence measurements of the transistor characteristics were mainly performed.

Contents

Abstract

I Introduction

I.1 Background of This Study

I.2 Ultimate CMOS downsizing

I.3 subthreshold leakage increasing

I.4 tunneling FET

I.5 Objective of this study

II Metal-Semiconductor Junction

II.1 Principle of the Schottky junction

II.1.1 Energy band diagram

II.1.2 Effect of the surface states

II.1.3 Image-force barrier lowering

II.2 Current transport mechanisms

II.2.1 Thermionic current

II.2.2 Tunneling current

II.3 Measurement of the barrier height

III Introduction to Schottky Barrier tunneling FET

III.1 Operation principles

III.2 Silicide materials

III.3 Advantage and performance of SBTT

III.3.1 Contact resistance improvement

III.3.2 Shape Source/Drain junction

III.3.3 Immunization short-channel effect

IV Fabrication and Characterization Method

IV.1 Schottky barrier tunneling FET Fabrication

IV.1.1 Fabrication Process

IV.1.2 Substrate Cleaning

IV.1.4 Photolithography and Metal Gate Etching

IV.1.5 RF Sputtering of Gate Electrode

IV.1.6 Thermal Oxidation of SiO₂ Dielectrics

IV.1.7 Thermal Annealing Process

IV.1.8 Thermal Evaporation of Al Layer (Source/Drain contact)

IV.2 Characterization Method

IV.2.1 J_g-V_g (J-V) measurement

IV.2.2 I_d-V_g (I-V) measurement

IV.2.3 I_d-V_d (I-V) measurement

IV.2.4 Subthreshold slope measurement

V Tunneling transport mode Analysis

V.1 Observing Schottky barrier tunneling

V.2 Low temperature Characterization model

VI Conclusion

Acknowledgement

I Introduction

I.1 Background of This Study

The first commercial release of a computer based on integrated circuit (IC) technology dates at end-60s. Due to the low-cost manufacturing potentialities offered by emerging ICs, researchers and industrial partners have directly joined their effort to convert a promising technology at its birth to the biggest technological revolution of the twentieth century. Initially mainly designed for military applications, the computers integrate nowadays our everyday's life: from basic communication and entertainment to fussy scientific supports for the forthcoming new technologies. In the heart of this tremendous adventure, lies the silicon Complementary Metal-Oxide-Semiconductor (CMOS) transistor - currently the most widespread semiconductor switch. The big success of the CMOS devices is explained by the possibility to increase in the same time the drive current and the cut-off frequency, only by reducing the size of the devices. The downscaling of the transistors has allowed very large scale integrated chips operating at increasingly high frequency. The functionalities of the computers have become more and more various and complex for a lower cost per functions of the chips.

The CMOS scaling has been governed by the so-called Moore's law since 1965 [1].

The co-founder of Intel company, G. Moore, predicted that the number of transistors on a chip would double every 24 months. In order to meet the Moore's law specifications and the market requirements, the International Technology Roadmap for Semiconductors (ITRS) [2], has suggested for more than 10 years the strategies to adopt for the semiconductor industry, forecasting the market evolution until 15 years ahead (see Table 1, Fig. 1.1).

Year	2002	2005	2008	2011	2013
Technology node (nm)	130	100	65	45	32
Supply Voltage (V)	1.3	1.0	1.0	1.0	0.9
Oxide thickness (nm)	2.2	1.5	1.0	0.7	0.5
I_{on} (mA/mm)	750	750	750	750	750

Table 1: Non exhaustive list of device requirements for the current and forthcoming transistors according to the ITRS

I.2 Ultimate CMOS downsizing

Nowadays, the best processors available on the market are clocked at a frequency of around 3GHz for a gate length of 0.13 microns (Intel has even released a 90 nm Pentium4). Meanwhile, microelectronic research is currently working towards the 65 nm technology node and even far beyond. According to the ITRS forecasts, research follows two different directions: either pushing the conventional Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) toward its physical limits, with a possible modification of the planar architecture, either exploring a new way of making transistors, e.g. devices based on Si nanowires or carbon nanotubes, single electrons FETs, and much more advanced devices such as quantum cellular automata or spin-based electronics. For the 10 years to come, it is believed that the aggressive downscaling of MOSFETs will be adopted for the mass-production devices. The downscaling of CMOS transistors is now facing several difficulties stemming from the reduced size of the devices. Technological solutions must be brought by the research centers in order to make the small transistors meeting the ITRS requirements. Currently, four trends emerge from the publications related to this subject:

New transistor architectures

The downscaling toward short-channel transistors implies a threshold voltage (V_t) reduction and a drain-induced barrier lowering (DIBL), i.e. the reduction of V_t induced by the drain voltage. Both effects belong to the new category of so-called Short-Channel Effects (SCE). Fully depleted silicon-on-insulator substrates and multiple gate devices such as FinFET have been proposed to overcome SCE due to the higher electric field in the channel region for a stronger control of V_t .

Replacements of the gate stack

Lot of studies are related to a better gate engineering. One of the biggest problems is the current leakage through the thinner and thinner gate oxide (scaled in the same way as the channel length). New high-k dielectric materials such as Hafnium oxide (HfO_2) with metal gate have been proposed to replace the usual SiO_2 oxide and the poly-silicon gate for sub-45 nm transistors.

Improvement of the channel

Another trend is the increase of the channel mobility. Alternative substrates such as Ge or strained-Si could be used for improving the hole and electron channel mobility. Although Ge substrate is difficult to introduce in CMOS technology, strained-Si could be the best alternative.

I.3 subthreshold leakage increasing

As the size of the MOSFET becomes small, the leakage current in the subthreshold region increases, so that the scaling in MOSFET becomes difficult. In order to overcome the issues, UTSOI or High-k gate oxide have been attempted to be incorporated to improve the controllability of the channel potential against the short channel effects.

Recently, nanowires with gate all-around structure have been studied intensively. However, due to the carrier injection from source to channel with these conventional types of transistors, Subthreshold slope cannot go below 60 mV/decade. Therefore, to suppress the leak current, FETs with new carrier injection concepts have been proposed.

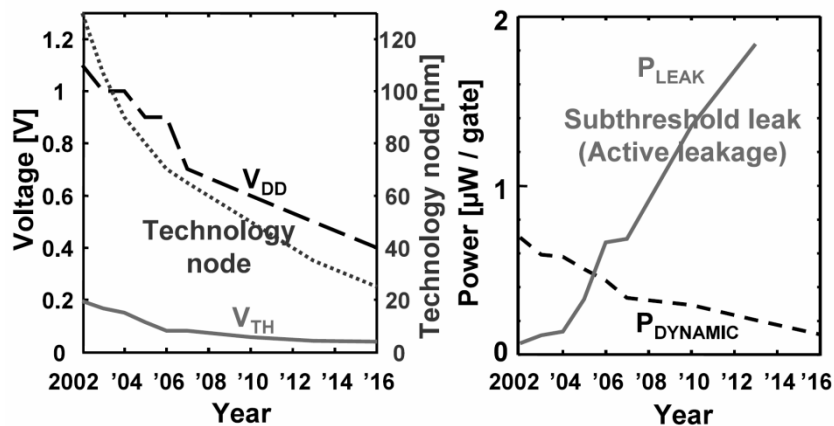


Figure 1.1 Active leakage makes things more challenging.

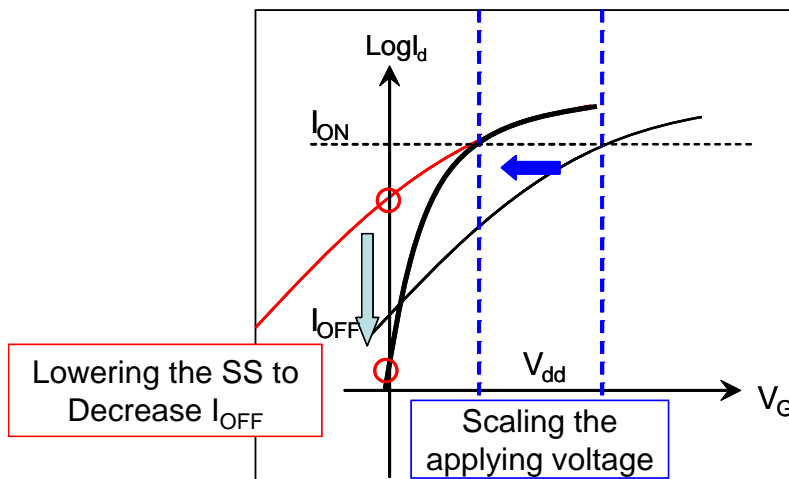


Figure 1.2 The more scaled device's Subthreshold region model.

I.4 tunneling FET

The table 1.1 shows the FETs with new carrier injection mechanisms. Tunneling FET uses the electron/hole tunneling probability so that a subthreshold slope less than 60 can be achieved. On the other hand, impact ionization FETs use impact ionization of the carrier to control the injection velocity of the carriers, so that the subthreshold slope can be kept small. Feedback FET uses the charge injection at the sidewall of the gate to modify the potential profile between on and off states. These new FETs have features that the off-current can be suppressed even at a temperature of operation. One of the issues of the FETs with new carrier injection mechanism is the degradation of the on-current, so that scaling in the operation voltage cannot be scaled. And also there exists a reliability problem with charge trappings during the operation. Therefore, among these devices, tunneling FET can be one of the candidates for future FETs with low power consumption.

Devicetype	n ⁺ -p-n ⁺ (Conv)	Tunnel(P-i-N) FET	Impactionizati onFET	FeedbackFET
SubthresholdSlope (mV/dec.)	60>	60<	60<<	60<<
TemperatureDepen dence of I _{off}	Large	Small	Small	Small
ON current	○	△	Small	Small
Scaling of V _{Apply}	○	○	△	△
Reliability Issues	—	—	Hot carriers	Charge injection into sidewall

Table1.1 Comparison of Various NEW Device types

I.5 Objective of this study

I perform a feasibility study of Schottky barrier FET as a tunneling FET. With the use of metal silicide, the parasitic resistance can be suppressed, so that the on-current can be increased. Moreover, by selecting the silicide material, we can modulate Schottky Barrier height to tune the device performance. It means the Device design can be flexible. Also, since dopants are not needed for device operation, metal/Si schottky interface is advantageous for device scaling, avoiding the punch-through effect in the FET.

II.1 Principle of the Schottky junction

The junctions between a metal and a semiconductor find numerous applications in microelectronic devices. Next to the implementation in Schottky source/drain transistors, the electronic industry has been using for several decades metallic junctions for the electric contacts between the semiconductor regions and the copper wires in integrated circuits.

II.1.1 Energy band diagram

In the case of metal and silicon contact, the potential that is called Schottky barrier height is formed at the metal and silicon interface that has the same commutation characteristics of a pn junction. The work function of metal and semiconductor is ϕ_m and ϕ_σ , respectively, and the electron affinity is χ . When the relationship $\phi_m > \phi_\sigma > \chi$ among ϕ_m , ϕ_σ and χ is defined $\phi_m > \phi_\sigma > \chi$, the Schottky barrier height is

$$\phi_B = \phi_m - \chi \quad (2.0)$$

The commutation is appeared from this potential. But, in fact the Schottky barrier height is measured that does not depend against metal work function ϕ_m . In generalization, the dependence on work function is small against ideal it. That reason is existence of interfacial trap and interfacial layer. A lot of models are suggested in relationship among Fermi level pinning. In this case, the only ideal case is considered. The transportation structure pass through thermal electron emission obtains over the potential and tunneling structure pass through Schottky potential as shown in Fig. 2.1.

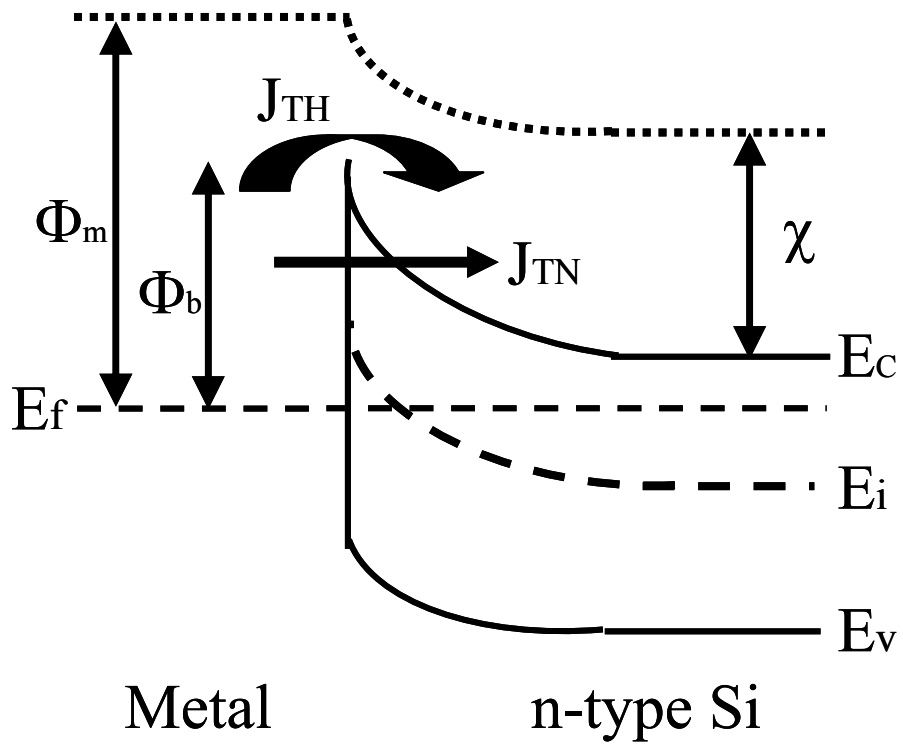


Fig. 2.1 schematic illustration of schottky diode band diagram

II.1.2 Effect of the surface states

The crystal configuration in bulk semiconductors differs from the surface due to the presence of dangling bonds at the boundaries of the lattice. Within the solid, the electrons are influenced by the periodic electrostatic potential resulting in the energy band configuration with the forbidden energy gap. At the surface, the potential is abruptly terminated and is no longer periodic. The band configuration no longer prevails, which means that electrons can occupy surface states whose wave function decays exponentially from the surface to the bulk (imaginary wave vector k). Some of these states have an energy located within the energy gap.

A simple model associates the surface states to the dangling bonds of the atoms at the surface. The unpaired atomic orbitals can either accept (acceptor states) or give up (donor states) an electron. The occupancy of donor and acceptor states is fully determined by the charge neutrality condition. A neutral level ϕ_0 is usually defined as the position of the Fermi level corresponding to electrical neutrality at the surface (Fig. I.2). The main effect of these surface states to the SBH is to reduce its dependency on the metal workfunction suggested by (I.1). Bardeen claimed that these surface states located at the Metal/semiconductor junction screen the effect of the metal to the semiconductor. In the absence of surface states, the negative charge Q_m on the surface of the metal must be equal and opposite to the positive charge Q_d due to the uncompensated donors in the depletion region. Due to their nature, surface states can also store charges, modifying the equilibrium situation $Q_m = Q_d$.

Let's consider the situation depicted in Fig. I.2-(a) where the band diagram is drawn following the Schottky model, assuming no effect of the surface states. The Fermi level is located below the neutral level of the surface. A positive charge is stored in the surface

states and the charge in the depletion region will be reduced accordingly to the neutrality condition. The reduction of the charge in the depletion region pushes the Fermi level towards ϕ_0 and the barrier height is lowered [see Fig. I.2-(b)]. Similarly, if the Fermi level is located above the neutral level, a negative charge is stored and the increase of the positive charge in the depletion region pushes again the Fermi level towards ϕ_0 . Therefore, E_0 acts as an attractor for the Fermi level. In the limit of high surface states density, the SBH remains constant whatever is the metal work function,

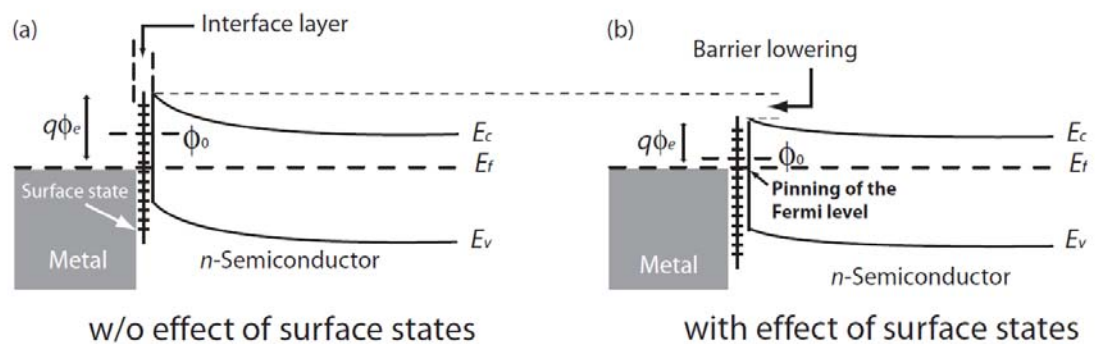


Figure 2.2 Energy band diagram of a Schottky contact without (a) and with (b) the effect of the surface states. The Fermi-level E_f is pushed towards the neutral level ϕ_0 .

II.1.3 Image-force barrier lowering

In the basic description of the Schottky junction, the Schottky barrier height (SBH) is said to assume a fixed value either given by (II.1.1) or by (II.1.2) in the first order of approximation. In practice, the barrier height is not only dependent on the nature of the metal and of the surface states, but also on the interaction between the metal and the carriers in the semiconductors. The effect of the metal to an electron is assumed to be equivalent to the interaction between the electron and a positive image charge located in the metal at the mirror-image of the electron with respect to the interface, which is the image-force mechanism. It modifies the band diagram according to Fig. 2.3 and yields an effective SBH lowering dependent on the electric field at the interface. The SBH lowering by image-force is observed either the Fermi level is pinned or not.

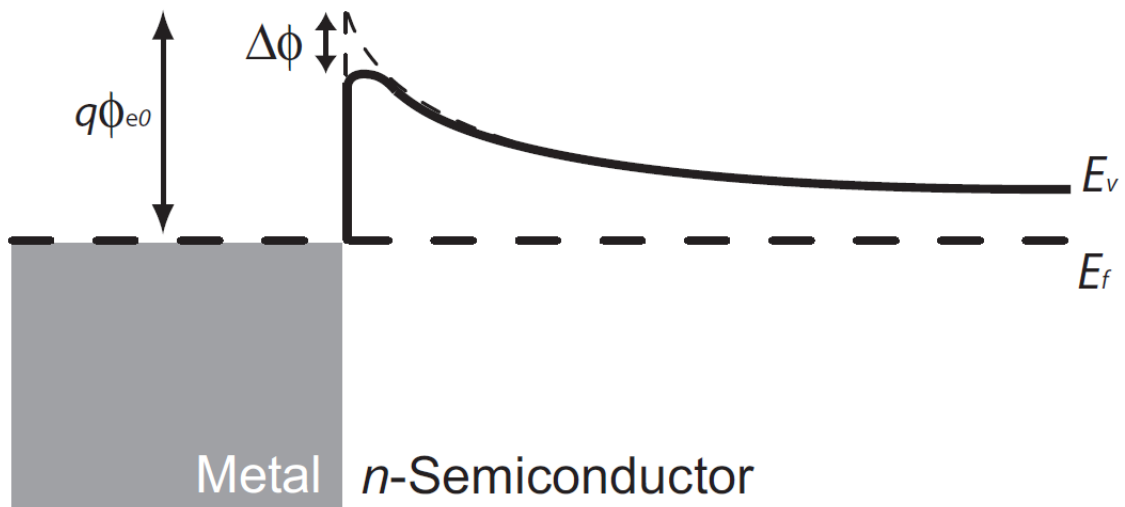


Figure 2.3 Sketch of the conduction band in a Schottky junction with image-force barrier lowering effect.

II.2 Current transport mechanisms

The current across a Schottky junction is mainly governed by two transport mechanisms:

1. The thermionic emission above the barrier
2. The quantum-mechanical tunneling (field emission) through the barrier

Moreover, when the carriers are transported through the depletion region the usual diffusion and drift mechanism appears in series with the thermionic and the field emission. The current is determined predominantly by the process causing the highest resistance to the carrier flow. For Si-based diodes at room temperature, it has been shown that the thermionic and field emission is the dominant factors for typical low SBH used in SBFETs.

II.2.1 Thermionic current

It is mentioned thermal emission structure. First of all, the electron current j_2 is considered about from semiconductor to metal as shown in Fig. 2.2. The electron does not collision in distance of space electron charge layer. The electron current pass over this layer to metal. The electron emission metal is higher electron energy than E_0 as shown Fig. 2.2.

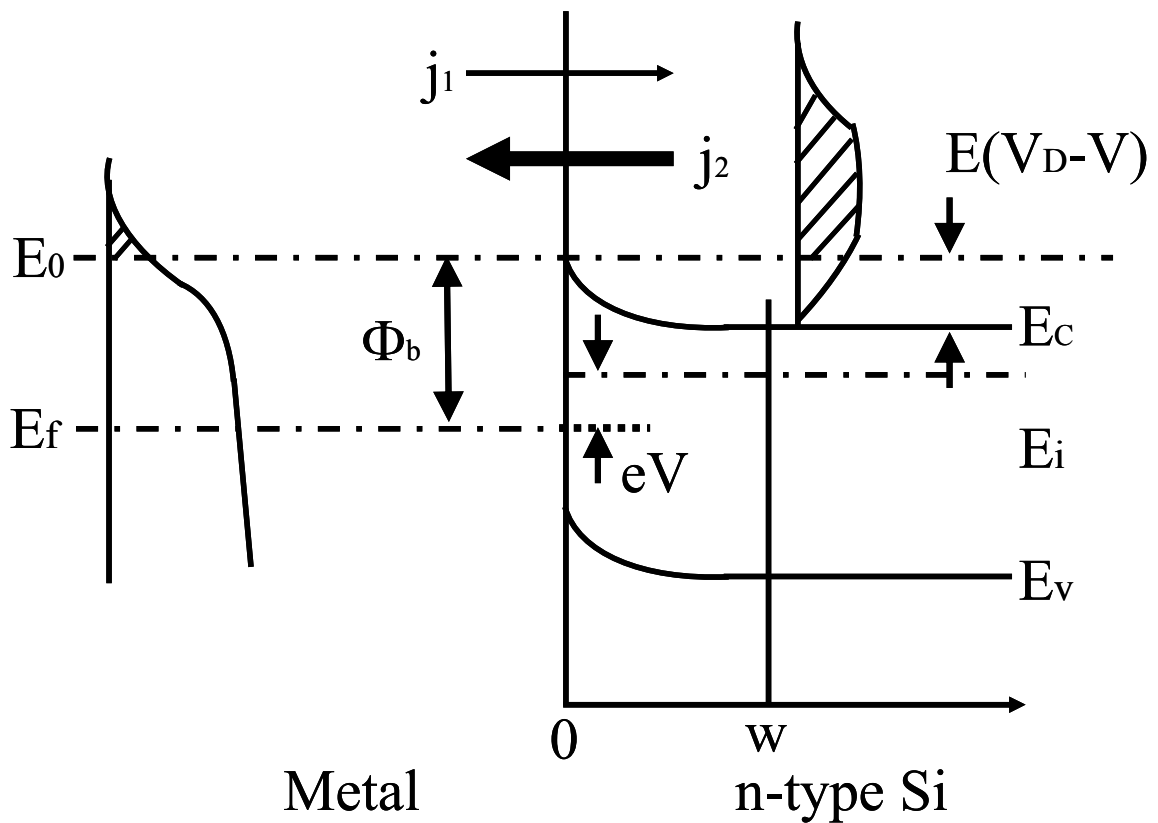


Fig. 2.2 schematic illustration of rectification of schottky contact [10]

$$j_2 = -\int v_x dn = -\int_{j_x > 0} V_x \cdot Z(E) f(E) dE$$

$$\begin{aligned}
&= -\int_0^{\infty} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} v_x \cdot 2 \frac{1}{8\pi^3} \cdot f(E) dk_x dk_y dk_z \\
&= -\frac{1}{4\pi^3} \int_0^{\infty} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} v_x \left\{ \exp\left(-\frac{E-E_f}{kT}\right) \right\} dk_x dk_y dk_z \quad (2.1)
\end{aligned}$$

But, $Z(E)$ is state density of electron, $f(E)$ is distribution function of electron, v_x is velocity element of x direction of electron, and m_e^* is actual mass of electron in semiconductor. The v_x is written

$$v_x = \frac{\hbar k_x}{m_e^*} \quad (2.2)$$

$$E = E_0 + \frac{\hbar^2}{2m_e^*} (k_x^2 + k_y^2 + k_z^2) \quad (2.3)$$

The equation (2.1) is equal to

$$\begin{aligned}
j_2 &= -\frac{1}{4\pi^3} \int_0^{\infty} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \frac{\hbar k_x}{m_e^*} \exp\left\{-\frac{\hbar^2(k_x^2 + k_y^2 + k_z^2)}{2m_e^* kT}\right\} \left\{ \exp\left(-\frac{E_0 - E_f}{kT}\right) \right\} dk_x dk_y dk_z \\
&= -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{E_0 - E_f}{kT}\right) \quad (2.4)
\end{aligned}$$

The semiconductor side is defined

$$E_0 - E_f = \phi_m - \chi - qV \quad (2.5)$$

$$\phi_B = \phi_m - \chi \quad (2.6)$$

The current pass through from semiconductor to metal is

$$j_2 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B - qV}{kT}\right) \quad (2.7)$$

And, the current from metal to semiconductor is $\phi_m - \chi - qV$ replaced by $\phi_m - \chi$.

$$j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \quad (2.8)$$

The net current is

$$j_2 - j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.9)$$

and current density is

$$j_{TH} = -\frac{4\pi q m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.10)$$

The current about thermal emission structure is

$$j_{TH} = J_0 \exp\left\{\left(\frac{qV}{nkT}\right) - 1\right\} \quad [8]. \quad (2.11)$$

$$j_0 = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \quad (2.12)$$

$$A^* = \frac{4\pi q m_e^* k^2}{h^3}. \quad (2.13)$$

A^* is Richardson constant, k is Boltzmann's constant, h is Planck's constant and T is absolute temperature. The n that is called ideal factor is $n=1$ in ideal Schottky contact, but in fact $n>1$. The reason of it is transport current in diffusion current, bias dependence of Schottky barrier height in image force, injection of minority carrier, and dependence of Schottky barrier in interfacial trap. The ϕ_b is written as

$$\phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_0}\right). \quad (2.14)$$

The ϕ_b can be looked for I-V measurement of Schottky diode. The other method for look for Schottky barrier height is relationship depletion capacitance and bias current.

II.2.2 Tunneling current

Next, it is considered about Tunneling structure. The tunneling is gave next equation [11]

$$J_{TN} = \frac{q^2 F^2}{8\pi\hbar\phi_B} \exp\left[-\frac{8\pi}{3hqF} \sqrt{2m_e^*(q\phi_B)^3}\right]. \quad (2.15)$$

But, F is field electric of vertical direction of semiconductor surface. The image of the image charge is added in schottky barrier ϕ_b

$$\phi_B = \phi_{B0} - \sqrt{\frac{qF}{4\pi\epsilon}}. \quad (2.16)$$

The ϕ_b is schottky barrier height when the field electric is not added, and the ϵ is silicon permittivity. The phenomenon that is lowered schottky barrier height in electric field is called schottky effect. The current in schottky interface expresses the sum of thermal emission current and tunneling current

$$J_{total} = J_{TH} + J_{TN}. \quad (2.17)$$

II.2.3 Space Charge capacitance of Schottky Contact

The space charge capacitance of schottky contact can be considered a kind of capacitor as well as pn junction. That has electric capacitance. If the potential in point x is $\phi(x)$, Poisson's equation is

$$\frac{d^2\phi(x)}{dx^2} = -\frac{qN_D}{\epsilon_0\epsilon_s}. \quad (2.18)$$

The (2.18) is done integral is

$$\frac{d\varphi(x)}{dx} = -\frac{qN_D}{\varepsilon_0\varepsilon_s}x + C_1 \quad (2.19)$$

$$\varphi(x) = -\frac{qN_D}{\varepsilon_0\varepsilon_s}x^2 + C_1x + C_2 \quad (2.20)$$

The x axis express Fig. 2.2, and beginning condition is $\varphi(x) = \varphi_0$ when x is equal to 0.

$$C_2 = 0 \quad (2.21)$$

x=w, and $d\varphi(x)/dx=0$

$$C_1 = -\frac{qN_D}{\varepsilon_0\varepsilon_s}w \quad (2.22)$$

The potential is

$$\varphi(x) = \frac{qN_D}{\varepsilon_0\varepsilon_s} \left(wx - \frac{x^2}{2} \right) \quad (2.23)$$

x=w, and $\varphi(w) = V_D - V$

$$w = \left\{ \frac{2\varepsilon_0\varepsilon_s(V_D - V)}{qN_D} \right\}^{\frac{1}{2}} \quad (2.24)$$

The electrostatic capacitance is

$$C = \frac{\varepsilon_0\varepsilon_s}{w} = \left\{ \frac{q\varepsilon_0\varepsilon_s N_D}{2(V_D - V)} \right\}^{\frac{1}{2}} \quad (2.25)$$

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_0\varepsilon_s N_D} (V_D - V) \quad (2.26)$$

The N_D and V_D can be search, if the function of $1/C^2$ versus bias V.

II.3 Measurement of the barrier height

The accurate extraction of SBH is crucial for the analysis of SBFETs. Typically, the barrier height of a Schottky diode can be measured in 4 ways:

1. from current-voltage (I-V) characteristics
2. from Arrhenius plot (saturation current vs temperature)
3. from capacitance-voltage (C-V) measurement
4. from photoelectric measurement

I will only focus our attention on the first method for practical reasons. The photoelectric measurement and the Arrhenius method require experimental setups that were not available for our study. Concerning the C-V method, the extraction of the barrier height is based on drastic hypothesis such as uniform doping profiles or nearly ideal diodes ($n \sim 1$). These conditions were not satisfied by our device lots. As mentioned in section II.2, the dominant transport mechanism in low doped Si-based diodes is the thermionic emission under forward biases. Considering the I-V characteristics for the SBH can be extracted by fitting the theoretical I-V relationship to the measurements.

$$I = AA^*T^2 e^{-q\phi_B/kT} (e^{qV/nkT} - 1) \quad (2.27)$$

It only works for relatively low forward bias ($V < 0.5$ V) and for diodes sufficiently close to ideal behavior (not so restrictive than for C-V measurements). In Fig 2.3, the SBH of a $1\mu\text{m}$ -by- $1\mu\text{m}$ PtSi/n-Si diode is extracted from the numerical fit to the measured I-V characteristics. Ideality factor is 1.2 and SBH is 741 meV. Since the linear region of the I-V characteristic is relatively small, the numerical fitting procedure may not be very accurate.

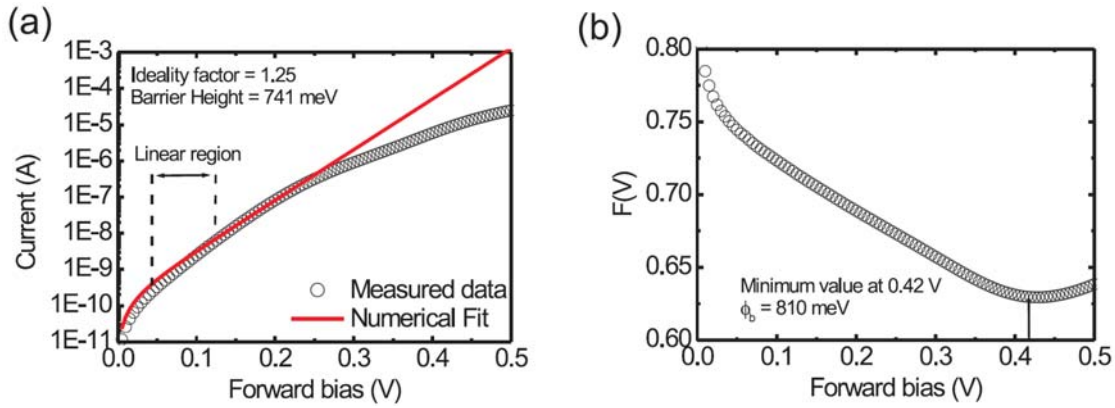


Figure 2.3 SBH extraction from IV curve by a numerical fit of (2.10) on the measured points (a) and by the minimum value (b) of the Norde function (1.8)

The reason of this lack of accuracy in the SBH extraction is the presence of a large series resistance mainly due to bad contact probes or not perfect ohmic contact on the backside of the Si substrate. H. Norde (1979) proposed an alternative way for the SBH extraction to avoid the effect of high series resistance by considering the following formula (2.28).

$$(2.28)$$

For small voltages, $F(V)$ is almost linearly decreasing with a slope of $-1/2$, while at large voltage the resistance may become dominant and $F(V)$ approaches a straight line with slope $= 1/2$. Between these two limit cases, $F(V)$ presents a minimum value, $F(V_0)$, which can be related to the barrier height, the barrier height is given by formula (2.29)

$$\phi_B = F(V_0) + \frac{V_0}{2} \frac{kT}{q} \quad (2.29)$$

The SBH extraction using (2.29) does not rely on a numerical fitting procedure and is therefore more accurate. Note that the method works also properly in the case of $R = 0$. In the following report, all the SBH are extracted from diode I - V curves with the Norte method.

III Introduction to Schottky Barrier tunneling FET

III.1 Operation principles

In Schottky barrier tunneling field effect transistor, the high doped semiconductor source and drain are replaced by metallic material.

III.2 Silicide materials

In MOSFET fabrication, Silicide often has been used for the materials of source/drain regions and gate electrodes. There are many kinds of metals (Ni, Ti, Co, Mo, W, Pt and so on...) for silicides. Especially, Ni-, Co-, and Ti- silicides with low resistivity have been studied for a long time. Though $TiSi_2$ was used in sub-micron era, it has relatively large sheet resistance when the line width becomes thin. Therefore, Ni and Co-silicides are used in 100nm- or smaller generations. Although $CoSi_2$ has very good electrical properties, its high Si consumption and junction spiking problems limit its application to deep sub-micrometer devices. The study on Ni silicide started to become an active research area in the 1970's and the silicide technology in MOSFET fabrication process since 1980's.

This thesis describes about Ni silicidation on bulk Si. Ni silicides are formed in variety formation, which are Ni_3Si , $Ni_{31}Si_{12}$, Ni_2Si , Ni_3Si_2 , $NiSi$, and $NiSi_2$. Fundamental data about Ni silicides are shown in table 3.1. The data indicate that $NiSi$ has the lowest resistivity, and the Ni to Si ratio is rather large for the formation of $NiSi$.

In the Ni- Si system, Ni atoms are the dominant diffusing species. Many people use silicide of $NiSi$ phase on bulk Si, a bilayer of Ni_2Si on top of $NiSi$ is formed first when Ni and Si films react.

Phase	Resistivity ($\mu\Omega\text{ cm}$)	Activation Energy E_a (eV)	Density (g/cm^3)	$T_{\text{silicide}}/$ T_{Ni}	Silicon consumed/ T_{Ni}
Ni	7-10	-	8.91	1	0
Ni₃Si	80-90	-	7.87	1.31	0.61
Ni₃₁Si₁₂	90-150	-	7.56	1.40	0.71
Ni₂Si	24-30	1.5	7.51	1.47	0.91
Ni₃Si₂	60-70	1.9	6.71	1.75	1.22
NiSi	10.5-18	1.4	5.97	2.20	1.83
NiSi₂	34-50	-	4.80	3.61	3.66
Si	Dopant dependent	-	2.33	-	-

Table 3.1 Fundamental data of Ni silicide.

III.3 Advantage and performance of SBTT

The SBFETs have been intensively studied for the last 10 years and have shown a growing interest from the industry because of their potentiality to replace the doped S/D region for sub-32 nm technology. In particular, the low contact resistance, the silicide/Si junction abruptness and the good immunization against short-channel effects together with a simple fabrication process make them very attractive as compared to conventional MOSFET.

III.3.1 Contact resistance improvement

Both the resistance of source/drain layer R_{sh} and the contact resistance to source/drain Si surface R_{co} are greatly reduced in advanced CMOS technology with self-aligned silicide. R_{sh} of the source-drain diffusion region is simply,

$$R_{sh} = \rho_{sd} \frac{S}{W} \quad (3.1)$$

, where W is the device width, S is spacing between the gate edge and the contact. The sheet resistance ρ_{sd} is of the order of 50-500 Ω/\square for the source drain without silicide.

As shown schematically in Fig.3.1, a highly conductive ($\approx 2-10 \Omega/\square$) silicide film is formed on all the gate and source-drain surfaces separated by dielectric spacers by the self-aligned process. Since the sheet resistance of silicide is 1-2 orders of magnitude lower than that of the source-drain, the silicide layer practically shunts all the currents, and the significant contribution to R_{sh} is from the nonsilicided region under the spacer. This technology is virtually regarded as the method which reduces the length S to 0.01-0.02 μm . $R_{sh}W$ should be no more than 50 $\Omega\text{-}\mu\text{m}$ in sub-micron MOSFETs. At the same time, R_{co} between the source-drain and silicide is also reduced, since now the

metal/semiconductor contact area is enlarged to the entire diffusion area. So it is one of the most important issues to enhance the on-current, especially for Nanowire MOSFETs in which the volume of source and drain region is limited as mentioned below.

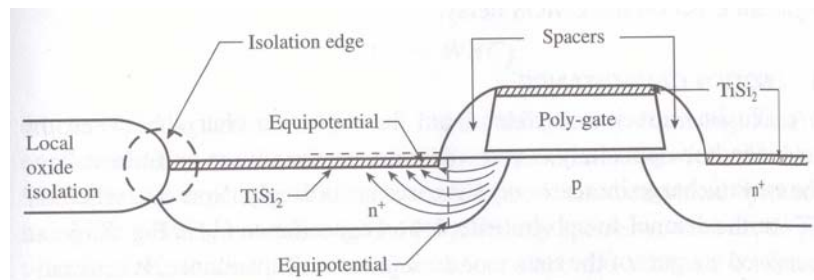


Figure 3.1 Schematic diagram of an- n-channel MOSFET fabricated with self-aligned TiSi_2 , showing the current flow pattern between the channel and the silicide .

III.3.2 Shape Source/Drain junction

Another problem associated with the aggressive downscaling towards 30 nm channel length and beyond is the bad abruptness of the doped S/D junctions. As it is shown in Fig. 3.2, the lateral diffusion of the S/D together with the large transition region from the S/D to the channel results in an overlap of the depletion region and even in an electrical contact between the S/D. The transistor switch behavior is therefore suppressed because the channel is always conducting, independently on the gate voltage. With silicidation reaction, the transition from silicide to Si is sharp to a single atomic layer for the composition and for the morphology. It also results in a better control of the

gate-S/D capacitive. Nevertheless, it produces also sharp edges where the electric field could be large, resulting in high leakage current from the edge of S/D. A solution has already been proposed in: longer Rapid Thermal Oxidation (RTO) times during the spacer deposition could round the edge and reduce the leakage current.

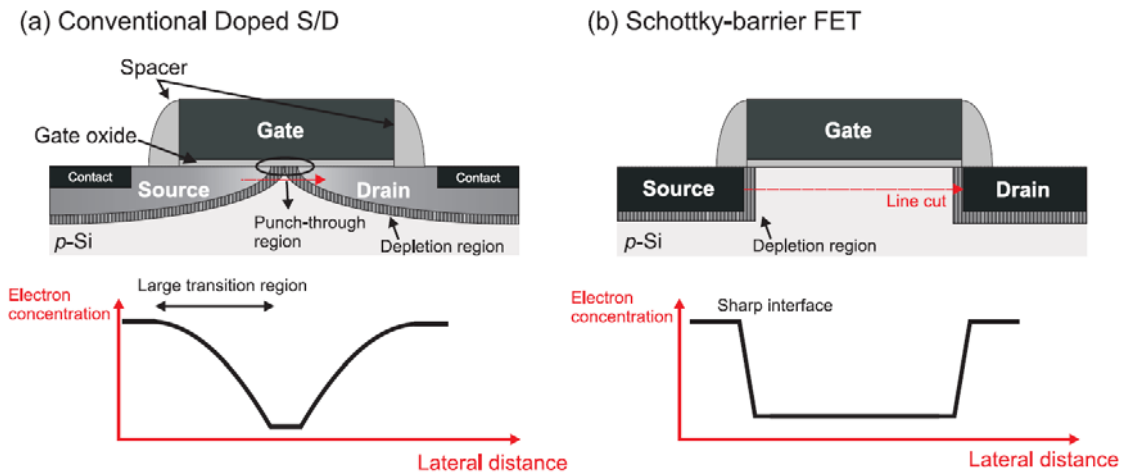


Figure 3.2 Illustration of the lateral junction diffusion in conventional MOSFETs (a) and in SBFETs (b).

III.3.3 Immunization short-channel effect

The influence of the SCE would be lowered with silicide S/D. Actually, the fixed potential barrier imposed by the Schottky junction properties prevents from electron/hole leakage and it is not modulated by the drain voltage. As a consequence, the thermal barrier for electrons and holes in the off-state is not reduced by the drain voltage as in conventional MOSFETs and DIBL is effectively reduced, leading to lower leakage current. But, the drain voltage has still an effect to the leakage because it increases the tunneling probability of electrons at the drain side through the substrate (as represented in Fig. II.6). The use of SOI substrate suppresses this leakage since the Si body is

isolated by the buried oxide from the substrate electrical contact.

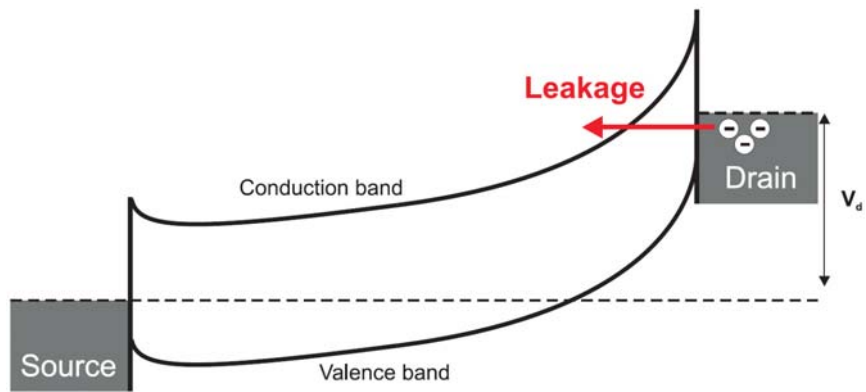


Figure 3.3 Influence of the drain voltage to the leakage current. Electrons tunnel from the drain to the channel at high drain voltage.

IV Fabrication and Characterization Method

IV.1 Schottky barrier tunneling FET Fabrication

IV.1.1 Fabrication Process

I fabricated the Schottky p-FET, using Ni silicide only at source region; Figure 4.1 shows the fabrication flow of the Schottky p-type FET.

40-nm thick SOI wafer was used for the starting material. Active area was defined by lithography and dry etching of SOI. The 30 nm gate oxide was formed by 1000°C dry oxidation. An amorphous Si layer was deposited and patterned for the gate electrode. To form a drain region in the SOI layer, PH₃, BF₂ was implanted at 30keV with a dose of 5x10¹⁴cm² to P⁺, N⁺ region respectively, followed by activation annealing was carried out at 800 °C for 5min. Source side of gate electrode as well as gate oxide were defined by the 2nd lithography and etched. After removing the gate oxide, Ni with the thickness 20 nm was deposited, followed by silicidation annealing at 600°C 30 sec. For the tunnel FET operation, the overlap of the schottky source/channel interface and the gate is essential. This was realized by NiSi encroachment phenomena; when Ni reacts with Si with limited volume such on SOI or nano-wire, NiSi encroaches into Si for certain silicidation condition as in ref[5]. We checked the overlap, using SEM observation as in figure 1(b). Finally, Al electrode 50 nm was deposited and patterned followed by F.G. annealing at 400°C 30 min.

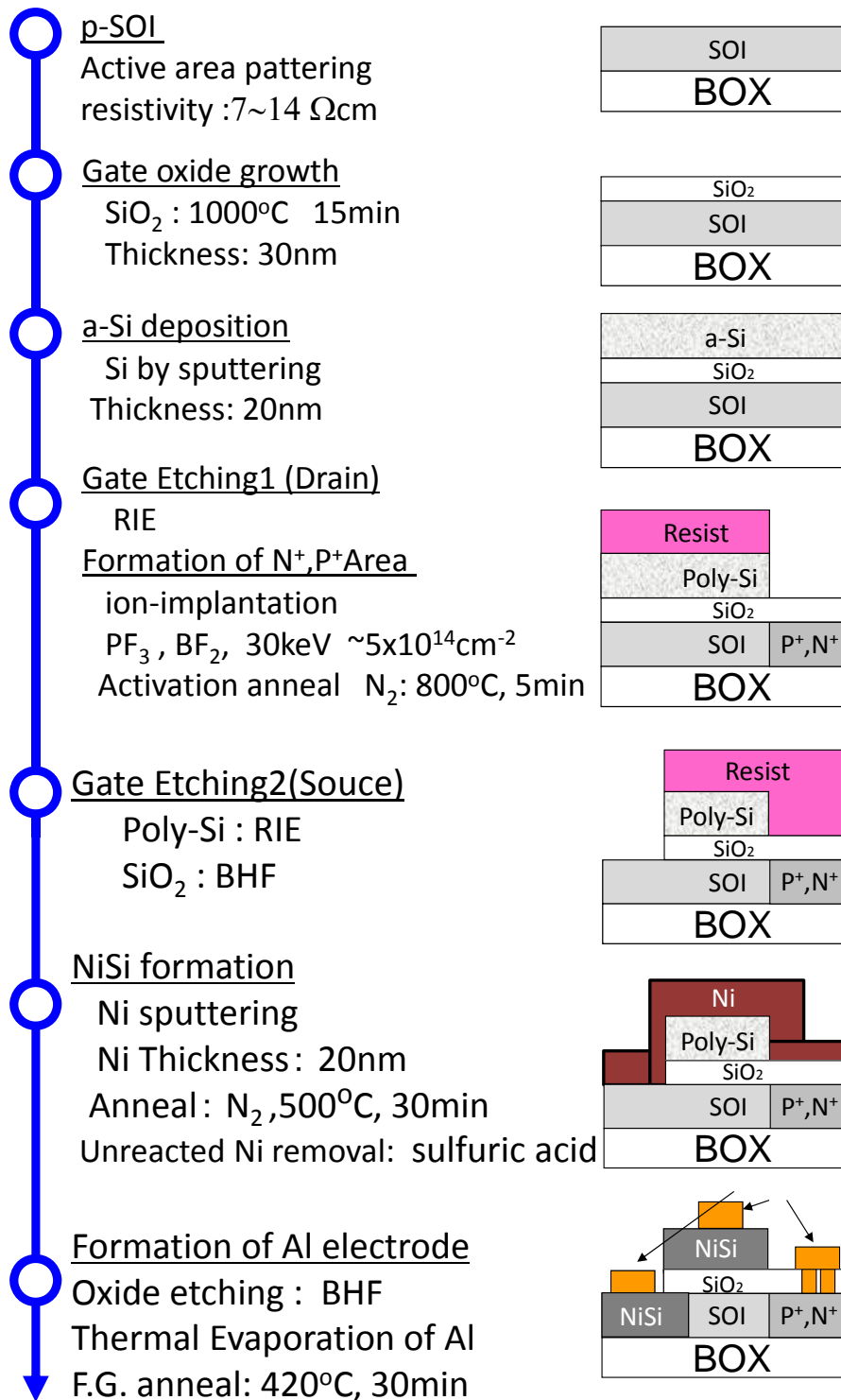


Figure 4.1 Schematic illustration of the two step Gate Etching fabrication flow.

IV.1.2 Substrate Cleaning

In order to facilitate high quality process technologies, ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness is required as a basis.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25°C. Ultra-pure water (UPW) system used in this study was that with the resistivity of more than 18.2 MΩc, which contains less than 1 colony of bacteria per milliliter and less than 1 particle per milliliter.

In this study, the Si substrate, oxide film and organic base resist was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al, although some steps were skipped. The first step, which use a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) ($H_2SO_4: H_2O_2=4:1$), was performed to remove organic materials and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid ($HF:H_2O=1:99$). Then the wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber for the next process as soon as it was dried by air gun. I showed the table 4.1 at wet chemical etching, the chemical reactivity of various silicides of interest.

Silicide	Insoluble In	Soluble In
TiSi ₂ ZrSi ₂ HfSi ₂	Aqueous alkali, all mineral acids except Hf, aqua regia, or H ₂ SO ₄ + H ₂ O ₂ mixture	HF—containing solutions
VSi ₂ NbSi ₂ TaSi ₂	Aqueous alkali, all mineral acids except Hf, aqua regia, or H ₂ SO ₄ + H ₂ O ₂ mixture	HF—containing solutions etch rate is low in (10:1) buffered hydrofluoric acid
MoSi ₂	Aqueous alkali, aqua regia, mineral acids	HF + HNO ₃
WSi ₂	Mineral acids, aqua regia	HF + HNO ₃
CoSi ₂	Nitric, sulfuric, or phosphoric acids; H ₂ SO ₄ + H ₂ O ₂ mixture	HF—containing solutions; boiling conc. HCl; conc. aqueous alkali
NiSi ₂	Nitric, sulfuric, or phosphoric acids; H ₂ SO ₄ + H ₂ O ₂ mixture	HF—containing solutions
PtSi	Aqua regia, HCl, HNO ₃ , H ₂ SO ₄ , HF, H ₂ SO ₄ + H ₂ O ₂	Slightly soluble in HF + HNO ₃
Pd ₂ Si	As above except for HNO ₃	HNO ₃ , HF + HNO ₃

Table 4.1 Chemical Reaction of Silicide

IV.1.4 Thermal Oxidation of SiO₂ Dielectrics

Thermal oxidation is accomplished by using an oxidation furnace (or diffusion furnace, since oxidation is basically a diffusion process involving oxidant species). A furnace typically consists of: 1) a cabinet; 2) a heating system; 3) a temperature measurement and control system; 4) fused quartz process tubes where the wafers undergo oxidation; 5) a system which transfers process gases into and out of the process tubes; and 6) a loading station used for loading (or unloading) wafers into (or from) the process tubes.

The heating system usually consists of several heating coils that control the temperature of the furnace tubes. The wafers are placed in quartz glassware known as boats, which are supported by fused silica paddles inside the process tube. The oxidizing agent (oxygen or steam) then enters the process tube through its source end, subsequently diffusing to the wafer surface where the oxidation occurs. Figure 4.2 shows a photo of Oxidation Furnace used in this study,.

Depending on oxidant species used (O₂ or H₂O), the thermal oxidation of SiO₂ may either be in the form of dry oxidation (wherein the oxidant is O₂) or wet oxidation (wherein the oxidant is H₂O). The reactions for dry and wet oxidation are governed by the following equations:

1) for dry oxidation: $\text{Si (solid)} + \text{O}_2 \text{ (vapor)} \rightarrow \text{SiO}_2 \text{ (solid)}$; and

2) for wet oxidation: $\text{Si (solid)} + 2\text{H}_2\text{O (vapor)} \rightarrow \text{SiO}_2 \text{ (solid)} + 2\text{H}_2 \text{ (vapor)}$.

Figure 4.3 shows the thermal oxidation rate using bulk P-Si substrate and SOI substrate which has 51 nm thick SOI, 137.8 nm thick BOX layer. The figure indicate that

SiO₂ thickness increases and residual SOI thickness decreases as increasing oxidation time.



Figure 4.2 Oxidation furnaces.

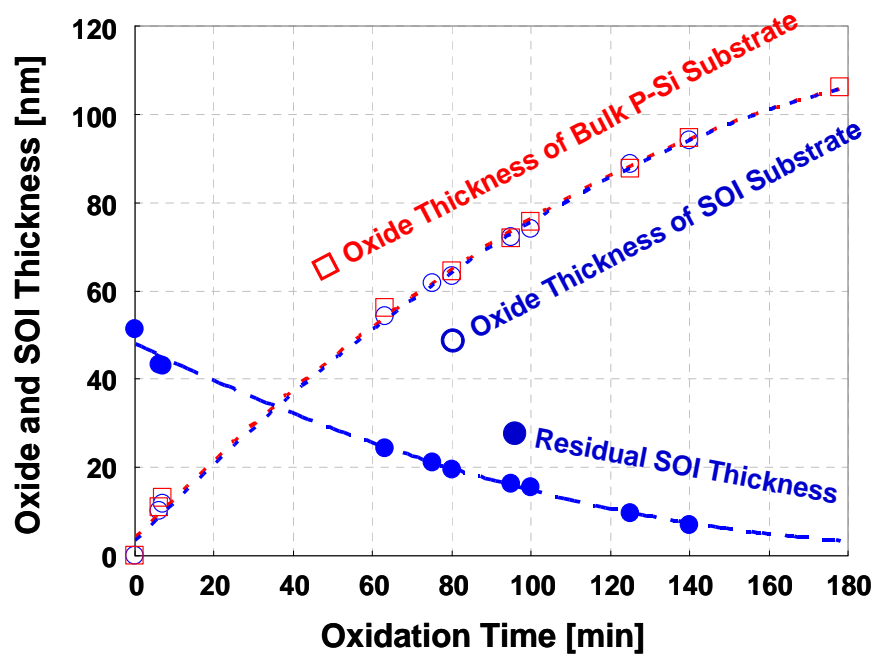


Figure 4.3 Oxide rate of dry oxidation.

IV.1.5 RF Sputtering of Gate Electrode

The film structures such as Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra-thin films on substrates. A high voltage across a low-pressure gas (usually argon at about 5 mTorr) is applied to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the “target,” composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to the substrate surface.

An UHV-sputtering system is used for thin film formations for the fabrication of electronic devices, for experiments of GMR, and for creating new high temperature superconductors materials. In this study, UHV Multi Target Sputtering System ES-350SU shown in fig.4.5 was used. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. For more details, Table 4.1 is attached for reference.

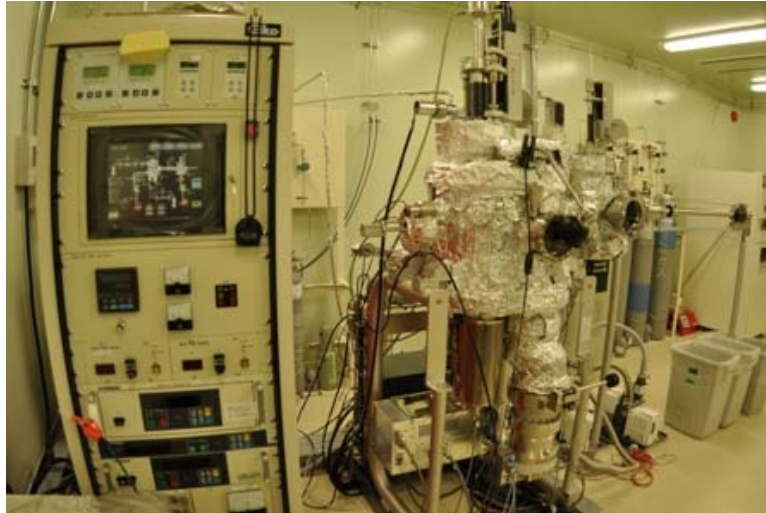


Figure 4.4 Photo of UHV Multi Target Sputtering System ES-350SU.

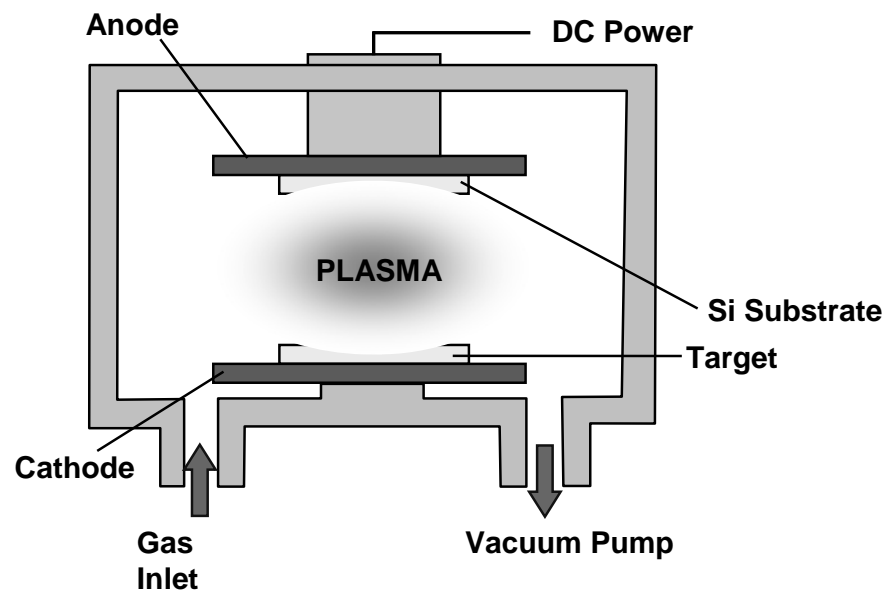


Figure 4.5 Structure of UHV sputtering system.

Growth chamber	1. Ultimate pressure	1.5 x 10 ⁻⁶ Pa
	2. Substrate size	2 inch in diameter
	3. Heating temperature	600°C
	4. Heater type	Lamp type heater
	5. Target	3 inch x 5 pieces (motor-driven)
Load lock chamber	6. Vacuum pumps	TMP 500L/sec and RP 250L/min
	7. Ultimate pressure	6.6 x 10 ⁻⁵ Pa
	8. Vacuum pumps	TMP60L/sec and RP90L/min
	9. Substrate holder with cooling function / Substrate holder with heating function / Cleaning function / Radical beam source	

Table 4.1 Specifications for UHV Multi Target Sputtering System ES-350S.

IV.1.6 Photolithography and Metal Gate Etching

The process flow and a photograph of the photolithography apparatus used throughout this study are shown in Figure.2.3. Electrical hotplate is used for the baking purposes. The spin-coated photoresist layer was exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light with the wavelength of 405 nm. MJB4 of Karl Suss contact-type mask aligner shown in Figure.4.6 was used for the photolithography process. The exposure duration was set to be 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.). The wafers were dipped into the solvent for 2 minute and baked at 130 °C for 5 minutes.

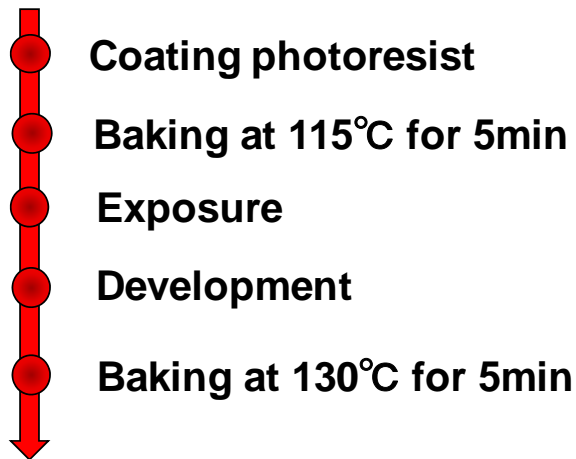


Figure 4.6 The process flow and the photo of photolithography apparatus.

IV.1.7 Thermal Annealing Process

Thin films of Ni/Si on Si substrate, was transferred to annealing furnace to perform thermal process. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation is QHC-P610CP (ULVAC RIKO Co. Ltd). Figure 4.7 is the photograph of the infrared annealing furnace, whose schematic illustration was shown in Figure 4.8. The annealing was performed by six infrared lamps surrounding the sample stage made of carbon-coated SiC. The heating temperature was controlled by thermocouple feedback loop.



Figure 4.7 Photo of infrared annealing furnace.

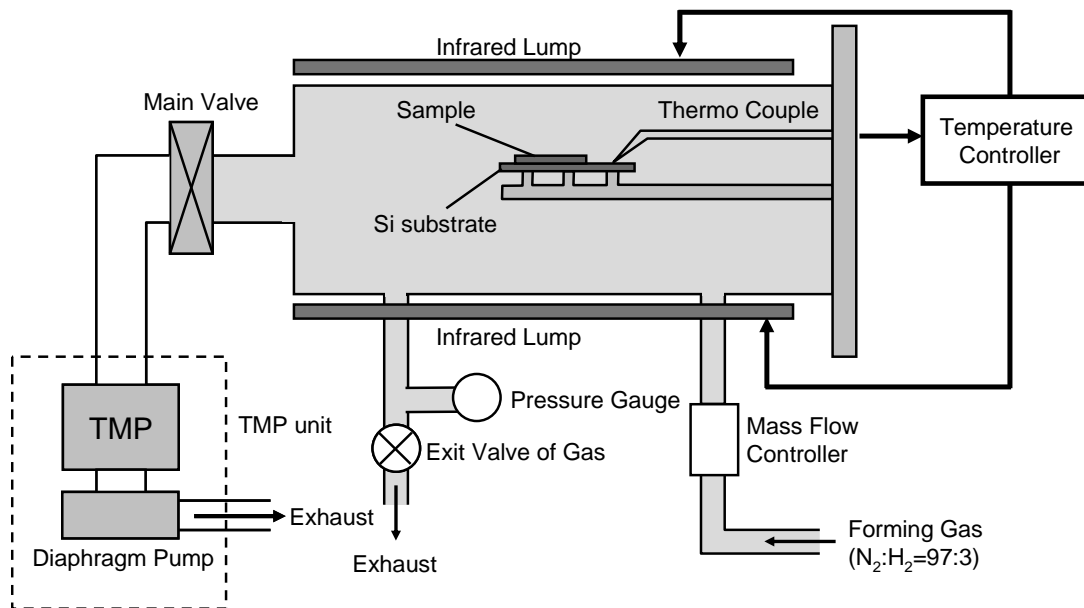


Figure 4.8 Schematic image of infrared annealing furnace.

IV.1.8 Thermal Evaporation of Al Layer (Source/Drain contact)

In this study, source, drain and backside electrodes were formed with Al. Al was deposited by thermal evaporation method in a vacuum chamber at a background pressure up to 1.0×10^{-3} Pa. A tungsten (W) filament is used to hold highly pure Al wires. Chamber pressure during evaporation was kept under 4×10^{-3} Pa. The illustration in Figure 4.9 shows the experimental setting.

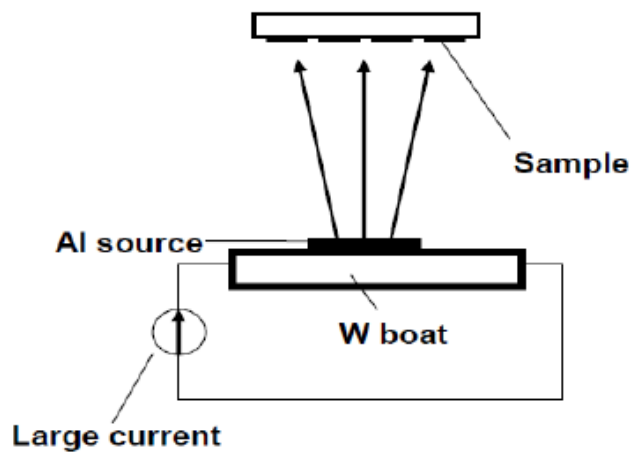


Figure 4.9 The schematic illustration of Al deposition

IV.2 Characterization Method and Result

After fabricating Schottky tunneling MOSFETs, I measured electrical characteristics of those devices. In this study, I mainly focused on subthreshold slope, V_{th} using various methods. In this section the method to estimate each parameter is explained.

IV.2.1 Characterization Method

This is done using HP4156A semiconductor analyzer with minimum measurement.

IV.2.2 I_d - V_g (I-V) Characterization

In this experiment, I fabricated Schottky barrier tunneling MOSFET for N-type and P-type, for electron and hole transportation. Threshold voltage was $-4.8V$ and $3.2V$,

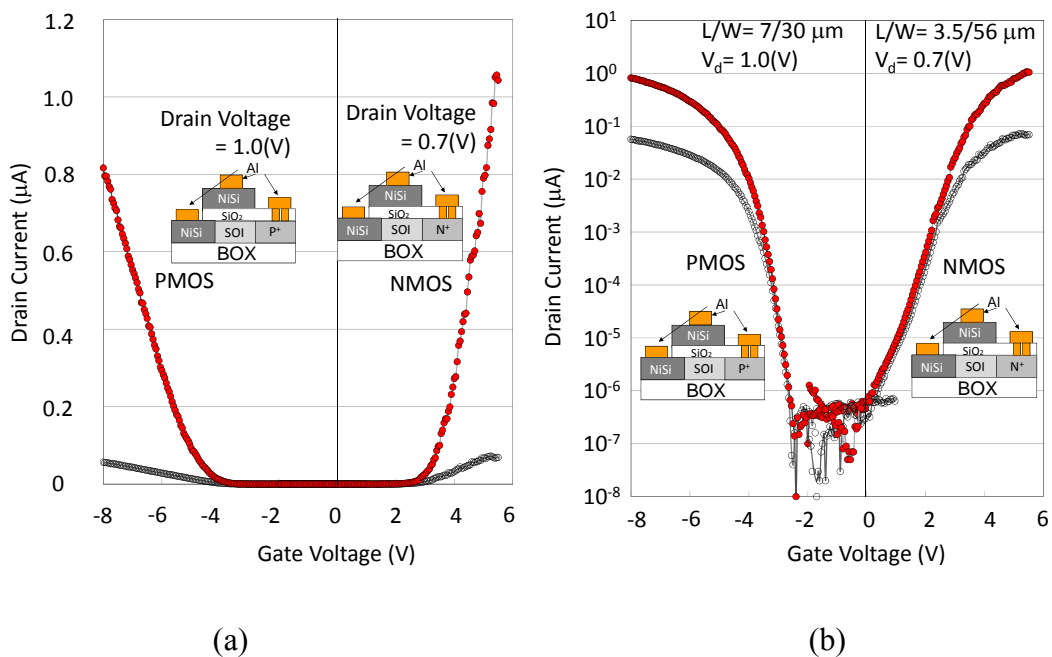


Figure 4.10 Electrical characteristics of NMOS and PMOS Schottky barrier tunneling MOSFET (a) $|I_d$ - V_g plot and (b) $\log |I_d$ - V_g plot.

IV.2.3 I_d-V_d (I-V) Characterization

In this result shows drain current – drain voltage characteristics of Schottky source P-type, N-type MOSFET. The measurement was performed at room temperature, solid transistor operation was obtained. Fairly nice FET operations were confirmed.

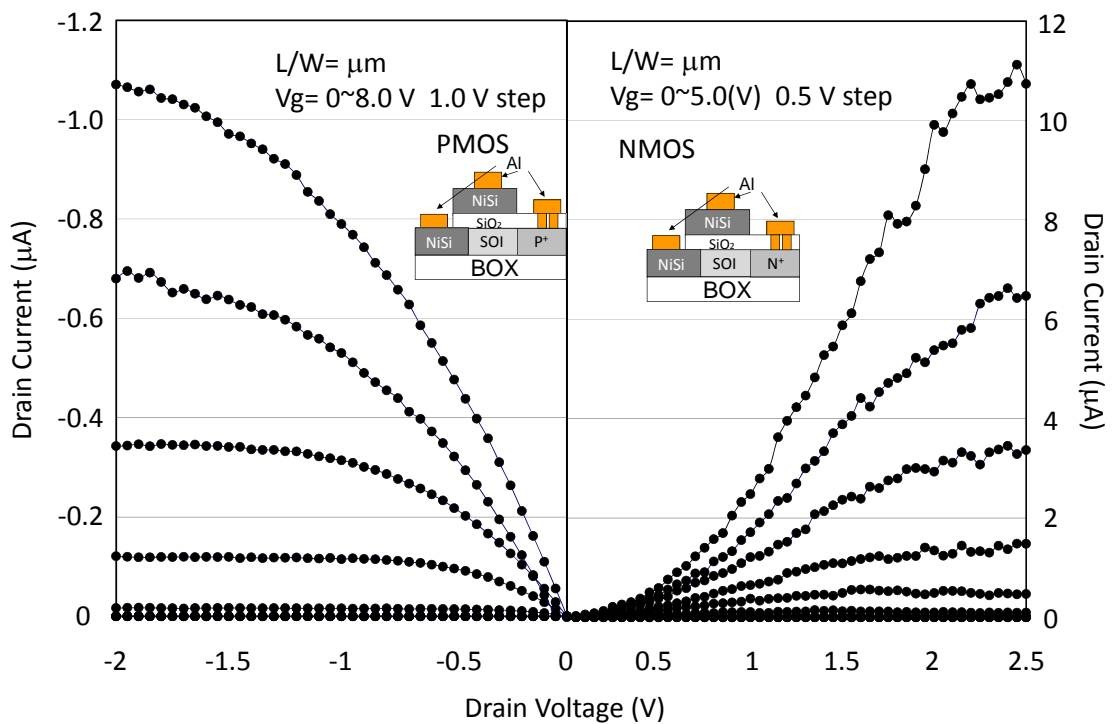


Figure 4.11 Electrical characteristics of PMOS Schottky barrier tunneling MOSFET I_d-V_d plot.

IV.2.4 Subthreshold slope measurement

Depending on the gate and source-drain voltages, a MOSFET device can be biased in one of the three following regions; subthreshold, linear or saturation. In the subthreshold region where $V_g < V_{th}$, the drain on the linear scale appears to approach zero immediately below the threshold voltage. However, on a logarithmic scale, the descending drain current remains at no negligible levels for several tenths of a volt below threshold voltage. This is because the inversion charge density does not drop to zero abruptly. Rather, it follows an exponential dependence on gate voltage. Subthreshold behavior is of particular important in modern ULSI application because it describes how a MOSFET device switches off (or turns on).

The subthreshold current is independent of the drain voltage once drain voltage is larger than a few kT/q , as would be expected for diffusion-dominated current transport. The dependence on gate voltage, on the other hand, is exponential with an inverse subthreshold slope (a.k.a. subthreshold swing).

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \quad (2-16)$$

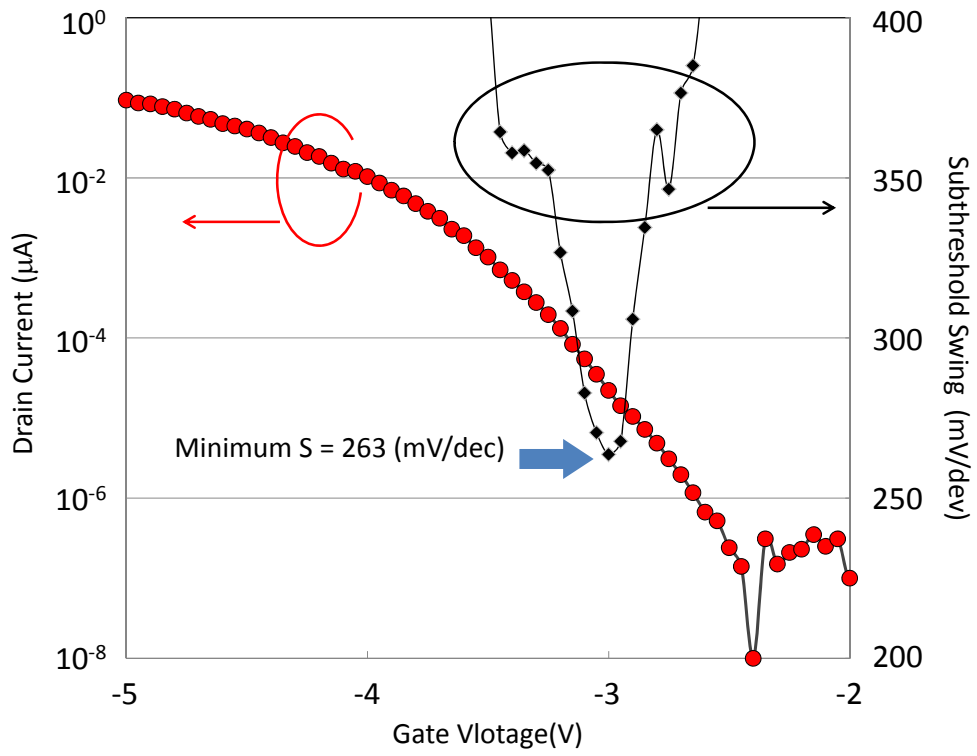


Figure 4.12 Electrical characteristics of PMOS Schottky barrier tunneling MOSFET I_d - V_d plot.

V.1 Observing Schottky barrier tunneling

Figure 5.1 shows the I_d - V_g characteristics of the device at varied measurement temperatures from 300K to 50K. The drain voltage was set to -1.5 V at P-type and 0.7 V at N-type. It is observed that the drain current decreases with the decrease in the measurement temperature at P-type and N-type respectively. This figure indicates that the thermionic emission current was decreased at low temperatures. On the other hand, SS is also decreased with the measurement temperature decrease.

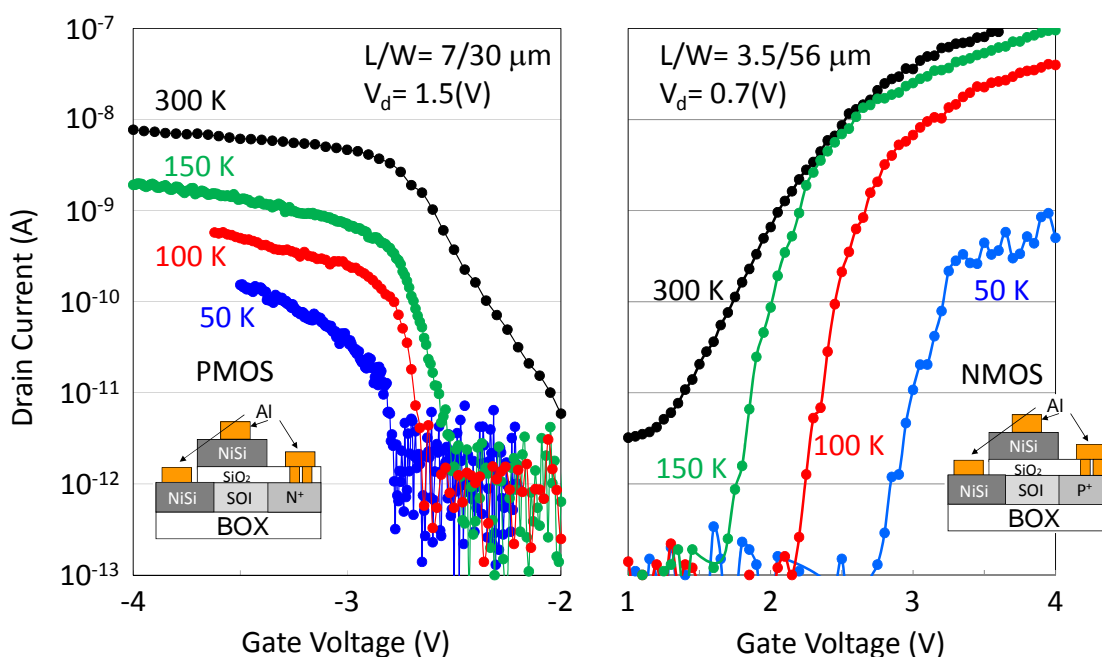


Fig. 5.1 Drain current vs. Gate voltage characteristics of the Schottky source P-type, N-type MOSFET for varied measurement temperatures

Figure 5.2 shows the dependence of the on-currents on temperature. Fairly straight relationship between $\ln(I_{on})$ and $1/T$ from room temperature down to 100K, was observed. This may suggest the suppression of thermally enhanced current component. However the decrease is rather saturated at 50K. We think that this phenomenon comes from the fact that true tunneling component dominate the conduction current.

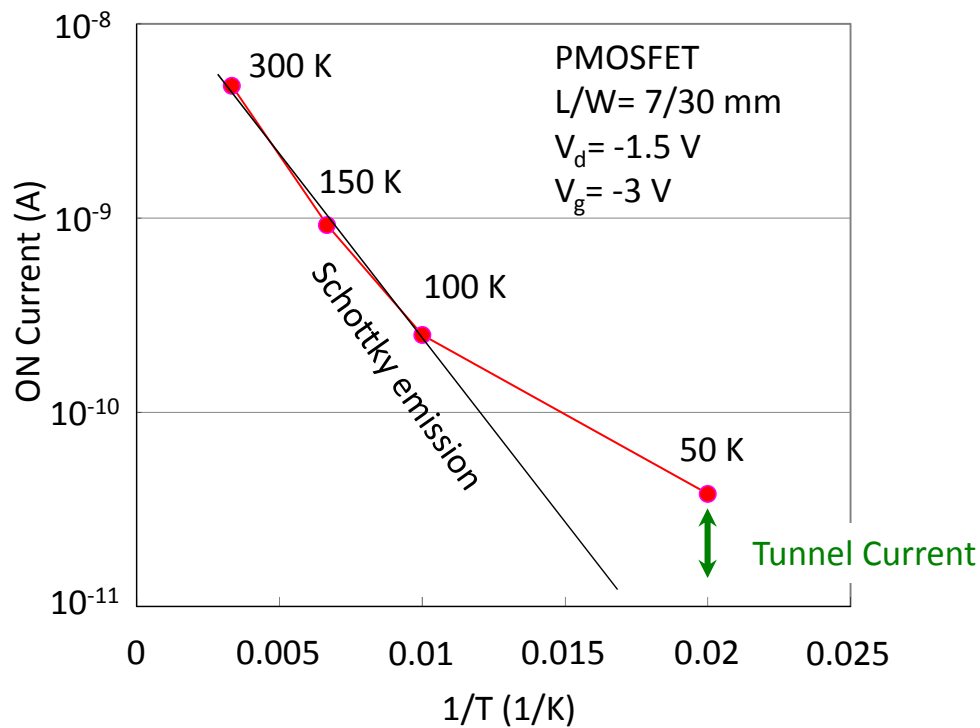


Fig. 5.2 On Current dependence on the measurement temperature.

Figure 5.3 shows the subthreshold slope dependence on the measured temperature. The result of the conventional MOSFET ($L=100\text{nm}$, $W=100\text{nm}$, $T_{\text{OX}}=15\text{nm}$) is also shown in this figure. The SS of the conventional MOSFET follows the equation $SS = \ln 10 kT/q$. Therefore, the SS shows a linear dependence on the absolute temperature passing through origin of coordinates as shown in the red line. However, our Schottky source FET, showed the drastic decrease in SS down to around 150K and very weak dependence of the SS on temperature below 150 K. As the tunneling current has weak dependence on the temperature, we can conclude that the constant subthreshold slope shows the fact that the device shows true tunnel FET characteristics at this temperature region.

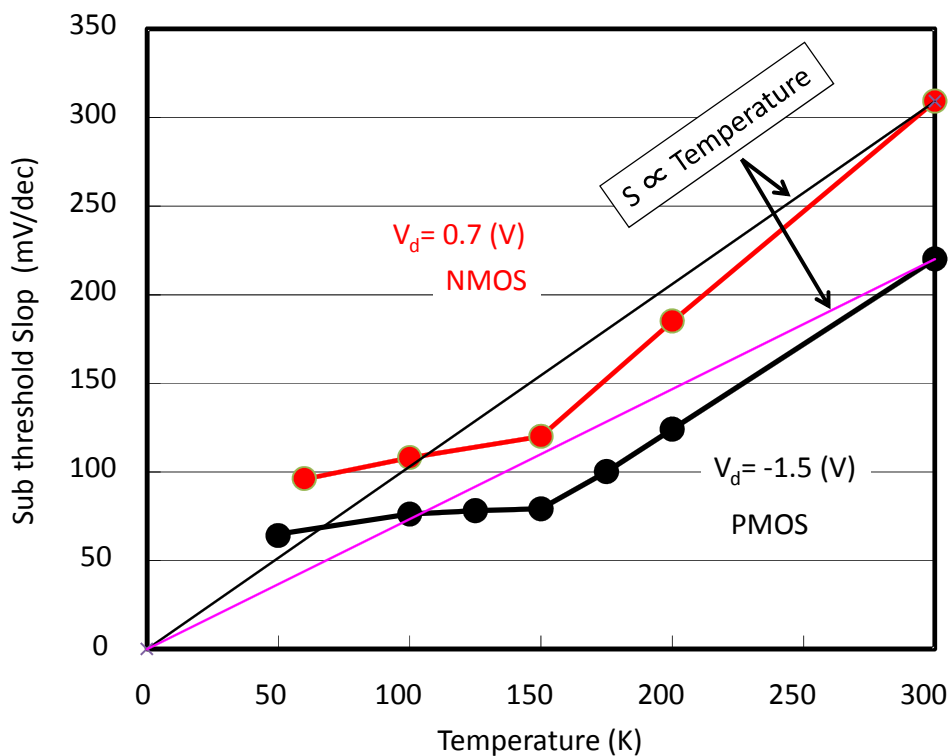


Fig. 5.3 Dependence of subthreshold-slope on temperature at drain voltage of N and P MOSFET.

V.2 Low temperature Characterization model

Figure 5.4 shows the concept of low temperature drain current measurement for the extraction of the tunneling component. At room temperature, the majority of the carrier injections are thermal emission, while the tunneling component cannot be detected easily in on-current because the ratio of the tunneling component is small among the whole on-current. However, at low temperature, the thermal injection decreases due to the carrier energy profile, and the component of the tunneling current becomes dominant. At off-state, both components are small however, as in the case of on-current, decreasing the measured temperature further reduces the thermal injection and not the tunneling current. Therefore, a weak dependence of the subthreshold slope should be observed.

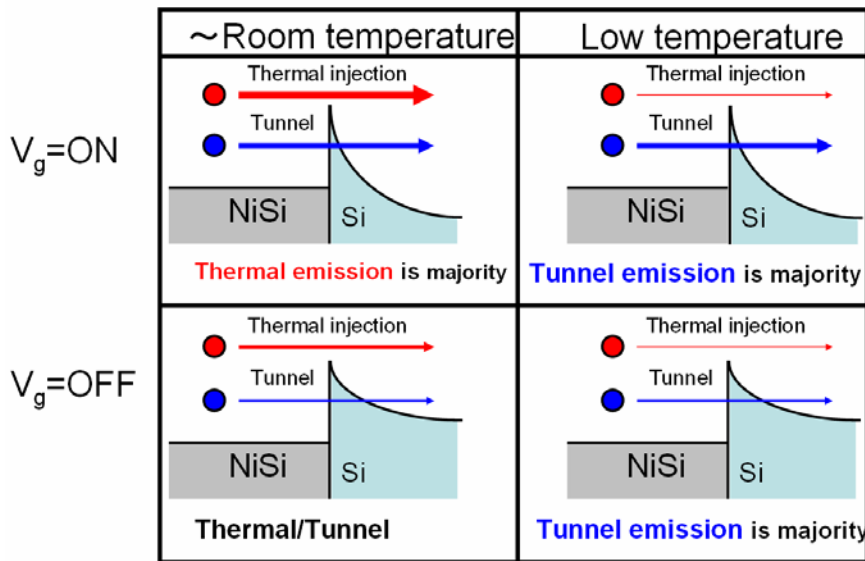


Fig. 5.4 The concept of low temperature drain current measurement for the extraction of the tunneling component

VI Conclusion

Schottky barrier p-type transistor with NiSi/Si schottky source was successfully fabricated and tunneling P-type and N-type FET characteristics was investigated through the low temperature measurement respectively. I could observe a current that does not follow the thermal emission model in on-current. And we could observe a weak dependency of subthreshold swing on the temperature below 150K. Finally, a pathway to increase the tunneling component was proposed.

$$J = J_0 \exp \left[-\frac{4\sqrt{2m^*} (q\phi_B)^{3/2}}{3q\hbar E_s} \right] \quad (1)$$

The tunneling current through a Schottky barrier can be express as the equation (1). Here we have Schottky barrier height ϕ_B , effective mass m^* and electric field E_s at the source/channel interface. Our purpose is to obtain T-FET which operate at room temperature. Therefore, in order to increase the tunneling current component at room temperature, the Schottky barrier height and the effective mass should be engineered to be small. The Schottky barrier can be tuned by material selection or by [6]. Also, the effective mass can be modulated by using strain techniques or by changing the substrates other than silicon. On the other hand, the electric field at the source contact should be large enough so that the width of energy barrier can be small. This can be achieved by changing the channel dopant concentration.