CONTENTS

Chapter 3

Ni Silicide into Si Nanowires using Nitrogen Incorporation

3.1 Introduction

   3.1 The effect of N Incorporation in Ni for Silicidation

3.2 Experiment

3.3 Result and Discussion

   3.3.1 SIMS depth profile of nitrogen in the deposited Ni film

   3.3.2 SEM images of Ni silicide formed in Si NWs

   3.3.3 Time dependence of the encroachment length of Ni silicide

   3.3.4 The effect of diameter on the encroachment length for silicidation

   3.3.5 Annealing Temperature Dependence of Ni Silicidation for Si Nanowire

3.4 Conclusion of this section

Reference

   Chapter 4

4.1 Introduction

   4.1.1 Suppression model of nitrogen Incorporation in Si Nanowire

4.2 Experiment

4.3 Result and Discussion

   4.3.1 The encroachment results for the four samples

   4.3.2 Discussion of Suppression model of nitrogen Incorporation

4.4 Conclusion of this section

Reference

Chapter 5

Conclusion of This Study

Acknowledgments

Chapter1

Introduction

1.1 Background of This Study

1.2 CMOS Downsizing limit and after that

1.3 Silicion Nanowire Field Effect Transistor

1.4 Silicon Nanowire Ni Siliside

1.4 Nickel Silicidation for Si Nanowire and The Encroachment Phenomenon

 1.4.1 The Reason for the Silicidation of Source and Drain regions

 1.4.2 Ni Silicide on Bulk Si

 1.4.3 Nickel Silicidation for Si Nanowire and The Encroachment Phenomenon

 1.4.4 Silicon Nanowire Ni Silicide

1.1 Background of This Study

Nowadays, CMOS Large Scale Integrated circuits (LSIs), are really indispensable components for our human society. Needless to say, but almost all the human activities, such as living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc. cannot work without the help of the CMOS LSI operation. For example, all the bank activities immediately stop without CMOS computation. Cellular phones do not exist without CMOS technology. Also, it should not be forgotten that CMOS semiconductor industry is one of big driving force of world economy, which is not limited to semiconductor fields but also includes many different kinds industries of materials, equipments, and software's required for the integrated circuits.

The continuous progress of CMOS technologies in terms of high-performance operation and low power consumption have been and will be very important because of the following three reasons.

At first, under the rapid progress of aging population and falling birth rate, we need to accelerate the replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example. For the penetration of such intelligent robots to the daily family use, much higher intelligence and much lower power consumption than those of today are required. Therefore the development of CMOS integrated circuits with much more high performance and low power consumption are indispensable.

Secondly, our society is now facing the global warming. The reduction of the CO_2 gas release is a critically urgent issue for the earth. Continuous progress of CMOS technologies contributes to the 'cooling of the earth' in two ways. One is direct contribution to the power reduction for IT (Information Technology) devices. Explosive

increase of energy consumption at office and home are demanded to be suppressed by so called 'Green IT' procedure. This can be done by the development of low power and high performance CMOS devices such used to data centers, routers and terminals, together with the high-efficient DC power feeding technology. Another contribution of the CMOS technology is to save the total power consumption of any kinds of systems – from those for entire city transportation traffic to those for individual car operation – by the optimum power saving control of the operation by intelligent CMOS processors.

Thirdly, continuous progress of CMOS technology is critically important from the semiconductor industry point of view, as well as from the global economical point of view. Because of the merits in performance and power consumption from 65 to 45 nm node logic devices, and because of the high-density or cost merit from 8 to 16 Gbit flash memories, LSI products are sold well in the market every 2 or 3 years to replace the products of previous generations. In case if there is no more progress in the CMOS technologies, semiconductor industry will face a disaster, and hence, the world economy will be in a crisis.

It is well known that the progress of CMOS LSI has been accomplished by the downsizing of MOSFETs. In the past, there were many downsizing limits predicted already from the 0.8 micron-meter generation since 1970's. It was fortunate, however, that those limits were proven not to be true by the fabrication of smaller dimension MOSFETs and confirmation of their excellent electric characteristics. However, it has been predicted by most of the engineers now, that the downsizing would reach its limit probably about the gate length of 5 nm around the year of 2020. 2020 is not too far, but there is no sufficiently clear image for the world after CMOS reaches its scaling limit.

1.2 CMOS downsizing limit and after that

Why it is expected that about 5 nm is the limit of the downsizing? There are four main reasons; A) Difficulty on off-current suppression, B) Difficulty on increase in on-current, C) Difficulty on decrease in gate capacitance, D) Production and development cost increase.

A. Difficulty on off-current suppression

With decrease in gate length, off-current – the subthreshold and direct-tunneling leakage currents between source and drain – becomes significant at the gate length of 5~3 nm. From the consideration of the integration of huge number of MOSFETs in a chip, and resulted huge entire off-leakage current, probably, around 5 nm could be regarded as the limit of the gate length reduction. It might be even 10 nm or 3 nm, depending on the number of MOSFET integrations. Below 3 nm, the direct-tunneling leakage current increases very significantly and it is almost impossible to suppress the off-leakage current.

B. Difficulty on increase of on-current

Already the conduction of the drain current enters in the semi-ballistic region and thus, no significant increase of the drain saturated current or on-current is expected by reducing the gate length below 5 nm. Also, increase in source/drain resistance of small geometry MOSFETs tends to suppress the on-current.

C. Difficulty on increase of MOSFETs speed

One of the scaling merits is to reduce the gate capacitance, C_g, because the switching

time of MOSFETs is defined by $C_g V_{dd}/I_d$, where I_d is the drain on-current and V_{dd} is power voltage. However, C_g will not decrease in proportion to the gate length because of gate electrode sidewall capacitance component and that of drain/source-to-gate electrode overlap. These capacitance components are very difficult to be reduced because the gate electrode thickness and source/drain areas are very difficult to be further reduced.

D. Production and development cost increase

It is expected that the structure and manufacturing process of such small dimension MOSFETs with huge number of integration on a chip becomes very complicated and the development and production cost of the CMOS LSI would become to expensive to retain the profit for the production.

E. Possible solution after that

It is not sure exactly at what gate length and exactly at what year, the downsizing of MOSFETs reach its limit, but most of the engineers are expected that it would be happen around at the gate length of 5 nm and around in the year of 2020, although it could be 10 nm in 2015 or 3 nm in 2030.

Then, what will be the world after we reached the limitation. Unfortunately, at this moment, there are no candidates among the so-called 'beyond CMOS' or 'Post Si' new devices, which are believed to really replace CMOS transistors used for the products of highly integrated circuits within 20 years. Our opinion is that we need to still continue CMOS based transistors with 'More Moore' approach with combining that of 'More than Moore.' Then, what is 'More Moore' approach after we reached the downsizing

limit or with no more decrease in gate length? Because the number of the transistors in a chip is limited by the power consumption, we could continue the 'More Moore' law for certain period by replacing current CMOS transistors by NW or nanotube MOSFETs with which the suppression of off-leakage current and increase of on-current under low voltage could be realized because of its nature such as quasi-one-dimensional conduction, multi- quantum channel per wire/tube and high-density integration of wire/tube in multi-layers. Figure 1.1 shows our roadmap for wire and tube MOSFETs after 2020.
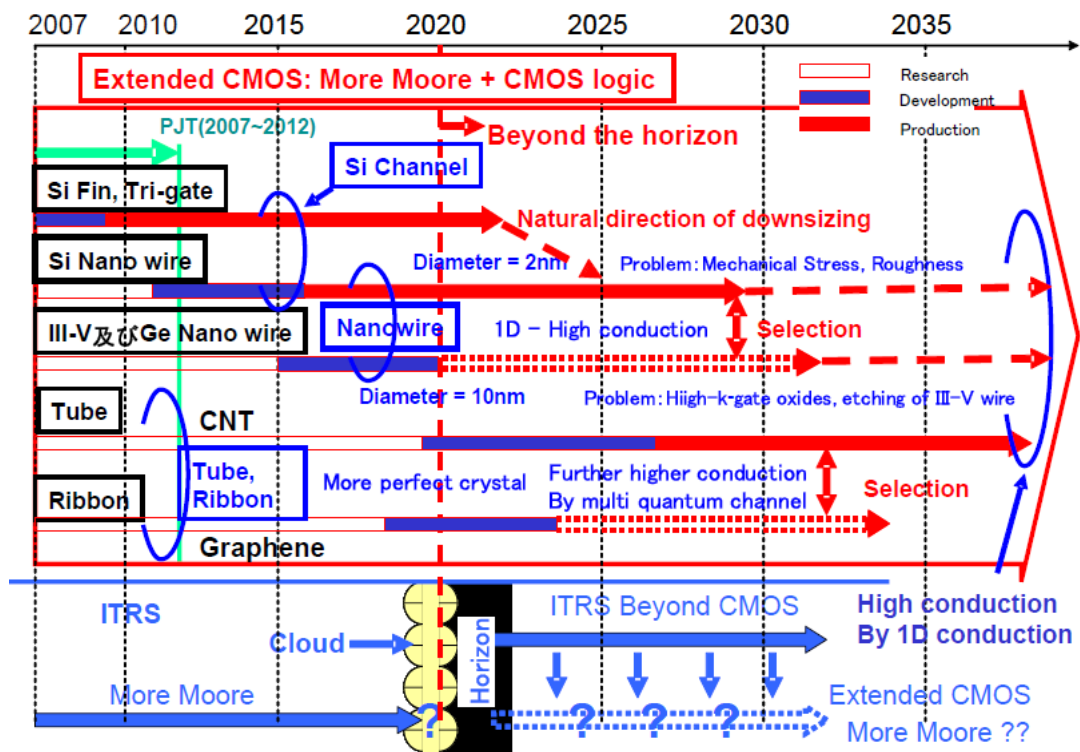

Figure 1.1 Rordmap for wire and tube.

1.3 Silicon Nanowire Field Effect Transistor

Si nanowire(NW) FET is considered as one of the promising technologies for further device downsizing, owing to its gate-all-around (GAA) structure which enables better gate control capability than planar transistors [1-2]. Figure 1.2 shows schematic image of GAA structure. Therefore, high I_{on}/I_{off} ratio can be achieved. Figure 1.3 shows comparison of the requirement to the bulk Si, the ultra-thin body fully depleted (UTB FD) SOI and the double-gate (DG) MOSFET in 2009 in ITRS2009 with previously reported data on Si NW FET fabricated using CMOS compatible processes [3-9]. Si NW FETs have already been obtained higher I_{on}/I_{off} ratio than any planer transistors.
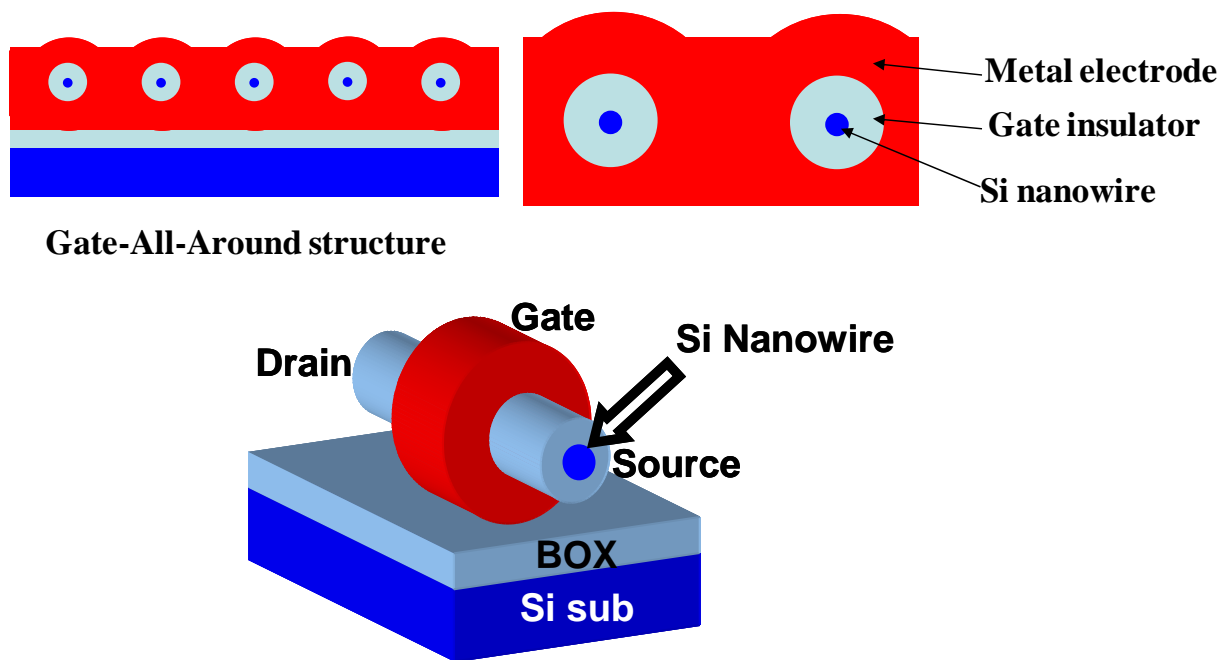

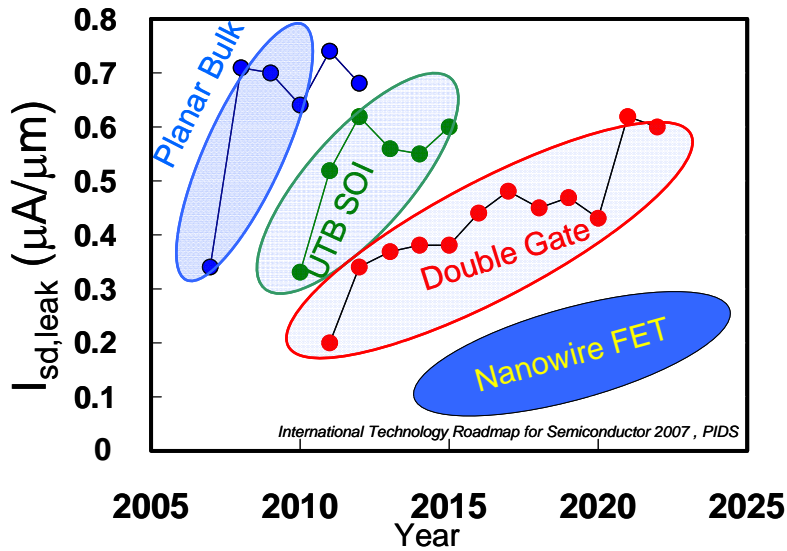**Figure 1.2** Schematic of GAA structure.

Figure 1.3 Comparison of the requirement to the bulk Si, UTB FD SOI and DG MOSFET in 2009 in ITRS2009 with previously reported data on Si NW FET fabricated using CMOS compatible processes.

Si NW FET has been fabricated by several techniques, Si fins are patterned by lithography and etching followed by the oxidation (Figure 1.4 (a) shows Top-down method) or Methods using CVD, MBE and other processes to grow Si NW with better controllability of the size of the wire (Figure 1.4 (b) shows Bottom-up method) [10-11].
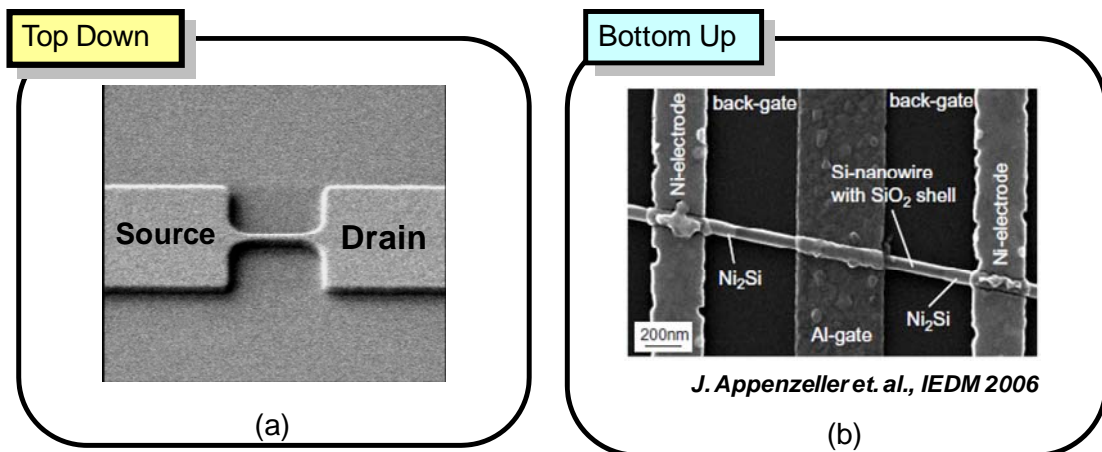

Figure 1.4 Fabrication methods of Si NW FET, (a)Top-down,(b)Bottom-up

The electrical characteristics of Si NW FET are not yet completely understood, therefore, it should be clarified. Fabrication guideline for the shape control of Si NW must be facilitated. In addition, the interface characteristic of the insulator on it, the geometry intolerances and surface roughness created by the Top-down processing as well as the strain, influence the transistor characteristic (mobility and threshold). In addition, another concern on Si NW FET is the increase in parasitic resistance at source and drain region, which eventually reduces the on-state current.

1.4 Nickel Silicidation for Si Nanowire and The Encroachment Phenomenon

1.4.1 The Reason for the Silicidation of Source and Drain regions

In MOSFET fabrication, Silicide often has been used for the materials of source/drain regions and gate electrodes. There are many kinds of metals (Ni, Ti, Co, Mo, W, Pt and so on…) for silicides. Especially, Ni-, Co-, and Ti- silicides with low resistivities have been studied for a long time. Though $TiSi_2$ was used in sub-micron era, it has relatively large sheet resistance when the line width becomes thin. Therefore, Ni and Co-silicides are used in 100 nm- or smaller generations. Although $CoSi_2$ has very good electrical properties, its high Si consumption and junction spiking problems limit its application to deep sub-micrometer devices [1]. The study on Ni silicide started to become an active research area in the 1970's and the silicide technology in MOSFET fabrication process since 1980's [2-4].

1.4.2 Ni Silicide on Bulk Si

This section describes about Ni silicidation on bulk Si. Ni silicides are formed in variety formation, which are NiSi, Ni_2Si, $NiSi_2$, Ni_3Si, $Ni_{31}Si_{12}$ and Ni_3Si_2. Fundamental data about Ni silicides are shown in table 3.1 [5-6]. The data indicate that NiSi has the lowest resistivity, and the Ni to Si ratio is rather large for the formation of NiSi.

Phase	Resistivity ($\mu\Omega$cm)	Activation Energy E_a (eV)	Density (g/cm3)	$T_{silicide}/T_{Ni}$	Silicon consumed/ T_{Ni}
Ni	7-10	-	8.91	1	0
Ni_3Si	80-90	-	7.87	1.31	0.61
$Ni_{31}Si_{12}$	90-150	-	7.56	1.40	0.71
Ni_2Si	24-30	1.5	7.51	1.47	0.91
Ni_3Si_2	60-70	-	6.71	1.75	1.22
NiSi	10.5-18	1.4	5.97	2.20	1.83
$NiSi_2$	34-50	-	4.80	3.61	3.66
Si	Dopant dependent	-	2.33	-	-

Table 3.1 Fundamental data of Ni silicide.

1.4.3 Nickel Silicidation for Si Nanowire and the Encroachment

This section describes about Nickel Silicidation for Si NWs and the Encroachment. Figure.3.1 shows Schematic figure of encroachment of Ni Siliside Si NWs. The reaction of Ni and Si take place at thermal treatment. Due to the diffusion of Ni atoms into Si NWs, Ni silicide starts to form inside the Si NWs, encroachment of Ni silicide occurs.

The Si NWs are covered with SiO_2. Therefore, Lateral Encroachment of Ni Silicide into Si NWs is different from bulk Si reaction. It has been reported that the full-silicidation leads to excessive Ni diffusion into Si NWs [7] and this phenomenon may lead to some adverse issues such as uncontrollable channel length as well as short circuit between source and drain.
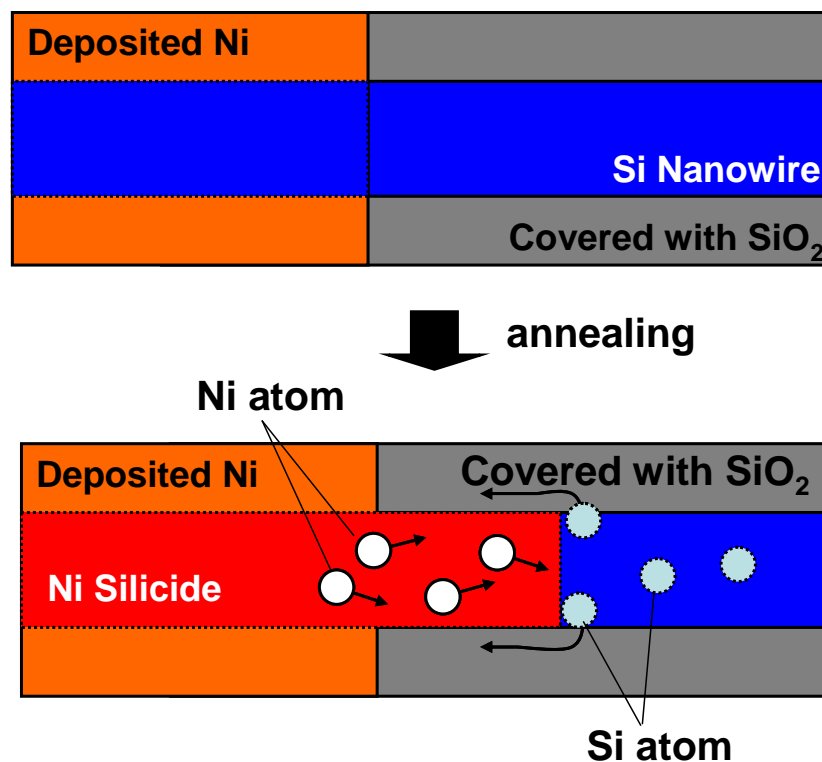

Figure. 3.1 Ni Siliside in Si NWs is formed by lateral Ni diffusion. Due to interstitial diffusion, Ni atom diffuse though Si than though silicide.

1.4.4 Silicon Nanowire Ni Silicide

The reaction of Ni and Si takes place at thermal treatment. Due to the diffusion of Ni atoms into Si NW, Ni silicide starts to form inside the Si NW, encroachment of Ni silicide occurs [17]. Figures1.5 shows schematic figures of the encroachment of Ni silicide into Si NW. The length of encroachment is a function of annealing time and temperature.
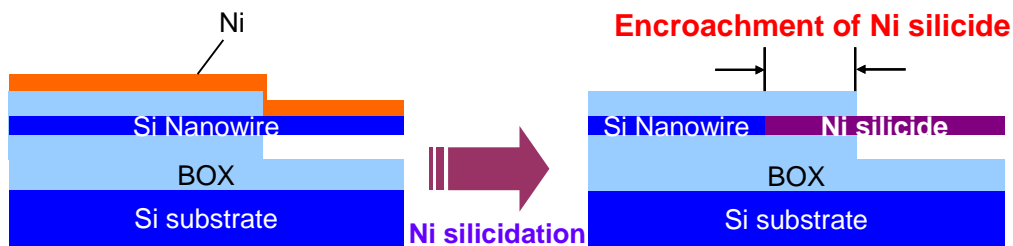

Figure. 1.5 Schematic figures of encroachment of Ni Silicide Si NW.

Figures1.5 show SEM and TEM images of Ni silicide contact for Si NW. Si NW with a diameter of 30 nm was covered with a SiO_2 of 50 nm. The Ni silicide NW is formed from the edge of the Si NW. A brighter contrast of the NW near the oxide edge indicates the formation of Ni silicide in this region. The figure on the right hand side shows the plane TEM image of the formed Ni silicide in the Si NW. A darker contrast in the NW also indicates the encroachment of Ni silicide into the Si NW. Here, we can see that there is no volume expansion due to the incorporation of Ni in the Si NW. And also Ni silicide and Si NWs are smoothly connected. When it occurs in sub-micron-generation MOSFETs, This phenomenon may lead to junction leakage of S/D as well as

uncontrollable effective channel length modulation. Therefore, in this thesis, A measure for the suppretion of this phenomenon is investigated in order to develop Ni full-silicidation of Si-NWs.
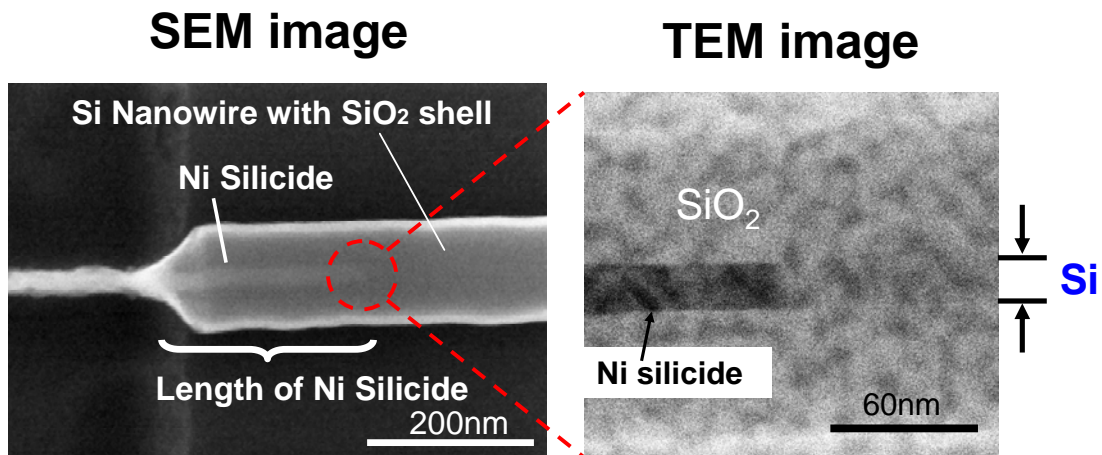

Figure. 1.6 SEM and TEM images of Ni Silicide of Si NW.

1.5 Purpose of this thesis

First, Si nanowire (NW) FET is one of the promising candidates for high-speed LSI devices in the future. Figure.1.7 shows Schematic figure of encroachment of Si NW MOSFET. In order to reduce the parasitic resistances of Si nanowires, the silicidation of the S/D regions is a very effective method. However, it has been reported that the full-silicidation leads to excessive Ni diffusion into Si NWs [17] and this phenomenon may lead to some adverse issues such as uncontrollable channel length as well as short circuit between source and drain. On the other hand, there is a report that the diffusion of Ni could be suppressed by nitrogen incorporation into the Ni film prior to the silicidation. [18-22]. This thesis describes about Nickel Silicidation of Si NW using nitrogen incirporation method and the mechanism for the suppression
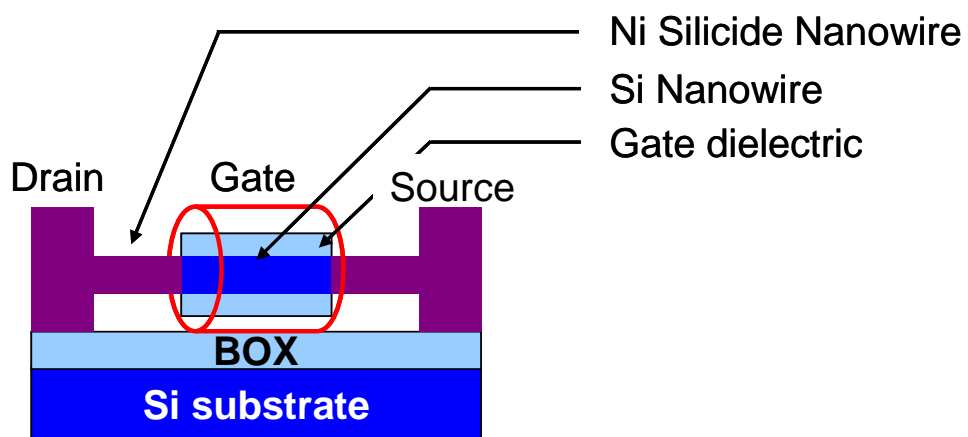

Figure.1.7 Schematic figure of encroachment of Si NW MOSFET

Refernces

[1] S. D. Suk *et al., IEDM Tech Dig.*, p. 717, 2005.

[2] S. D. Suk *et al., IEDM Tech Dig.*, p. 1, 2006.

[3] N.Singh et al., *IEDM*, p.547, 2006

[4] Y. Tian et al, IEDM, p.845, 2007

[5] K. H. Yeo et al., IEDM, p.539, 2006

[6] H. Lee et al., VLSI Tech. Symp., p.58, 2006

[7] W. W. Fang et al., *IEEE EDL*, vol. 28, no.3, p.211, 2007

[8] C. Dupre et al, IEEE, p749, 2008

[9] International Technology Roadmap for Semiconductor (ITRS), 2008 up data

[10] J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, and S. Guha , *Technical Digest of IEDM*, pp. 555 (2006).

[11] J. T. Sheu, S. P. Yeh, C. H. Lien, and S. T. Tsai, *Japanese Journal of Applied Physics*, Vol.45 , No.4B, pp. 3686-3689 (2006).

[12] R. Mukai, S. Ozawa and H. Yagi. *Thin Solid Film* 270 (1995)567

[13] H. Jeon, C. A. Sukow, J. W. Honeycutt, G. A. Rozgonyi and R. J. Nemanich. *J. Appl. phys.* **71** (1992) 4269

[15] F. Deng and R. A. Johonson. *J. Appl. Phys.* **81** (1997) 8047

[16] Toyota Morimoto, Tatsuya Ohguro, Hisayo Sasaki Momose , Toshihiko Iinuma, Iwao Kunishima, Kyouichi Suguro, Ichiro Katakabe, Hiroomi Nakajima, Masakatsu Tsuchiaki, Misuki Ono, Yasuhiro Katsumata, and Hiroshi Iwai, *IEEE TRANSACTIONS ON ELECTRON DEVICE*, VOL.42, NO.5 (1995)

[17] H. Arai, et al, ECS Transactions (2009) 25(7,ULSI Process Integration

6), 447-454.

[18] Sun II Kim et al., *J.Electrochem.Soc*., **157** (3), H231-H234 (2010).

[19] T. Ohguro et al., *International Electron Devices Meeting.,* 95-453 (1995)

[20] O. Soon-Young et al., *Japan Journal of Applied Physics.,* Vol, 44, No.4B, 2005, pp. 2142-2146

[21] S. Migita. et al., *Solid State Devices and Materials*., pp. 686-687 (2008).

[22] L. Wielunski et al., *Appl.Phys.Lett*., **38**, 106 (1981).

Chapter2

Fabrication and Characterization Method

Fabrication and Characterization Method

2.1 Experimental Procedure

2.1.1 Si Substrate Cleaning Process

At first, high quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25°C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩcm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the Si substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The first step, which use a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4: H_2O_2=4:1), was performed to remove any organic material and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:99). Then the cleaned wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber to deposit as soon as it was dried by air gun.

2.1.2 Oxidation Furnace

Thermal oxidation is accomplished by using an oxidation furnace (or diffusion furnace, since oxidation is basically a diffusion process involving oxidant species), which provides the heat needed to elevate the oxidizing ambient temperature. A furnace typically consists of: 1) a cabinet; 2) a heating system; 3) a temperature measurement and control system; 4) fused quartz process tubes where the wafers undergo oxidation; 5) a system which transfers process gases into and out of the process tubes; and 6) a loading station used for loading (or unloading) wafers into (or from) the process tubes.

The heating system usually consists of several heating coils that control the temperature of the furnace tubes. The wafers are placed in quartz glassware known as boats, which are supported by fused silica paddles inside the process tube. A boat can support many wafers. The oxidizing agent (oxygen or steam) then enters the process tube through its source end, subsequently diffusing to the wafers surface where the oxidation occurs. In this study, Figure 2.1 shows a photo of Oxidation Furnace.

Depending on oxidant species used (O_2 or H_2O), the thermal oxidation of SiO_2 may either be in the form of dry oxidation (wherein the oxidant is O_2) or wet oxidation (wherein the oxidant is H_2O). The reactions for dry and wet oxidation are governed by the following equations:

1) for dry oxidation: Si (solid) + O_2 (vapor) $\rightarrow$ SiO_2 (solid); and

2) for wet oxidation: Si (solid) + $2H_2O$ (vapor) $\rightarrow$ SiO_2 (solid) + $2H_2$ (vapor).

Figure 2.2 shows the thermal oxidation rate using bulk P-Si substrate and SOI substrate which has 51 nm thick SOI, 137.8 nm thick BOX layer. The figure indicat that SiO_2 thickness increases and residual SOI thickness decreases as increasing

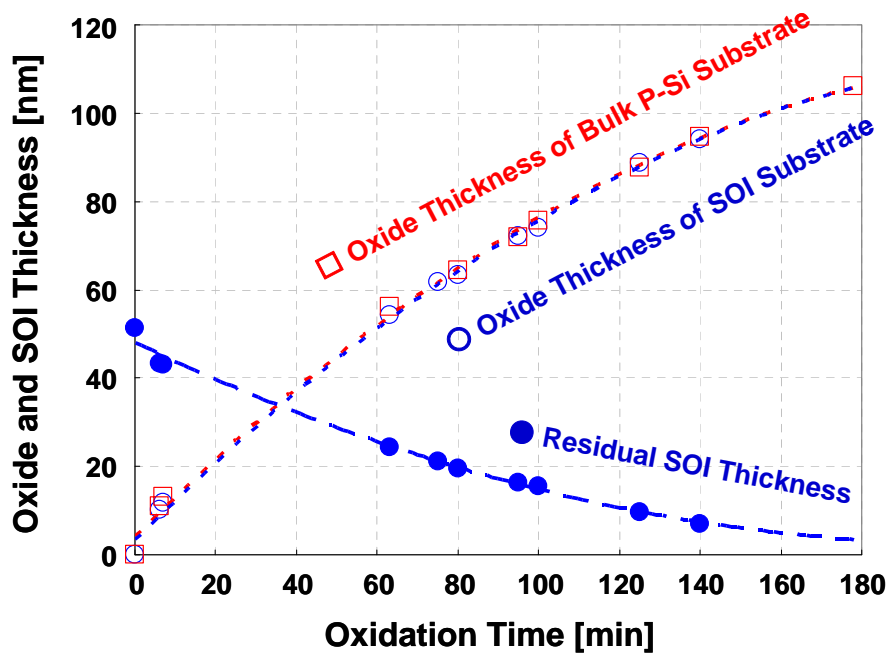oxidation time.

Figure 2.1 Oxidation furnace.

Figure 2.2 Oxide rate of dry oxidation.

2.1.3 Photolithography

The process flow and a photo of the photolithography apparatus used throughout this study are shown in Figure.2.3. Electrical hotplate is used for the baking purposes. The spin-coated photoresist layer was exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light with the wavelength of 405 nm. MJB4 of Karl Suss contact-type mask aligner shown in Figure.2.3 was used for the photolithography process. The exposure duration was set to 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.). The wafers were dipped into the solvent for 2 minute and baked at 130 ˚C for 5 minutes.

Coating photoresist

Baking at 115℃ for 5min

Exposure

Development

Baking at 130℃ for 5min

Figure 2.3   The process flow and the photo of photolithography apparatus.

2.1.4 Magnetron -Sputtering System

After cleaned by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive layer.) and Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. A high voltage across a low-pressure gas (usually argon at about 5 mTorr) is applied to create a "plasma," which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the "target," composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to the substrate surface.

An UHV-sputtering system is used for thin film formations of electronic devices, for experiments of GMR, and for creating new high temperature superconductors materials. In this study, UHV Multi Target Sputtering System ES-350SU shown Figure 2.5 was used. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. For other details, Table 2.1 is attached for reference.
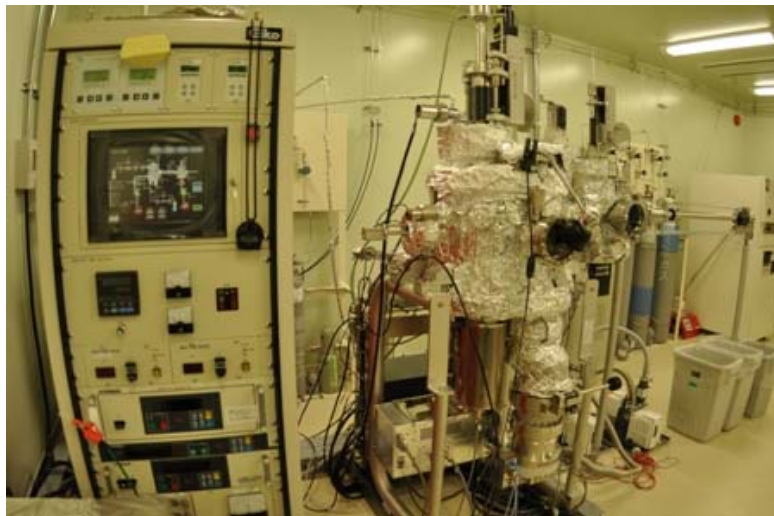
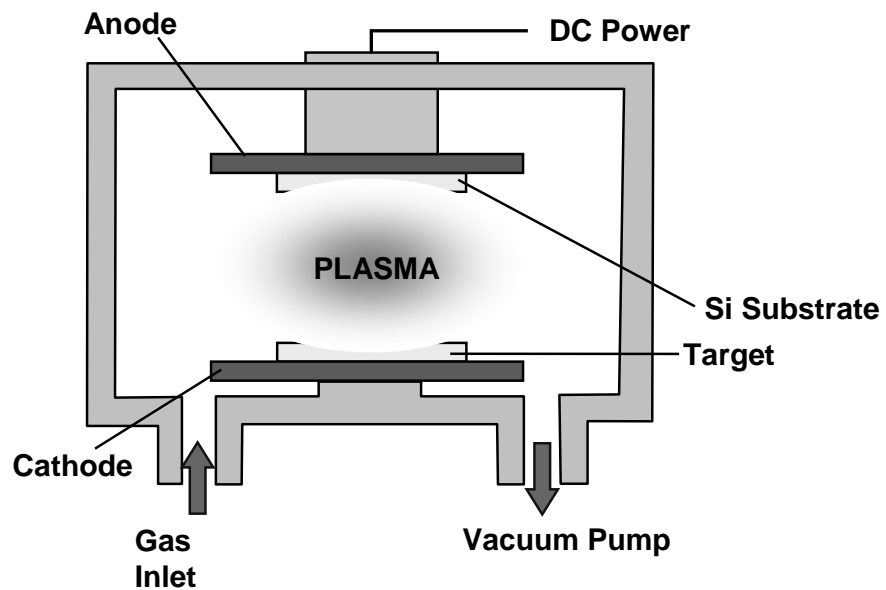**Figure 2.4** Photo of UHV Multi Target Sputtering System ES-350SU.

Figure 2.5 Structure of UHV sputtering system.

Growth chamber	1. Ultimate pressure	1.5×10^{-6}Pa
	2. Substrate size	2 inch in diameter
	3. Heating temperature	600ºC
	4. Heater type	Lamp type heater
	5. Target	3 inch x 5 pieces (motor-driven)
Load lock chamber	6. Vacuum pumps	TMP 500L/sec and RP 250L/min
	7.Ultimate pressure	6.6×10^{-5}Pa
	8. Vacuum pumps	TMP60L/sec and RP90L/min
	9. Substrate holder with cooling function / Substrate holder with heating function /Cleaning function / Radical beam source	

Table 2.1 Specifications for UHV Multi Target Sputtering System ES-350S.

2.1.5 Infrared Annealing Furnace

After formation in the UHV sputtering system, thin films of Ni/Si, Ni/M/Si, or M/Ni/Si were transferred to annealing furnace to perform thermal process. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation is QHC-P610CP (ULVAC RIKO Co. Ltd). Figure 2.6 is the photo of the infrared annealing furnace, whose schematic illustration was shown in Figure 2.7. The annealing was performed by six infrared lamps surrounding the sample stage made of carbon coated by SiC. The heating temperature was controlled by thermocouple feedback.

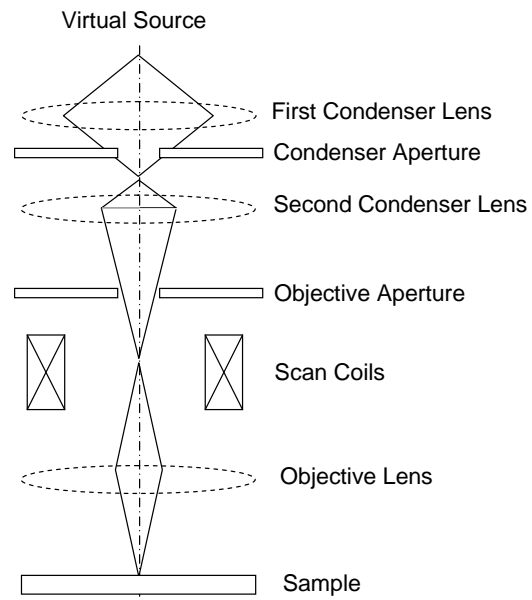**Figure 2.6** Photo of infrared annealing furnace.

Figure 2.9 Schematic drawings of SEM equipment.

2.2 Measurement Methods

2.2.1 Scanning Electron Microscope (SEM)

Figure.2.9 shows Scanning Electron Microscope (SEM) system. The equipment is S-4800 (HITACHI High-Technologies Corporation). The 'Virtual Source' at the top represents the electron gun, producing a stream of monochromatic electrons. The stream is condensed by the first condenser lens. This lens is used to both form the beam and limit the amount of current in the beam. It works in conjunction with the condenser aperture to eliminate the high-angle electrons into a thin, tight, coherent beam. A user selectable objective aperture further eliminates high-angle electrons from the beam. A set of coils then scan or sweep the beam in a grid fashion and make the beam dwell on points for a period of time determined by the scan speed. The final lens, the Objective, focuses the scanning beam onto the part of the specimen desired. When the beam strikes the sample, interactions occur inside the sample and are detected with various instruments interactions. Before the beam moves to its next dwell point these instruments count the number of interactions and display a pixel on a CRT whose intensity is determined by this number. This process is repeated until the grid scan is finished and then repeated, the entire pattern can be scanned 30 times per second.
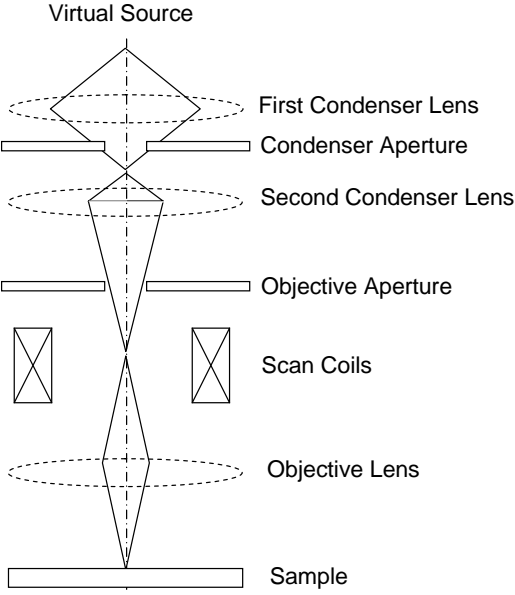
Figure 2.8 Photograph of SEM equipment.

Virtual Source

First Condenser Lens

Condenser Aperture

Second Condenser Lens

Objective Aperture

Scan Coils

Objective Lens

Sample

Figure 2.9 Schematic drawings of SEM equipment.

2.2.2 Auger Electron Spectroscopy (AES)

Auger electron emission is initiated by the creation of an ion with an inner shell vacancy. Auger electrons are emitted in the relaxation of the excited ion. In this process an electron from a higher lying energy level fills the inner shell vacancy with the simultaneous emission of an Auger electron. This simultaneous two electron coulombic rearrangement results in final state with two vacancies. Auger electron emission is one of two relaxation mechanisms possible in an excited ion. The other is x-ray fluorescence, in which a photon is emitted.

The two relaxation processes for an excited ion are shown in the energy level diagrams of figure 2.11. Note that all energies are referenced to the Fermi level Ef, which corresponds to zero binding energy. In these diagrams the initial vacancy occurs in the K shell. The incident particle is any particle that ionizes the K shell. Hence, Auger emission will result from bombardment of a sample with electrons, x-rays, or ions. However, dedicated Auger instruments typically employ electron irradiation since electron beams can be focused to very small diagram.

Both Auger electron emission and photoelectron emission occur as a consequence of the x-ray irradiation used in X-ray Photoelectron Spectroscopy (XPS) also known as Electron Spectroscopy for Chemical Analysis (ESCA). In XPS, low energy x-ray, such as the Mg or Al Kα, impinge on a sample and cause the emission by Auger electron emission, since x-ray fluorescence is a minor process in this energy range (up to ~1500eV).

The sum of the total Auger yield and the fluorescence yield is unity, since an excited ion can relax by either Auger electron emission or x-ray emission. Auger electron emission is the more probable decay mechanism for low energy transitions, i.e., for low

atomic number elements with initial vacancy in the K shell and for all elements with initial vacancies in the L or M shells. By choosing an appropriate Auger transition, all elements (except H and He) can be detected with high sensitivity. Auger transitions are typically labeled by the energy levels of the electrons involved, using x-ray spectroscopy nomenclature. The first label corresponds to the energy level of the initial core hole. The second and third labels refer to the initial energy levels of the two electrons involved in the Auger transition. Thus the Auger transition shown in Figure is a $KL_{II}L_{III}$ transition, or simply KLL transition [1].
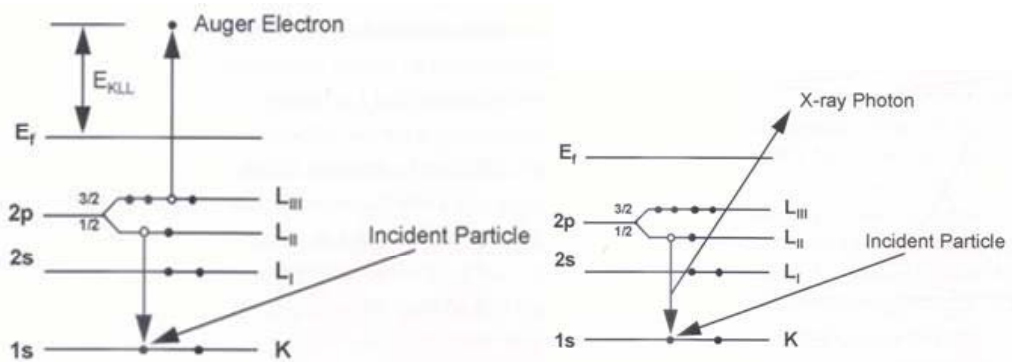

Fig. 2.11 Schematic diagrams of Auger electron emission and x-ray fluorescence. The incident particle causes the ejection of a K shell electron [1].

AES is a very useful analytical method to evaluate the elemental depth profile compositions of regions of several tens of nanometers in the near surface layer of a sample [2]. The equipment is PHI 700 (ULVAC-PHI, INC.).

References

[1] Handbook of Auger Electron Spectroscopy Third Edition.

[2] N. Urushihara et al, *J. Vac. Sci. Technol.* A 26(2008) 668-672.

Chapter3

Ni Silicide into Si Nanowires using Nitrogen Incorporation

3.1 Introduction

   3.1.1 The Reason for the Silicidation of Source and Drain regions

   3.1.2 Ni Silicide on Bulk Si

   3.1.3 Nickel Silicidation for Si Nanowire and The Encroachment Phenomenon

   3.1.4 The effect of N Incorporation in Ni for Silicidation

3.2 Experiment
3.3 Result and Discussion

   3.3.1 SIMS depth profile of nitrogen in the deposited Ni film

   3.3.2 SEM images of Ni silicide formed in Si NWs

   3.3.3 Time dependence of the encroachment length of Ni silicide

   3.3.4 The effect of diameter on the encroachment length for silicidation

   3.3.5 Annealing Temperature Dependence of Ni Silicidation for Si Nanowire

3.4 Conclusion of this section
Reference

3.1 Introduction

3.1 The effect of N Incorporation in Ni for Silicidation

The effect of N atom incorporation into Ni film on the silicidation was previously evaluated [8]. If Ni films are deposited by sputtering in Ar and N_2 gas mixture ambient, the condition forms nitrogen (N) doped Ni film. Silicide processes using Ni and N-doped Ni films are shown in figure.3.2 with the comparison to the conventional Ni silicide formation. When N-doped Ni films are used, poly-crystalline and epitaxial $NiSi_2$ films is formed by annealing at 500°C. In general, the annealing temperature at 500°C forms NiSi phase and the annealing temperature higher than 800°C is required for $NiSi_2$ formation. As figure.3.2 (a) shows, NiSi films grow from Ni film without N-doping is promoted by the fast diffusion of Ni atoms via grain boundary. Figure.3.2 (b) shows epitaxial $NiSi_2$ grows through uniform lattice diffusion by the assistance nitrogen in Ni film and the growth rate is very slow. Therefore it is considered to be useful for the suppression of the encroachment phenomenon, this technique is applied for the source and drain silicidation of Si nanowire FET in this chapter.
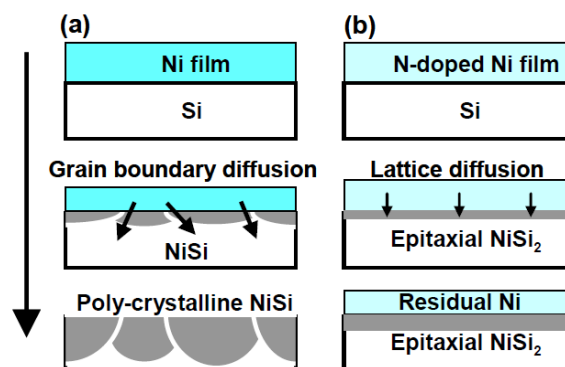

Figure. 3.2 Models explaining the different growth behavior of NiSi and epitaxial $NiSi_2$ films [8].

3.2 Experiment

We utilized top-down fabrication of Si NWs and investigated Ni silicidation phenomenon by the reaction of nanowires with Ni films deposited on them. Figure.3.3 shows the experimental procedure. Si NWs were fabricated by the formation of Si NW islands in the 30nm SOI layer followed by the thermal oxidation at 1000^oC 30min in a dry oxygen atmosphere. The thickness of SiO_2 formed around Si NWs is about 15nm, Oxides around Si NWs were partially removed by HF solution. 6-nm-thick Ni films were deposited on Si NWs by RF magnetron sputtering in an Ar or Ar/N_2 (Ar: N2=1:1) mixed ambient. Rapid thermal annealing (RTA) at 400^oC for 30 sec was performed to form silicides in nitrogen ambient. Unreacted Ni films were removed by SPM (mixed solution of H_2SO_4 and H_2O_2). Ni silicide encroachments into Si NWs were observed and measured by SEM.

① **Si patterning**

② **Si Nanowire formation by Thermal Oxidation**
(Dry O_2, 1000oC, 45min)

③ **Partial oxide removal**

④ **6nm Ni deposition**

in N_2 and Ar
(N_2:Ar=1:1)ambient
Using Sputter technique

⑤ **Rapid Thermal Annealing (RTA) in N_2ambient**

⑥ **Unreacted Ni removal**

⑦ **Observation by SEM**
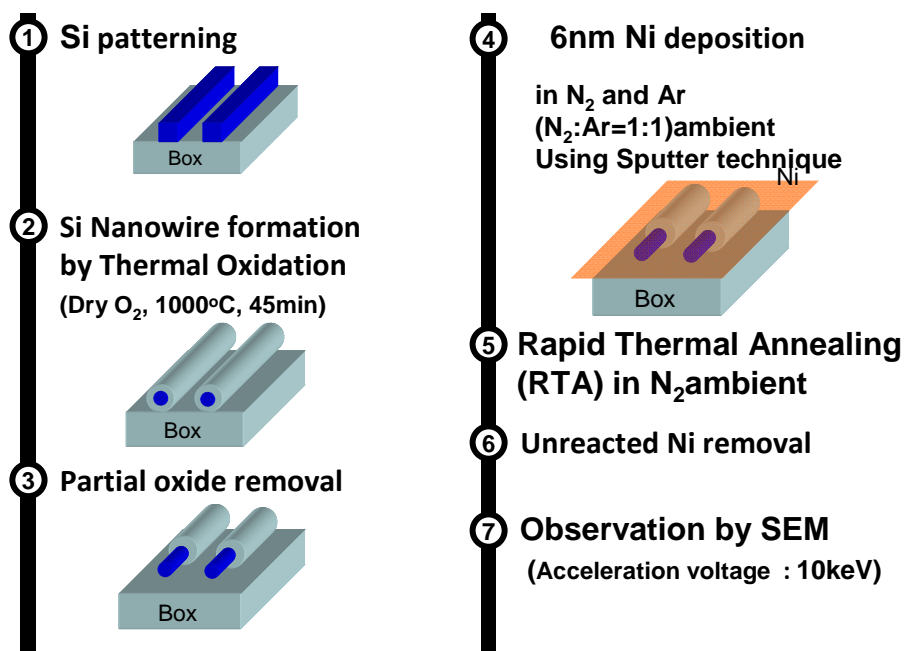(Acceleration voltage : 10keV)

Figure. 3.3 Fabrication process flow

3.3 Results and Discussion

3.3.1 SIMS depth profile of nitrogen in the deposited Ni film

Figure.3.4 shows the SIMS depth profile of nitrogen in the deposited Ni film in Ar/N$_2$ (Ar: N$_2$=1:1) mixed ambient. This figure.3.4 shows that quite large amount of nitrogen with a dose of 2.4×10^{16} [atoms/cm^2], are introduced in the entire depth range of Ni films.
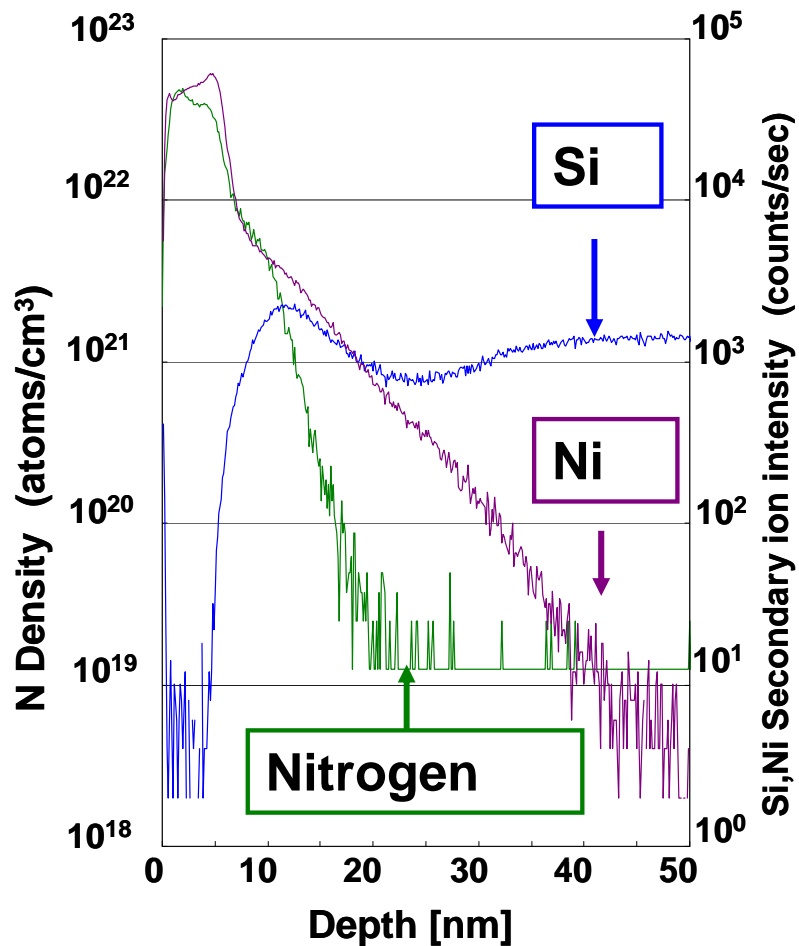

Figure. 3.4 The SIMS depth profile of nitrogen in the deposited Ni film.

3.3.2 SEM images of Ni silicide formed in Si NWs

Figures3.5 (a) and (b) show the SEM images of Ni silicide formed in Si NWs from Ni flim without and with nitrogen, respectively.. The width of the NWs was about 20nm. It can be observed that Ni sicilide formed in exposed Si NW in the right side encroached into Si NW covered by oxide both for cases, however, the encroachment length of Ni silicide from Ni with nitrogen is almost a half of that from Ni without nitrogen.
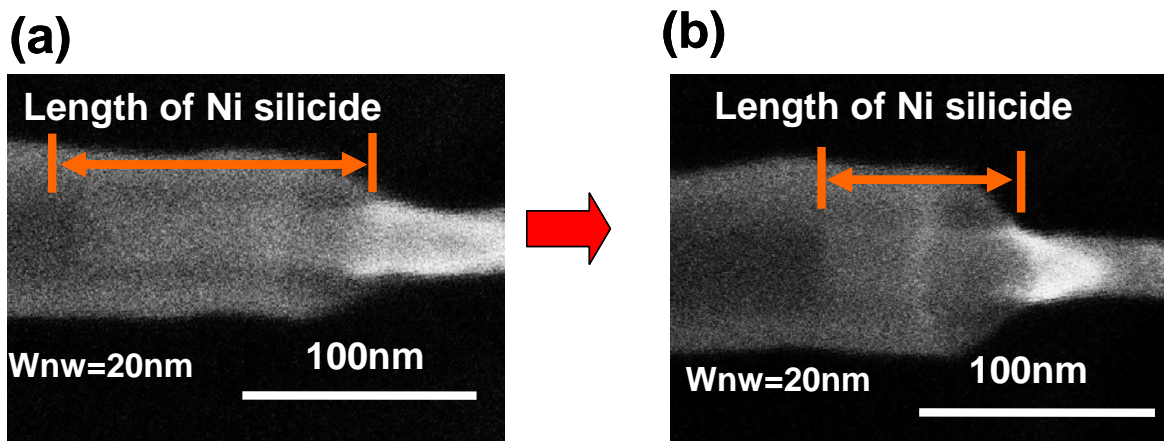
(a)
Length of Ni silicide
Wnw=20nm   100nm

(b)
Length of Ni silicide
Wnw=20nm   100nm

Figure. 3.5 SEM images of Ni silicide formed by two different processes: (a) Ni silicide from Ni without nitrogen, (b) Ni silicide from Ni with nitrogen. The silicidation were performed at $400^{o}C$ for 30 sec in nitrogen ambient for both cases.

3.3.3 Time dependence of the encroachment length of Ni silicide

Figure3.6 shows the dependence of encroachment lengths of Ni silicide on the square root of annealing time.   We evaluated the encroachment length of Ni silicides in Si NWs with a diameter of 10nm in this case. The annealing temperature was set to be 400°C and the atmosphere was nitrogen. We can observe a linear relationship between the length of Ni silicide and the square root of annealing time for both cases. The linear relationship of these plots indicates that this encroachment phenomenon is governed by the diffusion law such as,

$$\lambda \propto A\sqrt{t} \tag{1}$$

, where A is the slope of the plot.

  This fact indicates that Ni silicide encroachment is governed by the diffusion of Ni in silicide even with N incorporation, however, the diffusion coefficient observed in silicidation from Ni with nitrogen, which can be extracted from the slope of the corresponding line, was reduced from that in silicidation from Ni without nitrogen. Compared to that in the case of Ni without nitrogen (1.6×10^{-12} [cm^2/s]), the effective diffusion coefficient in the case of Ni with nitrogen was reduced by about 30% to 1.2×10^{-12} [cm^2/s].
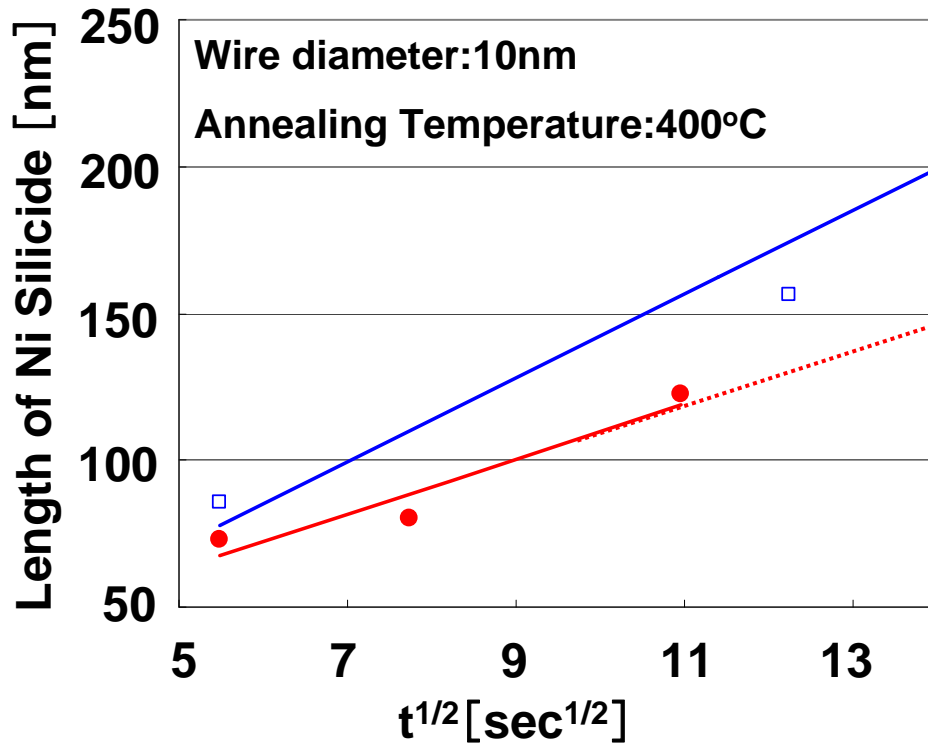
Figure. 3.6 Time dependence of the encroachment length of Ni silicide. The silicidation were performed at 400°C in nitrogen ambient. The diameter of Si NWs is 10nm in this case.

3.3.4 The effect of diameter on the encroachment length for silicidation

Figure.3.7 shows the effect of diameter on the encroachment length. Generally, the encroachment length increases with the increase in diameter of NW. However, we could confirm that the encroachment length of Ni silicide can be suppressed by about half in silicide from Ni with nitrogen incorporation for entire diameter range studied (8 to 23 nm). Therefore, it is concluded that nitrogen incorporation in Ni is very effective to suppress the encroachment of silicide for Si NWs. The reason for the increase in the encroachment in accordance with the increase in the diameter of is not clear, yet. The compressive strain imposed by the oxidation process may lead to the suppression of silicidation especially for narrow NWs.
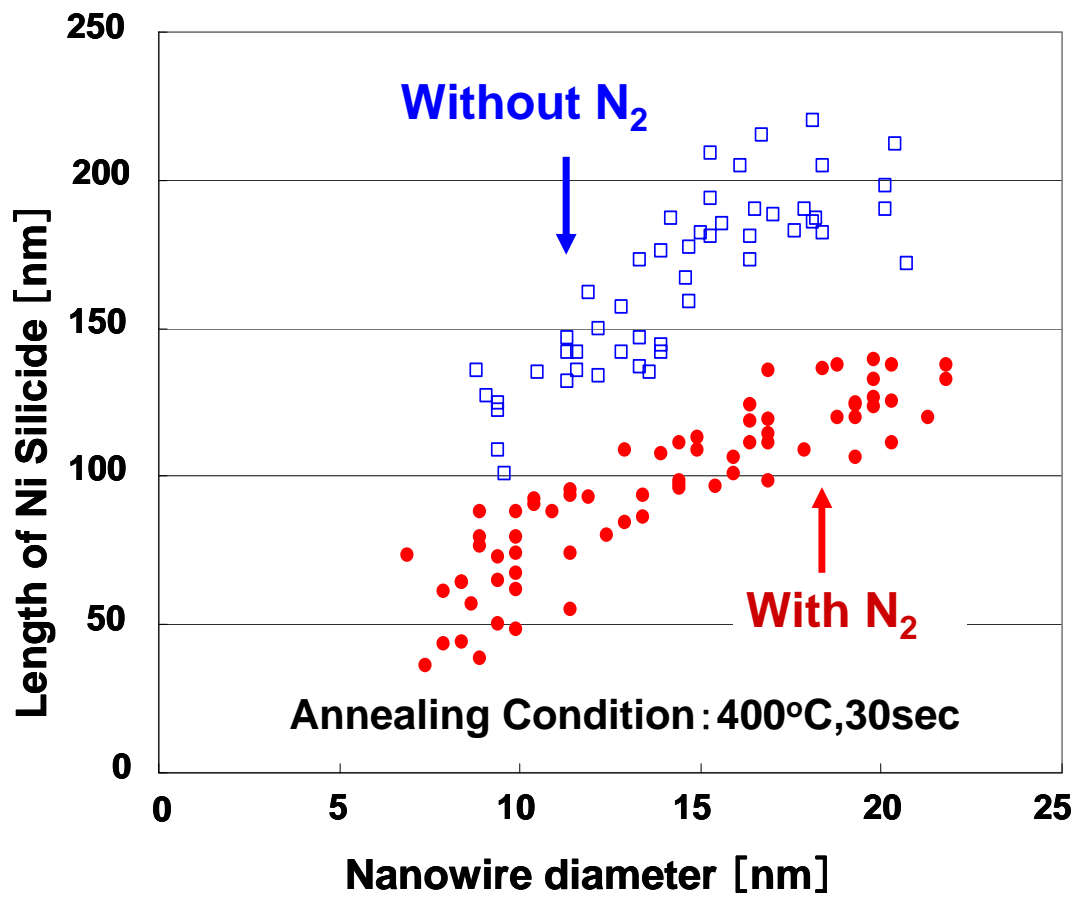
Figure. 3.7 The effect of diameter on the encroachment length for

silicidation from Ni with and without nitrogen incorporaton.

3.3.5 Annealing Temperature Dependence of Ni Silicidation for Si Nanowire

The dependence of the length of Ni Silicidation on annealing temperature is shown in Fig. 3.8. The diameter of Si NWs is 10nm in this case. It can be confirmed that suppress the diffusion of Ni in silicide from Ni with nitrogen incorporation is suppressed at the annealing temperature 400℃ or less . Below 350℃, the lateral diffusion was almost completely suppressed. However, the effect of the suppression of diffusion with nitrogen was not able to be confirmed at 450℃ or more in annealing temperature.
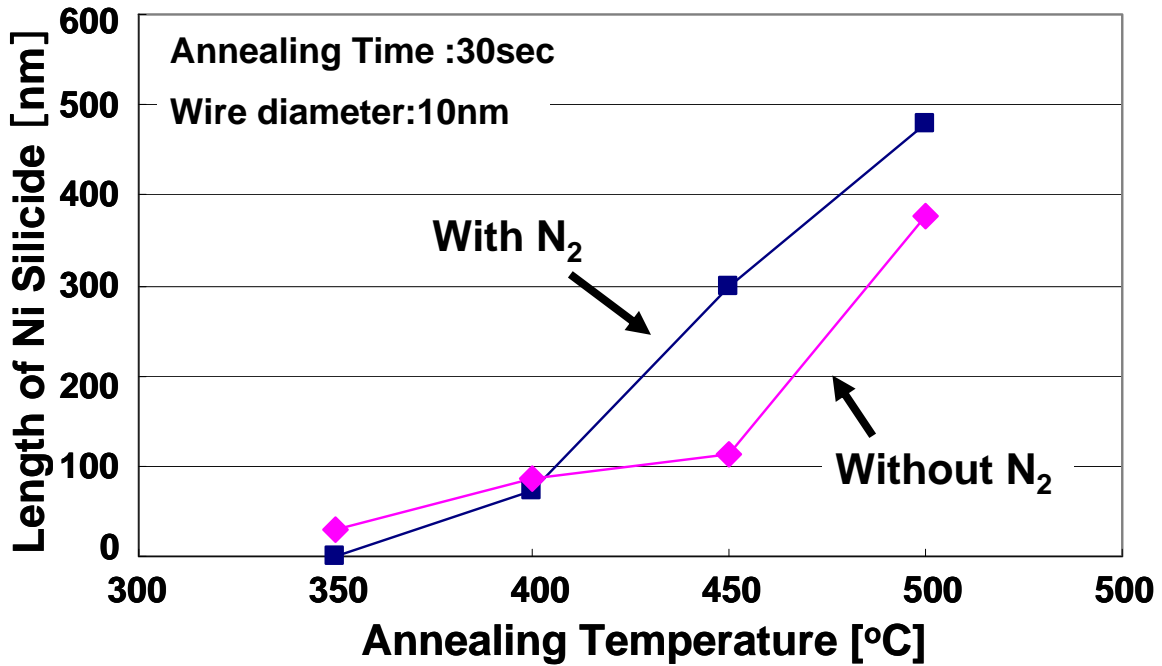

Figure. 3.8 Temperature dependence of the encroachment length of

Ni silicide from Ni with and without nitrogen incorporaton.

Arrhenius plots of nanowires are compared for the two case with and without nitrogen incorporation as shown in figure.3.9. The diameter of Si NWs is 10nm in this case. Calculated activation energy (E_a) of with nitrogen incorporation and without nitrogen incorporation were 2.2eV and 1.4eV respectively. The activation energy of NiSi and Ni_2Si were reported 1.4 eV and 1.5 eV in bulk Si, respectively. The activation energy obtained in Si NWs without nitrogen incorporation is close to that with NiSi and Ni_2Si [5].However, it is confirmed that this value is different in Ni with nitrogen incorporation. It is report that NiSi to $NiSi_2$ transformation activation energy 2.4eV [8]

In balk Si, $NiSi_2$ film s are obtained by depositing N dope Ni film followed by annealing at 500^oC,although the applied annealing temperature 500^oC is the typical condition for NiSi phase formation and annealing temperature higher than 800^oC is generally required for $NiSi_2$ formation[9-11]When using Ni with nitrogen incorporation in even nanowire, the change of the composition is thought about.
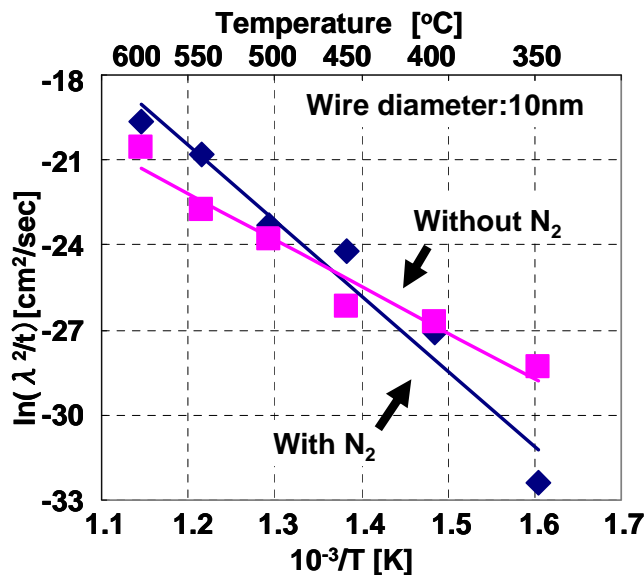

Figure. 3.9   Arrhenius plots of nanowires compared Ni with and

without nitrogen incorporaton

3.4 Conclusion of this section

In this section, indicates the encroachment of Ni silicide into Si NWs and the suppression of this phenomenon using nitrogen incorporation into Ni films are shown. First, I confirmed nitrogen in Ni film by SIMS depth profile. Quite large amount of nitrogen with a dose of 2.4×10^{16} [atoms/cm^2], are introduced in the entire depth range of Ni films.

Ni siclicide formed from Ni flim without and with nitrogen observed by SEM. The encroachment length of Ni silicide from Ni with nitrogen is almost a half of that from Ni without nitrogen.

Even with nitrogen incorporation, Ni silicide encroachment is governed by the diffusion of Ni in NWs. However its diffusion coefficient is reduced when nitrogen is incorporated. Nitrogen incorporation is effective to suppress the encroachment for all NW diameters experimented in the range from 8 to 23nm. N incorporation method is useful for fabrication of Si NW FET in the annealing temperature 400℃ or less temperature. However, the effect of the suppression of diffusion with nitrogen was not able to be confirmed at 450℃ or more in annealing temperature. Arrhenius plots were obtain by temperature dependent. Calculated activation energy (E_a) of with nitrogen incorporation and without nitrogen incorporation were 2.2eV and 1.4eV respectively. It is report that NiSi to NiSi$_2$ transformation activation energy 2.4eV. It can be confirmed to this value to be different in Ni with nitrogen incorporation. This reason is the change of NiSi to NiSi$_2$ in using Ni with nitrogen incorporation

Acknowledgement

Reference

[1] P. S. Lee, K. L. Pey, D. Mangelinck, J. Ding, D. Z. Chi and L. Chan. *IEEE Electron Device Lett*. **22** (2001) 568.

[2] K. N. Tu et al., *J. Appl. Phys.* **54** (1983), p. 758.

[3] T. Morimoto et al., *IEEE Trans. Electron Devices* **42** (1995) 915.

[4] K. N. Tu et al., *Thin Solid Films*, **25**, 403, (1975).

[5] S. P. Murarka, *SILICIDES FOR VLSI APPLICATIONS*. Academic Press, New York, 1983, Chap.5.

[6] L. J. Chen, *Silicide Technology for Integrated Circuits*. The IEE, London, 2004. Chap. 5.

[7] H. Arai, et al., *ECS Transactions* (2009), 25(7, ULSI Process Integration 6), 447-454.

[8]

[9] S. Migita. et al., *Solid State Devices and Materials*., pp. 686-687 (2008).

[10] N. Ikarashi et al., *J. Appl. Phys.* **107,** 033505 (2010)

[11] O. Nakatsuka et al., *J. J. Appl. Phys.* Vol. 44, No. A, 2005, pp. 2945-2947

Chapter4

Study of Suppression mechanism of nitrogen Incorporation

4.1 Introduction

4.1.1 Suppression model of nitrogen Incorporation in Si Nanowire

4.2 Experiment

4.3 Result and Discussion

4.3.1 The encroachment results for the four samples

4.3.2 Discussion of Suppression model of nitrogen Incorporation

4.4 Conclusion of this section

Reference

4.1 Introduction

4.1.1 Suppression model of nitrogen Incorporation in Si Nanowire

In this section, I discuss suppression model for the nitrogen incorporation method. Figure.4.1 shows Schematic figure of two suppression models of nitrogen incorporation. Suppression effect of the nitrogen incorporation is thought to be attributed to the effect of Ni-N bonds inside Ni films (Model ①) or the effect of formation of Si-N bonds at Ni/Si interface(Model ②). In the former case, bonding nitrogen with Ni atom in the Ni films suppresses reaction of Ni reaction with silicon, while in the latter case, thin Si-N bonds formed on the Si surface during the Ni deposition suppresses Ni diffusion at the silicidation reaction
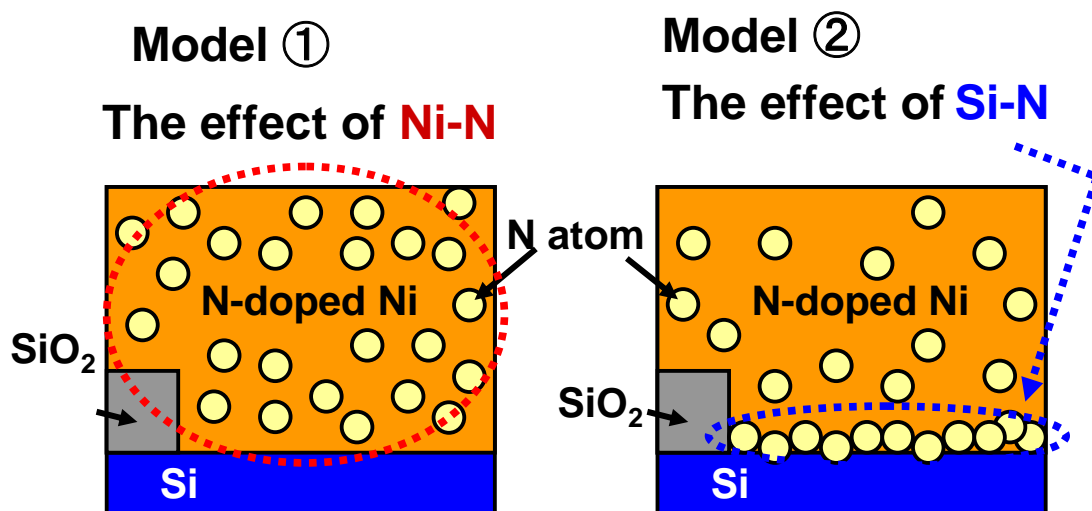

Figure. 4.1 Schematic figure of suppression models for the nitrogen incorporation

. As a matter of fact, there is a report that nitrogen incorporated Ni deposition on Si substrate leads to the formation of a thin Si-N layer at the interface by the immersion of the Si surface to nitrogen plasma at the beginning of the sputtering [1].Figure.4.2 shows TEM image at nickel nitride/Si interface. It is report that a thin Si-N layer at the

interface suppresses Ni diffusion [1-4]. Therefore, the experiment is designed in order to
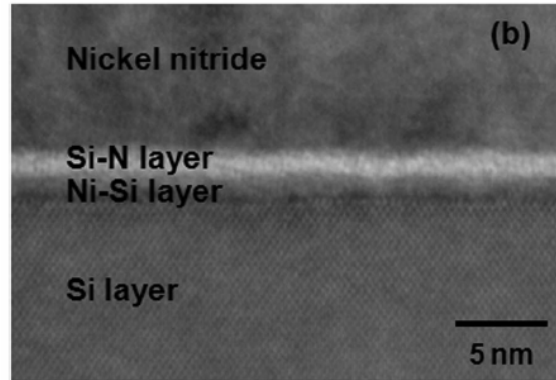
confirm the Si-N layer effect.

Figure. 4.2 TEM image at nickel nitride/Si interface [4]

4.2 Experiment

Figure.4.3 shows four kinds of samples formed for the experiment: Sample 1 is a reference sample with Ni 10nm without nitrogen. Sample 2 consists of nitrogen incorporated 10nm-thick Ni. Sample 3 uses a stacked structure with a 5nm-thick Ni on a 5nm-thick nitrogen incorporated Ni. Sample 4 is the inverse structure of the sample 3, where pure Ni is in contact with Si NW. Silicidation annealing was performed for using all of these samples at 400°C for 30sec in a nitrogen ambient. If suppression effect is confirmed in sample3, suppression of the encroachment by the nitrogen incorporation is thought to be mainly from the effect of Si-N. On the other hand, if the suppression effect is confirmed in sample4, suppression can mainly be attributed to the effect of Ni-N inside Ni films.
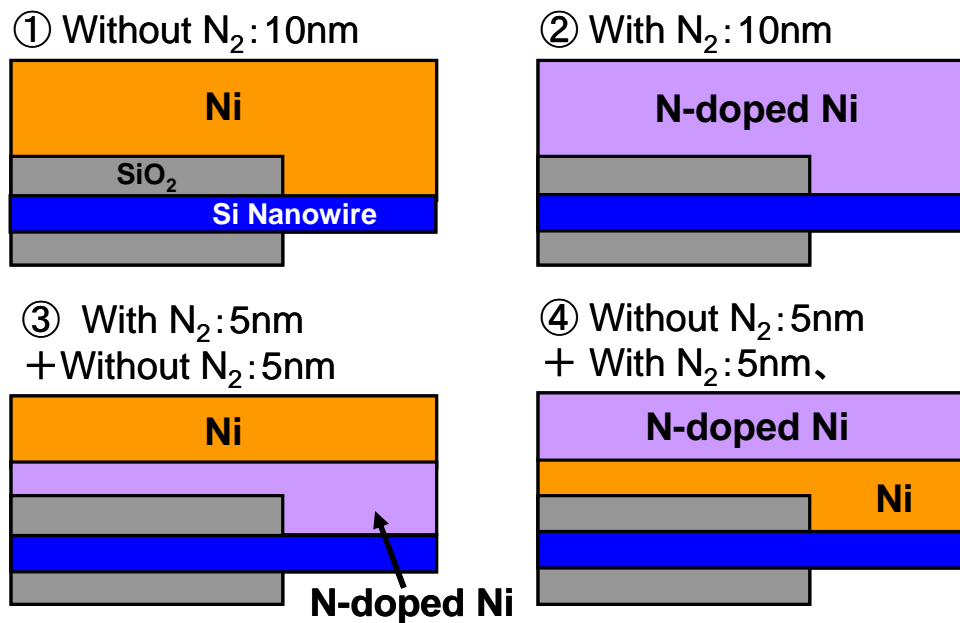

Figure. 4.3 Four kinds of samples used in order to extract the mechanism of the suppression of the encroachment during the silicidation by nitrogen incorporation.

3.3 Result and Discussion

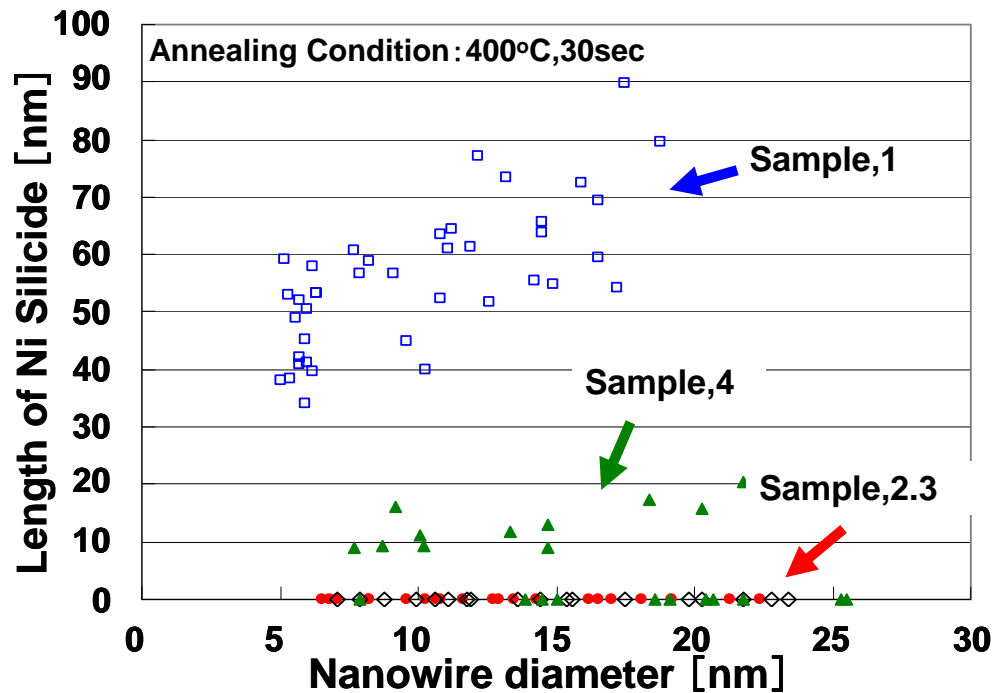### 4.3.1 The encroachment results for the four samples

Figure 4.4 Encroachment length of Ni silicide from samples 1,2,3, and 4 shown in

Fig4.3, as a function of NW diameter.

Figure4.4 shows the encroachment length of Ni silicide measured from four kinds of samples depicted in Fig.4.3, as a function of diameter of Si NWs. Here, the annealing condition was set to be at $400^{\circ}C$ for 30sec in nitrogen ambient. We can clearly see that the encroachment of Ni silicide can be well suppressed for samples 2 and 3, while the suppression in the sample 4 is limited. From this result, we can understand that thin SiN at the Ni/Si interface could be the main reason for the suppression of the encroachment of the silicide. This Si-N layer could suppress the silicidation and the diffusion of Ni atoms into the NWs

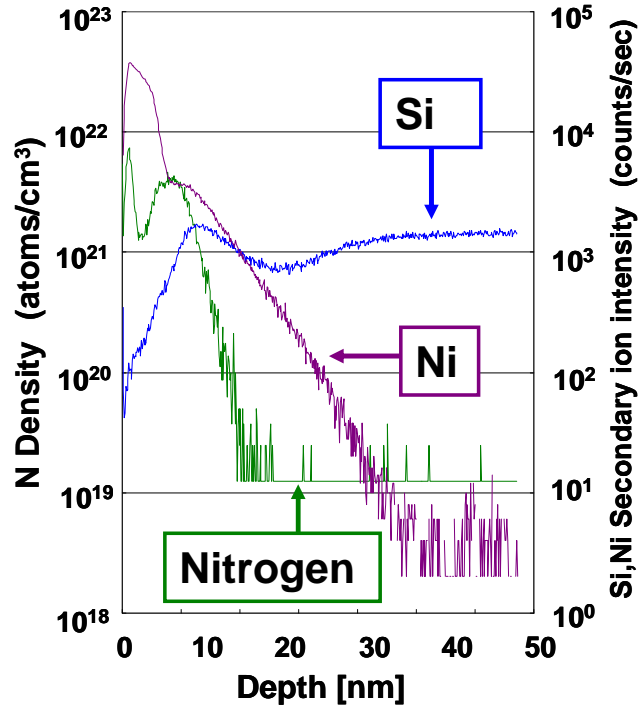## 4.3.2 Discussion of Suppression model of nitrogen Incorporation

Figure. 4.5 The SIMS depth profile of nitrogen in the sample after silicidation. The silicidation was performed at 400°C for 30 sec in nitrogen ambient.

Figure. 4.6 also showed smaller encroachment for Ni silicide in sample 4, in which pure Ni and nitrogen incorporated Ni were in stack. Therefore, it should be taken into consideration that the suppression effect still exists in sample 4. Although it is possible to conclude that Ni-N bonds inside the Ni film are also effective to suppress the phenomenon, we think even this result could be attributed to the SiN thin film formation at the Ni/Si interface. There is a report when N was implanted into upper part of Ni films and annealed at 375°C, nitrogen diffuse and reach Ni / Si interface and Si-N layers was formed [5]. Actually, according to the SIMS analysis of samples after

silicidation, nitrogen inside Ni is quite volatile and almost all amount of nitrogen inside the film desorbed during the silicidation annealing as shown in Figure.4.5. Therefore, it is quite probable that a part of nitrogen incorporated in Ni film could diffuse and react with Si at Ni/Si interface, as shown in fig4.6.
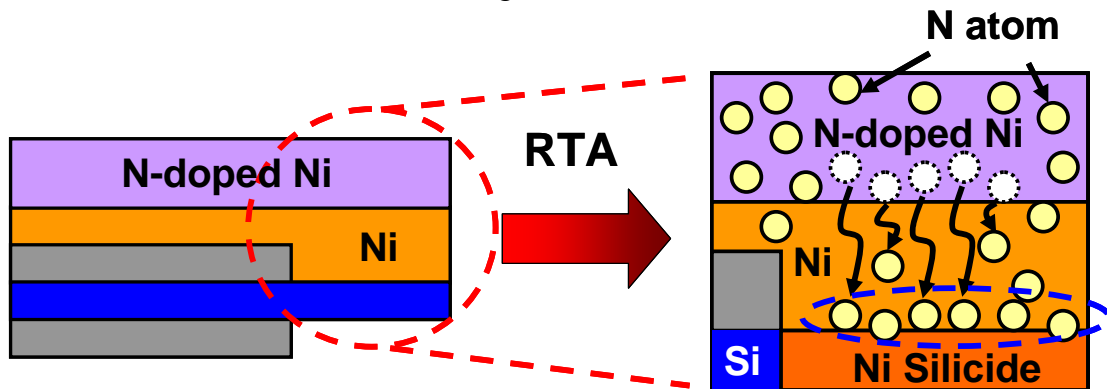

Figure.4.6 Schematic of sample4, where pure Ni and nitrogen incorporated Ni was in stack on Si NW. During annealing, nitrogen in Ni film is considered to diffuse to the interface and form SiN-layer on Si NW surface.

4.4 Conclusion of this section

The suppression mechanism of nitrogen incorporation was investigated. Four kinds of samples used in order to extract the mechanism of the suppression of the encroachment during the silicidation by nitrogen incorporation. From this result, suppression effect can be mainly attributed to thin Si-N layer formation at the interface between Ni and Si NW. Immersion of NW surface to nitrogen plasma at the beginning of the sputtering, as well nitrogen diffusing through Ni film is considered to react with Si and form SiN-layer on NWs.

Acknowledgement

Reference

[1] Sun II Kim et al., *J.Electrochem.Soc.*, **157** (3), H231-H234 (2010).

[2] T. Ohguro et al., *International Electron Devices Meeting.*, 95-453 (1995)

[3] O. Soon-Young et al., *Japan Journal of Applied Physics.,* Vol, 44, No.4B, 2005, pp.
2142-2146

[4] S. Migita. et al., *Solid State Devices and Materials*., pp. 686-687 (2008).

[5] L. Wielunski et al., *Appl.Phys.Lett*., **38**, 106 (1981).

Chapter5

Conclusion

In this thesis, we investigated nickel silicidation using nitrogen incirporation method and the mechanism for the suppression of its laterl encroachment in Si Nanowire. This chapter summarized the results of the studies in this thesis.

First, SIMS measurement nitrogen in the deposited Ni film was performed. Quite large amount of nitrogen with a dose of 2.4×10^{16} [atoms/cm^2], were introduced in the entire depth range of Ni films. Ni siclicide formed from Ni flim without and with nitrogen were observed by SEM. The encroachment length of Ni silicide from Ni with nitrogen was almost a half of that from Ni without nitrogen.

Even with nitrogen incorporation, Ni silicide encroachment is governed by the diffusion of Ni in NWs. However its diffusion coefficient is reduced when nitrogen is incorporated. Nitrogen incorporation is effective to suppress the encroachment for all NW diameters experimented in the range from 8 to 23nm. N incorporation method is useful for fabrication of Si NW FET in the annealing temperature 400℃ or lower temperature. Arrhenius plots were obtained by temperature dependence. However, the effect of the suppression of diffusion with nitrogen was not able to be confirmed at 450℃ or more in annealing temperature. Calculated activation energy（E_a）of with nitrogen incorporation and without nitrogen incorporation were 2.2eV and 1.4eV respectively. This reason is attributed the change of the composition of silicide by using Ni with nitrogen incorporation

The suppression mechanism of nitrogen incorporation was investigated. Four kinds of samples were fabricated in order to extract the mechanism of the suppression of the

encroachment during the silicidation by nitrogen incorporation. From this result, Suppression effect can be mainly attributed to thin Si-N layer formation at the interface between Ni and Si NW and its retardation effect of Ni diffusion and the silicidation. Immersion of NW surface to nitrogen plasma at the beginning of the sputtering and nitrogen diffusion through Ni film is considered to form SiN-layer on NWs.

Acknowledgments

The author would like to thank his supervisor at Tokyo Institute of Technology, Professor Akira Nishiyama and Professor Hiroshi Iwai for their excellent guidance and continuous encouragement.Prof. Nobuyuki Sugii, Prof.Takeo Hattori, and Prof. Kazuo Tsutsui of Tokyo Institute of Technology gave me their relevant suggestion and comments on my study at laboratory meeting during two year of master course.

Assistant Prof. Kuniyuki Kakushima gave me his continuous encouragements and fruitful advices. Assistant Prof.Parhat Ahmet gave us many insightful suggestions concerning material seience.

I am so happy to meet the member of Iwai laboratory. They told me not only their Morover, through the relationship with them study but also sociality. The information on their study was very helpful for me. I could sociability.　In particular, Soshi Sato, Yeonghun Lee and Masao Koyama who are studying about Si nanowire support my study. I would like to take this opportunity to thank their kindness.

The author would like to thank Ozawa kenji, Kanda Takashi, Koyanagi Tomotune, Mukai Kouki and Kitayama Daisuke for their helps and frendships for 2years in the laboratory.

The author would like to express sincere gratitude to laboratory secretaries,　Mrs. K. Karakawa, and Ms. A. Matsumoto.

This study was partially supported by Nanoelectronics Project by NEDO, Japan. Finally, I would like to thank my parents Syuuzou and Terumi and my brother Taketo and My sister Sawako and Keiko for their endless support and encouragement in my life.