2011 Master Thesis

Atomic layer deposition of advanced gate oxides for scaled MOSFET

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Chapter 1
INTRODUCTION

1.1 Background of This Study

In recent years, Information Technology society developed dramatically, for example the tremendous growing population of using internet, mobile phone, car navigation and many kinds of so called “IT products”. There is no doubt that the progress of recent Information Technology is realized by the improvement of the electronics, especially by the Silicon based Large Scale Integrated (LSI) circuits technology. The improvement of LSI has been achieved by the downsizing of its components such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Because of the downsizing, capacitance of the components reduces, resulting in high-speed, high-frequency and low power operation of the circuits. Of course, size reduction and high-integration of the circuits can be also realized at the same time with the performance improvement. Gordon Moore who is one of the founder of Intel Corporation, predicted that exponential growth in the number of transistors per integrated circuit and predicted this trend would continue, in a popular article written in 1965[1]. This law notes that the device feature size decreases each year and the number of transistors on a LSI doubled every two years. This simple statement is the foundation of semiconductor and computing industries. The International Technology Roadmap for Semiconductor (ITRS) [2] defines how the device parameters are scaled for the next technology node. microprocessor. The total number of transistors on microprocessor was increased double every 18-24 months. It was applied well to the Moore’s Law. [2]

1.2 Scaling Method of MOSFETS

The downsizing of the components has been accomplished by the scaling method [3]. In the electrical design of modern CMOS transistor, the power-supply voltage is reduced with the physical dimension in some coordinated manner. A great deal of design detail goes into determining the channel length, or separation between the source and drain, accurately, maximizing the on current of the transistor while maintaining an adequately low off current, minimizing variation of the transistor characteristics with process tolerances, and minimizing the parasitic resistances and parasitic capacitances [4]. To make circuit speed up, devices dimensions and the power-supply voltage must be scaled down. Figure 1.1 and Table 1.1 shows the schematic model of MOSFET constant-electric-field scaling by the same factor S.

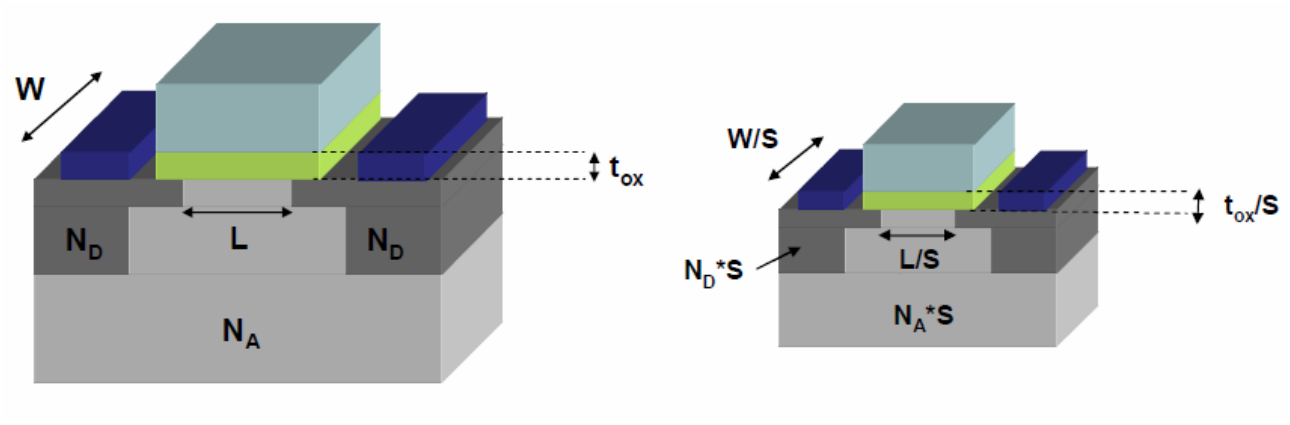


Figure 1.1 Scaling method

Table 1.1 Scaling of MOSFET by a scaling factor of S.

Quantity	*Before scaling*	*After scaling*
Channel length	L	$L' = L/S$
Channel width	W	$W' = W/S$
Device area	A	$A' = A/S^2$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Gate capacitance per unit area	C_{ox}	$C_{ox}' = S*C_{ox}$
Junction depth	x_j	$x_j' = x_j/S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{TO}/S$
Doping densities	N_A	$N_A' = S*N_A$
	N_D	$N_D' = S*N_D$

1.3 Scaling Limits of SiO_2 Gate Dielectric

It is well known that Silicon dioxide film (SiO2) is the most common materials as gate insulator film for MOSFET. According to Moore's low, SiO_2 gate film has become thin, however extremely thin gate oxide has large leakage current cased by direct-tunneling current. Now the thickness of SiO_2 reached sub-1nm. This thickness corresponds to 3 layers of atoms (Figure. 1.2). In addition, Table 1.2 shows the 2010 update of the ITRS, which suggests Equivalent Oxide Thickness (EOT) will be required under 1nm level in near future. On the other hand, thedirect-tunneling leakage current is too increasing to be neglected as shown in Figure 1.3.

Therefore, SiO2 gate oxide film reaches its limit so that an alternative material gateinsulator, such as high-k material is required to continue the scaling down of MOS transistors.

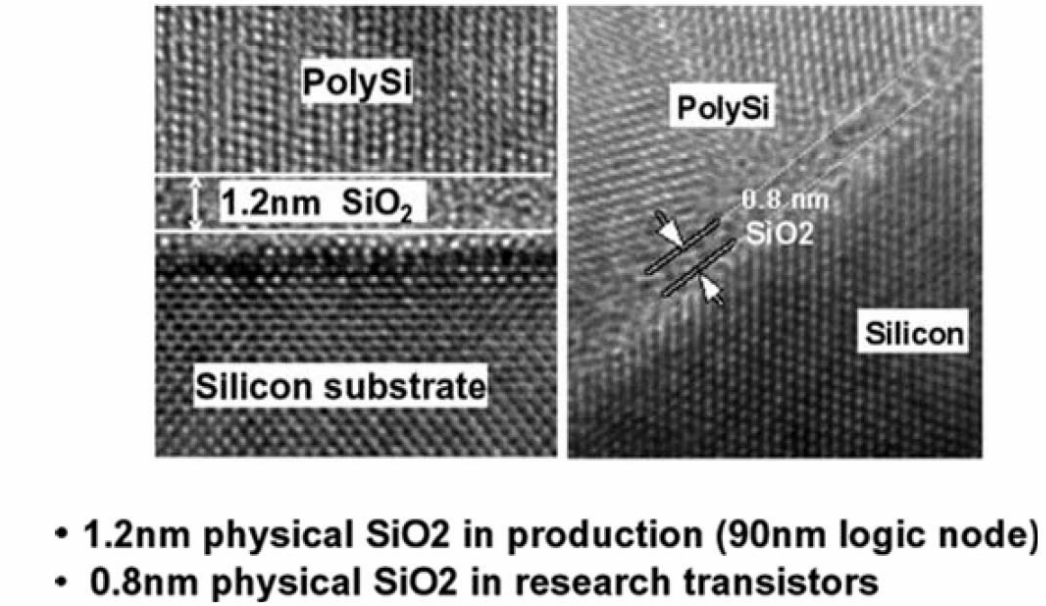


Figure 1.2 TEM cross section micrographs of polysilicon/SiO_2/Si with SiO_2 thickness of 1.2 nm and 0.8 nm, respectively.

Table 1.2 ITRS 2010 update[2].

Year of Production	2009	2011	2013	2015
Physical Gate Length (nm)	29	24	20	17
EOT (nm)	1	0.88	0.65	0.53
Gate Leakage Current density (A/cm^2)	0.65	0.9	0.1	1.3

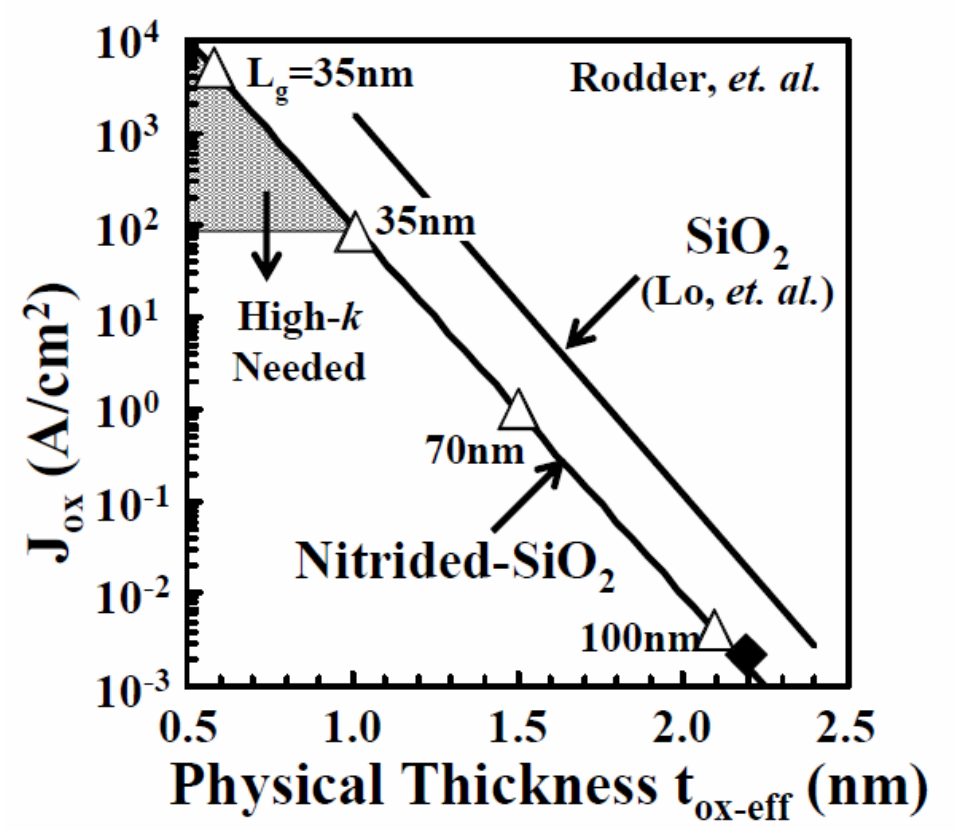


Figure 1.3 Relations between gate leakage current and physical thickness of SiO2 and SiON film

1.4 Requirements of High-k Materials

The high dielectric constant (high-k) materials have been attracted to suppress the leakage current. The key guidelines for selecting an alternative gate dielectric material are high dielectric constant, large band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Among them, high dielectric constant and large band gap are the minimum required characteristics to suppress the gate leakage current. The direct-tunneling leakage current (J_{DT}) flow through a gate insulator film is determined by the tunneling probability of carrier. The tunneling probability of carrier (D_{DT}) is shown in belowequation where physical thickness of insulator (d), electron effective mass in the gate insulator film (m^*) and barrier height of insulator (ϕ_b).

$$J_{DT} \propto \exp\left\{-\frac{4\pi d(2m^*\phi_b)^{\frac{1}{2}}}{h}\right\} \tag{1.1}$$

Relationship between physical thickness of SiO_2 ($dEOT$) and physical thickness of high-k gate insulator (d) obtained by the same gate capacitance value (C) is shown in below equation where dielectric constant of SiO_2 (ε_{ox}) and high-k gate insulator ($\varepsilon_{high\text{-}k}$).

$$C = \frac{\varepsilon_{high-k}}{d} = \frac{\varepsilon_{ox}}{d_{EOT}} \tag{1.2}$$

$$d = \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} d_{EOT} \tag{1.3}$$

Therefore, the gate leakage current can be suppressed by using high-k materials, which means that the physical thickness of high-k films can be thicken without changing EOT. In addition, the gate leakage

current can also be suppressed by using large band gap materials.

The possible candidate of several metal oxides system for the use of gate dielectric materials is shown in while spaces of Figure1.4.

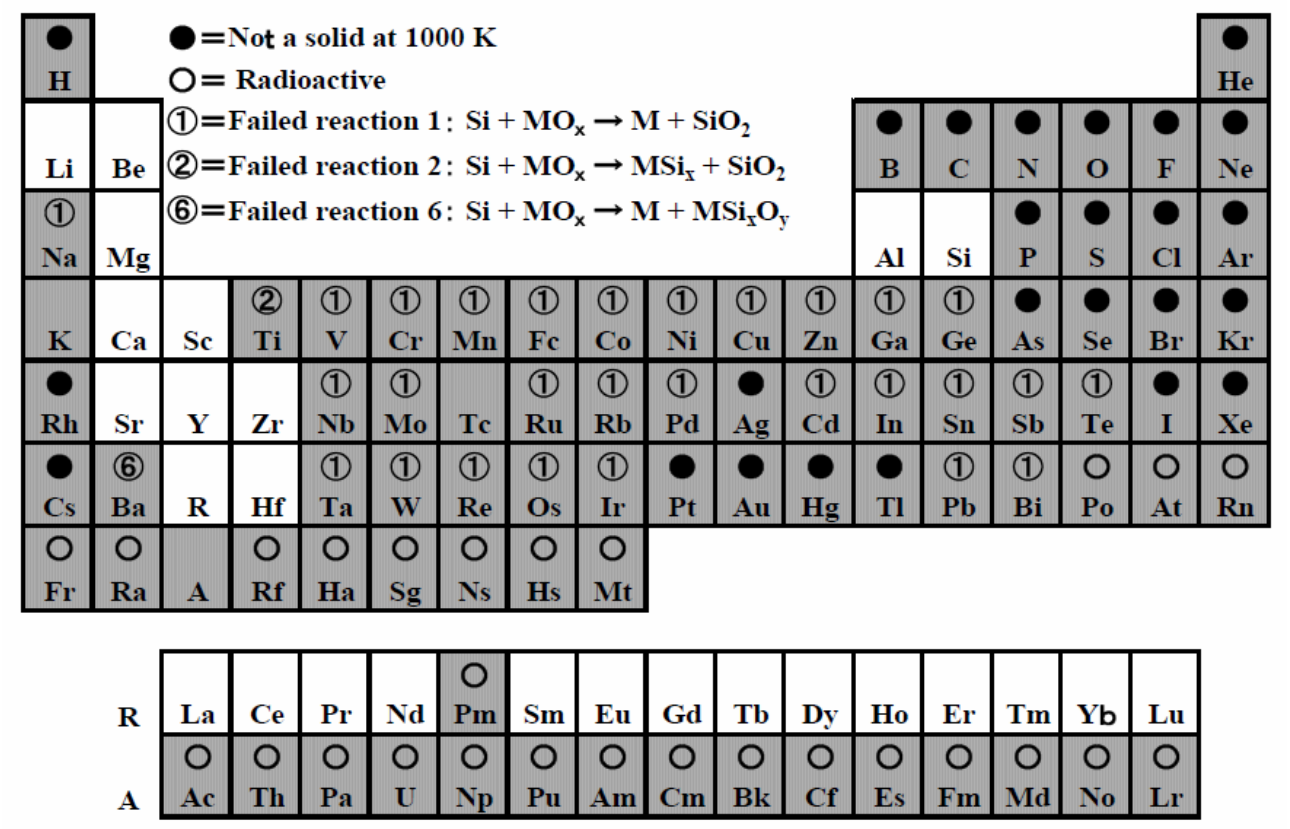


Figure.1.4 Relations between gate leakage current and physical thickness of SiO2 and SiON film

As shown in Figure 1.8, many papers on high-k materials are submitted in the primary conferences up to 2002. However, from 2003 to now, the candidate of high-k materials have narrowed down to Hf-based materials. Therefore, Hf oxides (HfO_2) and Hf-based silicates or nitrides (HfSiON), with dielectric constants of 25 and 10 to 15 respectively, are among the promising materials for the 45-nm-technology node.

Usually, when the EOT becomes small, the effective carrier mobility tends to decrease due to scattering

in the high-k layer or at the interface between the high-k layer and the substrate. It has reported that Hf-based films have reduced scattering when a SiO_2-based interfacial layer of 0.5 to 0.7 nm is inserted, however, this attempt increases the EOT.

Consequently, in this work, Lanthanum Oxide (La_2O_3), one of the rare earth oxides, has been tried as a gate insulator, because it has a relatively high dielectric constant of 23.4, which is slightly higher than that of HfO_2 and a high band offset of 2.3 eV from the conduction band of silicon to La_2O_3 has the advantage of further reducing the leakage current. La_2O_3 is expected to be the third generation gate dielectrics, which is Hf-based oxides below 45 nm nodes.

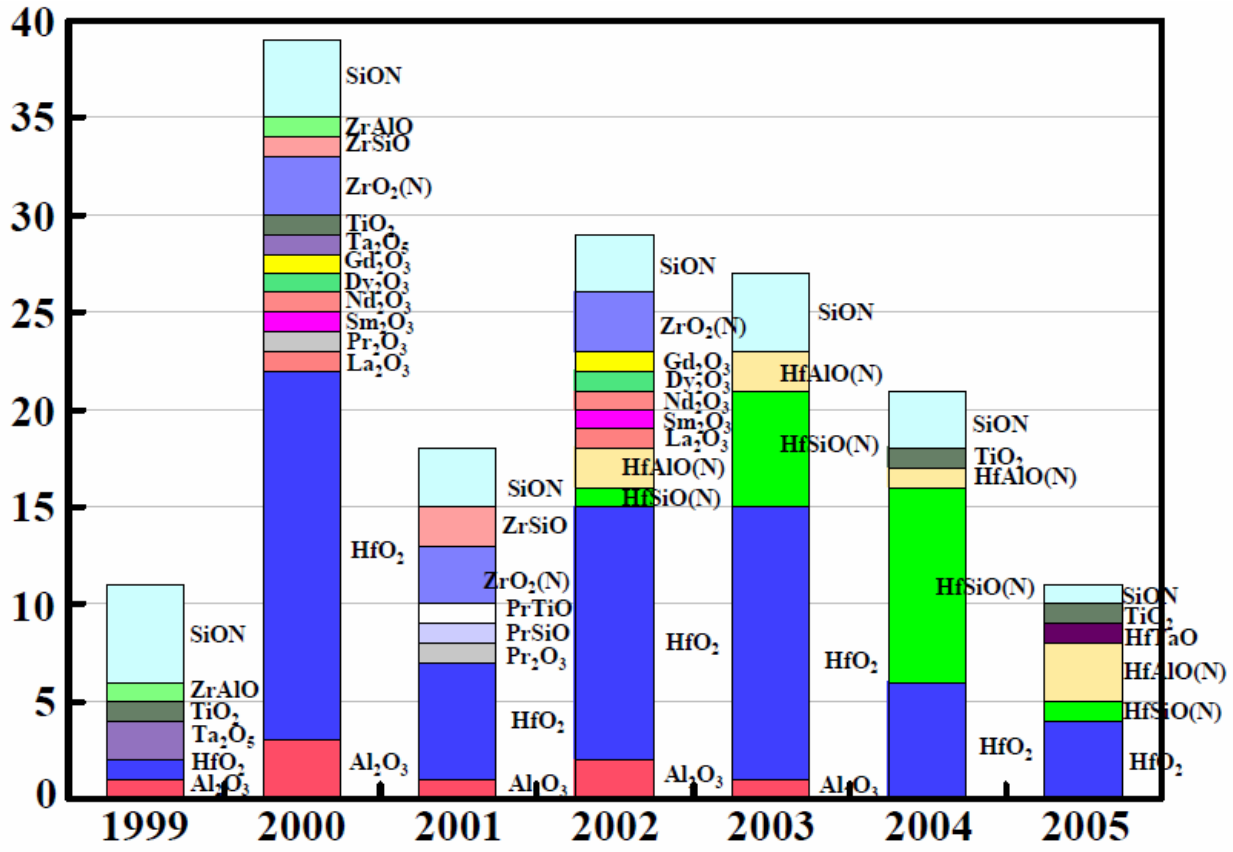


Figure.1.5 Relations between gate leakage current and physical thickness of SiO2 and SiON film

1.5 Properties of La_2O_3

For achieving a low EOT, high-k gate dielectrics materials must have high enough dielectric constant. However, material with very high dielectric constant tends to have narrower band gap that allows higher Schottky conduction currents and tunneling currents. Figure 1.6 shows band gap energy of several metal oxide and silicate materials as a function of dielectric constants. La_2O_3 gives high dielectric constant of 23.4 and wide band gap of 5.6 eV that is suitable for the use of gate dielectrics. So, La_2O_3 and its alloys with other metal oxides are promising insulators for the next-generation high-*k* gate insulators to achieve higher drivability as well as lower gate leakage [5]. Lower gate leakage density is shown in Figure.1.7.

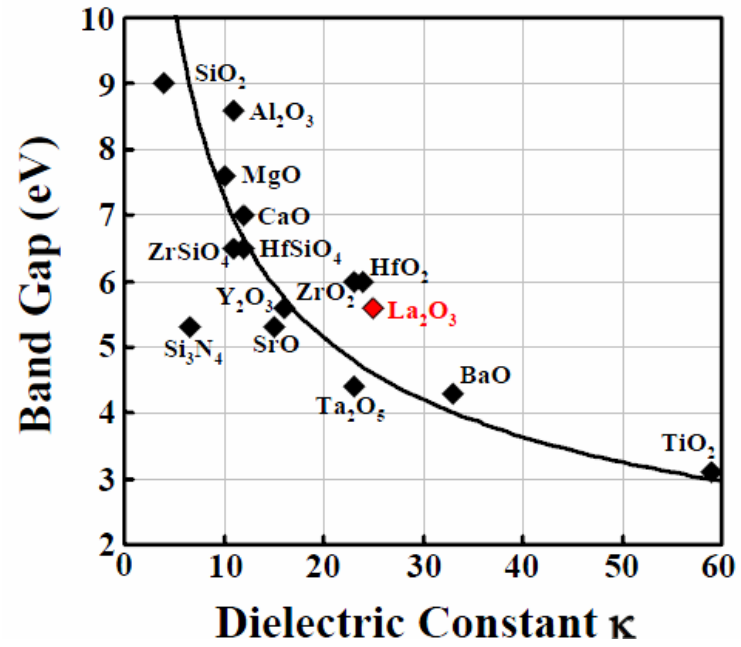


Figure 1.6 Band gap energy of several metal oxide and silicate materials as a function of dielectric constant.

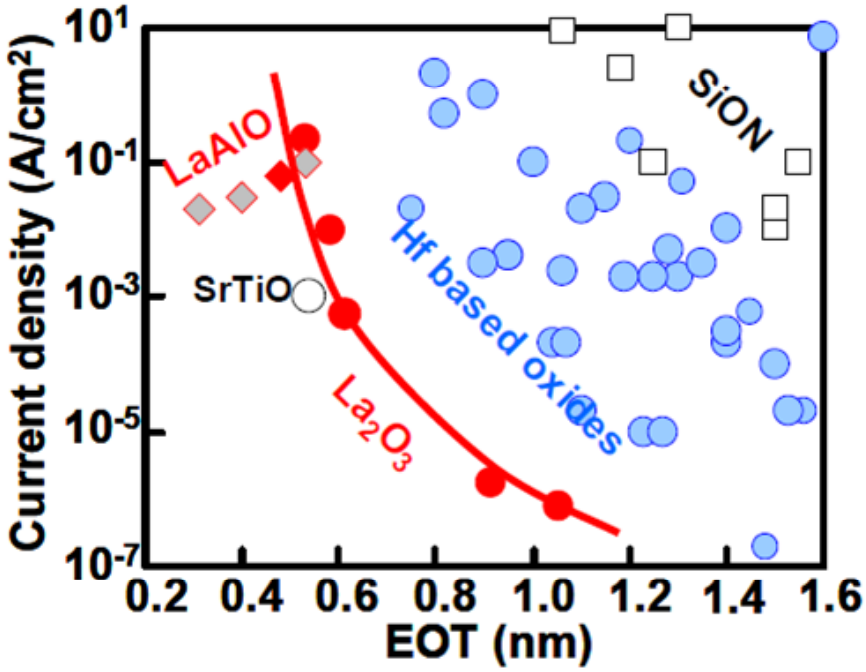


Figure 1.6 Band gap energy of several metal oxide and silicate materials as a function of dielectric constant.

1.6 Requirements of Atomic Layer Deposition.

There have been many studies to deposit La_2O_3 and related rare-earth oxides by physical vapor deposition such as electron-beam (EB) evaporation and sputtering. Implementation of these materials to CMOS manufacturing needs more studies of the Chemical vapor deposition (CVD) or Atomic Layer Deposition (ALD) process. There are following advantages in ALD process.

・uniform film can be formed over the wafer.

・A precise control of film thickness by the cycle number

・Alloy composition can be designed

・Applicable to 3D structures such as FinFET and nanowire

Therefore, the ALD becomes more and more important in future.

There are present issues in ALD. Optimal source material and process conditions are not clear. It's difficult to achieve small EOT with good MOS propertieties.

1.7 Purpose of This Study

La_2O_3 and it alloys have a excellent property. There have been many studies to deposit La_2O_3 and related rare-earth oxides by physical vapor deposition such as EB evaporation and sputtering. So, ALD insulator growth process, interface and insulator property are big room for consideration.

The purpose of this study is to identify the ALD growth conditions of La_2O_3 and to evaluate electrical characteristics. In addition, ALD growth conditions are also sought about another insulators(CeOx, MgO, SrO) to inform layer stuck structure.

Chapter 2
FABRICATION AND CHARACTERIZATION METHODS

2.1 Experimental Procedure

2.1.1 Fabrication Method MOS Capacitor

The fabrication procedure for MOS Capacitor is shown in Figure 2.1. Oxide thin films were deposited on n-type silicon (100) substrate by Atomic Layer Deposition(ALD). Substrate is H2SO4/H2O2 mixture (SPM) cleaning and HF-dip processes. Then, upper electrode and back side electrode were formed by Vacuum Evaporation Method or RF Magnetron Sputtering Method. In this experiment, we performed one type of the annealing method using Rapid Thermal Annealing (RTA) method. It is the Post Metallization Annealing (PMA). After metal formation, thermally evaporated Al was coated on backside of the wafer to characterize the electrical properties.

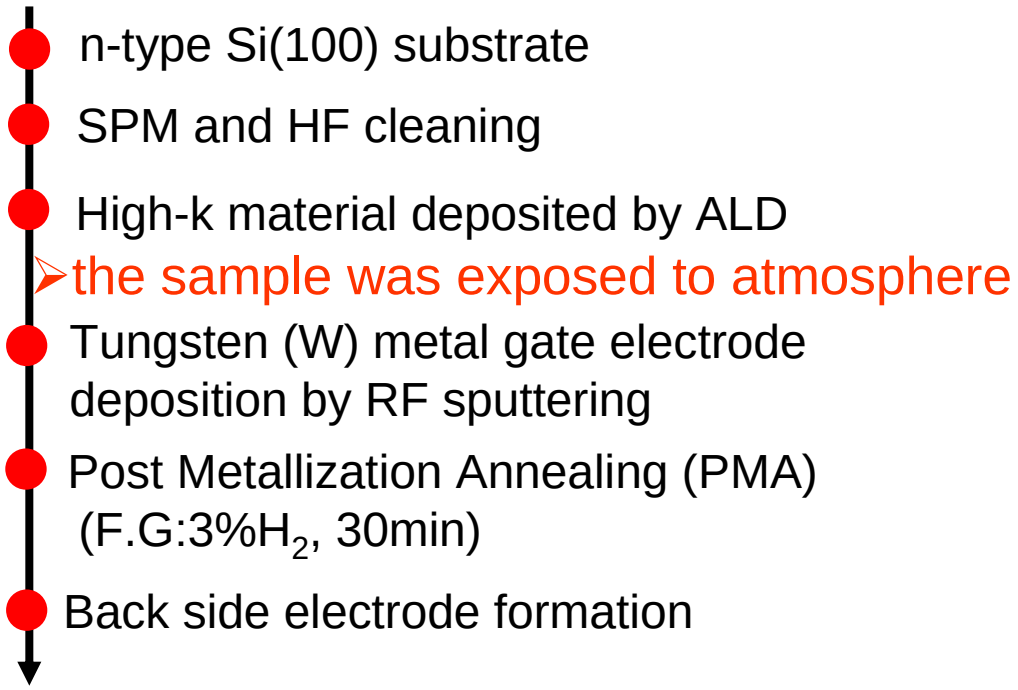


Figure 2.1 The fabrication procedure for MOSCAP

2.1.2 Cleaning Method of Si Substrate

For deposition of thin film maintaining the quality requires quite clean surface of Si substrate. There are many method of cleaning substrate. But one of the most used methods is wet cleaning by chemical liquid. There are some kinds of the liquids which are used in wet cleaning process shown in Table 2.1. And these liquid have each effect against substrate pollutions. So, one liquid can't eliminate all pollutions. In this Study, I used the process like figure.2.2. First step is SPM Cleaning (H_2SO_4:H_2O_2:H_2O=4 : 1) eliminates metal and organic materials. And then, the native or chemical oxide was removed by diluted hydrofluoric acid (H_2O_2:H_2O=1:100).

Table 2.1 Main cleaning process

The name of Cleaning	Chemical liquid	The Characteristic
APM Cleaning	$NH_4OH/H_2O_2/H_2O$	The effect of elimination against organic materials and particles
FPM Cleaning	$HF/H_2O_2/H_2O$	The effect of elimination against metal and oxidation layer
HPM Cleaning	$HCl/H_2O_2/H_2O$	The effect of elimination against metal
SPM Cleaning	H_2SO_4/H_2O_2	The effect of elimination against metal and organic materials
DHF Cleaning	H_2O_2/H_2O	The effect of elimination against metal and oxidation layer
BHF Cleaning	$HF/NH_4F/H_2O$	The effect of elimination against oxidation layer

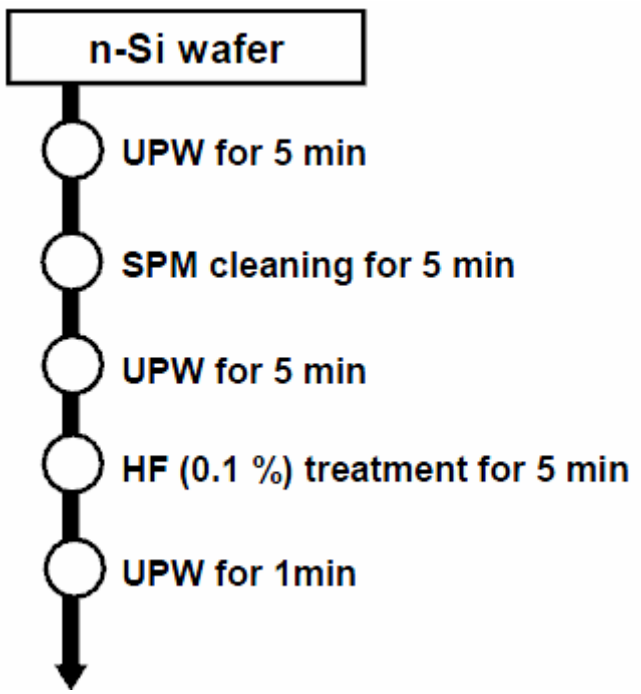


Figure 2.2 The fabrication procedure for MOSCAP

2.1.3 Atomic Layer Deposition Method

Figure 2.3 shows CVD machine that run ALD. This machine has no dead volume. Two TMP is used to evacuate source and H_2O gas. Used Si wafer size is 2 inch.

The gas-feed sequence of an ALD cycle is schematically shown in Figure 2.4. A Ar is used as Carrier gas and purge gas. Source gas/H_2O feed and purge periods were 100 and 300 sccm, respectively.

Table2.2 shows source materials are used ALD or CVD. As for the La_2O_3 growth, β-diketonate and silylamide precursors were initially used as the La source [6,7]. Recently, cyclopentadienyls (Cp) and amidinates were often used because of their high vapor pressures and moderate reactivity. Advantages and disadvantages of cyclopentadienyls (Cp) and amidinates are not clear. [8-13]

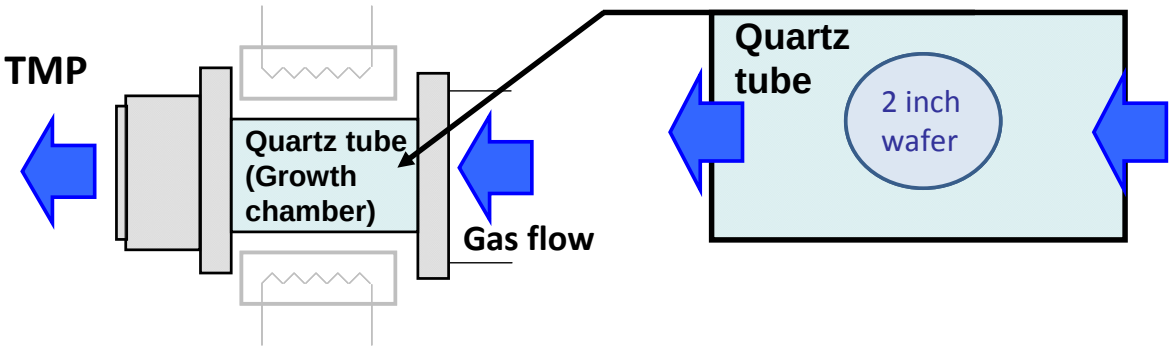


Figure 2.3 image of CVD machine

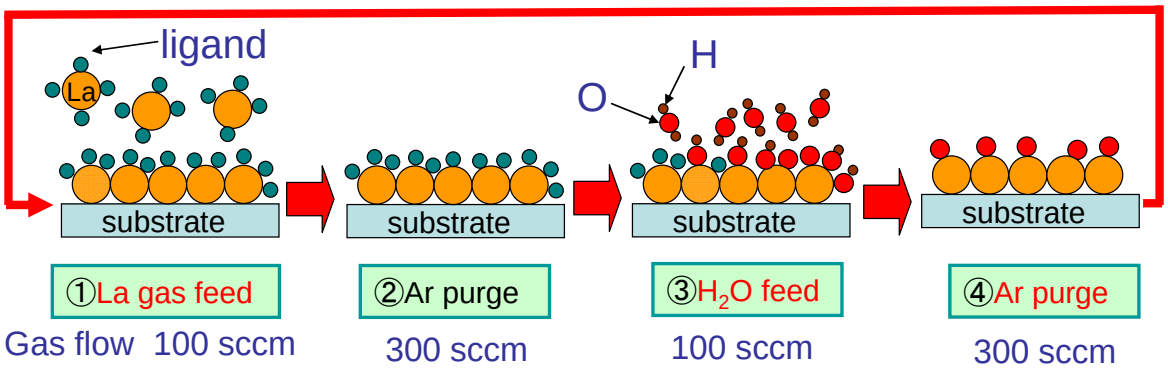
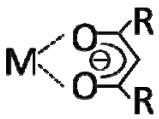
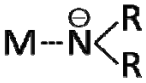
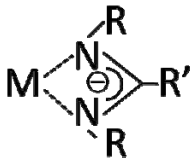


Figure 2.4 Flow sequence of ALD

Table 2.2 Source materials are used ALD or CVD

Materials	Structural formula	Properties
β -diketonate		Too stable → O_3 is necessary to form oxide. → EOT increases due to Si oxidation
silylamide		Films contain high Si concentration → k values are rather low
Cyclo-pentadienyl		Relatively new material High vapor pressure Modest reactivity with water (H_2O) → Strong candidates for ALD-source
amidinate		

2.1.4 RF sputtering

In this experiment, gate metals W was deposited using RF sputtering. The base pressure of sputtering chamber was maintained to be 10-7 Pa by TRP and RP (shown in Fig.2.4). In sputtering, Ar was flowed into the chamber and the pressure of which was set to be 10-4 Pa, the AC current power was 150W.

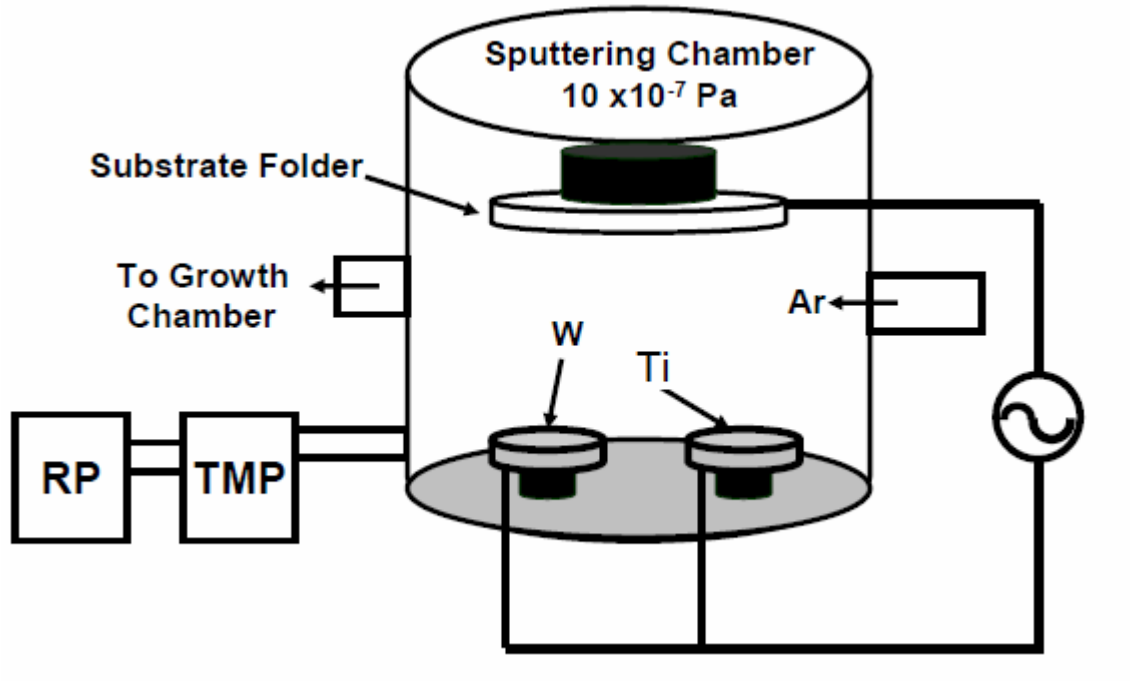


Figure 2.5 Schematic model of RF Sputtering

2.1.5 Photolithography

The process flow of photolithography that used throughout this study is shows in Figure.2.6. Electrical hotplate is used for baking purposes. The spin-coated layer photoresist was aligned and exposed through tungsten coated e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. MJB4 of Karl Suss contact-type mask aligner as shown Figure 2.7 was used for aligning and exposition purposes. The exposure duration was set to 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.) after dipped into the solvent for 2 minute and baked at 130 °C for 5 minutes.

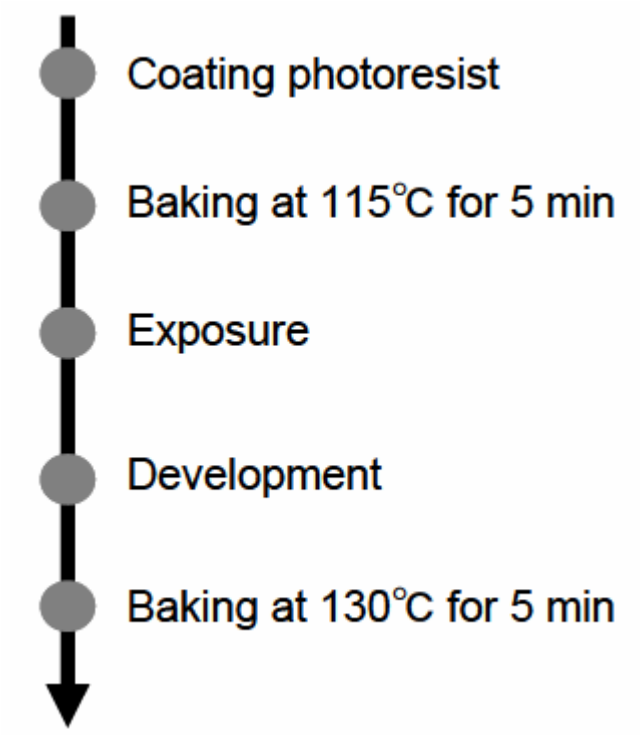


Figure 2.6 The process flow of photolithography

Figure 2.7 Photo of mask aligner

2.1.6 Reactive Ion Etching

Reactive Ion Etching (RIE) which uses one of chemical reactive plasma to remove materials deposited on wafers was adopted to etch gate electrode in this study. There are two electrodes in vacuum chamber (shown in figure 2.8). One is usually connected to ground and gas is put into the chamber and exits to the pump, in this study SF_6 and O_2 are used to remove gate W and resist each. And plasma is generated and ion direct for substrate and remove gate electrode and resist chemically.

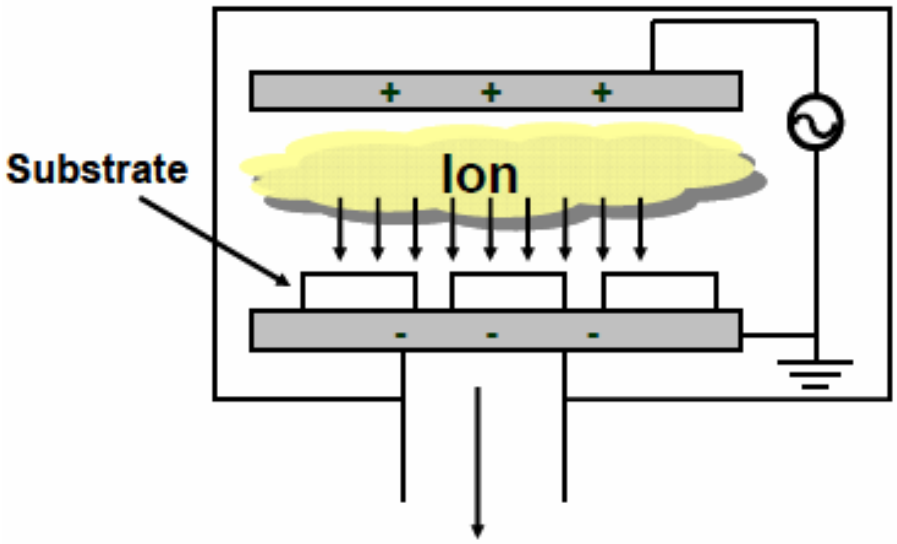


Figure 2.8 Schematic illustration of Reactive Ion Etching (RIE)

2.1.7 Rapid Thermal Annealing (RTA)

Thermal annealing processes (shown in fig. 2.8) are often used in modern semiconductor fabrication for defects recovery, lattice recovery and impurity electrical activation of doped or ion implanted wafers. In this study, MOS capacitors were post metallization annealed after gate electrode deposition.

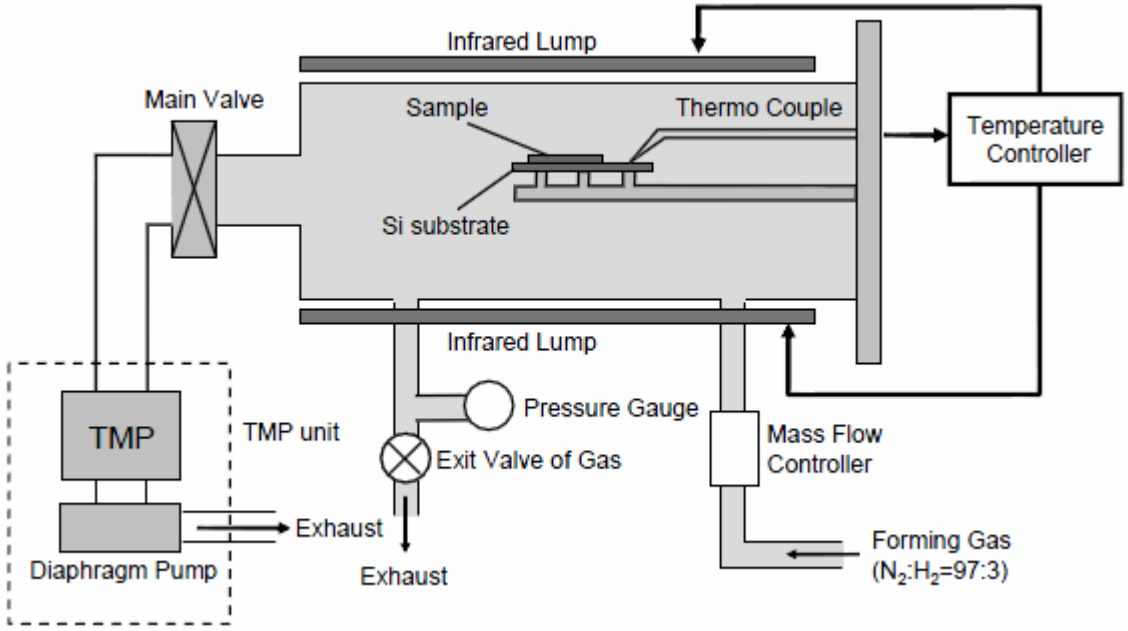


Figure 2.9 Schematic image of infrared annealing furnace

2.1.8 Vacuum Thermal Evaporation method

All of Al metals in this work were obtained from deposition with bell jar vacuum thermal evaporation. Figure 2.10 illustrates a schematic drawing for vacuum thermal evaporation system. The system is utilized with Turbo Molecular Pump (TMP) to pump down to several 10-5 Torr. In case of MOS capacitor fabrication, metal shadow mask with circle opening of 200 μm diameters was used. Filament is made of tungsten, was used for heating the Al source up to its vapor temperature. Both filaments and Al sources are made of Nilaco, inc. with material purity of 99.999%.

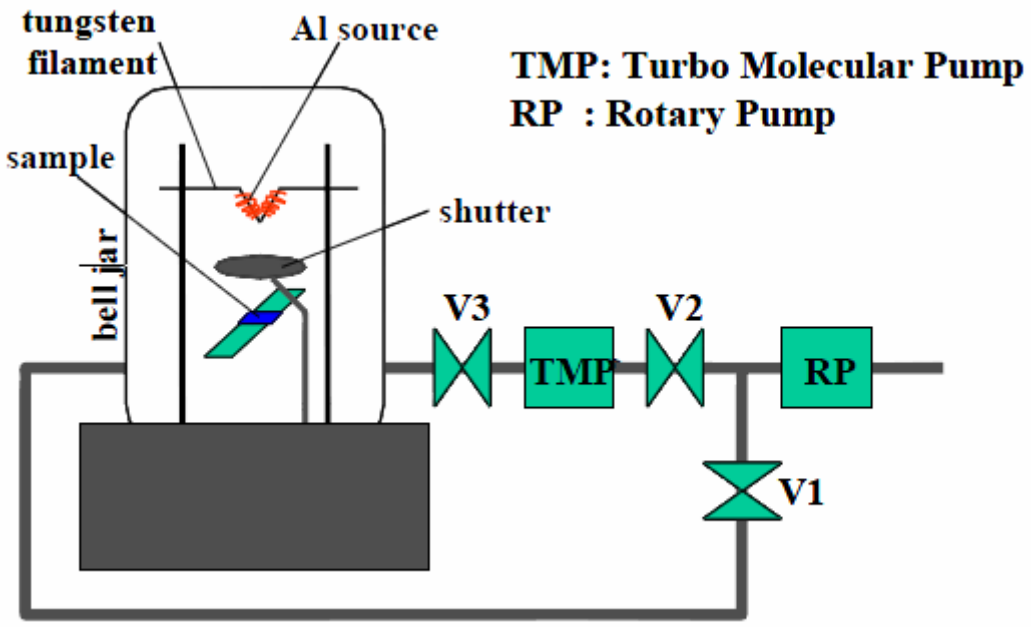


Figure 2.10 Schematic drawing for vacuum thermal evaporation system

2.2 Measurement Methods

2.2.1 Atomic Force Microscopy

AFM enables to measure surface morphology by utilizing force between atoms and approached tip. The roughness of sample surface is observed precisely by measurement of x-y plane and z. Fig. 2.11 shows the principle of AFM. Tip is vibrated during measurement, and displacement of z direction is detected. This method is called tapping mode AFM (TM-AFM). Resolution limit for normal AFM is 5~10nm depending on distance between surface and tip. On the other hand, resolution limit for TM-AFM is depended on size of tip edge. Thus, resolution limit for TM-AFM is about 1nm.

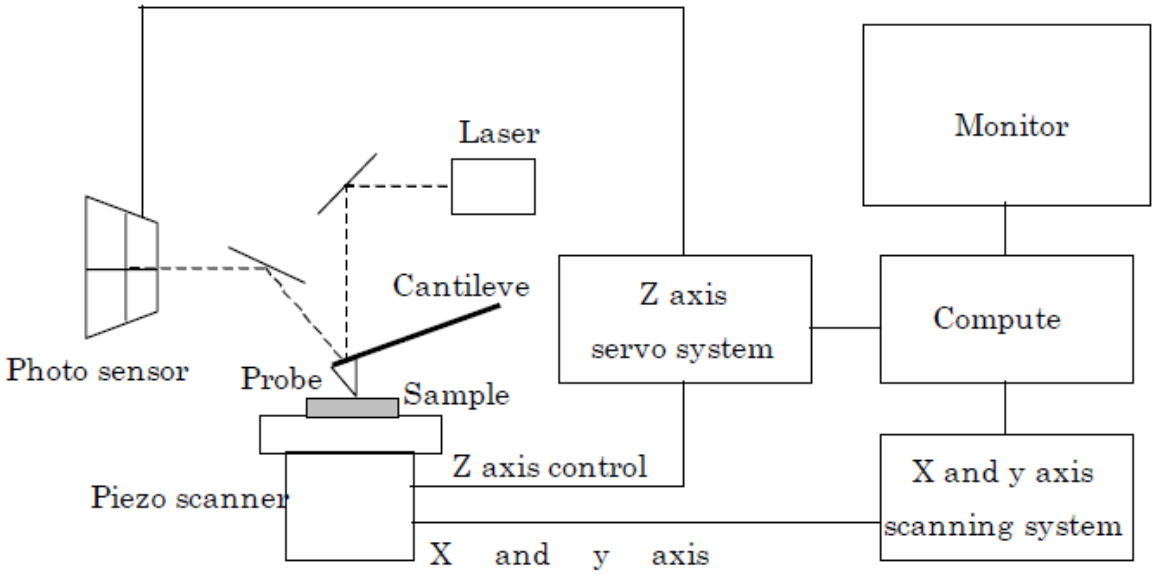


Figure 2.11 Schematic of AFM Principle

2.2.2 C-V (Capacitance-Voltage) Measurement

Figure 2.14 shows the ideal of C-V characteristic of p-type MOS diode. Here, “ideal” MOS diode means that there is no interface-trapped charge (Q_{it}), fixed charge (Q_f), oxide trap charge (Q_{ot}) and mobile ion charge (Q_m). The total capacitance (C) of MOS diode equals the oxide capacitance (C_0) which is accumulated and the silicon capacitance (C_{Si}) connected in series as follows,

$$C = \frac{C_0 C_{Si}}{C_0 + C_{Si}} \quad (\mathrm{F/cm^2}) \tag{2.1}$$

And we obtain

$$\frac{C}{C_0} = \frac{1}{\sqrt{1 + \frac{2\varepsilon_{ox}{}^2 V}{qNA\varepsilon_{Si} d^2}}} \tag{2.2}$$

where we have written out C_{Si} explicitly. This equation indicates that the capacitance decreases with increase of the gate voltage.

If applied voltage is negative, depletion layer is not generated but hole is accumulated in surface of silicon. As a result, the total capacitance equals approximately the oxide capacitance (ε_{ox}/d). Beyond strong inversion, even if the voltage increases more than that, the thickness of depletion layer doesn’t increase any longer. The gate voltage is called threshold voltage (V_T) in this condition as follows.

$$V_T = \frac{\sqrt{2\varepsilon_{Si} q N_A (2\psi_B)}}{C_0} + 2\psi_B \tag{2.3}$$

Moreover, capacitance is as follows

$$C_{\min} = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox} / \varepsilon_{Si}) W_m} \tag{2.4}$$

In conventional MOS diode, however, the difference of work function between metal and oxide (φms) is not zero and there are varies space charges, such as Q_{it}, Q_f, Q_{ot} and Q_m, in oxide and interface of oxide-semiconductor, therefore those affect characteristics of ideal MOS diode. As a result, flat band voltage (V_{FB}) is shifted from ideal that as follows,

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_0} \tag{2.5}$$

And C-V carve is parallel shifted as shown in Figure 2.12 (b) because φ_s, Q_m, Q_{ot} is not zero. And in addition to that, when there are much Q_{it}, that is changed by surface potential. Therefore, curve (c) as shown in Figure 2.12 is shifted and bended by Q_{it} value.

CET (Capacitance-equivalent-thickness) in other words, *Tox* electrical equivalent means the thickness of equivalent SiO2, can be calculated from accumulated capacitance of C-V characteristic as follows,

$$CET = \varepsilon_0 \varepsilon_{Si} \frac{S}{C_0} \tag{2.6}$$

where ε_0, ε_{Si} and S are permittivity of vacuum, dielectric constant of SiO_2 and area of a capacitor. In this study, HP4284A (Hewlett-Packard Co. Ltd.) is used for measurement C-V characteristics. The range of measurement frequency is from 1k to 1MHz

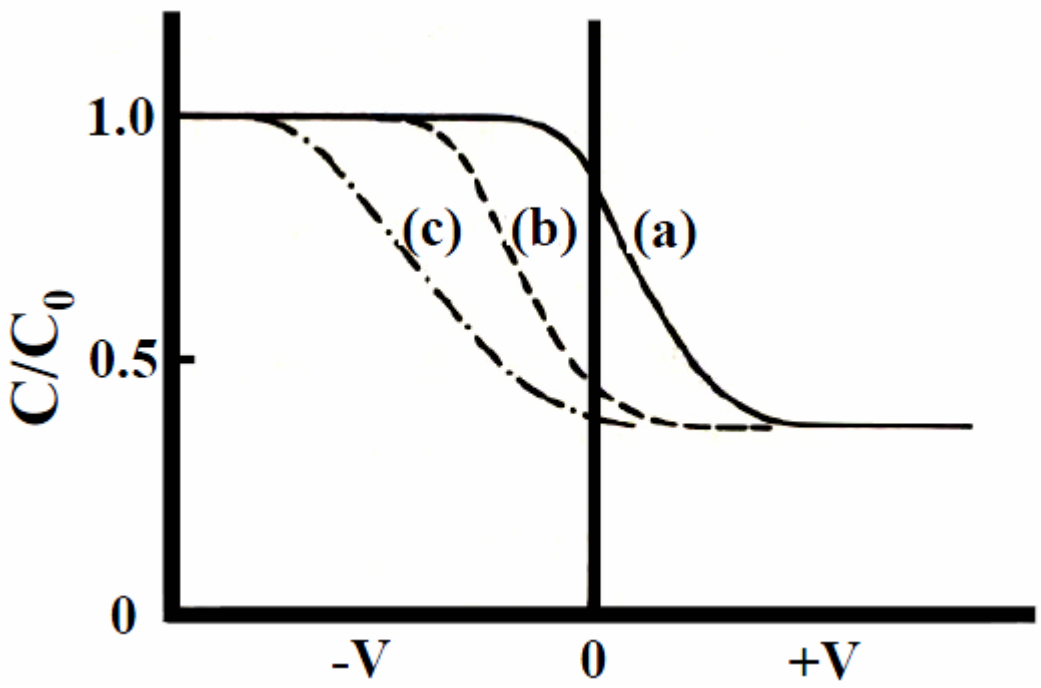


Figure 2.12 The ideal of C-V characteristics of p-type MOS diode.

2.2.3 J-V (Leakage Current Density-Voltage) Measurement

It is important to suppress the leakage current of the gate dielectric film as small as possible in order to lower the power consumption of LSI. To estimate the leakage current density, J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

Chapter 3

GROWTH CHARACTERISTICS

OF ALD

3.1 Self-limiting Growth Condition

A self-limiting growth is generally characterized by a constant growth rate per cycle with varying the feed time or pressure of the source gases. In addition, the self-limiting growth is only weakly dependent on Growth temperature (T_s).

In this section, we clarify the process window to achieve self-limiting ALD with each metal source and H_2O.

3.1.1 La_2O_3

La_2O_3 insulators were prepared by ALD using La(^{i}PrCp)$_3$ and La(^{i}PrFAMD)$_3$ as the metal source and H_2O as the oxidant. The gas-feed sequence of an ALD cycle is schematically shown in Figure 3.2

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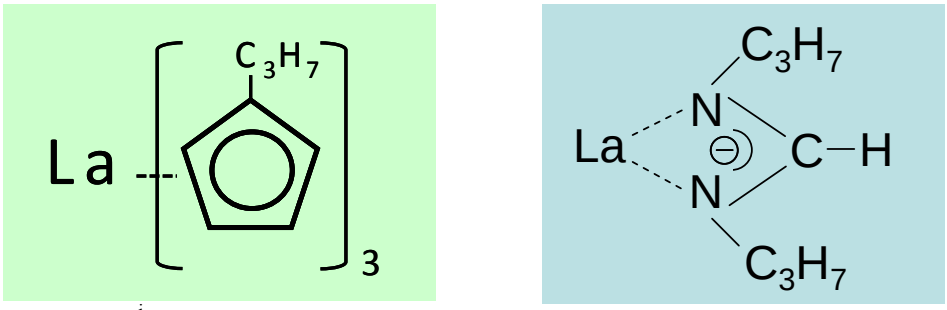


La(^{i}PrCp)$_3$ La(FAMD)$_3$

Figure 3.1 Used metal source

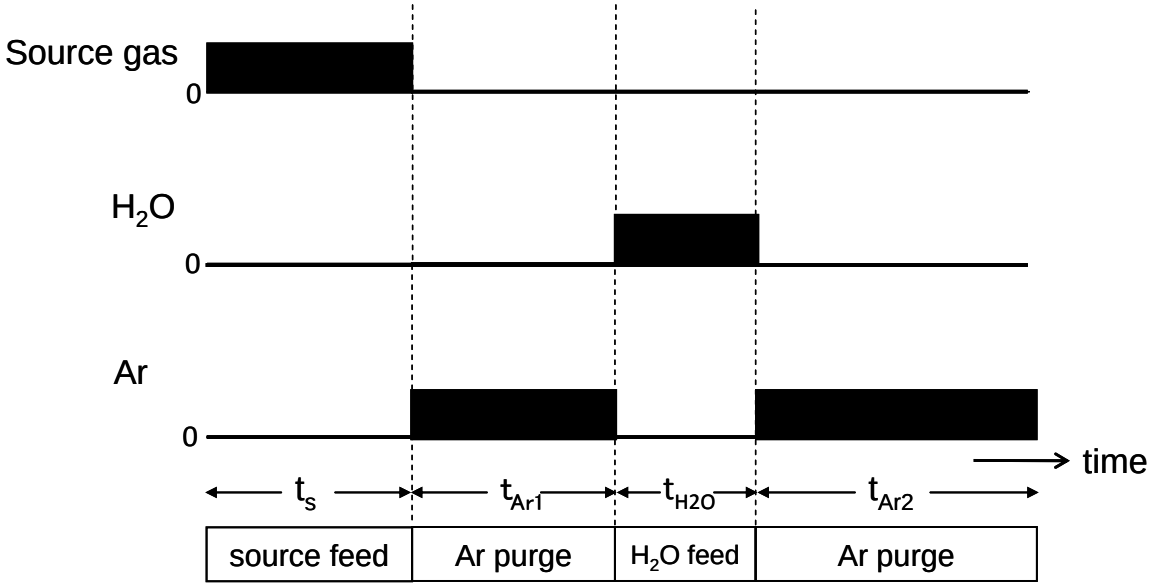


Figure 3.2 Flow sequence of ALD

3.1.1.1 La(^{i}PrCp)$_3$

The first, growth characterization ALD using La(^{i}PrCp)$_3$ and H_2O is considered. Figures 3.3, 3.4, and 3.5 show, respectively, the effects of the La feed time (t_S), H_2O feed time (t_{H2O}), and T_s on the growth rate. Figure 3.3 shows that the growth rate does not depend on t_{H2O} for both the low T_s (175 °C) and high T_s (250 °C) conditions. In figure 3.4, the growth rate was almost constant for t_S of 2.5 – 10 s when T_s was below 200 °C. On the other hand, the growth rate increased with increasing t_S at T_s higher than 200 °C. These results indicate that T_s needs to be below 200 °C to achieve the self-limiting growth and that growth above 200 °C gives rise to the CVD-like mechanism. Figure 3.5 shows the Arrhenius plot of the growth rate in the T_s range from 135 to 250 °C. The growth rate is only weakly dependent on T_s, with an activation energy of 12 kJ/mol (0.12 eV). Figures. 3.3, 3.4, and 3.5 clearly show that La_2O_3 growth using La(^{i}PrCp)$_3$ and H_2O is self-limiting when the T_s is kept below 200°C.

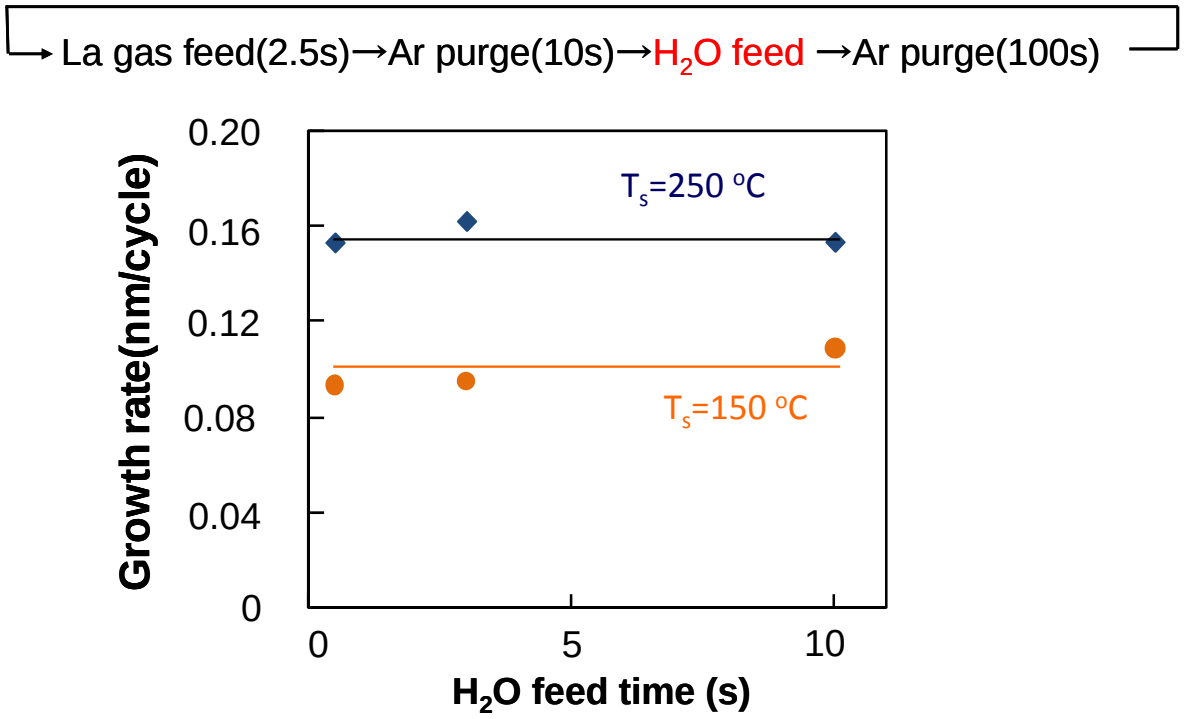


Figure3.3 Dependence of growth rate on H_2O feed time at 175 and 250℃

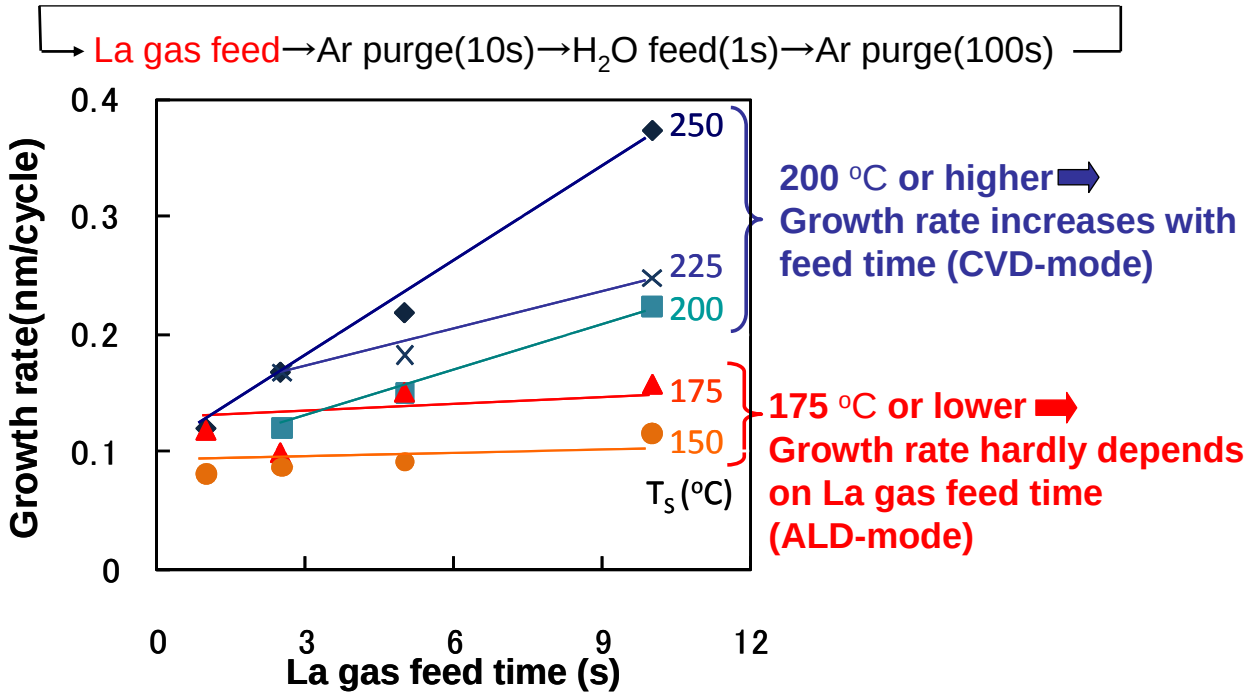


Figure3.4 Dependence of growth rate on La source feed time at various temperature

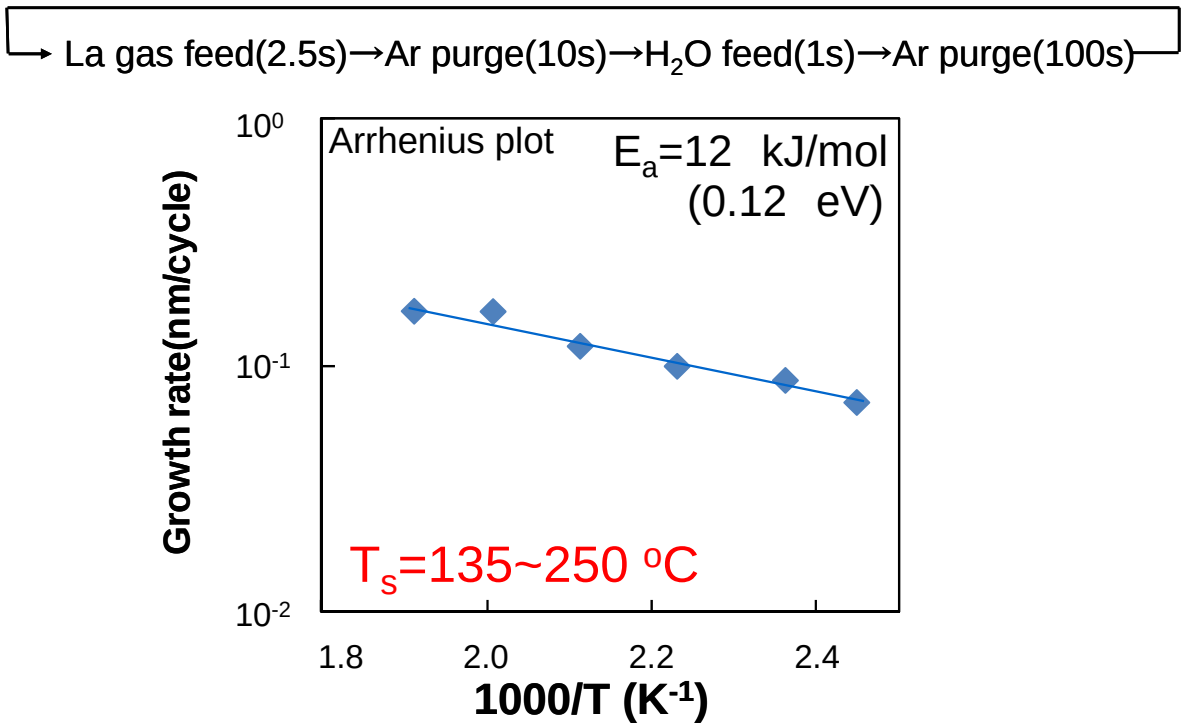


Figure3.5 Arrhenius plot of the growth rate. t_S and t_{H2O} were 2.5 s and 1 s.

Under self-limiting growth, good thickness uniformity is observed (Figure 3.6). Then standard deviation of thickness is 1.8 percent.

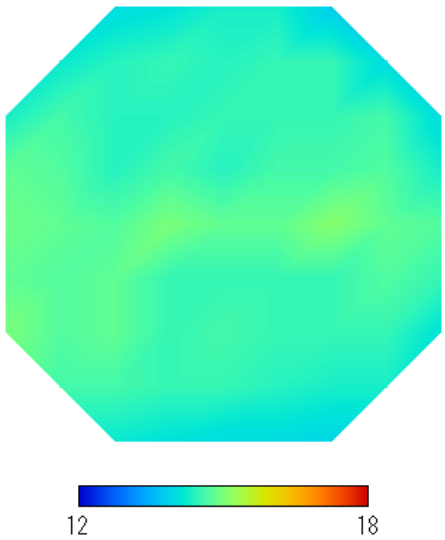


Figure3.6 Thickness uniformity under self-limiting growth condition.

Table 3.1 Comparison with past report

		Oxide source	Growth temperature	Growth rate
S. Y. No et al. (Seoul National University)	J. Appl. Phys. **100**, 024111 (2006)	H_2O	370 °C	0.09 nm/cycle
W. He et al. (NUS, Singapore; Samsung)	J. Electrochem. Soc. **155**, G189 (2008)	H_2O	260-480 °C	0.03-0.01 nm/cycle
S. Schamm et al. (CNR, Italy)	J. Electrochem. Soc., **156**, H1 (2009)	H_2O	260 °C	unknown
W.-S. Kim et al. (Hanyang University)	J. Vac. Sci Technol. B **26**, 1588 (2008).	O_2 plasma	400 °C	unknown
H. Jin et al. (NIMS; Chungbuk National University; Samsung)	Appl. Phys. Lett. **93**, 052904 (2008)	Ozone	450 °C	unknown
This study		H_2O	< 200 °C	0.15

Table 3.1 shows comparison with past reports. In the past studies, growth temperature was in the range from 260 to 480 ℃. Clear evidence of self-limiting growth was not reported. In this study, self-limiting growth condition is clearly identified at <200 ℃

3.1.1.2 La(^{i}PrFAMD)$_3$

Figure 3.7 shows thickness profiles of the La_2O_3 film prepared by La(^{i}PrFAMD)$_3$ along the gas flow direction. T_S was changed from 125 to 250 ℃. As T_S was high, there is a tendency for growth rate to increase by the upper of gas flow. It is suggested that the growth depends on CVD structure. Thickness uniformity is improved with decreasing T_S. However in that case, the growth rate increased with increasing La source feed time. Therefore, this condition to realize a self-limiting growth was not found by La(^{i}PrFAMD)$_3$.

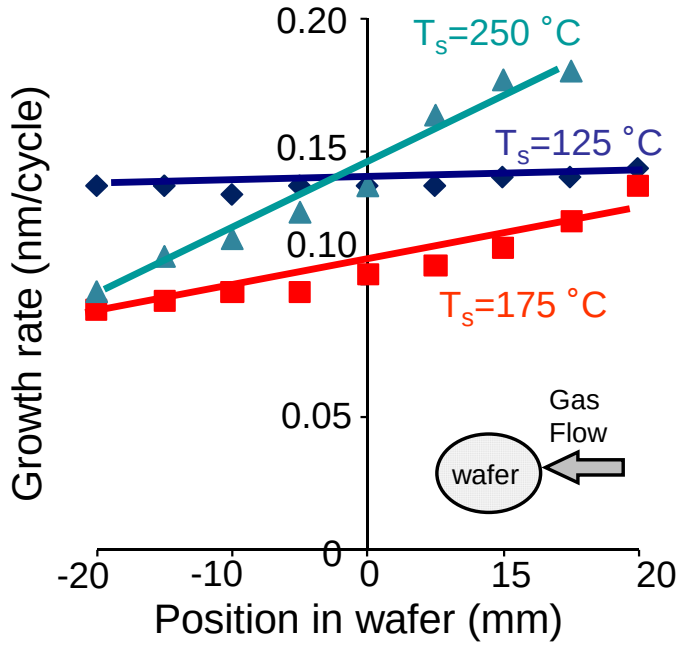


Figure3.7 Thickness profiles of the La_2O_3 film along the gas-flow direction was T_S changed from 125 to 250 ℃. t_S, t_{Ar2} and t_{H2O} were 10, 100 and 1s.

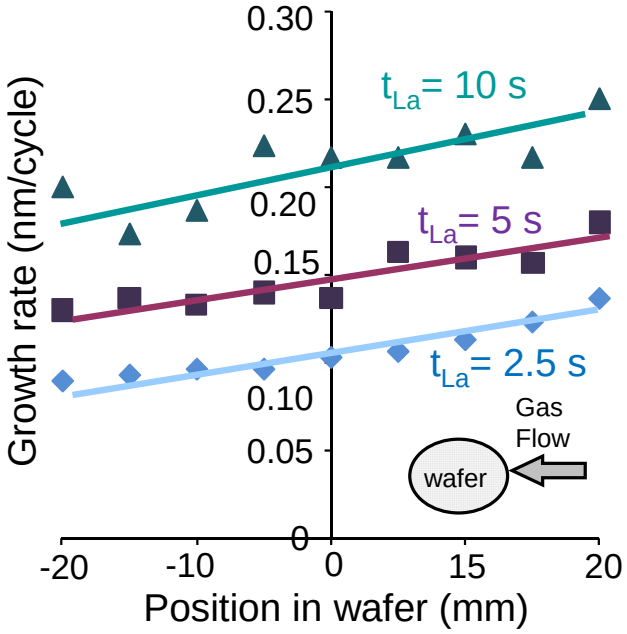


Figure3.8 Thickness profiles of the La_2O_3 film along the gas-flow direction. T_S was fixed at 175 ℃ and t_S changed from 2.5 s to 10 s are compared.

3.1.1.3 Effect of Ar Purge Time on Thickness Uniformity

In this section, Ar purge time after H_2O feed time is important process condition to realize self-limiting growth or to gain good thickness uniformity is shown below. Figure 3.9 shows growth rate uniformity along the gas flow direction in the case of $La(^{i}PrCp)_3$. The Ar purge time is 10 or 100 seconds. Even if growth temperature was 175 ℃ that condition is self-limiting growth, it is understood that long purge time of 100 seconds was necessary. In the case of 250 ℃ CVD structure contributes, contribution of the CVD structure become more remarkable with decreasing purge time. The similar result was observed even with $La(^{i}PrFAMD)_3$

The result that contribution of the CVD structure becomes larger with decreasing Ar purge time shows La source reacts with the residual H_2O of the infinitesimal quantity. Purge gas flow rate is condition that replace reactor 100 times per one second. Reactor is cannular and has no dead volume. Nevertheless, particle H_2O is stayed behind. It is thought that causes of staying behind H_2O is the result the H_2O which was detached from La_2O_3 (or the hydrate) after H_2O feed reacts La source is fed by next cycle. As rare earth oxides have high hygroscopicity is used as a oxidant, this is the essential problem. If O_3 is used as a oxidant, this problem will be avoided. However, in the case of O_3, basic Si is become oxidized.

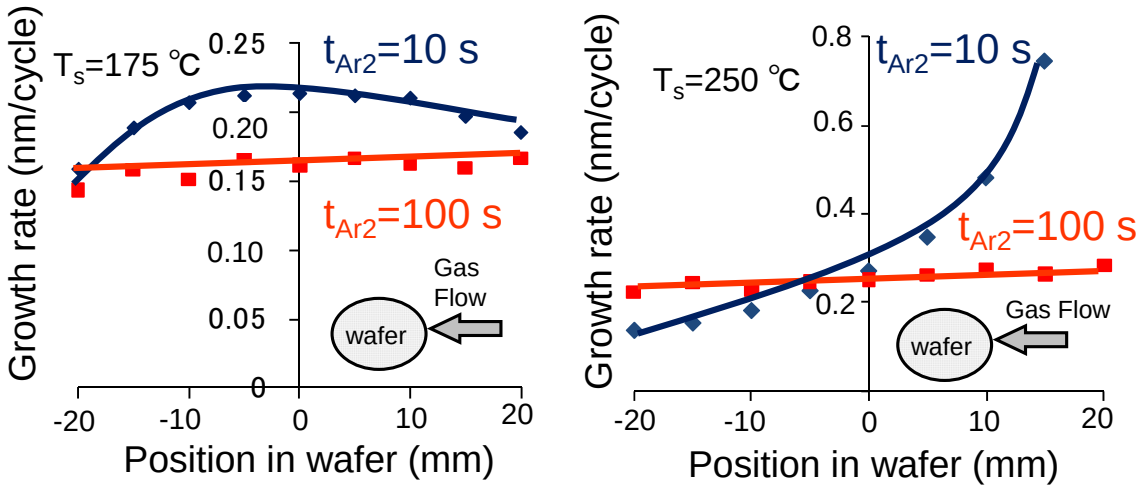


Figure3.9 Effects of Ar purge time after H_2O feed t_{Ar2} or thickness uniformity.
La source was La(^{i}PrCp)$_3$ t_{Ar} was 10 or 100s. Data for T_S = 175 and 250 ℃ are shown.

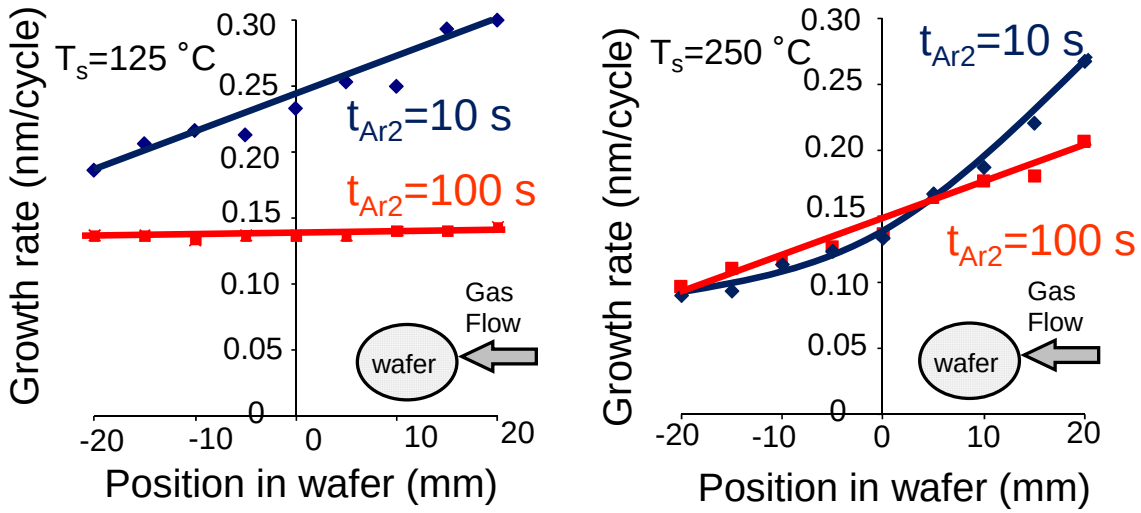
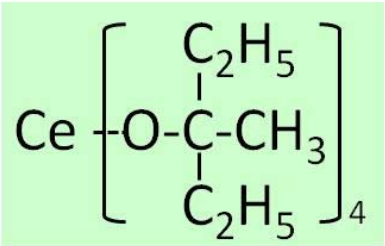
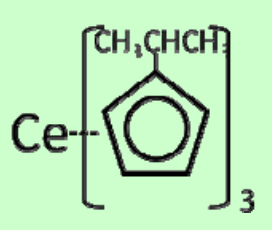


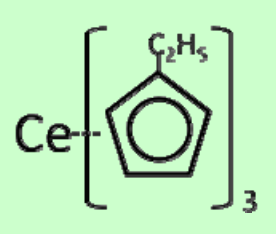
Figure3.10 But for the La(^{i}PrFAMD)$_3$ source. Data for T_S = 125 and 250℃

3.1.2 CeOx

CeOx insulators were prepared by CVD using Ce(mp)$_4$ and ALD using Ce(EtCp)$_3$ and Ce(^{i}PrCp)$_3$ as the metal source and H_2O as the oxidant.







$Ce(Mp)_4$ $Ce(EtCp)_3$ $Ce(^{i}PrCp)_3$

Figure3.11 Source material using CVD or ALD

3.1.2.1 $Ce(Mp)_4$

$Ce(Mp)_4$ can run CVD without a oxidant by autolysis with heat. CVD is easy because only $Ce(Mp)_4$ feed without Ar purge and oxidant feed. The growth property of CVD prepared by $Ce(Mp)_4$ is shown as follows.

Figure 3.12 shows Arrhenius plot of growth rate using $Ce(Mp)_4$. Pressures of growth chamber are 1 and 10 Pa. In this figure, only the data in the experiment that was able to confirm uniform growth on a 2 inch Si wafer is shown. Active energy of 1.53 eV is derived. Growth rate increase with high pressure but the dependence property is not linear dependency. Figure 3.12 shows thickness uniformity. Good thickness uniformity was obtained even with the CVD. Then standard deviation of thickness is 3.9 percent.

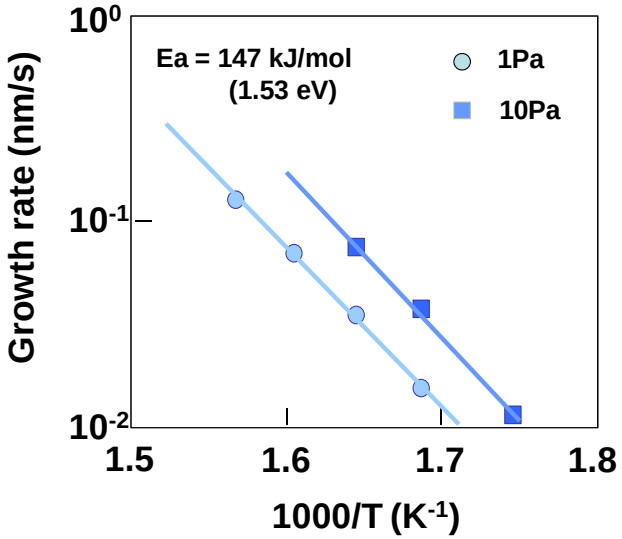


Figure3.12 Arrhenius plot of growth rate using $Ce(Mp)_4$. The circle and square plots are for total pressures of 1 and 10 Pa, respectively.

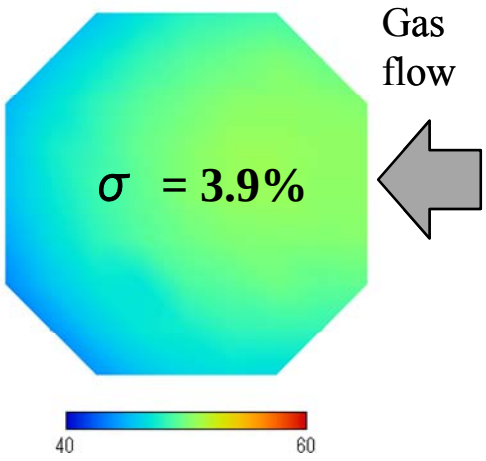


Figure3.12 Thickness uniformity

3.1.2.2 $Ce(EtCp)_3$ and $Ce(^{i}PrCp)_3$.

Growth characteristics is similar to resembles $Ce(EtCp)_3$ with $Ce(^{i}PrCp)_3$ but $Ce(iPrCp)_3$ is easy to use by high vapor pressure. Figure 3.13 shows dependence of growth rate on growth temperature with La_2O_3 data. $Ce(EtCp)_3$ and $Ce(iPrCp)_3$ growth is CVD-mode from figure 3.13. There is a problem in thickness uniformity. So thickness uniformity is bad. The standard deviation of thickness

in 2 inch wafer is 3.9 percent.

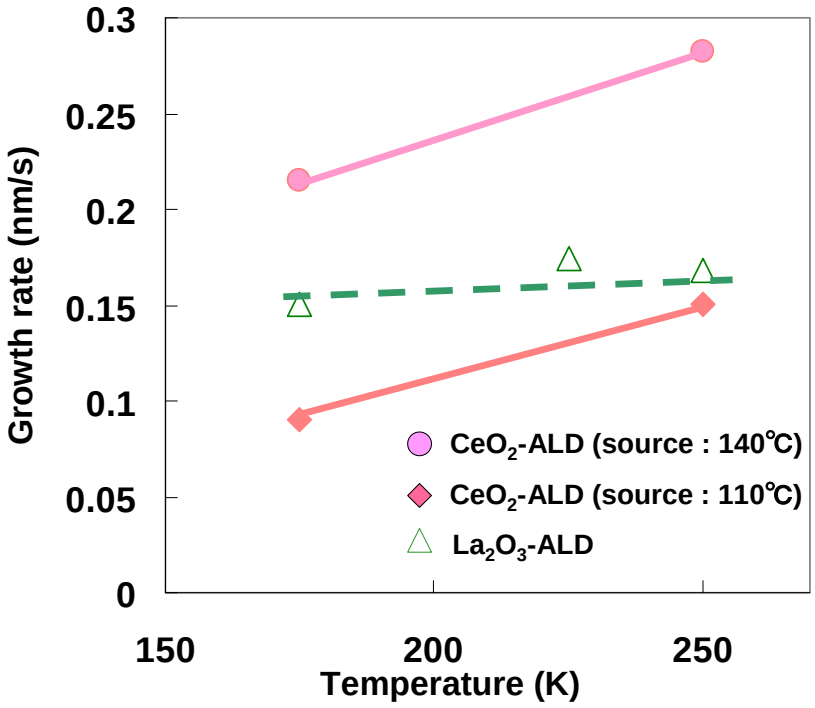


Figure3.13 Dependence of growth rate on growth temperature. Comparison with ALD using La(^{i}PrCp)$_3$.

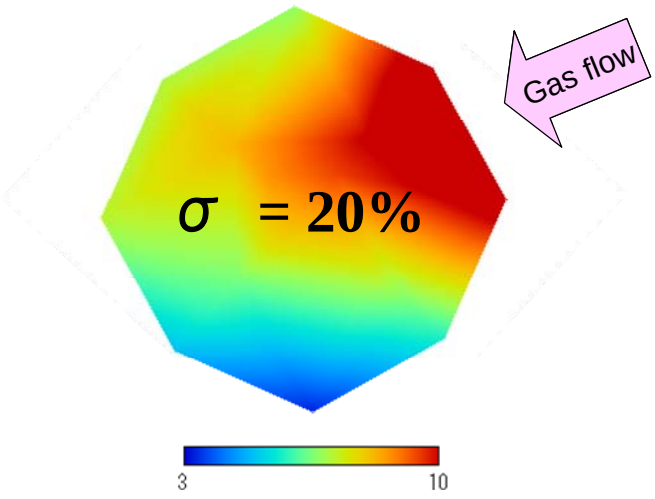
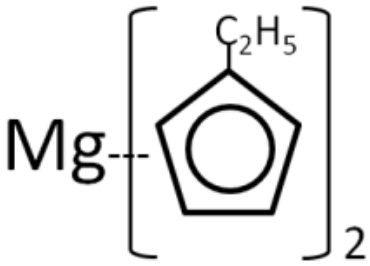


Figure3.14 Thickness uniformity

3.1.3 MgO

MgO insulator is run ALD using $Mg(EtCp)_2$ and H_2O as the metal source and the oxidant. This source is known that self-limiting growth is realized [14]. In fact, self-limiting growth is realized (figure 3.16). Unlike ALD of rare earth, ALD using $Mg(EtCp)_2$ can obtain uniformity growth with short Ar purge time (Figure 3.17).



$Mg(EtCp)_2$

Figure3.15 Mg source

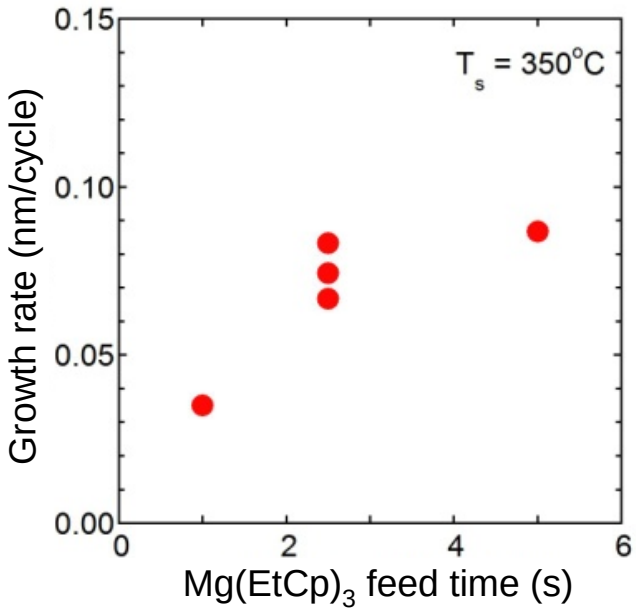


Figure3.16 Dependence of growth rate on Mg source feed time at T_S = 350 ℃

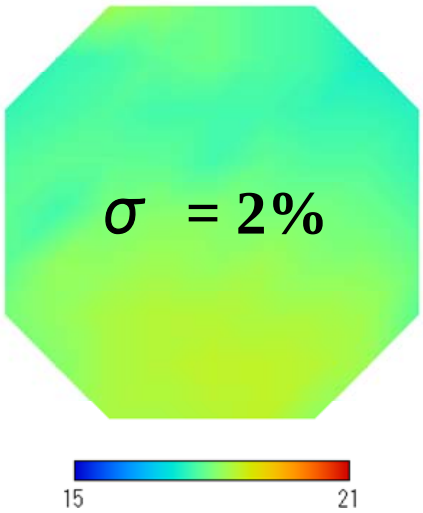
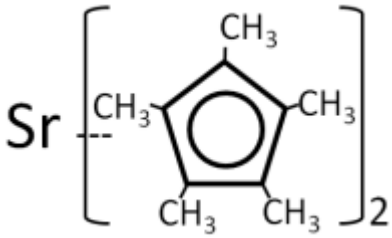


Figure3.17 Thickness uniformity

3.1.4 SrO

SrO insulator prepared by ALD using $Sr(Me_5Cp)_2$ and H_2O as the metal source and the oxidant. Condition to realize self-limiting is not found by the $Sr(Me_5Cp)_2$. In addition, thickness uniformity is very bad. So thickness uniformity is bad. The standard deviation of thickness in 2 inch wafer is 22 percent.



$Sr(Me_5Cp)_2$

Figure3.18 Sr source

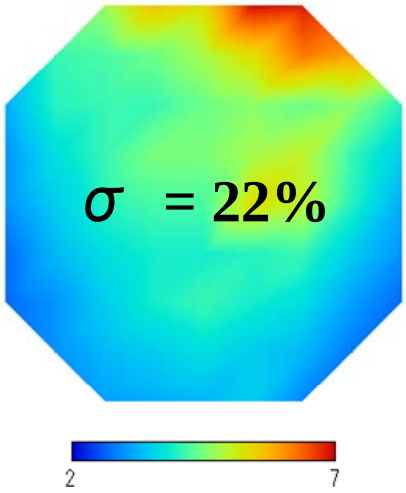


Figure3.19 Thickness uniformity

3.2 Physical Analysis

3.2.1 Reactive Index of ALD Films

The reactive index of insulator is closely related to density of insulator. So reactive index can be paraphrased as density of insulator. Reactive index of ALD insulator is measured to evaluate density of insulator prepared by ALD. The results of $La(^{i}PrCp)_3$ and $La(^{i}PrFAMD)_3$ are shown in figure 3.20. Figure 3.20 shows reactive index of insulator deposited by various conditions. Ideal reactive index of La_2O_3 insulators is about 1.7. Experimental result vary widely but each reactive indexes of La_2O_3 deposited by ALD are about 1.7.

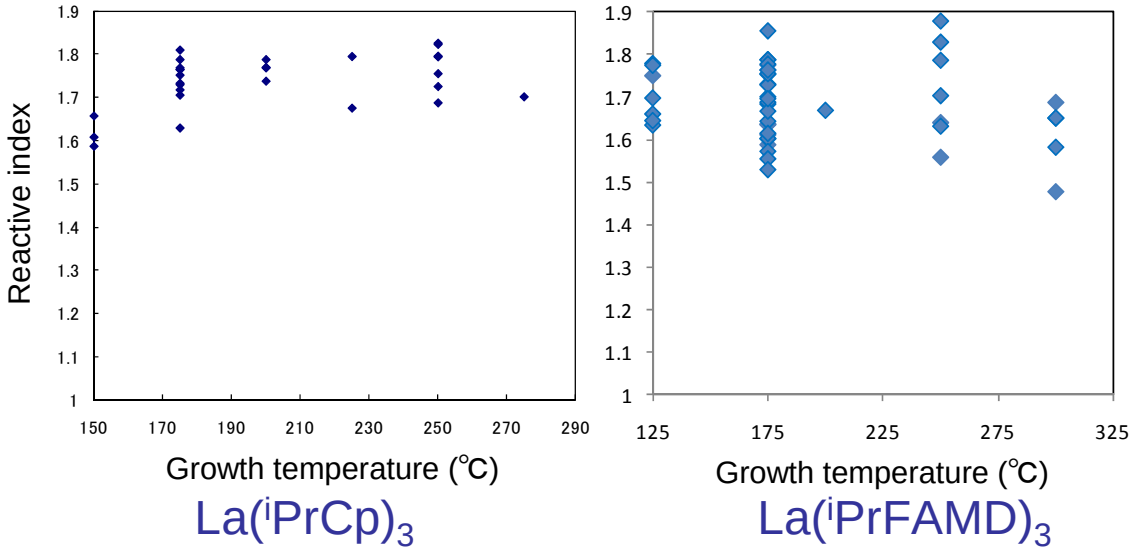


Figure3.20 Reactive index of La_2O_3 films

3.2.2 AFM

Surface roughness and condition of insulators is found from AFM. In this section, Surface roughness and condition of ALD insulators are evaluated. RMS is indicative value of surface roughness. RMS value about Si wafer is said 0.1 to 0.3 nm. RMS of Si wafer is used by experiment is about 0.2 nm. Figure 3.21 shows AFM of La_2O_3 film prepared by ALD using $La(^iPrCp)_3$. RMS is improved for annealing After 5 cycle ALD. Figure 3.22 shows AFM of La_2O_3 film prepared by ALD using $La(^iPrFAMD)_3$. RMS is 0.35 nm. So RMS is not good. AFM of CeOx film prepared by CVD using $Ce(Mp)_4$ is shown in figure 3.23. Because of polycrystal film, RMS increased with increasing thickness of film. Figure3.24 shows AFM of CeOx film prepared by ALD using Ce cyclo-pentadienyl. RMS of CeOx on Si is bad. But RMS is improved by growing CeOx on SiO_2. AFM of MgO film prepared byALD using $Mg(EtCp)_2$ is shown figure 3.25. RMS is not good. Figure 3.26 shows AFM of

SrO film prepared by $Sr(Me_5Cp)_2$ Because growth is granularity, RMS and reactive index is bad.

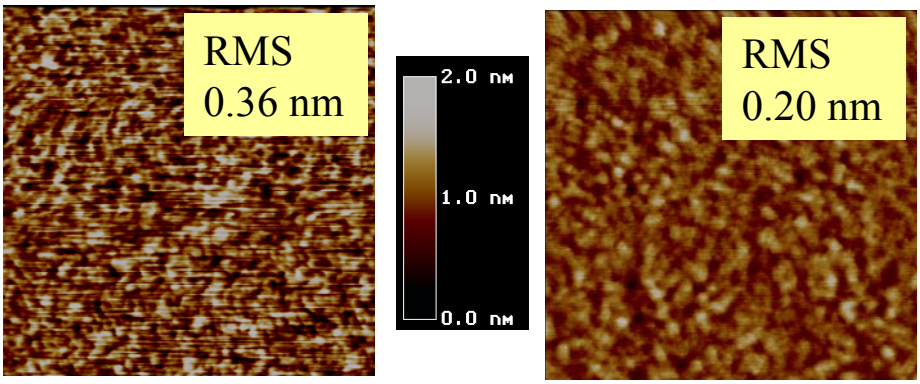


Figure3.21 AFM of La_2O_3 film prepared by ALD using $La(^iPrCp)_3$. The size is 500nm×500nm

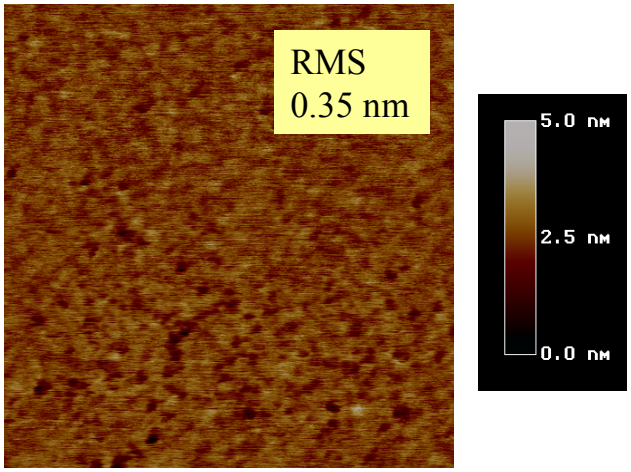


Figure3.22 AFM of La_2O_3 film prepared by $La(^iPrFAMD)_3$. The size is 500nm×500nm
Film physical thickness is 6 nm

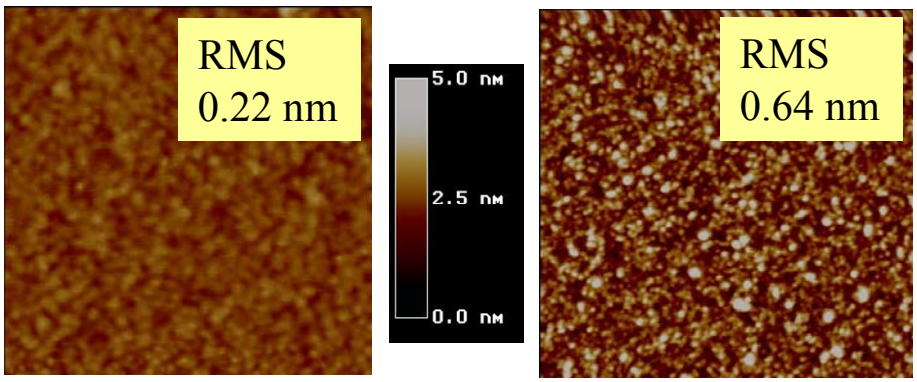


Figure3.23 AFM of CeOx film prepared $Ce(Mp)_4$. The size is 500nm×500nm

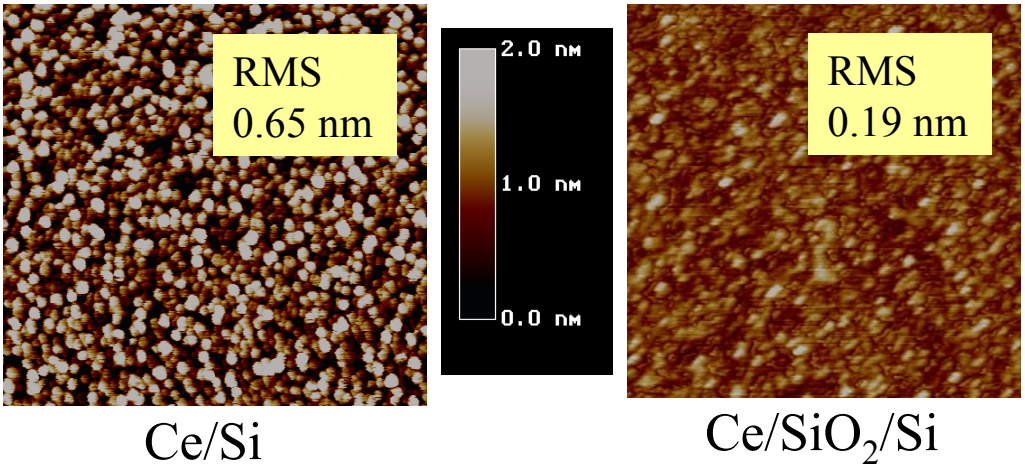


Figure3.24 AFM of CeOx film prepared by Ce cyclo-pentadienyl. The size is 500nm×500nm

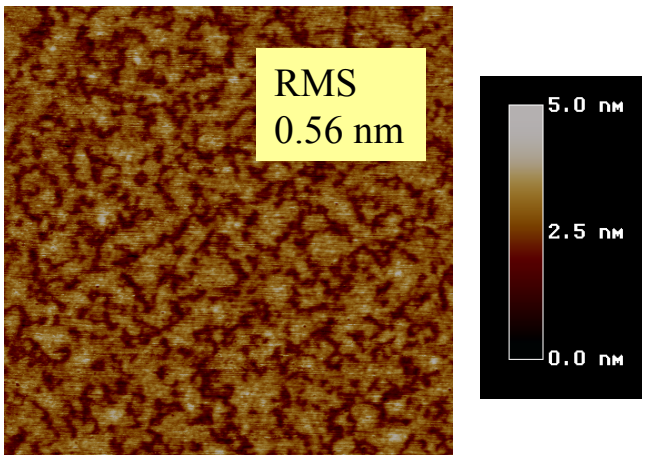


Figure3.25 AFM of MgO film prepared byALD using $Mg(EtCp)_2$. The size is 2 μ m×2 μ m.

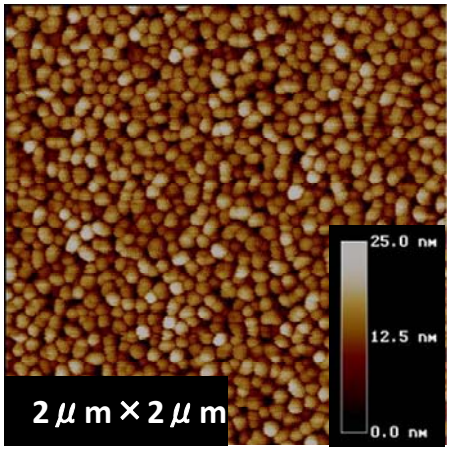


Figure3.26 AFM of SrO film prepared by $Sr(Me_5Cp)_2$. The size is 2 μ m×2 μ m. Film thickness is 19 nm.

Chapter 4

ELECTRICAL CHARACTERISTICS of n-MOSCAPACITOR

4.1 Introduction

In this chapter, we report C-V and J-V characteristics of MOS capacitor deposited by CVD or ALD. The sample is used ALD or CVD is exposed to atmosphere between ALD and electrode formation. Electrode formation is tungsten (W). Each sample, post-metallization anneal (PMA) was carried out in a 3% H_2 forming gas at 500°C for 30 min.

4.2 C-V (Capacitance-Voltage) Characteristics

4.2.1 La_2O_3 Single Layer

Since growth temperature to realize a self-limiting about $La(^iPCp)_3$ is low (175 ℃ less or equal) ,we were worried about quality of La_2O_3 film. And so, figure 4.1 shows C-V characteristics of the MOS capacitor with 13.4 nm La_2O_3 prepared by $La(^iPrCp)_3$ deposited at self-limiting growth temperature (175 ℃). As-deposited sample showed a large hysteresis. This problem is improved by PMA at 500 ℃. Even if La_2O_3 is deposited at temperature as low as 175 ℃, without hysteresis can be obtained by proper annealing.

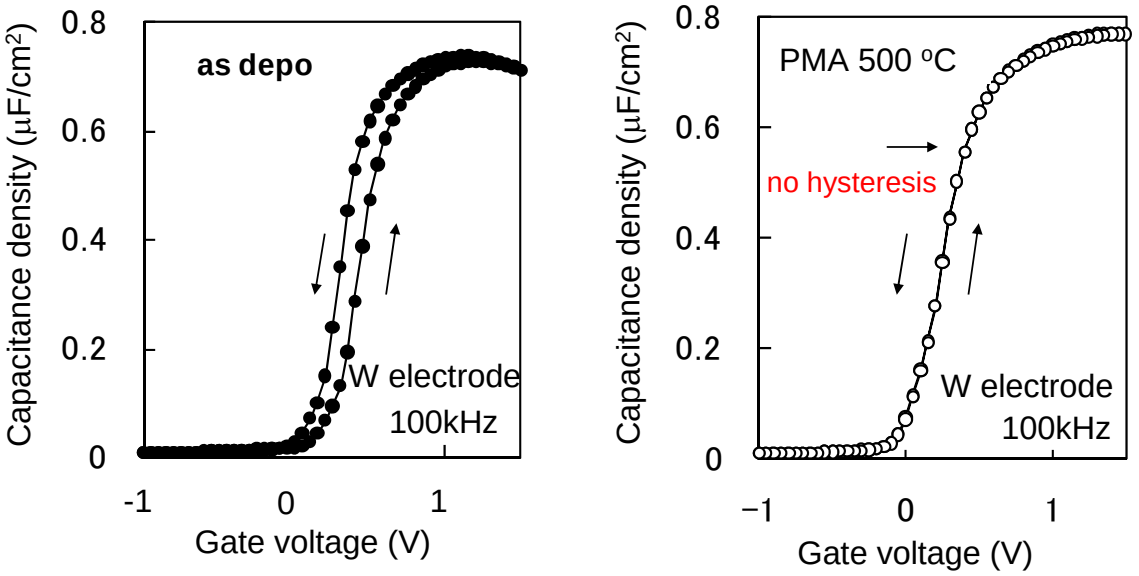
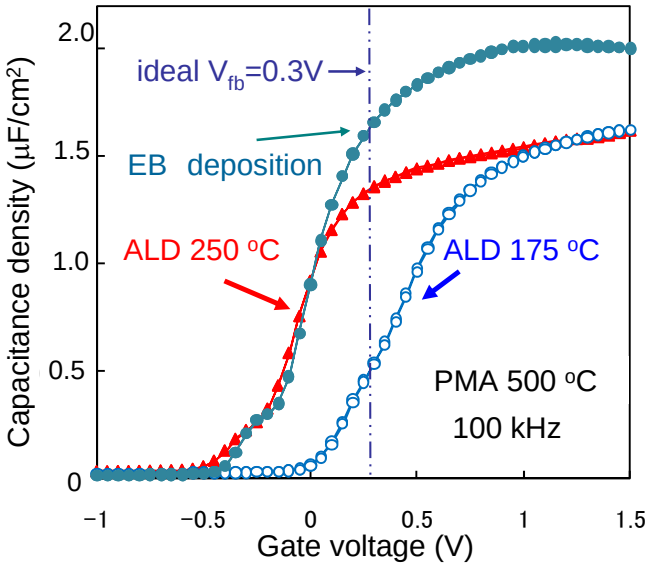


Figure 4.1 C-V characteristics of the MOS capacitor with 13.4 nm La_2O_3 prepared by La(^{i}PrCp)$_3$ deposited at 175 ℃

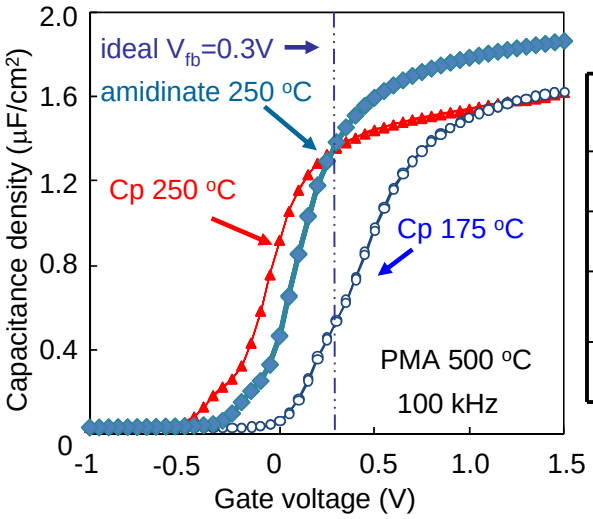
Figure 4.2 shows comparison of the C-V characteristics of La_2O_3 insulators prepared by ALD using La(^{i}PrCp)$_3$ and EB deposition. La $_2O_3$ thickness was 5.2, 5.5 and 5.0 nm for ALD and EB deposition respectively.Each films received PMA at 500 °C. Ideal V_{fb} is +0.3 V. MOS capacitor using ALD film has difference by growth temperature. About 250 ℃ ALD sample, V_{fb} is negatively shift. On the other hand, V_{fb} shift is small in 175 ℃ ALD sample. But the C-V curve is slightly streched out. About EB sample, V_{fb} negative shift is similariy to 250 ℃ ALD sample. k-value for ALD is about 12. So k-value for ALD is lower than EB sample of about 15. The low k-value of ALD sample may be due to carbon and / or OH impurities.

Next, Figure 4.3 Comparison of the C-V characteristics of La_2O_3 insulators prepared by ALD is using La(^{i}PrCp)$_3$ and La(^{i}PrFAMD)$_3$. About amidinate sample, V_{fb} shift is similary to Cp 250's.



	Thickness (nm)	EOT (nm)	k	V_{fb} (V)
EB deposition	5.0	1.31	~15	-0.19
ALD (T_s=175℃)	5.2	1.68	~12	0.26
ALD (T_s=250 ℃)	5.5	1.73	~12	-0.26

Figure 4.2 Comparison of the C-V characteristics of La_2O_3 insulators prepared by ALD and EB deposition. La $_2O_3$ thickness was 5.2, 5.5 and 5.0 nm for ALD and EB deposition respectively.Each films received PMA at 500 °C. Ideal V_{fb} is +0.3 V.



	Growth rate (nm/cycle)	Thickness (nm)	EOT (nm)	k	V_{fb} (V)
Cp (T_s=175 ℃)	0.15	5.2	1.68	~12	0.26
Cp (T_s=250 ℃)	0.17	5.5	1.73	~12	-0.26
Amidinate (T_s=175 ℃)	It is not possible measure because of leakage current.				
Amidinate (T_s=250 ℃)	~0.14	—	1.45	—	-0.09

Figure 4.3 Comparison of the C-V characteristics of La_2O_3 insulators prepared by La(^{i}PrCp)$_3$ and La(^{i}PrFAMD)$_3$. All films received PMA at 500℃

4.2.2 CeOx Single Layer

Figure 4.4 Effects of 500 ℃ annealing on the C-V characteristics for CeO_2 MOS capacitors.(a) is CVD using Ce(Mp)$_4$ at 350 ℃ and under 1Pa. (b) is ALD using Ce(EtCp)$_4$ at 250 ℃. Problem of hysteresis is improved by PMA 500 ℃ even MOS capacitor using ALD or

CVD CeOx insulator like MOS capacitor using La_2O_3 film. About CVD sample (a), V_{fb} after PMA was +0.21 V which was close to the ideal value, +0.3 V. By fitting the 100kHz data using CVC program [15], EOT for the 11 nm-thick film was 1.94 nm and the dielectric constant was 22. It was observed that the C-V characteristics for CVD-CeO_2 tend to exhibit frequency dispersion under the accumulation condition. This may be due to a high density of trapping states near the conduction band edge of Si, or the dielectric relaxation effect. On the other hand, about ALD sample shows the C-V characteristics of ALD-CeO_2 MOS capacitors before and after PMA. PMA was also effective to suppressed hysteresis and leakage current. V_{fb} after PMA was equal to that for CVD-CeO_2, +0.21 V.

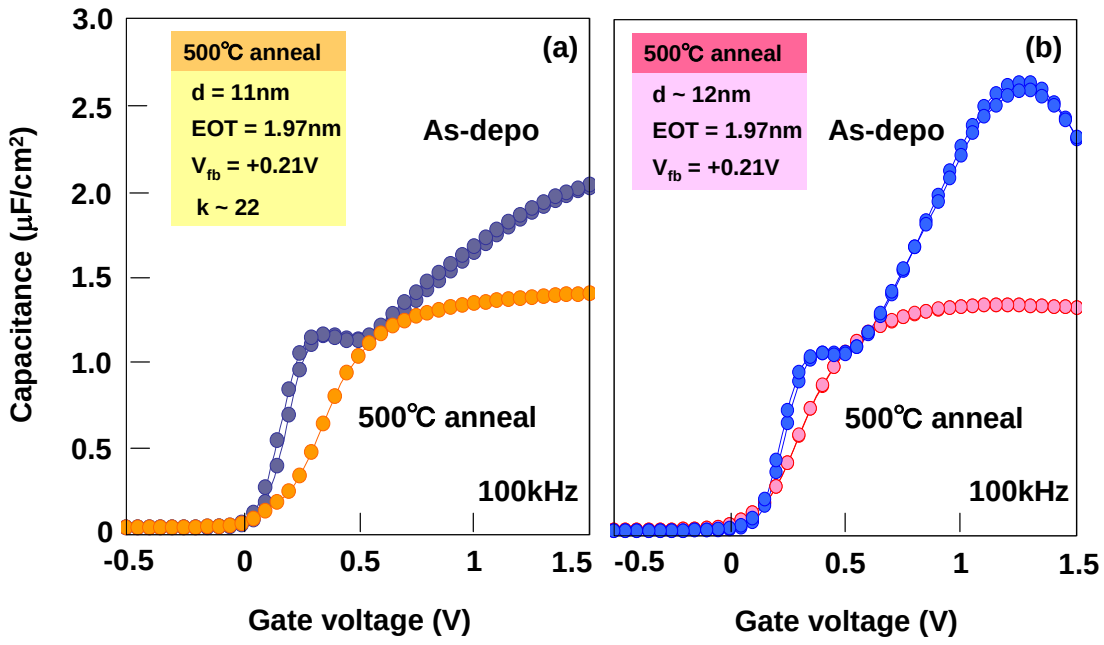


Figure 4.4 Effects of 500 ℃ annealing on the C-V characteristics for CeO_2 MOS capacitors. (a) CVD at 350 ℃ and under 1Pa. (b) ALD at 250 ℃

C-V characteristics of MOS capacitor is shown figure 4.5. This figure shows difference of frequency dispersion by process. In the case of $Ce(EtCp)_4$ ALD, because storage capacitor is almost constant with changing frequency, good property is obtained. On the other hand, the case of $Ce(^{i}PrCp)_3$ and $Ce(Mp)_4$, large frequency dispersion is obtained on storage capacitor. It is thought that cause is dielectric relaxation by measurement changing CeOx film thickness and capacitor area[16]. Optical absorption property of film the same growth condition is measured to find out Cause of frequency dispersion growth process relativity (figure 4.6). The result, 4 eV peak is the lowest about $Ce(EtCp)_4$ is not obtained frequency dispersion. Frequency dispersion appears with sharp 4 eV peak. Intensity and breadth of optical absorption peak reflect crystalline characteristics. Therefore, it is suggested that result of figure 4.5 and 4.6 show prominence of frequency dispersion with encouraging crystallization. Because Suppression of frequency dispersion is necessary the case of gate insulator application, the above result show important of forming a film process development.

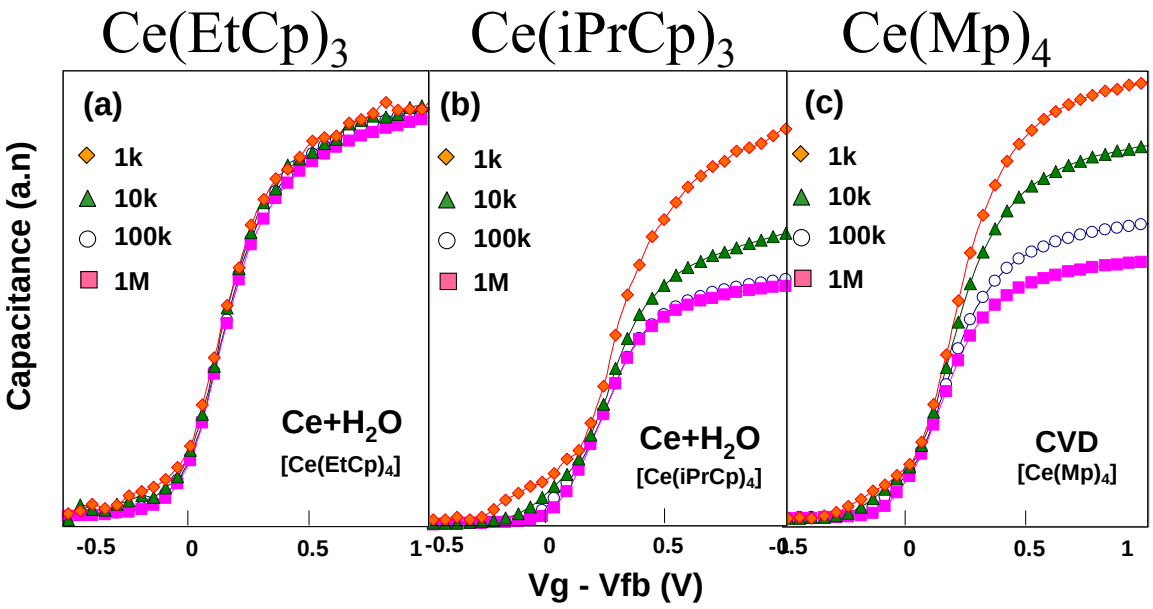


Figure 4.5 Comparison of the C-V characteristics of CeO_2 insulators prepared by $Ce(EtCp)_3$, $Ce(^iPrCp)_3$ and $Ce(Mp)_4$. All films received PMA at 500℃

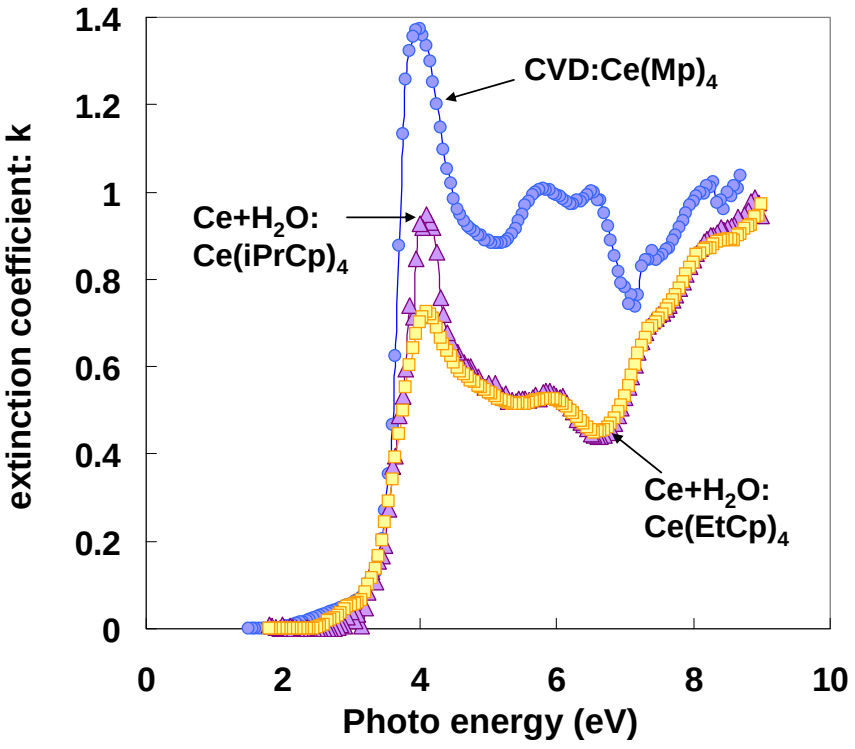


Figure 4.6 Optical absorption of CeOx films.

4.3 J-V (Leakage Current Density-Voltage) Characteristics

4.3.1 La_2O_3 SinglLayer

Figure 4.7 shows a benchmark plot of the leakage characteristics. EB data is also shown to compare the other data in figure 4.7. Electrode of EB sample is formed in situ. The leakage current for annealed Cp La_2O_3 under +1 V bias is ~1/100 lower than the ITRS requirements for the LOP devices and is close to those for the LSTP devices. J of amidinate La_2O_3 is lower than Cp La_2O_3. J of amidinate is comparatively close to J of EB sample. However, ALD La_2O_3 film is necessary to improve about leakage current density. There are two factors to be addressed in this regard. First, since La_2O_3 is hygroscopic, La_2O_3 films must be capped by the electrode material immediately following proper annealing treatments. Thou This was done for the EB evaporation sample in Fig. 4.7, but not for the ALD sample. Second, carbon impurities in the ALD samples presumably cause degradation in *k* and leakage characteristics. These issues are now under investigation in our research group.

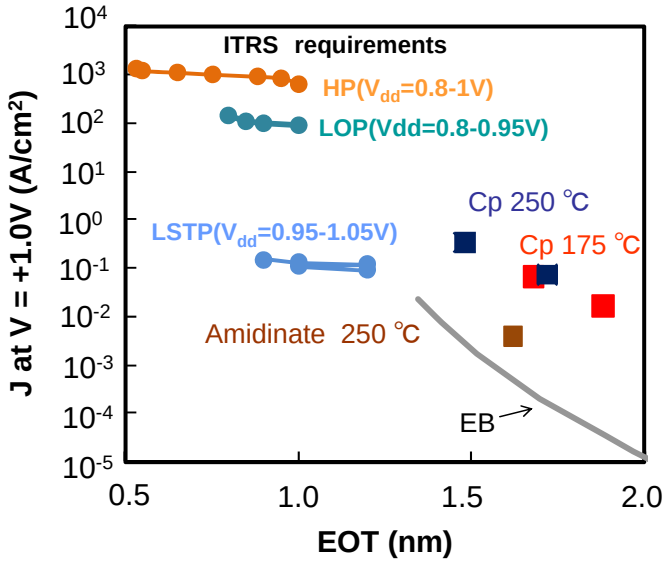


Figure 4.7 Bench mark plot of leakage current under +1 V with respect

the ITRS requirements. Data for the 500 ℃ PMA.

4.2.2 CeOx Single Layer

Figure 4.8 shows bench mark plot of CeOx leakage current under +1 V with respect the ITRS requirements and EB sample. J of CVD-Ce(Mp)$_4$ is lower than j of ALD. It is thought that large leakage current density of cause is the same La_2O_3. ALD or CVD CeOx film is necessary to improve about leakage current density after all.

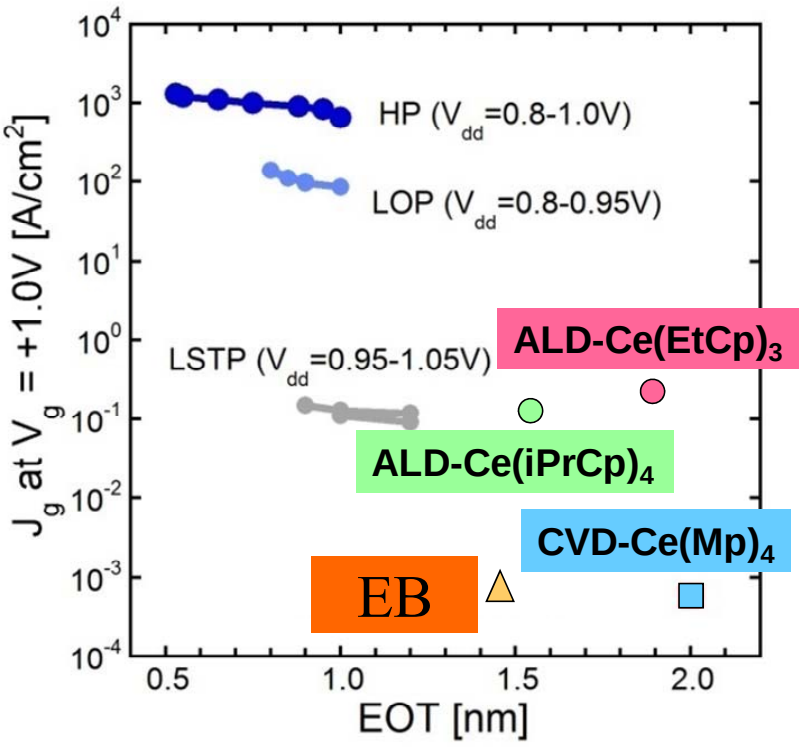


Figure 4.8 Bench mark plot of leakage current under +1 V with respect the ITRS requirements. Data for the 500 ℃ PMA.

Chapter 5
CONCLUSION

5.1 Result of this study

In this thesis, we identified the growth characteristics of insulators (La_2O_3, CeOx, MgO and SrO) prepared by ALD or CVD. The following was found about growth condition. Sources to realize self-limiting growth are $La(^iPCp)_3$ and $Mg(EtCp)_2$. ALD of rare earth is necessary long Ar purge time after H_2O feed. In addition, we evaluate electrical properties of ALD-La_2O_3 and CVD or ALD CeOx MOS capacitor. Though the sample is used ALD or CVD is exposed to atmosphere between ALD and electrode formation, electrical properties is accordingly good. An EOT 1.45 nm in ALD La_2O_3 MOS capacitor. The k value of about 22 is obtained in CVD CeOx MOS capacitor. About each ALD-La_2O_3 and CeOx MOS capacitor, leakage current density is necessary to be improved.

5.2 Future Works

In this work, we evaluate ALD or CVD insulator MOS capacitor. However, the sample is xposed to atmosphere between ALD and electrode formation. Therefore, we evaluate electrical properties of MOS capacitor with electrode formed in situ. This time, La_2O_3 or CeOx single layer MOS capacitor is evaluate. So laminate structure of ALD insulator MOS capacitor is necessary to be evaluated.

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