Master Thesis

Effect of Alkali-earth-elements Incorporation on La_2O_3 Dielectrics for Scaled Silicon MOS Device

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Abstract of Master Thesis

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High dielectric (k) materials as gate dielectrics in metal-oxide-silicon field effect transistor (MOSFET) have been studied to improve very large scaled integrated-circuit (VLSI) technology. To realize continuous equivalent oxide thickness (EOT) scaling for sub-0.5-nm, the high-k dielectrics should be in direct contact with Si-substrate without any SiO_2 based interfacial layer. Among many high-k dielectrics, La_2O_3 is expected to be one of the promising materials, because it is reported that La_2O_3 can achieve an EOT below 1 nm with fairly nice performance. However, like other high-k materials, La_2O_3 suffers from the problem of degradation to the electrical characteristics with EOT scaling. One of the reasons of the degradation can be considered as the generation of defects in the dielectrics. Therefore,

mechanism for preventing the degradation is required. Recently, it has been reported that Mg incorporation into the dielectrics of Hf-based MOSFETs improved its electrical properties. Therefore, La_2O_3 gated n-MOS capacitors and n-FETs with and without incorporation of Mg, MgO, CaO, SrO or BaO, alkali-earth-elements, into La_2O_3 gated n-MOS capacitors and FET has been investigated. Flat-band voltage (V_{fb}) of capacitors with La_2O_3 dielectrics has changed depending on EOT and V_{fb} roll-off and roll-up behavior has been observed. It is reported that fixed charges are induced by the diffusion of W, which is used as a metal gate, and V_{fb} roll-off and roll-up behavior is caused by the fixed charges within the La-silicate layer. The phenomena were quantitatively analyzed using a model, which assume the two kind of fixed charges in the dielectrics. With Mg incorporation, V_{fb} roll-of characteristic has been suppressed indicating the suppression of fixed charge generation and effective mobility(μ_{eff}) of n-FETs incorporated with Mg were improved indicating the degrease of remote Coulomb scattering(RCS). On the other hand, with MgO, CaO, SrO or BaO incorporation, more negative shift of V_{fb} has been observed than the capacitors without the incorporation. It is considered as the enhancement of La-silicate growth and the increase of the fixed charges in La-silicate layer. The effect of enhancement of La-silicate growth was confirmed with XPS analysis in the case of BaO incorporation. One of the reasons of the enhancement of La-silicate formation can be explained by the ionic oxygen conductivity of the oxides. It is reported that the incorporation of alkali-earth-elements into La-silicate enhances the conduction of O atoms.

Therefore, Mg incorporation seems to be preferable to improve the electrical properties of La_2O_3 gated MOSFET. This thesis provides one of the methods to choose high-k dielectrics for scaled silicon MOS devices.

Contents

1 Introduction

1.1 Si-MOSFETs in VLSI Technology

Electrical manufactures have been developed in the last few decades and our life is filled with the manufactures such as PC, digital camera, mobile phone and TV. Without them, our life would be inconvenient and uncomfortable. Very large scaled integrated circuit (VLSI) technology is used in units of the electrical manufactures including central processing unit (CPU), dynamic random access memory (DRAM), imaging sensor and so on. The sustained growth in the VLSI technology plays a part in the development of the manufactures and the growth is fueled by the continuous miniaturization and integration of transistors.

Bipolar transistor technology was developed in the 1940s and was applied to the first integrated circuit memory in mainframe computers in the 1960s [1]. However, the integration level of the bipolar circuit is limited to 10^4 circuits per chip, which is quite low by today's VLSI standard, because of the large power dissipation. The first metal-oxide-semiconductor field effect transistor (MOSFET) on a silicon substrate using SiO_2 as the gate dielectrics was fabricated in 1960 and single-polarity MOSFET circuits were widely used along with bipolar transistors. Though the MOSFET devices had a higher layout density and were relatively simple to fabricate, they also suffered from the large power dissipation. However, the invention of complementary MOS (CMOS) achieved a breakthrough in the level of integration. A CMOS circuit typically consists of n-channel and p-channel MOSFETs, which are constructed on the same substrate as shown in

fig.1.1.1 and they are connected in series between the power-supply terminals, so that standby power dissipation can be suppressed.

For example, the characteristic especially appears in CMOS inverter, which is one of the most basic elements of CMOS circuits. Fig.2(a) shows circuit diagram of a CMOS inverter. The source terminal of the n-MOSFET is connected to the ground, while the source of the p-MOSFET is connected to V_{dd}. The gates and drains of the two MOSFETs are tied together as the input node and the output node, respectively. Thanks to such an arrangement, only one MOSFET conducts and the other MOSFET doesn't conduct in both of the two stable states, which are on and off. As shown in fig.2(b), when the input voltage is V_{dd}, the gate-to-source voltage of the n-MOSFET equals V_{dd}, which turns it on. At the same time, the gate-to-source voltage of the p-MOSFET is 0, so the p-MOSFET is off. The output node is then pulled down to the ground potential by currents through the conducting n-MOSFET. Fig.2(c) shows the condition that the input voltage is 0. In this case, the output node is pulled up to V_{dd} and n- and p-MOSFET are off and on, respectively. Because the output voltage is opposite to the input voltage, this circuit is called an inverter. Notice that there is little static current or static power dissipation since only one of the transistors is on in the stable state (not transient state).By cleverly designing the switching activities of the circuits on a chip to minimize active power dissipation, hundreds of millions of CMOS transistors can be integrate on a single chip. As linear dimensions reached the 0.5-μm level in the early 1990s, the performance advantage of bipolar transistors was outweighed by the significantly greater

circuit density of CMOS device. Bipolar transistors are used only where raw circuit speed makes an important difference. Consequently, bipolar transistors are usually used in small-size bipolar-only chips or in so-called BiCMOS chips where most of the functions are implemented using CMOS transistors and only a relatively small number are implanted using bipolar transistors. [2]

In this way, the main device in the VLSI technology has been transferring from bipolar transistors to MOSFETs. The development of process technologies such as lithography and etching has enabled the industry to scale down transistors in physical dimensions and to pack more transistors in the same chip area. In fact, more than 700 billion MOSFETs are packed in the CPU of Intel® Core™ i7-975, which package size is about 4.2 x 4.5cm^2[3]. Therefore, it is not an exaggeration to say that the development of one MOSFET, which has become one of the most fundamental devices in the VLSI, leads to the advance of the VLSI technology.

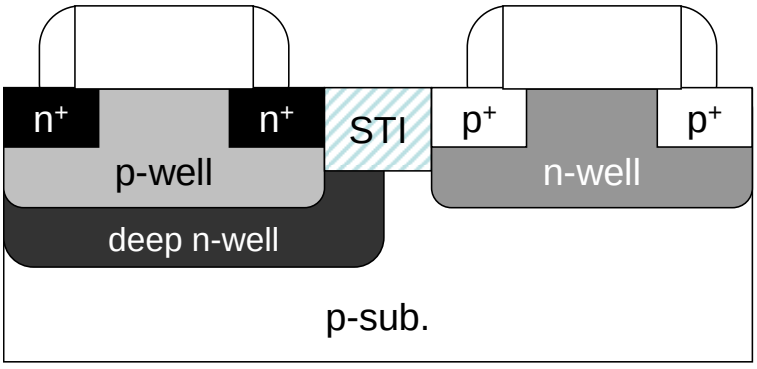

Figure 1.1.1 Schematic cross section of a basic CMOS device. Both n- and p-MOSFET can be constructed on the same substrate.

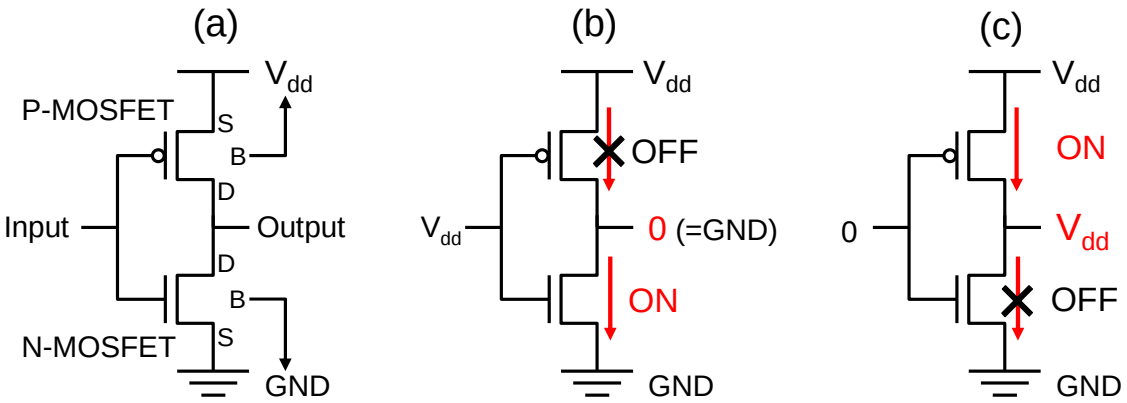

Figure1.1.2 (a) Circuit diagram of a CMOS inverter

(b)Input voltage = V_{dd} (c)Input voltage = 0

1.2 Introduction of high-k dielectrics into MOSFET

For realizing the speed-up of the integrated circuit, it is important for the MOS devices to be miniaturized and to be densely packed. It is called “device scaling”. Of course, the Si-MOSFETs are not exception. SiO_2 have been used as gate dielectrics of the MOSFETs because of its high stability and heat resistance. But, as the device scaling goes on, physical thickness (t_{py}) of SiO_2 dielectrics has become thin and large leakage current by quantum tunneling effect between gate electrode and Si-substrate has increased exponentially. Because of the extreme leakage current (I_{leak}), MOSFETs consume large power. In this reason, it is difficult for MOSFETs with SiO_2 dielectrics to realize the further scaling. Therefore, attention is focused on the materials which have higher dielectric constant (k) than SiO_2 dielectrics. The materials are so-called “high-k materials”. Even if high-k dielectrics which have smaller physical thickness than SiO_2 dielectrics are used in Si-MOSFET, the high-k dielectrics can get more capacitance than

SiO_2 one thanks to the larger k-value as shown in fig.1.2.1. Therefore, the high-k dielectrics are effective for suppressing the Ileak. At the same time as the introduction of high-k materials into dielectrics, the term of equivalent oxide thickness (EOT) has been in use. It is useful index in comparing the high-k materials, which have different k-values and EOT can be written as

$$EOT = \frac{\varepsilon_{SiO2}}{\varepsilon_{highk}} t_{py}, \text{ (Eq.1.1)}$$

where ε_{SiO2} and ε_{highk} are respectively the permittivity of SiO_2 dielectrics and that of high-k dielectrics. EOT is regarded as important index.

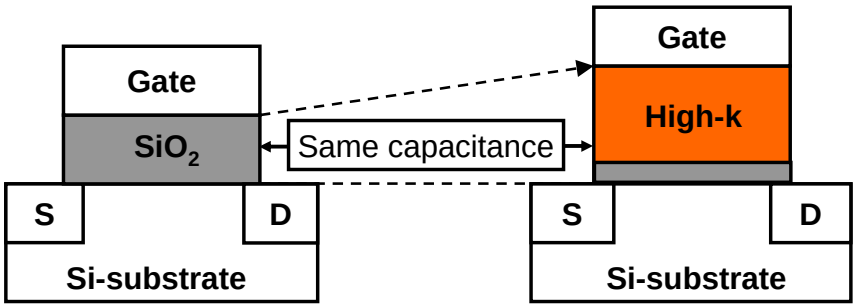

Figure1.2.1 Schematic illustration of the FET, which high-k dielectrics are used in. The high-k dielectrics can get more capacitance than SiO_2 one thanks to the larger k-value

1.3 Advantage of La_2O_3 as Gate Dielectrics

In fact, smaller EOT can be achieved using the high-k dielectrics. However, many of them have poor interfacial property at high-k/ Si-substrate interface. To avoid the degradation of the interfacial characteristic,

0.5~0.7-nm-thick SiO_2 interfacial layer is required between the high-k dielectrics and Si-substrate. However, according to the ITRS roadmap, EOT of sub-0.5nm is required by 2015 as shown in fig.1.3.1. To realize continuous EOT scaling, the high-k dielectrics should be in direct contact with Si-substrate without any SiO_2 based interfacial layer as shown in fig.1.3.2.

La_2O_3 is one of the most promising high-k dielectrics among all high-k materials thanks to its good interfacial property. It is reported that La_2O_3 can achieve an EOT below 1 nm with fairly nice performance by forming La-silicate layer at Si interface [4]. La-silicate is reactively formed after heat treatment as shown in fig. 1.3.3 and it also has high k-value ranging from 8 to 14 depending on the amount of silicon composition. Therefore, La_2O_3 dielectrics are expected to be a one of the materials for next-generation technology of Si-MOSFETs.

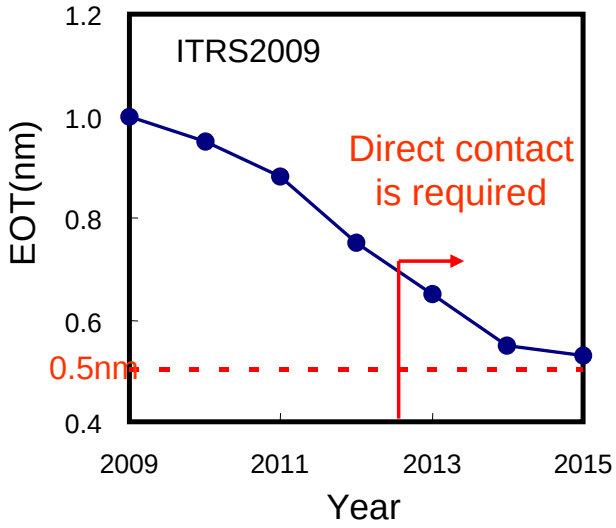

Figure 1.3.1 EOT scaling road map of planer bulk MOSFET in ITRS 2009. EOT of sub-0.5nm is required by 2015.

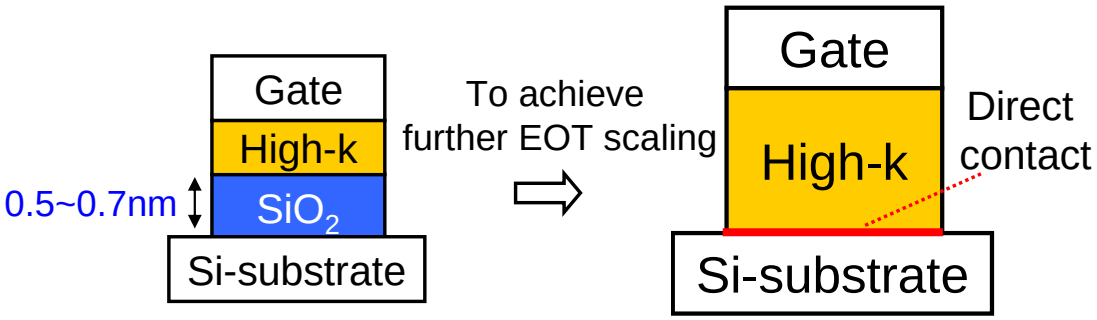

Figure 1.3.2 High-k dielectrics should be directly contacted with Si-substrate to achieve further EOT scaling.

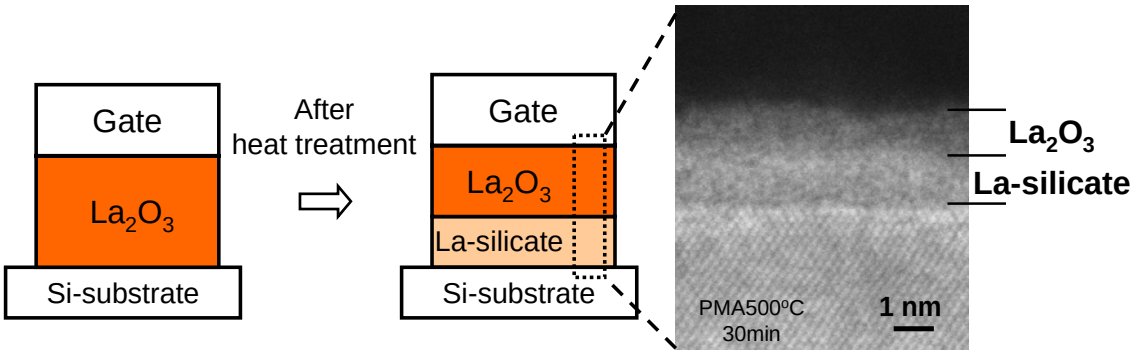

Figure 1.3.3 Schematic illustration of La_2O_3 dielectrics after heat treatment. La-silicate is reactively formed and it is observed from TEM image.

1.4 Problem of High-k Dielectrics for EOT Scaling

Introduction of high-k materials into gate dielectrics of MOSFET can achieve the EOT scaling than only the use of SiO_2 dielectrics. However, degradation in the electrical properties with EOT scaling is one of the major problems and La_2O_3 also suffers from this problem. Fig.1.4.1 shows the effective electron mobility (μ_{eff}) dependence on the effective electrical field (E_{eff}) of La_2O_3 gated n-MOSFET. The mobility is found to degrade as the EOT decreases from 1.74 to 1.04nm. Accordingly, negative shift in the

threshold voltage (V_{th}) as well as in the flat-band voltage (V_{fb}) are also observed below an EOT of about 1.3nm as shown in fig.1.4.2. One of the reasons of the degradation can be considered as the generation of defects in the dielectrics. It is reported that the metal gate induced fixed charge generation and the electrical properties degrade as shown in fig.1.4.3[5]. Therefore, mechanism for preventing the increase of the fixed charge is required.

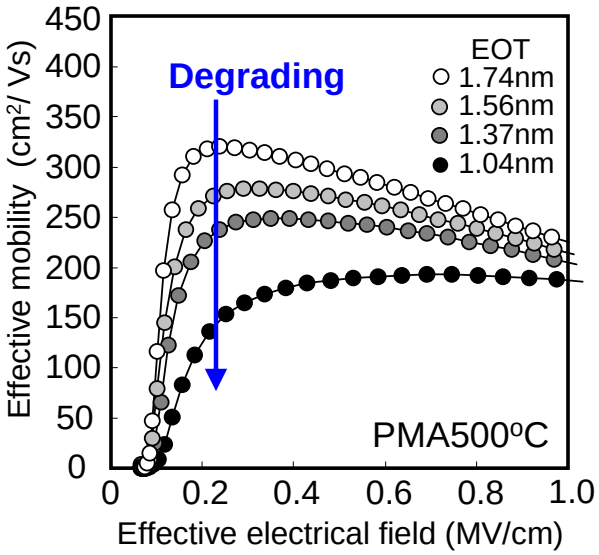

Figure 1.4.1 Effective electron mobility dependence on the effective electrical field of W/La_2O_3/Si n-MOSFET. The mobility degrades as the EOT decreases from 1.74 to 1.04nm.

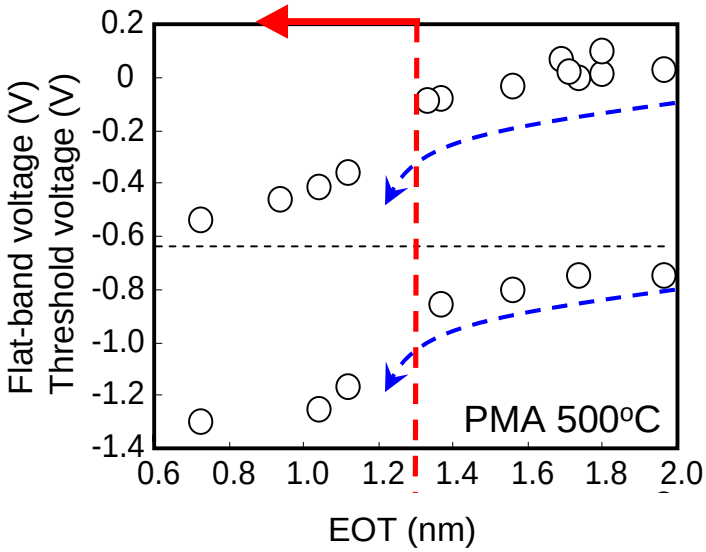

Figure 1.4.2 Threshold voltage (V_{th}) and flat-band voltage (V_{fb}) of W/La_2O_3/Si n-MOS FETs and capacitors. Negative shift of them are also observed below an EOT of about 1.3nm

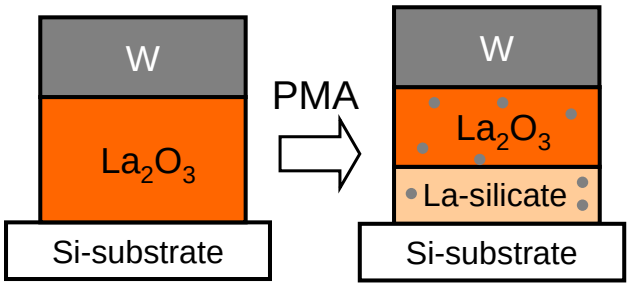

Figure 1.4.3 Schematic illustration of the W as metal gate diffusion. It is reported that diffused W atoms induced fixed charge generation and the electrical properties degrade

1.5 Purpose of This Study

It has been reported that incorporation of Mg into Hf-based dielectrics shows marked improvement in mobility, as shown in fig.1.4.1, and

reliability as well[6]. This is mainly attributed to the decrease of charged defects associated with oxygen vacancies. [7] The purpose of this study is analysis of the fixed charges in the La_2O_3 dielectrics and investigation of the effect of Mg, MgO, CaO, SrO or BaO, alkali-earth-elements, incorporation into La_2O_3 gated MOS device.

Chapter 1 indicates the background and the purpose of this study. Chapter 2 expresses the experimental procedure and the principles performed. In chapter 3, the Vfb dependence on EOT of W/La2O3/n-Si capacitors is analyzed and a model to express the phenomena is supposed. Effect of alkali-earth-elements incorporation is discussed in Chapter 4. Chapter 5 summarizes this study and the outlook is described.

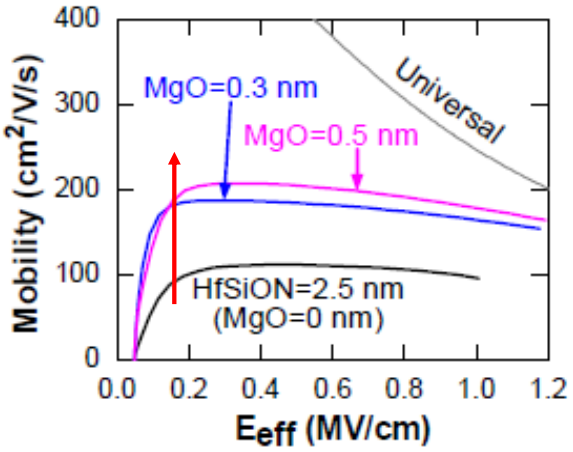

Figure 1.5.1 Effective electron mobility dependence on the effective electrical field of Hf-based n-MOSFET w/ and w/o MgO incorporation. Improvement of the mobility is observed with MgO incorporation.

Refferences

[1] Y.Taur, T.H. Ning : ”Fundamentals of MODERN VLSI DEVICES”, p.1-5 Cambridge University Press(1998)

[2] Y.Taur, T.H. Ning : ”Fundamentals of MODERN VLSI DEVICES”, p.224-227 Cambridge University Press(1998)

[3] http://ark.intel.com/Product.aspx?id=37153&processor=i7-975

[4] K. Kakushima et al., Proc. *ESSDERC*,126-129 (2008).

[5] K. Kakushima et al., *Solid-State Electronics*, **54,** 720−723 (2010)

[6] N. Mise et al., IEDM Tech Dig. (2007) 527.

[7] N. Umezawa et al., APPLIED PHYSICS LETTERS **93**, (2008) 223104.

2 Experiments

2.1. SPM Cleaning and HF Treatment Process

To achieve high reliability of MOSFETs, the cleaning of the wafer is important factor. Sulfuric-peroxide mixture (SPM) cleaning is one of the most effective cleaning methods to eliminate particles on Si wafer. The Si wafer is immersed into the H_2O_2 and H_2SO_4 mixed liquid (H_2O_2:H_2SO_4 = 1:4) and heated. As the liquid is strong oxidizing agent, the Si is oxidized and forms SiO_2, which contains the particles. The SiO_2 layer, which is about 0.8-nm-thick and called chemical oxide, is eliminated with being immersed in HF. In this study, 1% HF solution was used to avoid the over-etching of Si wafer. Thanks to this process, high-k materials can be deposited on the clean Si wafers. Schematic illustration of this process is shown in fig.2.1.

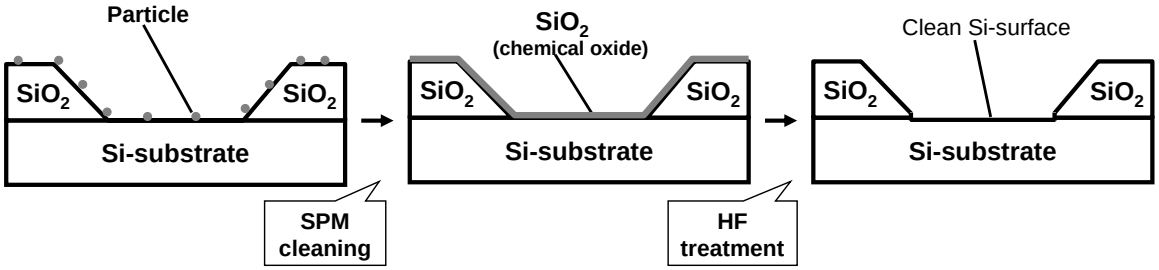

Figure 2.1 Schematic illustration of SPM cleaning and HF treatment. SiO_2 layer containing particles, which is formed with SPM, is eliminated with HF treatment.

2.2 E-beam Deposition and RF Magnetron Sputtering Deposition

Electron beam (E-beam) deposition is one of the effective methods for

depositing the thin dielectrics. In ultra high vacuum, the e-beam is spotted on the source material. The current generates on the surface of the targeted material and Joule heat is caused. Because of the Joule heat, the material is heated and its atoms evaporate. The atoms are in the ultra high vacuum, so they evaporate without striking other molecular to be deposited on the wafer. In this experiment, La_2O_3, Mg, MgO, CaO, SrO and BaO were deposited using this method as shown in fig.2.2.1(a). By moving the shutter as shown in fig.2.2.1(b), the thickness of La_2O_3 or the materials for incorporation was controlled and the various values of EOT were obtained.

Radio frequency (RF) magnetron sputtering is also one of the deposition methods. In this study, W as the gate metal was deposited by RF magnetron sputtering using the Ar gas. In the chamber filled with the Ar gas, the high voltage is applied in high frequency between the target (W) side and the sample side. The Ar molecules are divided into Ar ions and electrons because of the difference of mass. Because the sample side keeps conductive and the target side keeps dielectric, the electrons gathered on the sample side can flow into the circuit but those on the target side are kept gathered. The target side has the minus bias and Ar ions with momentum crash to the target. By the crush, the particles of the target are emitted and deposited on the wafer. Thanks to the magnetron sputtering, which can generate the plasma on the W target side by the magnetic force, the plasma damage can be decreased as shown in fig.2.2.2. [1]

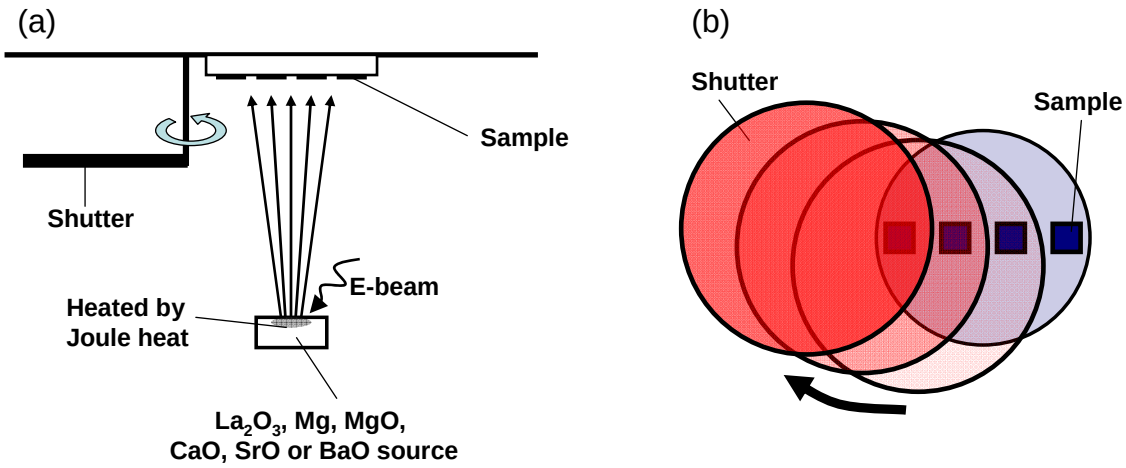

Figure 2.2.1(a) La_2O_3, Mg, MgO, CaO, SrO and BaO were deposited using e-beam deposition. (b)Thickness of them can be controlled with moving a shutter.

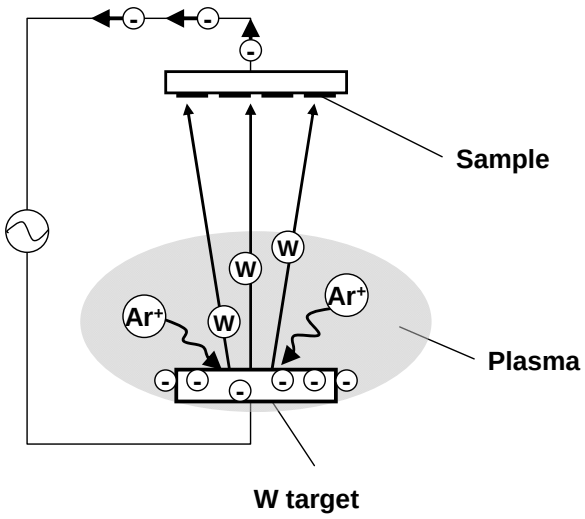

Figure 2.2.2 Schematic illustration of RF magnetron sputtering. By the confliction of the Ar ions, the W molecules were emitted an deposited on the samples.

2.3 Dry and Wet Etching Process

Reactive ion etching (RIE) is one of the dry etching methods. In the same way as the RF sputtering, the gas in the chamber is plasmanized and crashed to the samples. But, in the RIE process, not the physical crash but the chemical reaction between the ions and samples is important. W combined with F^- and forms WF_6, which boiling point is 18^oC. WF_6 is evaporated and eliminated from the sample. Therefore, in this experiment, SF_6 is used as etching gas for W etching. On the other hand, photoresist, which is attached to the sample by the photolithography, reacts with not SF_6 but O_2 to be eliminated. This phenomenon is called ashing. O_2 is used as the etching gas of the resist. Fig.2.3.1 shows the RIE process.

HCl and buffered HF (BHF) were used for the wet etching. BHF is the mixture liquid of HF, NH_4F and H_2O. HCl dissolves La_2O_3 (,where sometimes Ar gas was used by RIE for etching the La_2O_3 layer) and BHF dissolves SiO_2. However, both HCl and BHF don't dissolve the resist. The resist is dissolved by the acetone. By these chemical reactions, the dielectrics are etched. The wet etching process is shown in fig.2.3.2.

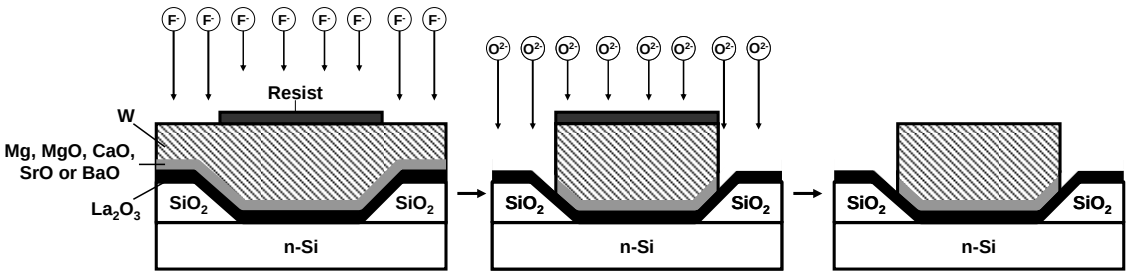

Figure 2.3.1 Schematic illustration of RIE. W and photoresist layer are eliminated using the gases of SF_6 and O_2, respectively.

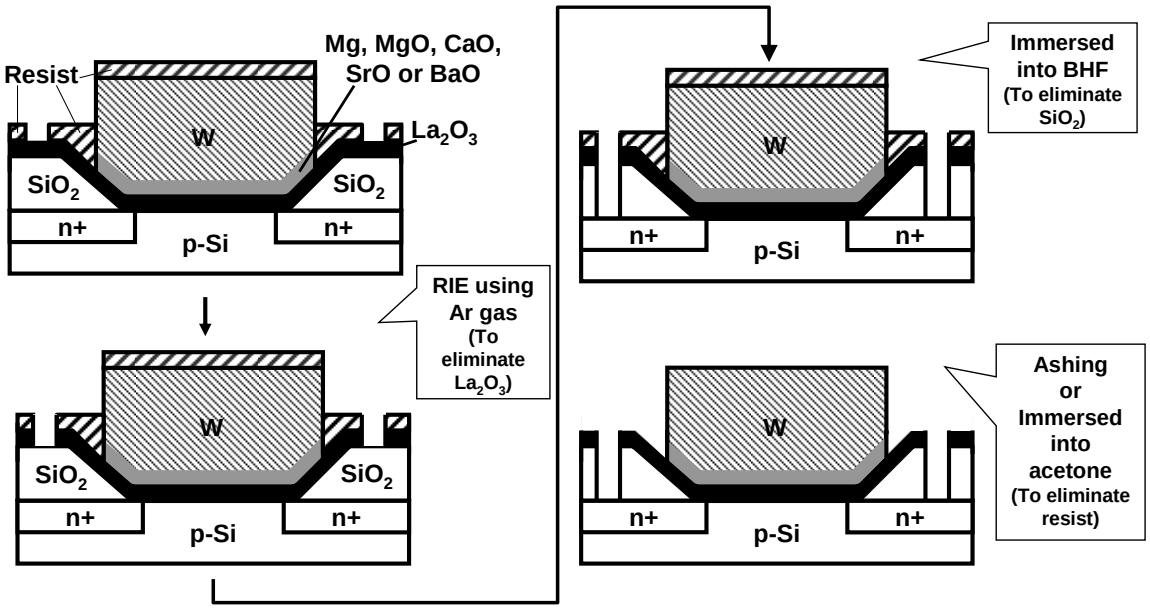

Figure 2.3.2 Schematic illustration of the wet etching process. Mainly, wet etching was used to dissolve SiO_2 with BHF in this experiment.

2.4 Decrease of D_{it} by PMA

Post-metalization annealing (PMA) in a hydrogen-containing ambient is one of the effective methods to improve the interfacial state density (D_{it}) at the Si interface. Dangling bonds of Si at the interface is one of the causes to degrade D_{it} and they can be eliminated by combining with H atoms, which are contains in the ambient gas as shown in fig.2.4. Therefore, in this experiment, PMA was carried out in forming gas (FG) (N_2: H_2 = 97% : 3%) ambient.

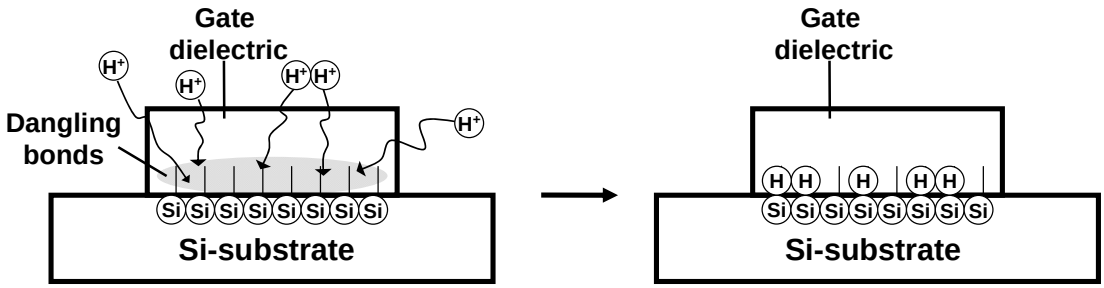

Figure 2.4 Dangling bonds of Si interface, which degrade $\boldsymbol{D_{it}}$, can be eliminated with PMA carried out in FG ambient.

2.5 Al Deposition by Vacuum Evaporation Method

In this study, Al was used for the backside electrode and Al wiring. Al was deposited by vacuum evaporation method. Al source was set on W boat in the chamber. The large current was passed in the W boat and the W boat was heated by the Joule heat. Because the boiling point of Al and the melting point of W are about 2000^{o}C and 3400^{o}C, respectively, in the atmosphere, the Al source evaporates without the W boat melting. In this way, Al was deposited on the samples. The schematic illustration of this deposition is shown in fig.2.5.

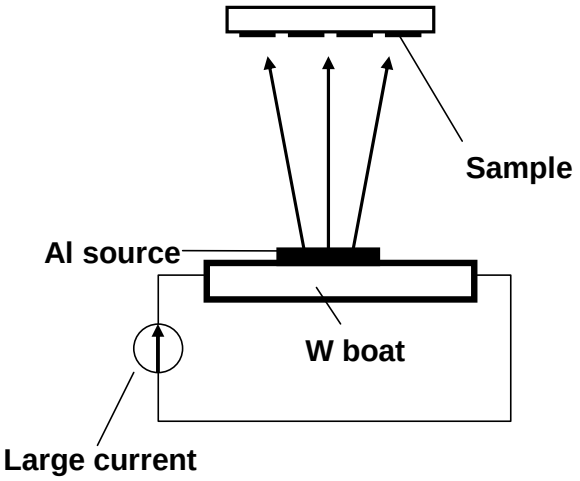

Figure 2.5 Large current is passed in the W boat to heat the Al source by Joule heat. As a result, Al source evaporates and can be deposited on the samples.

2.6 Effective Mobility Calculation by Split C-V Method

The effective mobility (μ_{eff}) is one of the most important electrical characteristics of MOSFETs. In order to determine the μ_{eff}, split C-V method is often used.

In the condition of the low voltage between source and drain (V_{ds}), I_{ds} can be express:

$$I_{ds} = \frac{W\mu_{eff} Q_n V_{ds}}{L}, \text{ (Eq.2.1)}$$

where W is the channel width, L is the channel length, Q_n is the mobile channel charge density and μ_{eff} is the effective mobility.

Eq.2.1 can be written as

$$\mu_{eff} = \frac{g_d L}{W Q_n}, \quad \text{(Eq.2.2)}$$

by using the drain conductance (g_d) defined as

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{Vg=Vg'(=const.)} . \text{ (Eq.2.3)}$$

Q_n is also expressed by measuring the gate-to-channel capacitance (C_{gc}) as

$$Q_n = \int_{\infty}^{V_g'} C_{gc} dV_g . \text{ (Eq.2.4)}$$

In fact, Q_n in the low V_g region ($V_g < V_{fb}$) is very low and negligible. So, Eq.(2.4) can be written as

$$Q_n = \int_{V_{fb}}^{V_g'} C_{gc} dV_g . \text{(Eq.2.5)}$$

The circuit for measuring C_{gc} is shown in fig.2.6.1. It is called split C-V method. In this study, C_{gc} was measured at 100kHz. Using eq.(2.3) and eq.(2.5), μ_{eff} is calculated from the slope of the I_{ds}-V_{ds} characteristic and the are of the C_{gc}-V_g characteristic as shown in fig.2.6.2(a) and (b). [2]

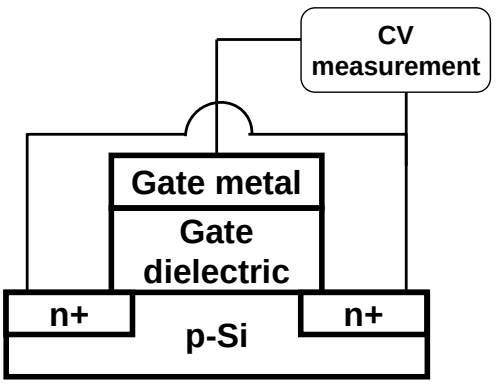

Figure 2.6.1 Schematic illustration of C_{gc} measurement using split C-V method.

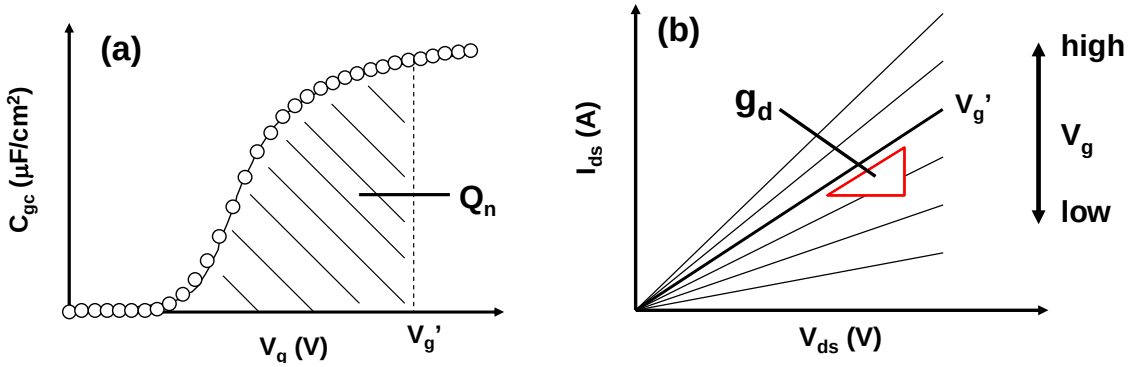

Figure 2.6.2(a) Q_n is obtained with integrating C_{gc}-V_g characteristics. (b)g_d can be estimated from the slope of I_{ds}-V_{ds} characteristics.

2.7 Subthreshold Slope

Generally, I_{ds}-V_g characteristic of MOSFETs is described as fig.2.7 and subthreshold slope (S) is defined as

$$S = \left(\frac{d(\log I_{ds})}{dV_g} \right)^{-1} \text{, (Eq.2.6)}$$

where V_g is the gate voltage and satisfies the relation of $V_g < V_{th}$. So, S is one of the important characteristics of MOSFETs indicating how MOSFETs switch on or off. [8]

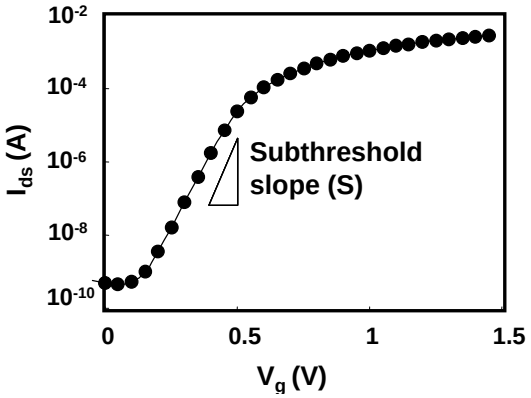

Figure 2.7 General I_{ds}-V_g characteristic of MOSFETs. S is obtained from the slope of the characteristics.

2.8 Charge Pumping Method

D_{it} is the value of describing the interfacial state between Si-substrate and the gate dielectric. Charge pumping method is one of the most effective methods for measuring D_{it} of the MOSFETs. Considering the n-MOSFET, under the inversion condition, the electron are induced at the interface and trapped by the interfacial traps. If the condition is immediately changed to the accumulation by the high frequency pulse voltage, the holes are induced and recombine with the trapped electrons. Because of the recombination, the surface recombination leakage current is generated and this is defined as charge pumping current (I_{cp}). By measuring the I_{cp}, D_{it} can be estimated. This is the charge pumping method. Fig.2.8 shows the schematic illustration of the principle of the charge pumping method. Using I_{cp}, D_{it} can be expressed as

$$D_{it} = \frac{I_{cp}}{q \cdot f \cdot A_g}, \quad \text{(Eq.2.7)}$$

where q is electronic charge, f is the frequency of the applied pulse voltage and A_g is the area of the channel.[3]

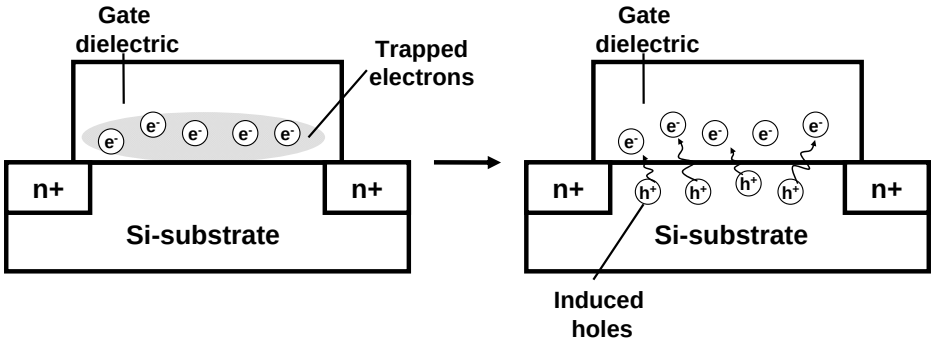

Figure 2.8 Schematic illustration of the principle of charge pumping method.

2.9 Fabrication of MOS Capacitor

Fig.2.9 shows the schematic illustrations of fabrication of La_2O_3-gated MOS capacitors. 300-nm-thick SiO_2 isolated n-Si (100) wafer was used for capacitor. After SPM cleaning and HF treatment, La_2O_3 layer were deposited by e-beam deposition at a deposition rate of 0.1 ~ 0.2 nm/min at a pressure of 10^{-7}~10^{-6} Pa. Either Mg, MgO, CaO, SrO or BaO layer was successively evaporated onto the formed La_2O_3 layer as the same way with the La_2O_3 layer. It is reported that, with exposing La_2O_3 dielectrics to air, La_2O_3 absorbing H_2O changes other formation such as $La(OH)_3$ and the permittivity of the dielectrics and electrical properties of the MOS device degrade. Therefore, 60-nm-thick W as metal gate was deposited without exposing the wafers to air (*in situ* deposited) using RF magnetron sputtering at a rate of 2 nm/min. This *in-situ* deposition can also avoid absorbing some moisture or carbon-related contamination. W metal gate was patterned by RIE using SF_6 chemistry to form gate electrode. PMA using a rapid thermal annealing (RTA) furnace was carried out in FG ambient at a raising rate of 10^{o}C/s. A 50-nm-thick Al layer on the backside of the substrate was finally deposited as a bottom contact by thermal evaporation.

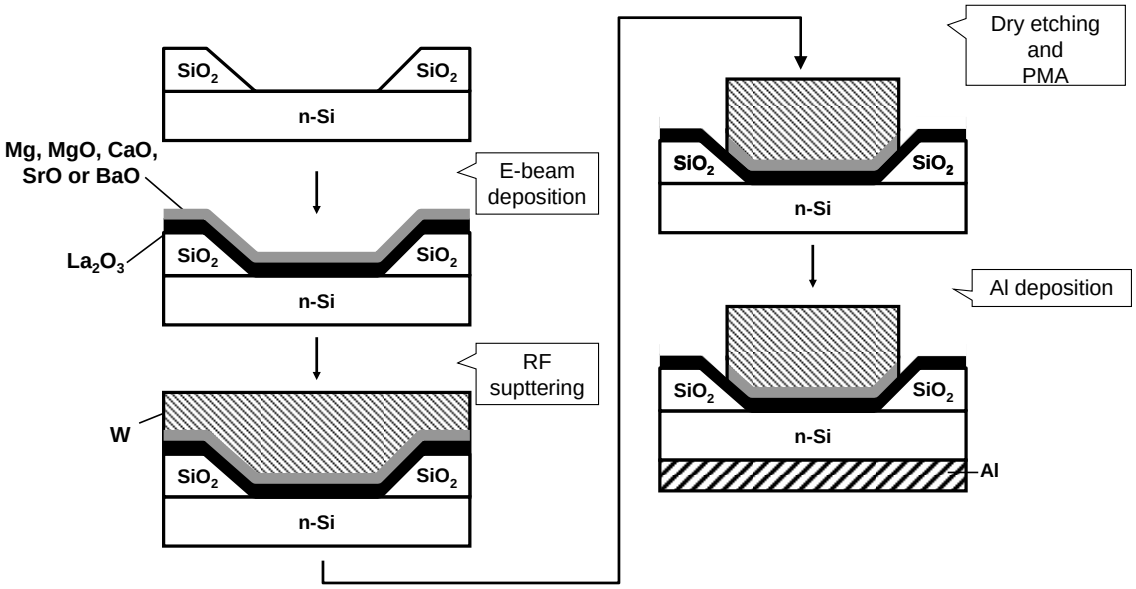

Figure 2.9 Fabrication flow of W/La_2O_3/n-Si gate stack structure MOS capacitor w/ and w/o alkali-earth-elements incorporation.

2.10Fabrication of MOSFET

For n-MOSFET, local-oxidation-of–silicon (LOCOS) isolated p-Si (100) wafer was used. The wafer has pre-formed n+-doped source/drain. After SPM cleaning and HF treatment, La_2O_3 was deposited and either Mg, MgO, CaO, SrO or BaO layer was successively evaporated onto the formed La_2O_3 layer by e-beam deposition. 60-nm-thick W as metal gate was *in-situ* deposited and patterned. These processes were carried out in the same way as the fabrication process for MOS capacitors. To contact with source and drain, the dielectrics and SiO_2 were etched by RIE or wet etching using Ar gas or BHF, respectively. After PMA using a RTA furnace in FG ambient, 50-nm-thick Al layer for contact hole and 50-nm-thick Al layer on the backside of the substrate were deposited by thermal evaporation. Schematic illustration of fabrication of MOSFET is shown in fig.2.10.

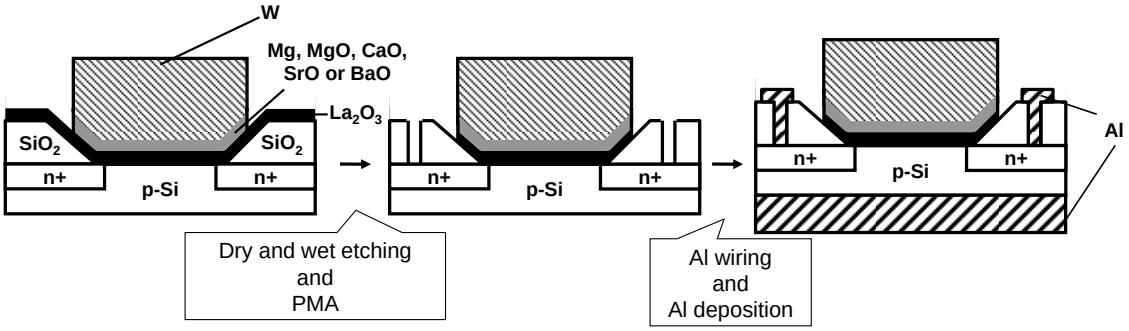

Figure 2.10 Fabrication flow of W/La_2O_3/Si gate stack structure n-MOSFET w/ and w/o alkali-earth-elements incorporation.

2.11 Analysis of Dielectrics and Measurement of Electrical Properties

In order to reveal the movement of incorporated Mg atoms and the condition of dielectrics after PMA, one capacitor of W/Mg/La_2O_3/p-Si gate stack structure after thermal treatment was analyzed by transmission electron microscope (TEM), energy dispersion x-ray (EDX) and hard x-ray photoemission spectroscopy (XPS). The principles of these physical analyses are described in Appendix A.

Electrical characteristics of MOS capacitors and MOSFETs were measured using an Agilent E4980A precision LCR meter and Agilent 4156C semiconductor parameter analyzer.

Both experimental procedures of MOS capacitors and MOSFETs are shown in fig.2.11.

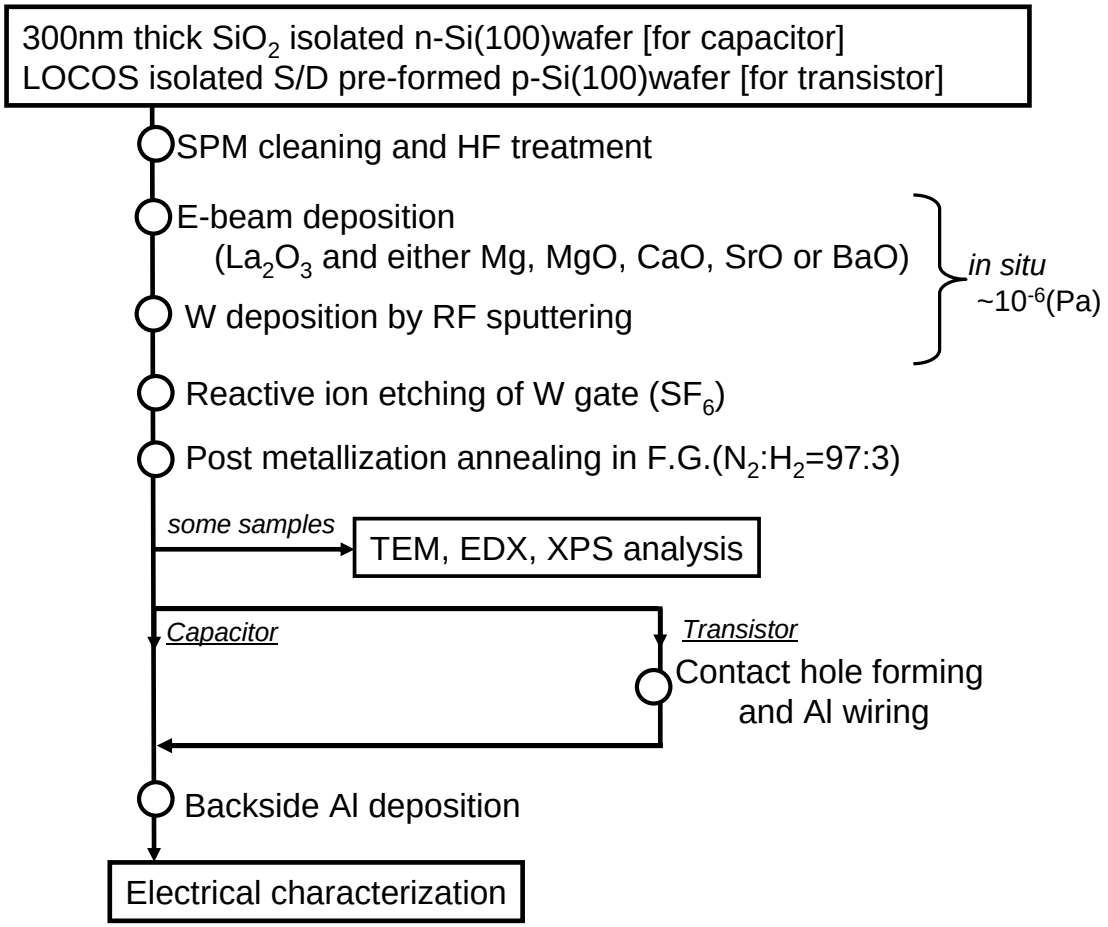

Figure 2.11 Experimental procedures of W/La_2O_3/n-Si gate stack structure n-MOS capacitors and n-FETs.

Refferences

[1] http://www.sanyu-electron.co.jp/genri/sptr_01.html

[2] Y.Taur, T.H. Ning: ”Fundamentals of MODERN VLSI DEVICES”, p.82-84,Cambridge University Press(1998)

[3] D.K.Schroder: “Semiconductor Material and Device characterization Third Edition”, p.489-500, IEEE Press (2005)

3 Modeling of the V_{fb} Dependence on EOT

3.1. V_{fb} Roll-off and Roll-up Behavior

Fig.3.1.1 shows the *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors. The thickness of La_2O_3 layer was changed from 2 to 7 nm, which corresponds to the EOT from 2 to 0.6 nm. PMA using RTA furnace was carried out in FG ambient at 500°C for 30min. The both values of V_{fb} and EOT are estimated using NSCU CVC simulation. It is observed that V_{fb} shifts towards negative direction as the EOT decreases from 2.0 to 0.91 nm and it moves to positive direction below 0.91 nm. These results indicate that the value of V_{fb} depends on EOT. V_{fb} dependence on EOT is summarized in fig.3.1.2. From this figure, V_{fb} roll-off and roll-up are clearly observed.

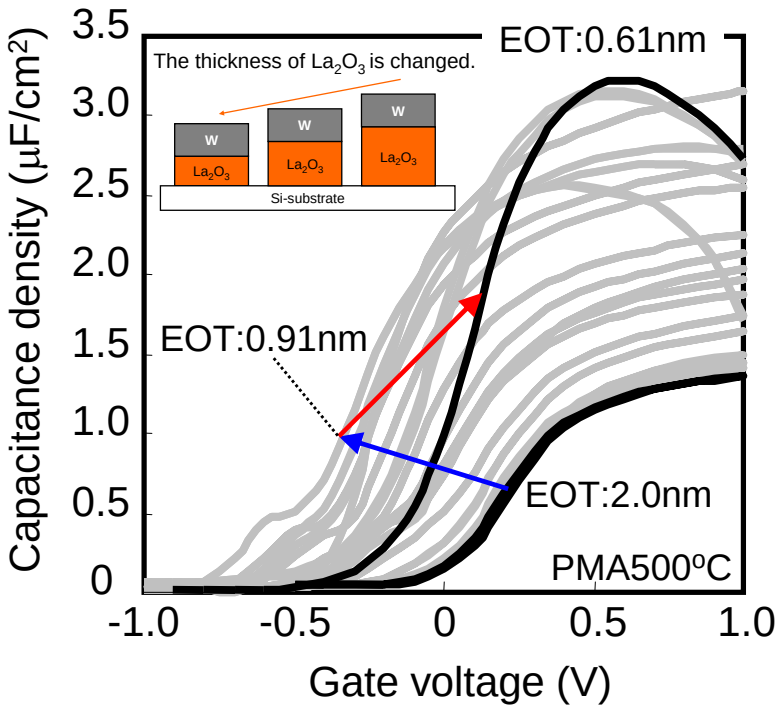

Figure 3.1.1 *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors indicating the dependence of V_{fb} on EOT.

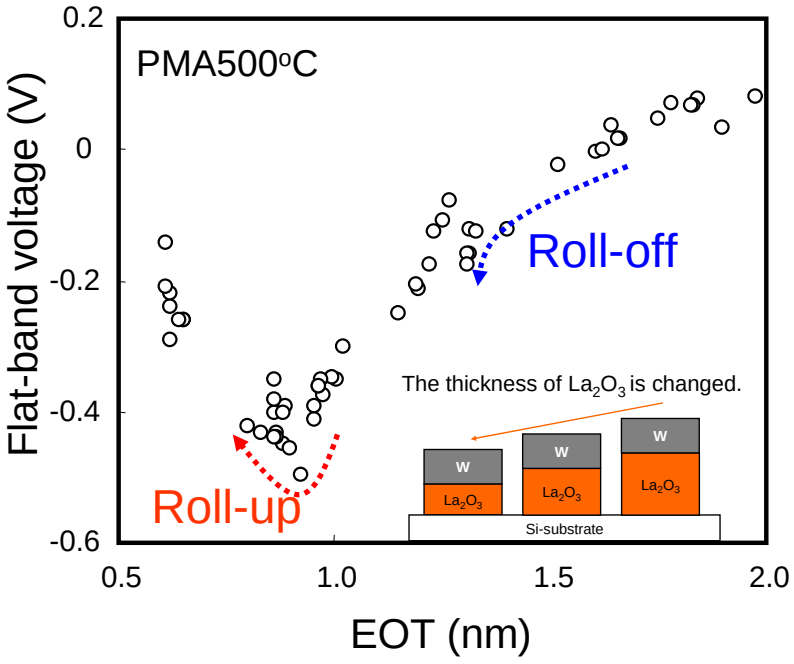

Figure 3.1.2 V_{fb} dependence on EOT of W/La_2O_3/n-Si gate stack structure MOS capacitors. V_{fb} roll-off and roll-up behavior is clearly observed.

It is reported that fixed charges are induced by the diffusion of W atoms and V_{fb} roll-off and roll-up behavior is caused by the fixed charges within the La-silicate layer as shown in fig.3.1.3[1].

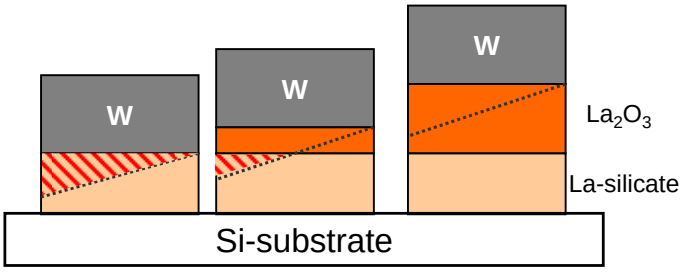

Figure 3.1.3 W atoms diffusion induces fixed charges in La-silicate layer and the fixed charges causes V_{fb} roll-off and roll-up behavior.

3.2 Model for V_{fb} Roll-off and Roll-up

To quantitatively analyze the relation of the fixed charges and V_{fb} roll-off and roll-up behavior, a model was developed. Two kinds of fixed charges are assumed. One exists at the La_2O_3/La-silicate. The other charges exist in the bulk of La_2O_3 layer and these fixed charges increase in proportion to the diffusion of W atoms. Both densities of the fixed charges are defined as $\rho(x)(cm^{-3})$ and $\sigma(x)(cm^{-2})$, respectively. Using these parameters, V_{fb} can be expressed as

$$V_{fb} = -\frac{q}{\varepsilon(x)}\left(\int_{o}^{T_{phy}} x\rho(x)dx + \sigma(x)t_{LaO}\right) + \phi_{ms} \quad \text{, (Eq.3.1)}$$

where q is the electronic charge density. $\varepsilon(x)$ is the permittivity of the dielectrics[2]. T_{phy} and t_{LaO} are the physical thickness of the whole dielectrics and La_2O_3 layer, respectively. ϕ_{ms} is the work function difference of the metal and the Si-substrate. Assuming that the $\rho(x)$ and $\sigma(x)$ are constant and both of their value is defined as $\rho(cm^{-3})$ and $\sigma(cm^{-2})$, (where σ exists if $t_{LaO} > 0$,) respectively, V_{fb} can be expressed by using three kinds of equations. The parameters are summarized in fig.3.2.1.

In the condition that W atoms doesn't diffuse into La-silicate layer as shown in fig.3.2.2, V_{fb} can be expressed as

$$V_{fb} = -q\frac{\sigma t_{LaO}}{\varepsilon_{La2O3}} + \phi_{ms} \quad \text{, (Eq.3.2)}$$

where ε_{La2O3} is the permittivity of La_2O_3.

In the condition that La_2O_3 layer exists and W atoms diffuse into La-silicate layer as shown in fig.3.2.3, V_{fb} can be expressed as

$$V_{fb} = -q\left(\frac{\sigma t_{LaO}}{\varepsilon_{La2O3}} + \frac{\rho t_w t_{LaO}}{\varepsilon_{La2O3}} + \frac{\rho t_w^{\,2}}{2\varepsilon_{LaSi}}\right) + \phi_{ms}$$, (Eq.3.3)

where t_w is diffusion length of the W atoms. ε_{LaSi} is the permittivity of the La-silicate..

In the condition that only La-silicate layer exists as shown in fig.3.2. 4, V_{fb} can be expressed as

$$V_{fb} = -q\frac{\rho t_W^{\,2}}{2\varepsilon_{LaSi}} + \phi_{ms}$$. (Eq.3.4)

It is considered that total amount of fixed charge decreases because diffusion of W atoms into La-silicate layer is limited. Using eq.3.2~3.4, the previous experimental value of V_{fb} dependence on EOT of W/La_2O_3/n-Si gate stack structure MOS capacitors can be well fitted as shown in fig.3.2.5. From the results of fitting, the both value of ρ and σ are estimated 7.6 x 10^{19} cm^{-3} and 3.7 x 10^{12} cm^2, respectively.

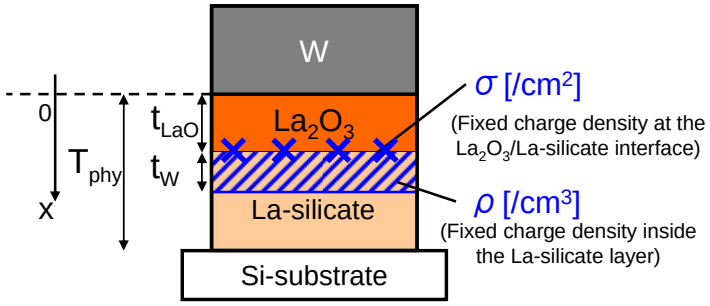

Figure 3.2.1 Two kinds of fixed charges are assumed. One exists at the La_2O_3/La-silicate. The other charges exist in the bulk of La_2O_3 layer and these fixed charges increase in proportion to the diffusion of W atoms.

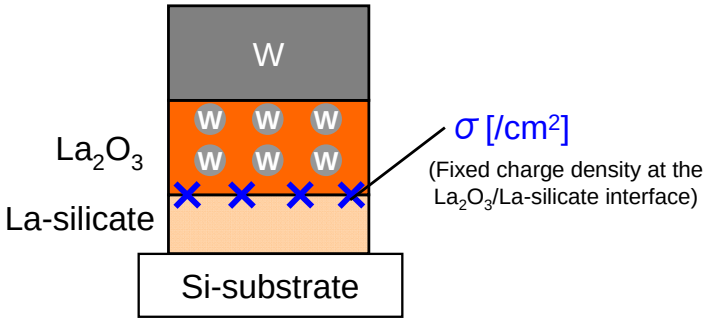

Figure 3.2.2 In the condition that W atoms doesn't diffuse into La-silicate layer, fixed charges exist only at the La_2O_3/La-silicate.

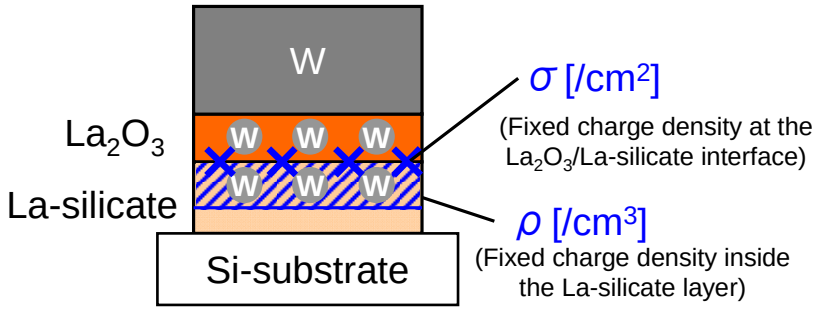

Figure 3.2.3 In the condition that La_2O_3 layer exists and W atoms diffuse into La-silicate layer, both of fixed charges at La2O3/La-silicate interface and inside La-silicate layer exists.

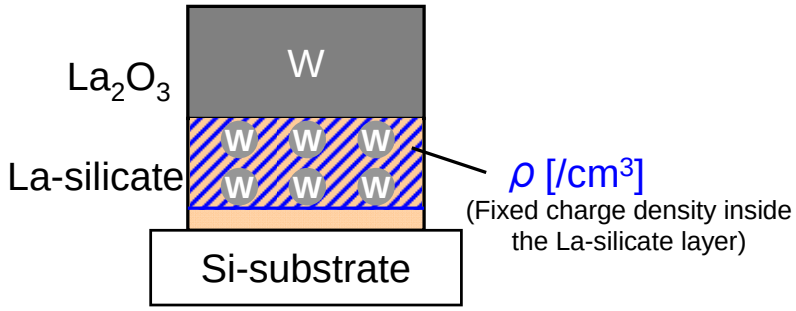

Figure 3.2.4 In the condition that only La-silicate layer exists, fixed charges exists only inside La-silicate layer.

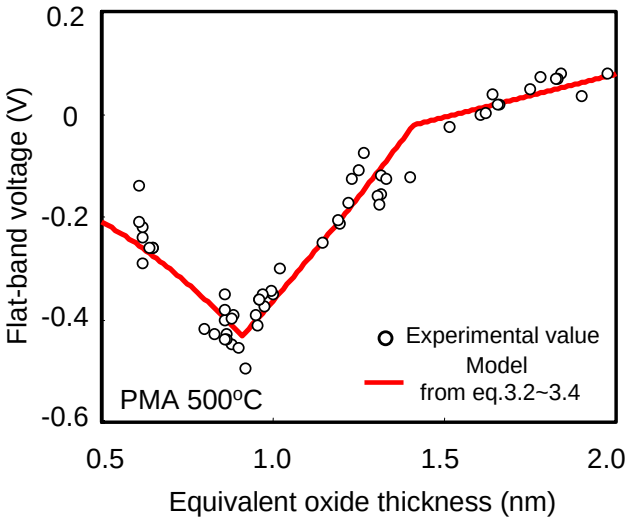

Figure 3.2.5 Using eq.3.2~3.4, experimental value of V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors can be well fitted.

Refferences

[1] K. Kakushima et al., *Solid-State Electronics*, **54,** 720−723 (2010)

[2] Y.Taur, T.H. Ning: ”Fundamentals of MODERN VLSI DEVICES”, p.86-89,Cambridge University Press(1998)

4 Effect of Alkali-earth-elements Incorporation on La_2O_3 Gated MOS Device

4.1 Effect of Mg Incorporation on Electrical Properties

Fig.4.1.1 shows V_{fb} dependence on EOT of W/La_2O_3/n-Si gate stack structure MOS capacitors with and without 1-nm-thick metal Mg incorporation. The thickness of La_2O_3 layer was changed to get the various values of EOT. PMA using RTA furnace was carried out in FG ambient at 500^{o}C for 30min. The both values of V_{fb} and EOT are estimated using NSCU CVC simulation. Suppression of the negative shift of V_{fb} is observed. Using eq.3.2~3.4 and the assumed fixed charges as shown in fig.3.2.5, the fixed charge density of at La_2O_3/La-silicate interface (σ) and inside La-silicate layer (ρ) is estimated as 3.3 x 10^{12} cm-^{2} and 1.3 x 10^{19} cm^{-3}, respectively. Compared to the result of the capacitors without Mg incorporation, generation of fixed charges inside La-silicate layer can be effectively suppressed with Mg incorporation by one fifth.

The μ_{eff} comparison with an *EOT* around 1.1 nm is shown in fig.4.1.2(a). μ_{eff} of the FETs was evaluated with split *C-V* technique. A large improvement in μ_{eff}, especially at low effective field was observed. To analyze the additional scattering factor was performed based on Mattissen's rule as the samples have the same doping concentration. The calculated results demonstrates that the additional scattering (μ_{add}) obeys with $E_{eff}^{0.5\sim0.6}$ dependency, indicating a remote Coulomb scattering, as shown in fig.4.1.2(b)[1]. Therefore, the improvement in μ_{eff} can be attributed to the reduced fixed charges, which is in good agreement with the V_{fb} shift.

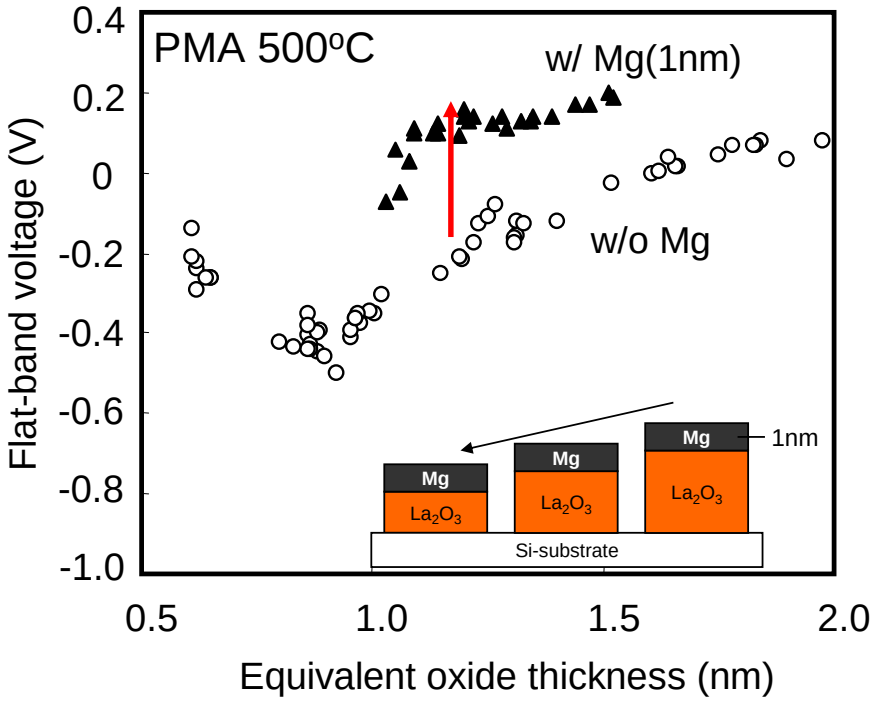

Figure 4.1.1 V_{fb} dependence on EOT of W/La_2O_3/n-Si gate stack structure MOS capacitors w/ and w/o 1-nm-thick metal Mg incorporation.

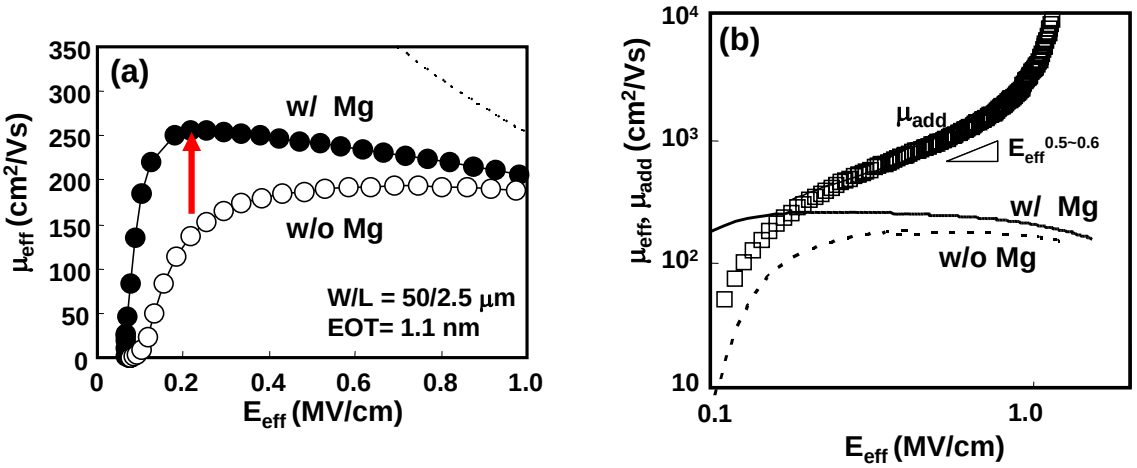

Figure 4.1.2(a) μ_{eff} with the same EOT around 1.1nm. (b)Extracted μ_{add} with $E_{eff}^{0.5\sim0.6}$ dependency indicating remote Coulomb scattering.

4.2 Mechanism of Suppression of Fixed Charge with Mg Incorporation

It is reported that O atoms in W layer as metal gates diffuse into La_2O_3 layer and La-silicate is formed[3]. It is considered that with Mg incorporation, Mg atoms combine with O atoms to suppress the excess supply of O atoms into La_2O_3 as shown fig.4.2.1. Fig.4.2.2 is the result of XPS analysis. The result shows the Mg was found to be in oxide state so that combination of Mg and O also confirmed[4]. As a result, the generation of La-silicate is suppressed so that the total fixed charges in the La-silicate layer can be decreased.

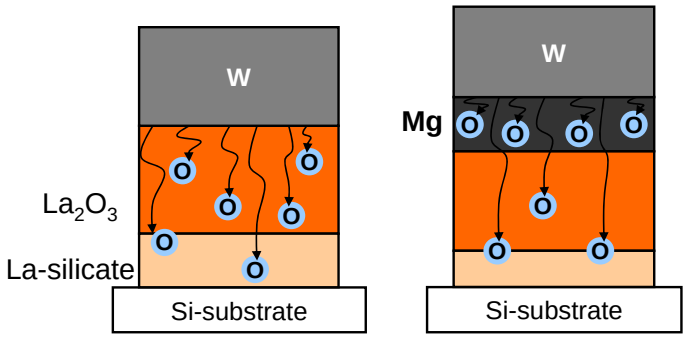

Figure 4.2.1 Mg atoms combine with O atoms to suppress the excess supply of O atoms into La_2O_3 to suppress fixed charge generation in La-silicate layer.

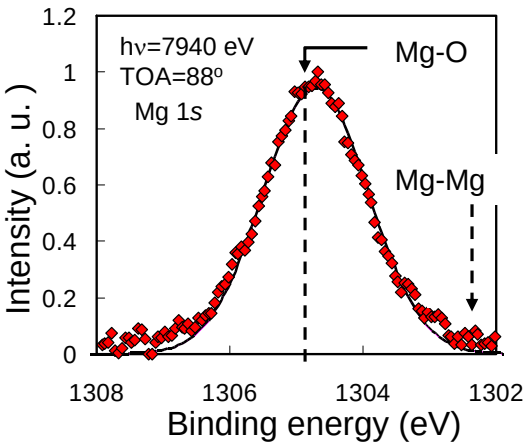

Figure 4.2.2 Result of hard XPS analysis. The result indicates the incorporated Mg is in oxide state.

4.3 Effect of MgO Incorporation on Electrical Properties

Fig.4.3.1 shows the *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors with and without MgO incorporation measured at 100 kHz. The thickness of La_2O_3 is 4nm and incorporated MgO thickness is 1nm and 1.3nm. PMA using RTA furnace was carried out in FG ambient at 500^{o}C for 30min. EOT increases from 1.6nm to 2.0 and 2.1 nm with incorporation of 1-nm-thick and 1.3-nm-thick MgO incorporation, respectively. It is considered as the increase of the physical thickness of dielectrics with MgO incorporation. Fig.4.3.2 shows the *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors with 1-nm-thick MgO incorporation measured at 100 kHz. The thickness of La_2O_3 layer was changed to get the various values of EOT. PMA was carried out in the same way as the previous MOS capacitors. It is observed that V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive

direction. V_{fb} dependence on EOT is summarized in fig.4.3.3 and V_{fb} roll-off and roll-up are observed. It can be observed that the point from V_{fb} roll-off to roll-up shifts to a little larger EOT and more negative flat-band voltage region.

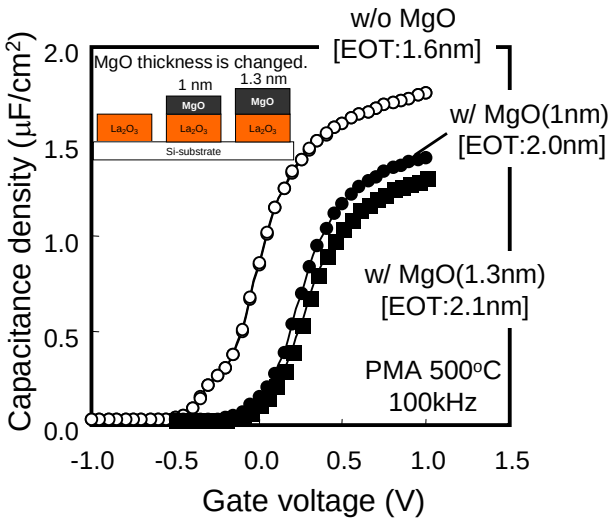

Figure 4.3.1 *C-V* characteristics of W/La_2O_3/n-Si MOS capacitors with and without MgO incorporation. A slight increase of EOT is observed.

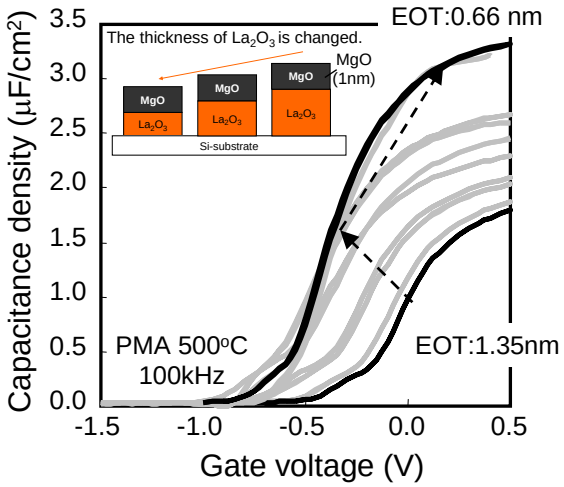

Figure 4.3.2 *C-V* characteristics of W/La_2O_3/n-Si MOS capacitors with 1-nm-thick MgO incorporation. V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive direction.

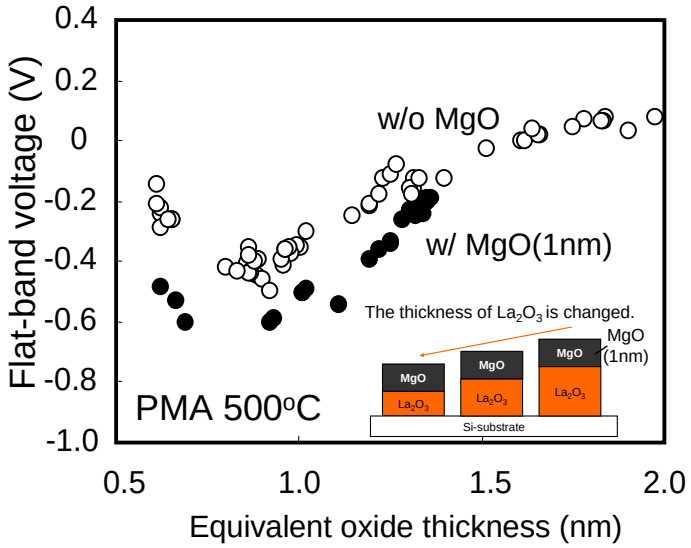

Figure 4.3.3 V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors with 1-nm-thick MgO incorporation. V_{fb} roll-off and roll-up are observed.

4.4 Effect of CaO Incorporation on Electrical Properties

Fig.4.4.1 shows the *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors with 0.7-nm-thick CaO incorporation measured at 100 kHz. The thickness of La_2O_3 layer was changed to get the various values of EOT. PMA using RTA furnace was carried out in FG ambient at 500°C for 30min. It is observed that V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive direction. V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors with 0.7-nm-thick and 0.3-nm-thick CaO incorporation is summarized in fig.4.4.2 and V_{fb} roll-off and roll-up are observed. It can be observed that the point from V_{fb} roll-off to roll-up shifts to larger EOT and more negative V_{fb} region. The more negative shift in the capacitors with 0.7-nm-thick CaO is observed than 0.3-nm-thick CaO.

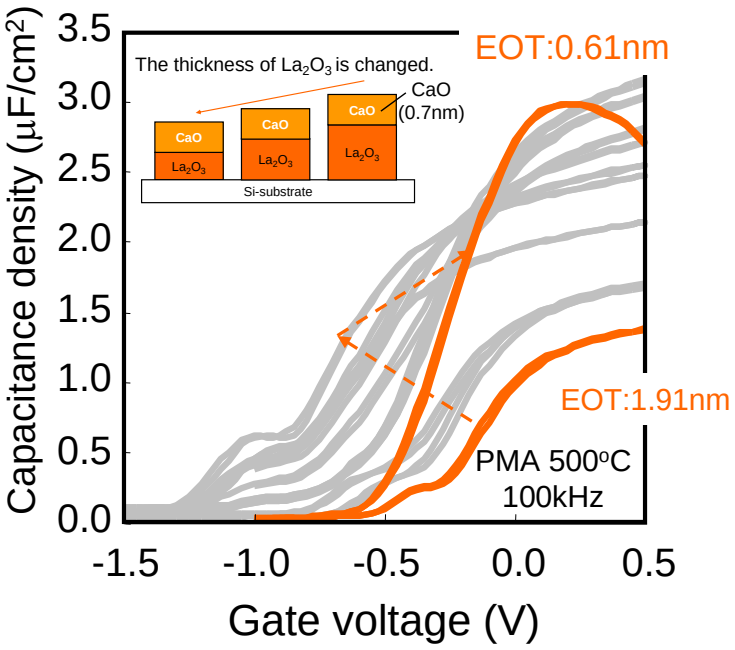

Figure 4.4.1 *C-V* characteristics of W/La_2O_3/n-Si MOS capacitors with 0.7-nm-thick CaO incorporation. V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive direction.

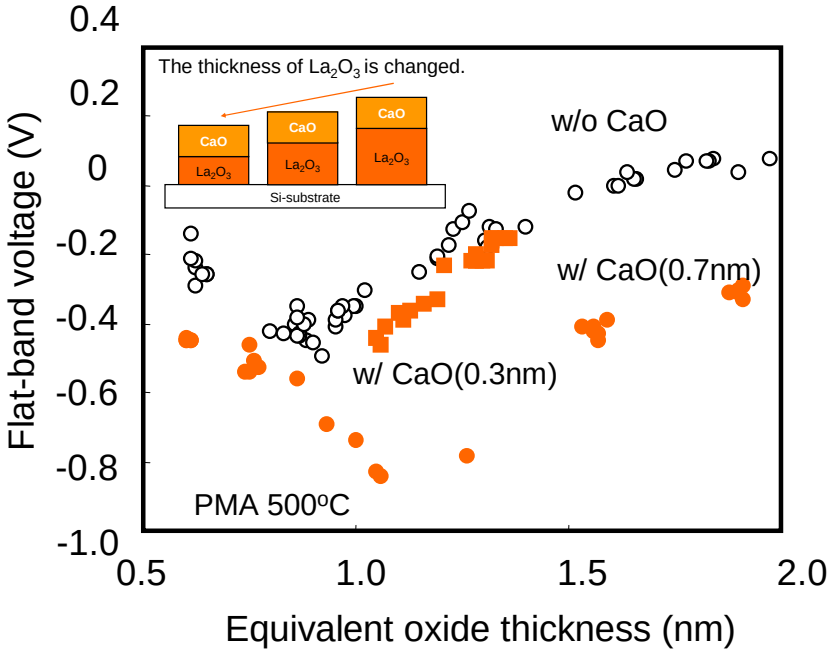

Figure 4.4.2 V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors with 0.7-nm-thick CaO incorporation. V_{fb} roll-off and roll-up are observed.

4.5 Effect of SrO Incorporation on Electrical Properties

Fig.4.5.1 shows the *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors with 1-nm-thick SrO incorporation measured at 100 kHz. The thickness of La_2O_3 layer was changed to get the various values of EOT. PMA using RTA furnace was carried out in FG ambient at 500^{o}C for 30min. It is observed that V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive direction. V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors with 0.5-nm-thick and 1-nm-thick SrO incorporation is summarized in fig.4.5.2 and V_{fb} roll-off and roll-up are observed. It can be observed that the point from V_{fb} roll-off to roll-up shifts to larger EOT and more negative V_{fb} region. The more negative shift in the capacitors with 1-nm-thick SrO is observed than 0.5-nm-thick SrO.

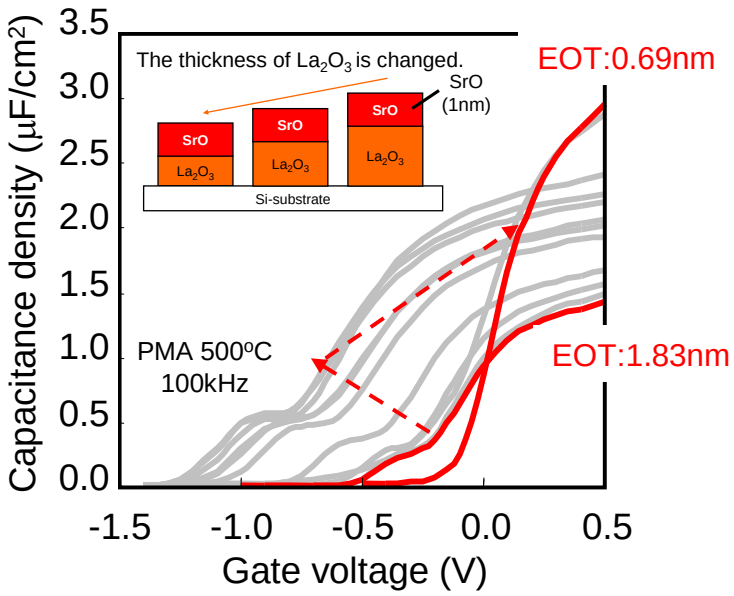

Figure 4.5.1 *C-V* characteristics of W/La_2O_3/n-Si MOS capacitors with 1-nm-thick SrO incorporation. V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive direction.

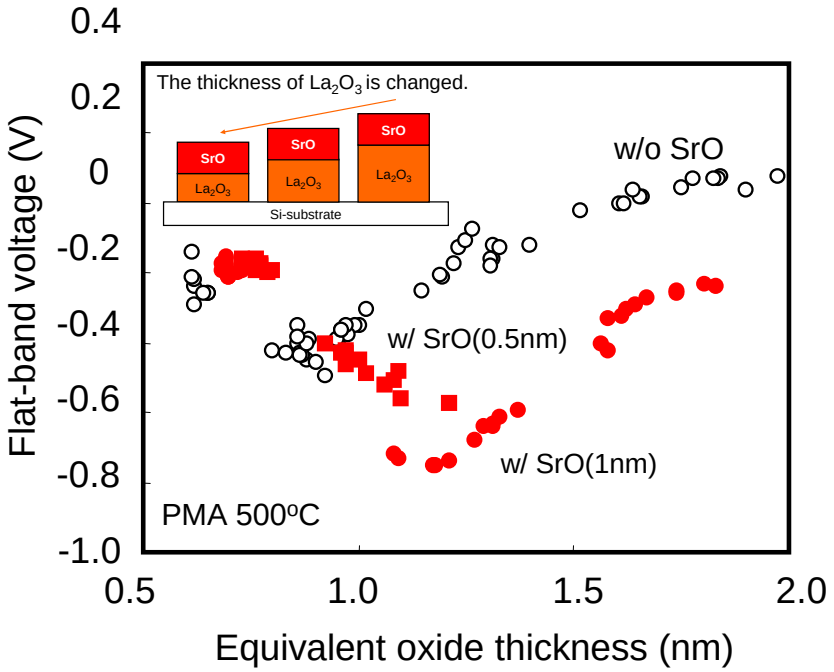

Figure 4.5.2 V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors with 0.5-nm-thick and 1-nm-thick SrO incorporation. V_{fb} roll-off and roll-up are observed.

4.6 Effect of BaO Incorporation on Electrical Properties

Fig.4.6.1 shows the *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors with and without BaO incorporation measured at 100 kHz. The thickness of La_2O_3 is 2.5 nm and incorporated BaO thickness is 1nm and 1.3nm. PMA using RTA furnace was carried out in FG ambient at 500°C for 30min. EOT extremely increases from 0.62 nm to 1.86 and 1.93 nm with incorporation of 1-nm-thick and 1.5-nm-thick BaO incorporation, respectively. Fig.4.6.2 shows the *C-V* characteristics of W/La_2O_3/n-Si gate stack structure MOS capacitors with 0.3-nm-thick BaO incorporation. The

thickness of La_2O_3 layer was changed to get the various values of EOT. PMA was carried out in the same way as the previous capacitors. It is observed that V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive direction. V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors with 0.3-nm-thick BaO incorporation is summarized in fig.4.6.3 and V_{fb} roll-off and roll-up are observed. It can be observed that the point from V_{fb} roll-off to roll-up shifts to larger EOT and more negative V_{fb} region.

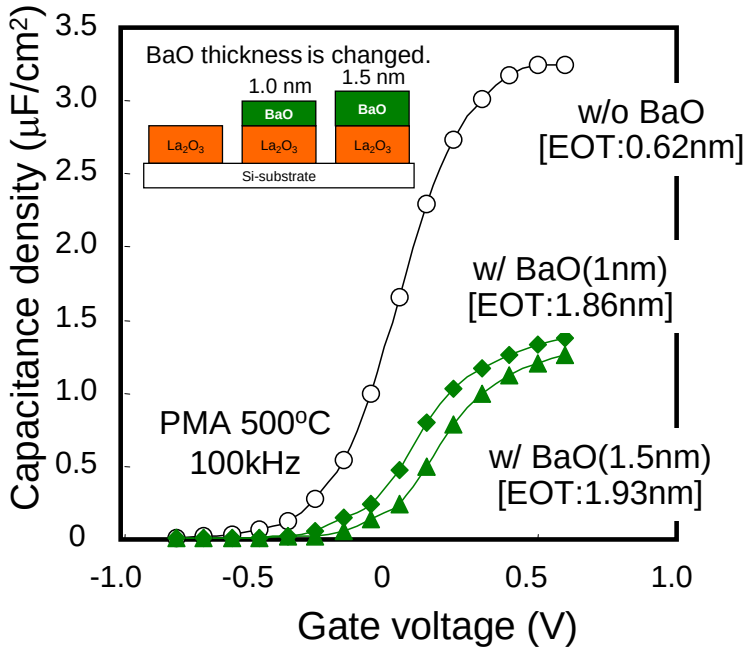

Figure 4.6.1 *C-V* characteristics of W/La_2O_3/n-Si MOS capacitors with and without BaO incorporation. An extreme increase of EOT is observed with BaO incorporation

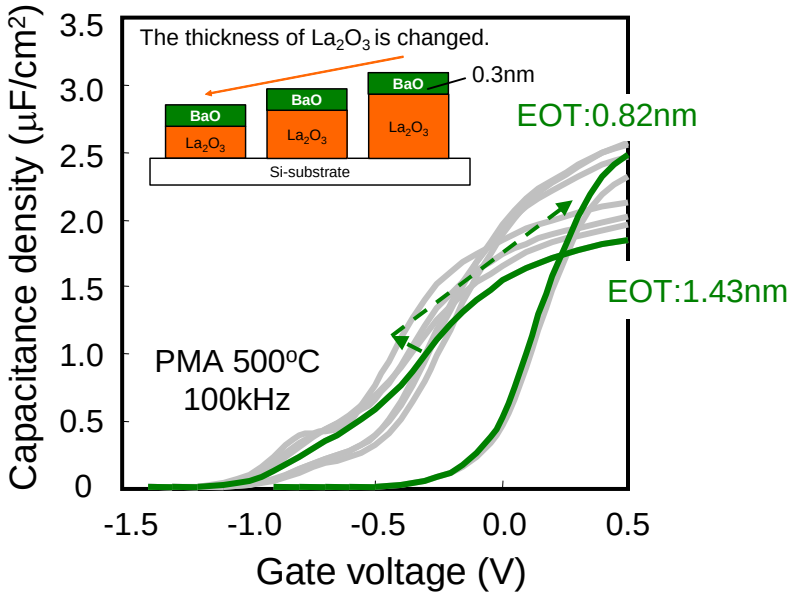

Figure 4.6.2 *C-V* characteristics of W/La_2O_3/n-Si MOS capacitors with 0.3-nm-thick BaO incorporation. V_{fb} shifts towards negative direction as the EOT decreases and then it moves to positive direction.

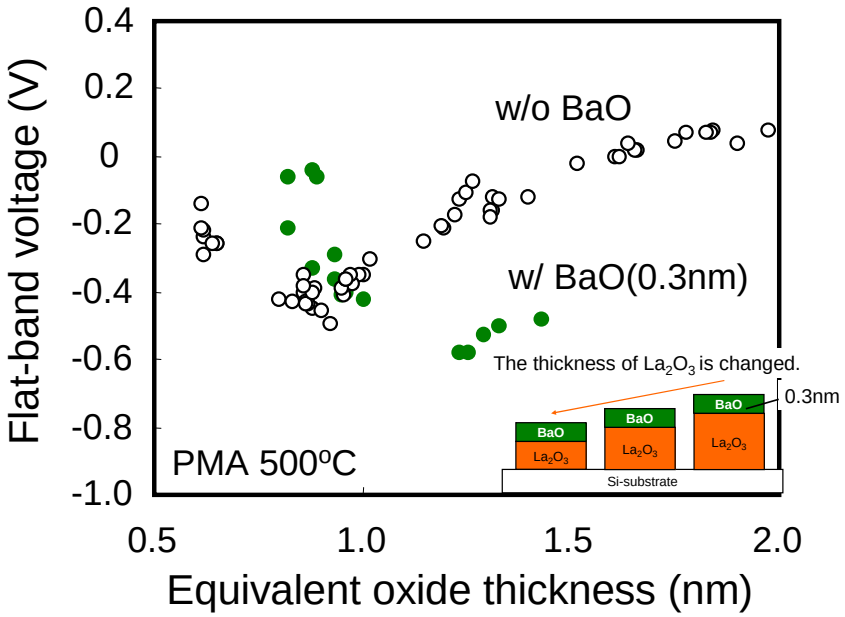

Figure 4.6.3 V_{fb} dependence on EOT of W/La_2O_3/n-Si MOS capacitors with 0.3-nm-thick BaO incorporation. V_{fb} roll-off and roll-up are observed

4.7 Enhancement of La-silicate Formation

With alkali-earth-oxide incorporation, more negative shift of V_{fb} was observed than the capacitors with no incorporation. The reason of the shift can be considered as the enhanced generation of La-silicate. Si *1s* of the capacitors with and without 1-nm-thick BaO incorporation were analyzed by XPS after PMA at 500^{o}C for 30min. Fig.4.7.1 shows the results. The photo-electrons at higher binding energy to the Si-substrate show the formation of La-silicate. A large increase in the intensity of La-silicate was observed with BaO incorporated sample.

O atoms, which are supplied from W layer, combine with La_2O_3 and Si to form La-silicate [5]. Therefore, one of the reasons of the enhancement of La-silicate formation can be explained by the ionic oxygen conductivity of the oxides. It is reported that the incorporation of alkali-earth-elements into La-silicate enhances the conduction of O atoms. With the addition of alkali earth elements into silicates, O atoms can diffuse from 3 to 7 times higher as shown in table 4.7.1 and slight increase of oxygen ionic conductivity is also reported [6,7]. Therefore, the addition of alkali-earth-elements into La-silicate can enhance the growth of silicate layer as shown in fig.4.7.2.

So, the reason of the flat-band voltage roll-off and roll-up behavior with alkali earth elements incorporation is considered to be the combination of the enhancement in the lanthanum silicate formation and the tungsten atom diffusion into the formed layer .

Table 4.7.1 Oxygen ionic conductivities of La-silicate

Composition	Oxygen ionic conductivity (mS/cm)@700°C
$La_{9.33}Si_6O_{26}$	0.3
$La_{9.6}Si_6O_{26.4}$	1.8
$La_9Ca_1Si_6O_{26.5}$	6.3
$La_9Sr_1Si_6O_{26.5}$	8.7
$La_9Ba_1Si_6O_{26.5}$	11.4

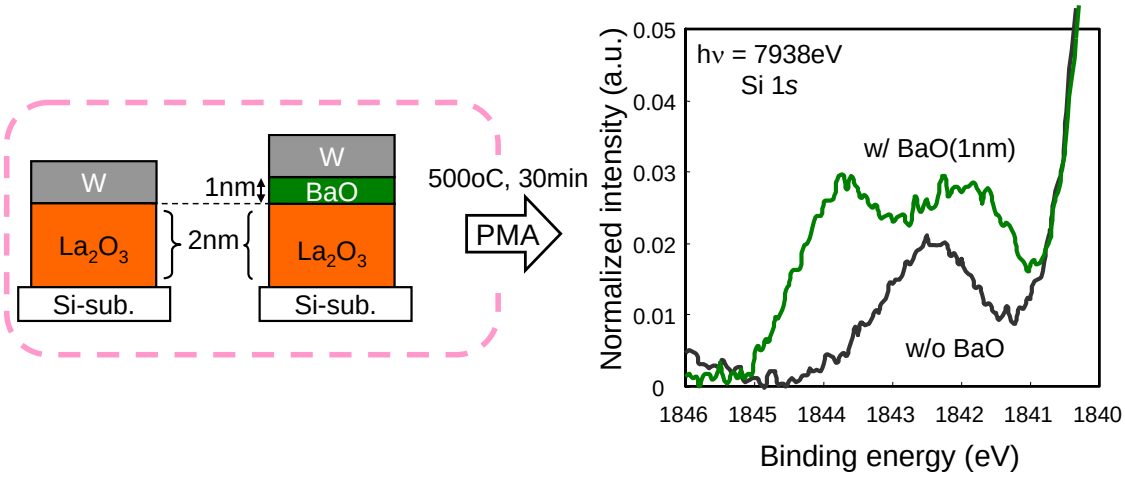

Figure 4.7.1 Result of hard XPS analysis. A large increase in the intensity of La-silicate was observed with BaO incorporated sample.

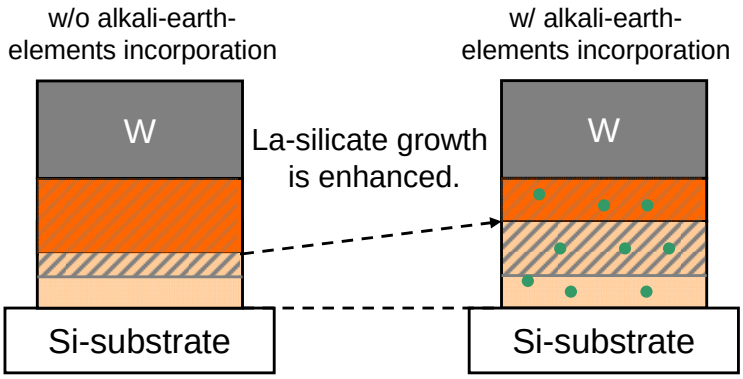

Figure 4.7.2 Alkali-earth-elements incorporation into La-silicate can enhance the growth of the silicate layer

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5 Conclusion

The effect of alkali-earth-elements incorporation into La_2O_3 gated MOS device on electrical characteristics have been conducted. The V_{fb} roll-off and roll-up have been observed and main cause of the phenomena have been considered as fixed charges in La-silicate. With the incorporation of CaO, SrO and BaO into La_2O_3, La-silicate generation have been enhanced to increase the amount of fixed charge. Slight enhancement of La-silicate and fixed charge generation has been observed with MgO incorporation. On the other hand, Mg incorporation can well suppress the generation of fixed charge. It is considered that, with Mg incorporation, excess supply of O atoms can be suppressed.

Appendices

A.1 The principle of TEM and EDX analysis

TEM is one of the electron microscopes. By irradiating electrons to the thin sample, some electrons are scattered and others are transmitted. Because the amount of transmitted electrons depends on the structure or component of each portion, the image is generated by the interference of the transmitted electrons. The image is observed by being magnified with the use of the coil. On the other hand, the elements composing the sample are observed by EDX. By irradiating electrons to atoms in ground state, the electron at the inner shell is exited to outside of the atom and the hole is generated at the inner shell. Other electron moves into the hole and the characteristic x-ray is emitted. Because the x-ray is peculiar to each element, the elements consisting of the sample is determined by measuring the x-ray. The analysis by TEM and EDX can be done at the same time. The schematic illustration of TEM and EDX is shown in fig.A.1(a) and(b)[1].

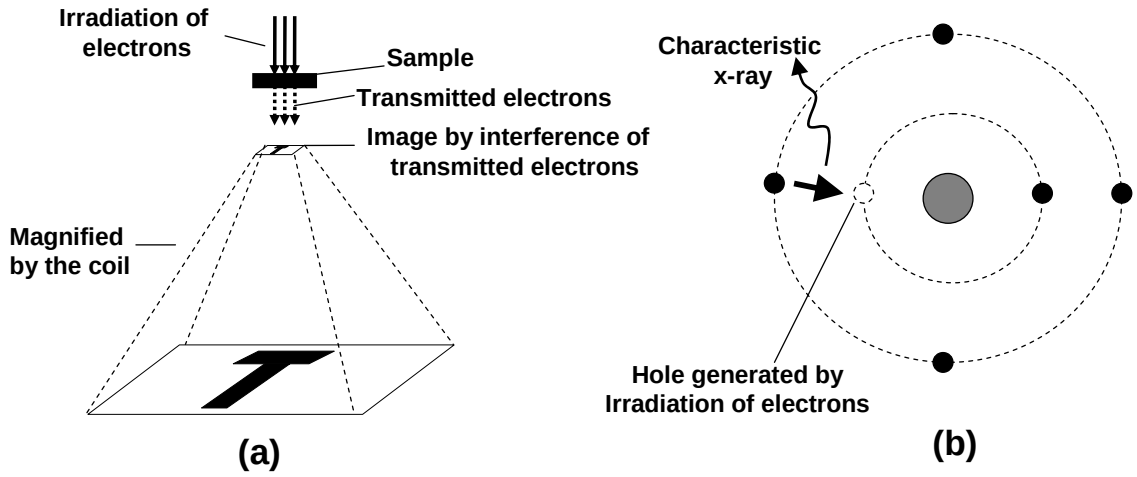

Figure A.1 (a) Magnified image is obtained by using the interference of transmitted electrons. (b)Characteristic x-ray is emitted by the transition of the electron from the outer shell to the inner.

A.2 The principle of XPS analysis

XPS is one of the most effective methods of determining the elements, which composing the sample. By irradiating x-ray to the thin sample, the electrons obtain the energy from the x-ray to be emitted with the kinetic energy. The relation of the energies can be expressed:

$$h\nu = E_k + E_b , \qquad \text{(b.1)}$$

where $h\nu$ is the energy of the x-ray, E_k is the kinetic energy of the emitted electron and E_b is the binding energy of the emitted electron. Because the value of $h\nu$ is constant, the E_b is determined by measuring the E_k as shown in Fig.b.2. The E_b is peculiar to each element and the elements consisting of the sample is also determined. [2]

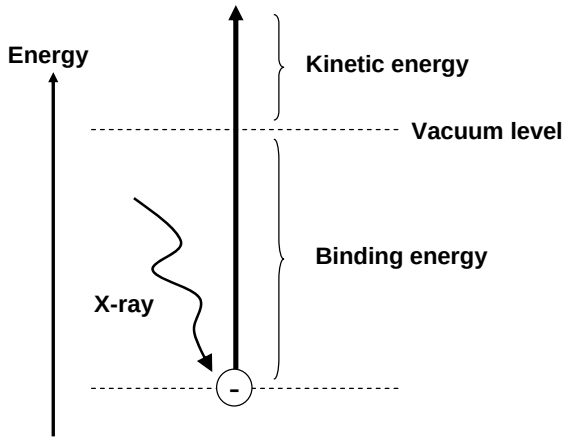

Figure A.2 Schematic illustration of the principle of XPS. By measuring the K.E., the elements composing the sample are determined..

Refferences

[1] http://www.mst.or.jp/010104.html

[2] http://www.mst.or.jp/010103.html

Acknowledgement

First of all, the author would like to express my gratitude to my supervisor Prof. Hiroshi Iwai at Tokyo Institute of Technology. Without his continuous encouragement and advices, my study could not have success. He also gave me many opportunities to attend conferences of both international and domestic. The experiences are precious for my present and future life. The author show reverence for his spirit of contribution.

The author deeply thanks Prof. Takeo Hattori, Prof. Kenji Natori, Prof. Nobuyuki Sugii, Prof. Akira Nishiyama, Prof. Kazuo Tsutsui, Associate Prof. Parhat Ahmet and Associate Prof. Kuniyuki Kakushima giving me useful advices and great help.

The author also thanks research colleagues of Iwai lab. for their friendship, active many discussions and many of encouraging words.

The author would like to appreciate the support of laboratory secretaries, Ms. Karakawa, Ms.Nishizawa and Ms. Matsumoto.

Finally, the author would like to thank all of his friends and his family, especially my parents Tateoki and Chieko and grand-mother Michiko.

Tomotsune Koyanagi

March, 2011