Master Thesis

Interface Properties of $In_{0.53}Ga_{0.47}As$ MOS Capacitors with La_2O_3 and HfO_2 Gate Dielectrics

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Chapter 1.

Introduction

1.1 Background of this study

Semiconductor materials are one of the most important materials in electronics major and the semiconductor properties depended on electrical conductivity which is sensitive on temperature, optical, magnetic, and impurity. In recent years, semiconductor device technologies such as mobile phones, personal computers, lasers, memory media, and so on, have been developed dramatically and have great influences on society. One of the major factors of the technology developments has been integrated large scale integrated circuits (LSI) high density. Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a factor of LSI and very important device for the sophisticated integrated circuits (IC). MOSFET scaling has been proceeded for integrated LSI and is useful to progress with many device parameters for the scaling assumptions in Table 1.1, so that improve the performances of high density, high speed performance and low power consumption. Scaling size trends at present and in the future are shown in Fig. 1.1.

	MOSFET Device and Circuit Parameters	Multiplicative Factor (k > 1)
Scaling assumptions	Device dimensions	$1/k$
	Doping concentration	k
	Voltage	$1/k$
Derived scaling behavior of device parameters	Electric field	1
	Carrier velocity	1
	Depletion-layer width	$1/k$
	Capacitance	$1/k$
	Inversion-layer charge density	1
	Current, drift	$1/k$
	Channel resistance	1
Derived scaling behavior of circuit parameters	Circuit delay time	$1/k$
	Power dissipation per circuit	$1/k^2$
	Power-delay product per circuit	$1/k^3$
	Circuit density	k^2
	Power density	1

Table 1.1 Scaling circuit parameters.

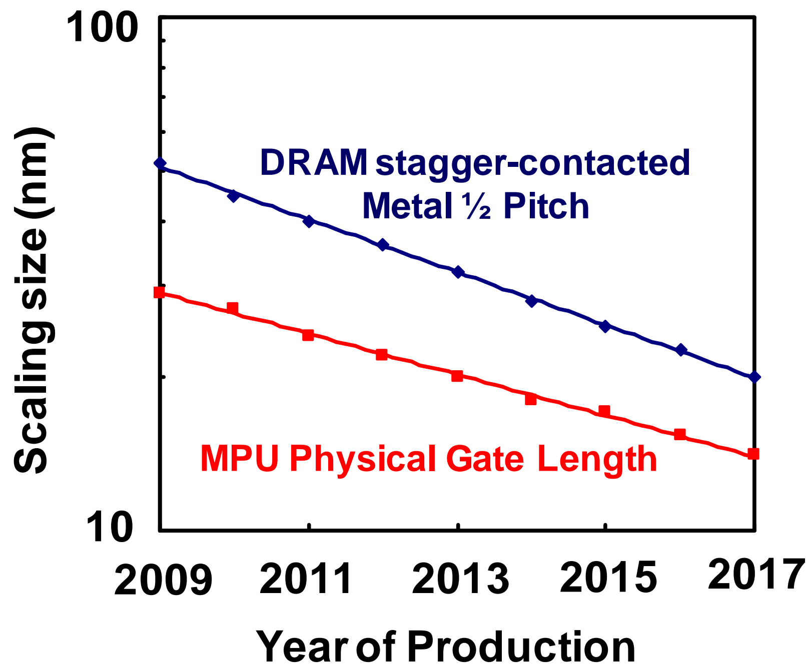
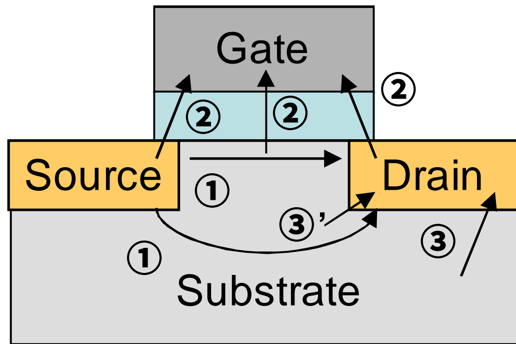


Figure 1.1 Scaling size trends at present and in the future.

1.2 Leakage current increase

MOSFET scaling size has been reached nm order to improve the performances so that leakage current problem is not neglected. Leakage current is one of the most important factors for MOSFETs. Large leakage current prevents to achieve the higher performance for scaling. Si-MOSFET scaling can be limited in the future. Instead of Si channel, MOS devices with III-V channels, for example indium-gallium-arsenide (InGaAs) which is discussed in section 1.3, and IV channels, such as Ge, have been of great interests as one of the promising candidates for future MOSFET. On the other hand, gate leakage current which components are shown in Table 1.2 is especially influenced by MOSFET scaling. As MOSFET scaling rule proceeds one generation, the



(a)

	Kinds	Phenomena	Causes	Rate of leakage current increased	Influence on temperature
①	Subthreshold leakage current	Leakage current of source - drain	Threshold voltage reduction for high speed performance	10 times for 0.1 V threshold voltage reduction	Large
②	Gate leakage current	Leakage current of gate - channel, source or drain passed gate insulator	Gate insulator thinned for scaling	10 - 1000 times for one scaling generation proceed	Small
③	Junction leakage current	Leakage current of source or drain - substrate	Doping concentration increased, crystallization defect, and so on for scaling	Depending on doping concentration and structure	Small
③	GIDL (A kind of junction leakage current)	Leakage current for electric field of gate - drain	Gate insulator thinned for scaling	Several times for one scaling generation proceed	Small

(b)

Table 1.2 Leakage current (a) component image and (b) components in detail of MOSFET.

gate leakage current value increases 10-1000 times larger. High dielectric constant (high-*k*) materials which are discussed in section 1.4 are attractive to decrease the influence of the gate leakage current in Table 1.2 (a) ②.

1.3 Properties of compound semiconductor materials

Period	Column II	III	IV	V	VI
2		B	C	N	O
3	Mg	Al	Si	P	S
4	Zn	Ga	Ge	As	Se
5	Cd	In	Sn	Sb	Te
6	Hg		Pb		

Table 1.3 A part of the periodic table depended on semiconductor materials.

Silicon (Si) is the major material for semiconductor devices because Si devices have good properties on room temperature (R.T), and form high quality SiO_2 layers by heat oxidation. In addition, plenty amounts of Si reside in nature resources. Therefore, Si device technology progresses compared to other semiconductor devices. On the other hand, compound semiconductor substrates are very attractive because of higher electron mobility compared to Si substrate so that many compound semiconductor materials have been studied in recent years. Table 1.3 is a part of periodic table depended on semiconductor materials. Si is IV channel, on the other hand indium (In), gallium (Ga), and arsenic (As) which is studied in this thesis are III and V channels so that compound semiconductor materials have electrical and optical properties which Si material does not have. The parameters with some of the compound semiconductor channels compared that of Si channel are shown in Table 1.4. Electron mobility is high as In concentration is deeper, but energy band-gap is low. $In_xGa_{1-x}As$ channels are very attractive for high electron mobility. On the other hand, the dependences of energy

	Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electron Mobility (cm^2/Vs)	600	4600	7800	20000	30000
Electron Saturation Velocity ($\times 10^7$ cm/s)	1	1.2	0.8	3.5	5
Ballistic Mean Free Path (nm)	28	80	106	194	226
Energy Band-gap (eV)	1.12	1.42	0.72	0.36	0.18

Table 1.4 Channel material properties at 295 K.

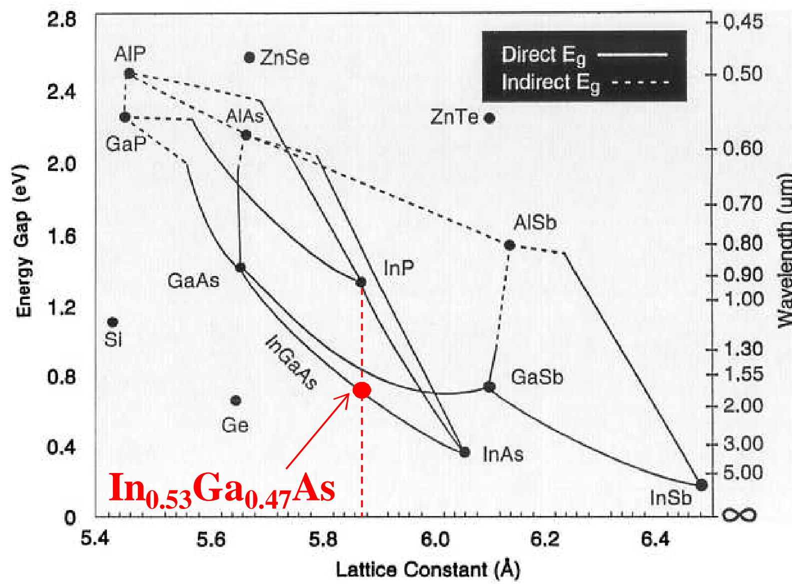


Figure 1.2 Energy gap vs. Lattice constant on semiconductor substrates.

band-gap and lattice constant on semiconductor substrates are shown in Fig. 1.2. $In_xGa_{1-x}As$ layers are epitaxially grown on InP substrates so that In concentration of 53% and Ga concentration of 47% were used because of lattice match with InP substrates. The electron mobility of $In_{0.53}Ga_{0.47}As$ channels are 7800 cm^2/Vs which is more 10 times than that of Si channel (Table 1.4). However, one of the major current issues in InGaAs MOS devices is the lack of acceptable electrical properties at high-*k*/substrate interface discussed in section 1.4.

1.4 Requirement high-*k* materials

MOSFET scaling size has been reached nm order so that thin gate dielectrics are easy to flow the gate leakage current (Table 1.2 (a) ②). However, high-*k* materials can reduce the leakage current with gate capacitance values saved. The gate capacitance values (C) are calculated in Eq. (1.1).

$$C = \frac{\varepsilon_{high-k}}{d} = \frac{\varepsilon_{ox}}{d_{EOT}} \quad (1.1)$$

$\varepsilon_{high\text{-}k}$: dielectric constant of high-*k* materials ε_{ox} : dielectric constant of SiO_2

d : gate dielectric physical thickness d_{EOT} : physical thickness of SiO_2

Because scaling is evaluated by d_{EOT}, high-*k* materials can be thicker to save same gate capacitance values so that the gate leakage currents are decrease. The high-*k* materials are very attractive to reduce gate leakage currents and progress scaling of gate thickness in MOSFETs. On the other hand, InGaAs MOS devices are lack of acceptable electrical properties at high-*k*/substrate interface except for aluminum-oxide

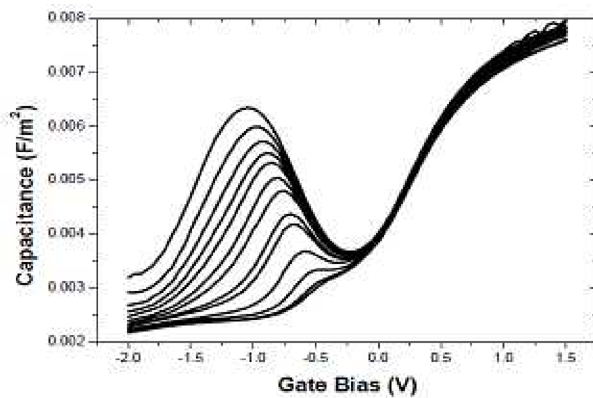


Figure 1.3 *C-V* curves of Al_2O_3/InGaAs MOS capacitor.

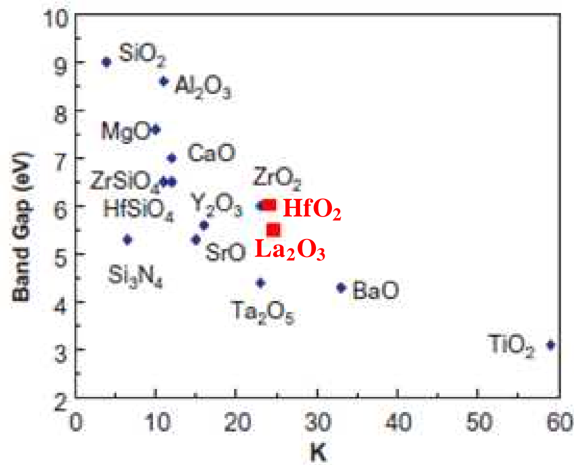


Figure 1.4 Band gap vs. *k*-value of insulator materials.

(Al_2O_3). Al_2O_3 has been reported to have small interface state density with reduced hysteresis in the capacitance-voltage (*C-V*) curve which is shown in Fig. 1.3. High-*k* material with larger *k*-value is required for scaling the oxide film thickness. Some of the insulator materials are compared their parameters of band gap and *k*-value which is shown in Fig. 1.4. A large band gap material of gate insulator in MOSFET can reduce the gate leakage current compared to lower band gap materials. The *k*-value of Al_2O_3 is not high (k ~10), on the other hand the *k*-values of lanthanum-oxide (La_2O_3) and hafnium-oxide (HfO_2) written in red captions in Fig. 1.4 are higher. In addition, their parameters of band gap are relatively large and they have been reported as promising candidates for next generation Si technology.

1.5 Purpose of this study

InGaAs channels are very attractive for high electron mobility. One of the major current issues in InGaAs MOS devices is the lack of acceptable electrical properties at high-*k*/substrate interface. High-*k* material is required for scaling the oxide film thickness. La_2O_3 and HfO_2 which have been reported as promising candidates for next generation Si technology, have high *k*-values and large band gap, relatively. The purpose of this study is evaluation of the interface characteristics of $In_{0.53}Ga_{0.47}As$ MOS capacitors with La_2O_3 and HfO_2 as the gate dielectrics on annealing condition and O_2 flow process. The device properties were measured by electrical characteristics.

Chapter 2.

Fabrication Process

2.1 Fabrication process of InGaAs MOS capacitors

300-nm-thick Si doped InGaAs layers with indium (In) concentration of 53% and gallium (Ga) concentration of 47% were epitaxially grown on lattice matched *n*-InP (100) wafers. The doping concentration Si is 1×10^{17} cm^{-3}. Fabrication process of InGaAs MOS capacitors as the La_2O_3 and HfO_2 as the gate dielectrics is shown in Fig. 2.1. Wafers were degreased by using the mixed solution of acetone and ethanol, and rinsed in deionized water, followed by etching native oxides in 20% HF solution for 3 minutes at room temperature. High-*k* layer was deposited by e-beam evaporation (10^{-6} Pa) at room temperature. A 50-nm-thick W film was successively *in situ* deposited by RF magnetron sputtering. After gate lithography and SF_6 reactive ion etching (RIE), a 50-nm-thick Al contact layer on the backside of the substrates was deposited by thermal evaporation. Rapid thermal post-metallization annealing (PMA) was performed in forming gas (F.G) (N_2:H_2=97%:3%) ambient in the range from 300 to 500 °C for 0.5, 5, or 30 minutes. *C-V* characteristics were measured at frequency in the range from 1 kHz to 1 MHz.

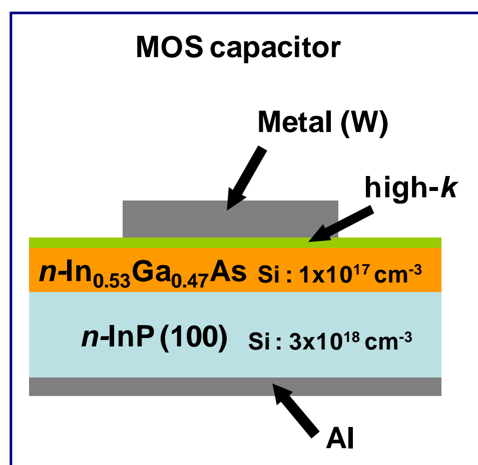
300 nm thick $In_{0.53}Ga_{0.47}As$ on *n*-InP wafer

- Acetone and ethanol cleaning
  HF 20% (3 min) treatment
- High-*k* e-beam deposition @ R.T

  in-situ
- Gate metal (W) deposition by sputtering
- Reactive ion etching (RIE) of W gate
- Backside Al contact
- Annealing in F.G from 300 to 500 °C
  for 30 sec, 5 min, or 30 min

Electrical Characterization

(a)



(b)

Figure 2.1 (a) Fabrication process of InGaAs MOS capacitors. (b) Structure of MOS capacitor.

2.2 Fabrication Methods

2.2.1 Surface treatment

InGaAs substrates were cleaned by using the mixed solution of acetone in ultrasonic cleaning and ethanol, and rinsed in deionized water. After cleaning, the substrates were etched native oxides in 20% HF solution for 3 minutes at room temperature, and rinsed in deionized water.

2.2.2 Electron-beam evaporation

After etching native oxides in 20% HF solution for 3 minutes, high-*k* layers were deposited by electron-beam evaporation (10^{-6} Pa) at room temperature. High-*k* material tablets are heated by 5kV electron beam near the source, and ultra-thin high-*k* layers were deposited on the substrate which schematic is shown in Fig.2.2. Film thickness monitor is used for real time physical thickness of the film calibrated before the experiment.

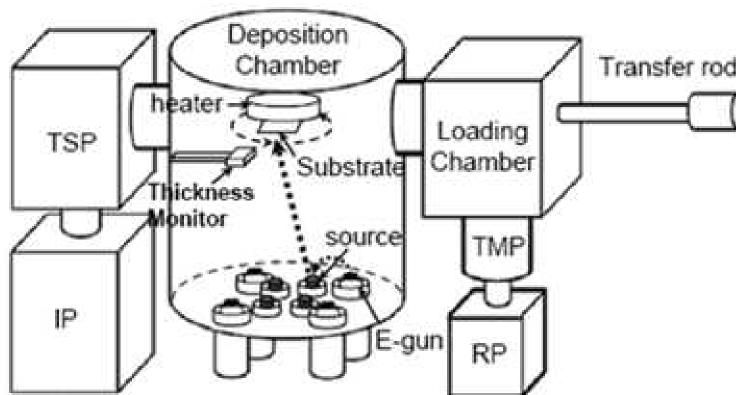


Figure 2.2 Schematic of high-*k* layers deposition by electron-beam evaporation.

2.2.3 RF magnetron sputtering

A 50-nm-thick W film was successively *in situ* deposited by RF magnetron sputtering after depositing high-*k* layers on the substrate. Argon (Ar) gas flow was set to 7sccm while holding the deposition chamber pressure at of which was set to be 1.33Pa, the 150W RF current power used to produce plasma.

2.2.4 Gate lithography and SF_6 reactive ion etching (RIE)

Positive photo-resist layers were coated on the samples by spin coating followed by baking samples at 115 °C for 5 minutes on a hot plate. The photo-resist layered samples were aligned and exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. A part of mask pattern is shown in Fig.2.3. Post-baking was done at 130 °C for 10 minutes on the hot plate. After the gate lithography, reactive ion etching (RIE) was done to etch the patterned samples. The patterned sample was etched by SF_6 gas at 30 W in 1.5 minutes. Photo-resist layer on

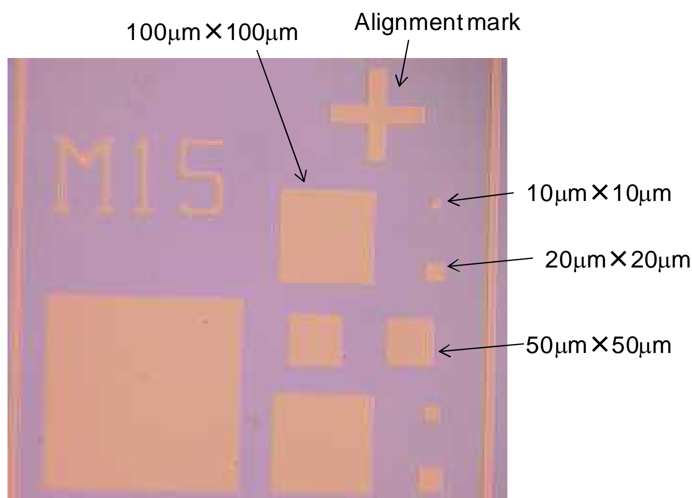


Figure 2.3 A part of mask patterning.

top of metal gate was removed by O_2 gas ashing which can be resist stripping. However, a few minutes ashing is hard to strip the resist, completely. Therefore, after the O_2 gas ashing, the samples were cleaned by acetone in ultrasonic cleaning and ethanol, and rinsed in deionized water to strip their resists, completely.

2.2.5 Thermal evaporation for Al contact

A 50-nm-thick Al contact layer on the backside of the samples was deposited by thermal evaporation (Fig. 2.4). W boat was heated by large current, Al is melted and evaporated. After Al evaporation, Al contact layer on the backside of the samples was deposited (~3×10^{-3} Pa).

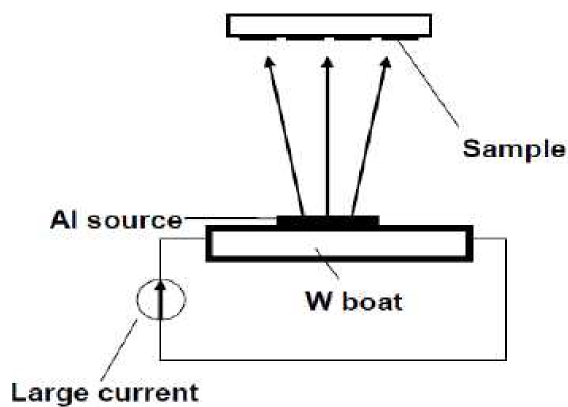


Figure 2.4 Schematic of Al layers deposition by thermal evaporation.

2.2.6 Rapid thermal post-metallization annealing (PMA)

Forming gas (F.G) was flowed after vacuumed air adequately. Rapid thermal post-metallization annealing (PMA) was performed in F.G (N_2:H_2=97%:3%) ambient in the range from 300 to 500 °C for 0.5, 5, or 30 minutes. Cool down process is done flowing in F.G. Samples were taken out at about 100 °C.

2.3 Electrical characteristic methods

2.3.1 Measurement of capacitance-voltage (*C-V*) characteristics

Capacitance-voltage (*C-V*) characteristics of MOS capacitors were determined various charges. Energy band diagram of an MOS capacitor on a *p*-type substrate is shown in Fig. 2.5. The intrinsic energy level E_i or potential ϕ in the neutral part of the devices taken as the zero reference potential. The surface potential ϕ_s is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \quad (2.1)$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitance from the gate, $C = dQ_G/dV_G$, where dQ_G and dV_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, $Q_G = -(Q_S + Q_{it})$ assuming no oxide charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \phi_s$, where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential, allowing Eq. (2.1) to be rewritten as

$$C = -\frac{dQ_S + dQ_{it}}{dV_{ox} + d\phi_S} \quad (2.2)$$

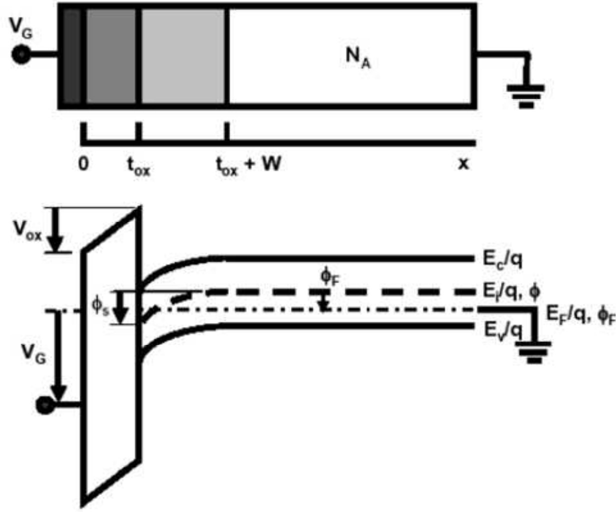


Figure 2.5 Cross-section and potential band diagram of an MOS capacitor.

The semiconductor charge density Q_S, consists of hole charge density Q_p, space-charge region bulk charge density Q_b, and electron charge density Q_n. With $Q_S = Q_p + Q_b + Q_n$, Eq. (2.2) becomes

$$C = -\frac{1}{\dfrac{dV_{ox}}{dQ_S + dQ_{it}} + \dfrac{d\phi_S}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \qquad (2.3)$$

Utilizing the general capacitance definition of Eq. (2.1), Eq. (2.3) becomes

$$C = \frac{1}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_p + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \qquad (2.4)$$

The positive accumulation charge Q_p dominates for negative gate voltages for *p*-substrate devices. For positive V_G, the semiconductor charges are negative. The minus sign in Eq. (2.3) cancels in either case.

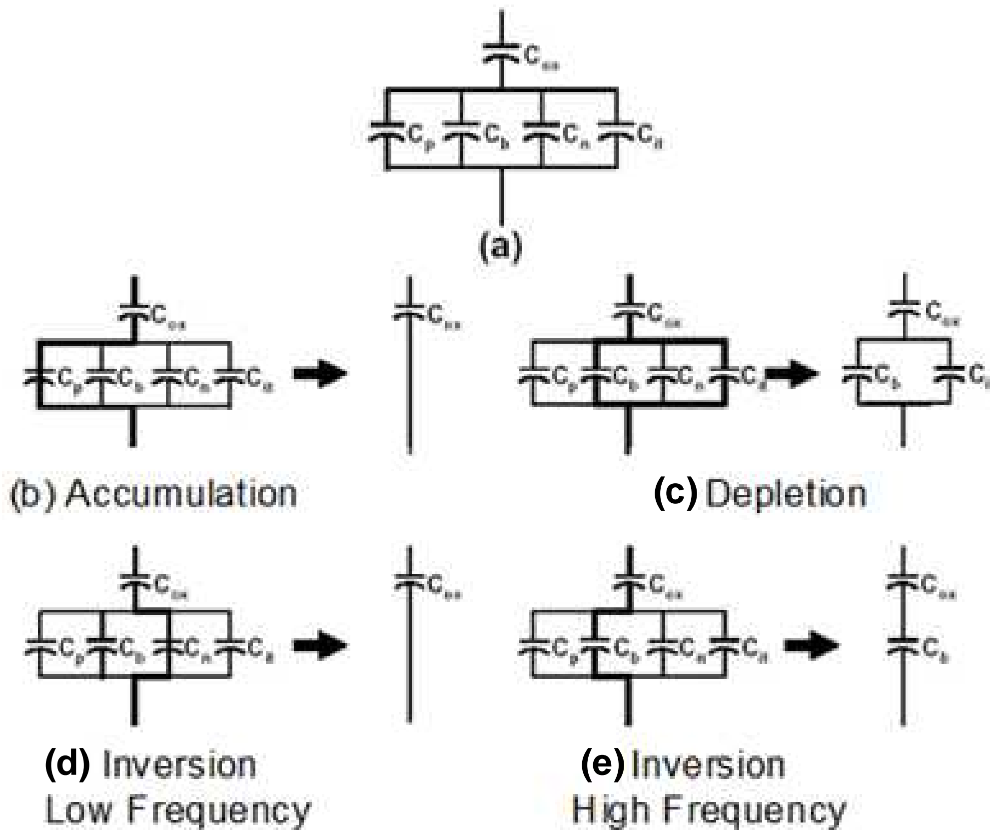


Figure 2.6 Capacitances of an MOS capacitor for various bias conditions.

Eq. (2.4) is represented by the equivalent circuit in Fig. 2.6 (a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is very high approaching a short circuit. The four capacitances are shorted as shown by the heavy line in Fig. 2.6 (b) and the overall capacitance is C_{ox}. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = -qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in Fig. 2.6 (c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (Fig. 2.6 (d)) becomes the oxide capacitance again. When the inversion charge is

unable to follow the ac voltage, the circuit in Fig. 2.6 (e) applies in inversion, with $C_b = K_S\varepsilon_o/W_{inv}$ with W_{inv} the inversion space-charge region width.

2.3.2 Measurement of leakage current density-voltage (*J-V*) characteristics

The gate leakage current in Table 1.2 (a) ② with a MOS capacitor is very important parameter. The leakage currents were measured by semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

2.3.3 Measurement of interface state density (D_{it}) values by conductance method

Conductance method, proposed by Nicollian and Goetzberger in1967, is one of the most sensitive methods to determine D_{it}. Interface trap densities of 10^9 $cm^{-2}eV^{-1}$ and lower can be measured. It is also the most complete method, because it yields D_{it} in the depletion and weak inversion portion of the band gap, the capture cross-sections for majority carriers, and information about surface potential fluctuations. The technique is based on measuring the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

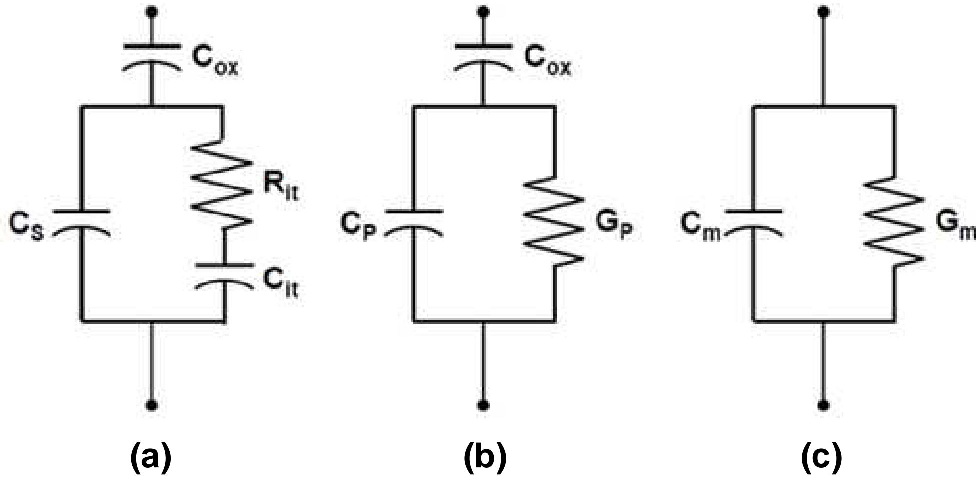


Figure 2.7 Equivalent circuits for conductance measurements; (a) MOS capacitor with interface trap time constant, (b) simplified circuit of (a), (c) measured circuit.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in Fig. 2.7 (a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_S, and the interface trap capacitance C_{it}. The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it}. It is convenient to replace the circuit of Fig. 2.7 (a) by that in Fig. 2.7 (b), where C_p and G_p are given by

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \qquad (2.5)$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \qquad (2.6)$$

Where $C_{it} = q^2 D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$, the interface trap time constant, given by $\tau_{it} = [v_{th}\sigma_p N_A \exp(-q\phi_s/kT)]^{-1}$. Dividing G_p by ω makes Eq. (2.6) symmetrical in $\omega\tau_{it}$. Eq. (2.5) and (2.6) are for interface traps with a single energy level in the band gap. Interface traps at the SiO_2-Si interface, however, are continuously

distributed in energy throughout the Si band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1+(\omega\tau_{it})^2\right] \qquad (2.7)$$

Eq. (2.6) and (2.7) show that the conductance is easier to interpret than the capacitance, because Eq. (2.6) does not require Cs. The conductance is measured as a function of frequency and plotted as G_p/ω versus ω. G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$. For Eq. (2.7) we find $\omega = 2/\tau_{it}$ and $D_{it} = 2.5G_p/q\omega$ at the maximum. Hence one can determine D_{it} from the maximum G_p/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis.

An approximate expression giving the interface trap density in terms of the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{\max} \qquad (2.8)$$

Capacitance meters generally assume the device to consist of the parallel C_m—G_m combination in Fig. 2.7 (c). A circuit comparison of Fig. 2.7 (b) to Fig. 2.7 (c) gives G_p/ω in terms of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}{}^2}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2} \qquad (2.9)$$

assuming negligible series resistance. The conductance measurement must be carried out over a wide frequency range. The portion of the band gap probed by conductance measurements is typically from flat band to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50 mV or less to prevent harmonics of the signal frequency giving rise to spurious conductance. The conductance depends only on the device area for a given D_{it}. However, a capacitor with thin oxide has a high capacitance relative to the conductance, especially for low D_{it} and the resolution of the capacitance meter is dominates by the out-of-phase capacitive current component. Reducing C_{ox} by increasing the oxide thickness helps this measurement problem.

Chapter 3.

Electrical characteristics of $In_{0.53}Ga_{0.47}As$ MOS capacitors with La_2O_3 and HfO_2 as the gate dielectrics

3.1 Introduction

This study purpose is improvement of the high-k layer/InGaAs interface. I have investigated electrical characteristics of InGaAs MOS capacitors with La_2O_3 and HfO_2 as the gate dielectrics upon various annealing temperatures ranging from 300 to 500 °C with duration of 0.5, 5, or 30 minutes. C-V characteristics, leakage current, and interface state densities by conductance method were measured.

3.2 Electrical characteristics

3.2.1 La_2O_3 (8 nm)/*n*-type InGaAs MOS capacitors

An 8-nm-thick La_2O_3 layer deposited *n*-type InGaAs MOS capacitors were fabricated. Rapid thermal post-metallization annealing (PMA) was performed in forming gas (F.G) (N_2:H_2=97%:3%) ambient in the range from 300 to 450 °C for 0.5, 5, or 30 minutes. Figure 3.1 (a)-(d) shows capacitance-voltage (*C*-*V*) characteristics with annealing from 300 to 450 °C for 5 minutes, respectively. The *C*-*V* characteristics were measured at frequency in the range from 1 kHz to 1 MHz at room temperature. With increasing the annealing temperature, hysteresis was improved and capacitance in accumulation was larger. Frequency dispersion in accumulation and inversion is observed. The frequency dispersion in the accumulation region (positive gate voltage) is effect on the interface traps which is referred as weak Fermi-level pinning effect. The strong frequency dispersion in inversion region (negative gate voltage), is the effect on minority carrier response due to the presence of interface trap states. On the other hand, the *C*-*V* curves measured at low frequency (1 kHz and 10 kHz) in Fig. 3.1 (c) and (d) differ from those at higher frequency at $Vg > 0.5$ V. These behaviors were caused by the gate leakage current. Indeed, the gate leakage current after annealing at the temperature from 300 to 450 °C for 5 minutes as a function of gate voltage increased with increasing annealing temperature (Fig. 3.2). The same tendency was also observed with the samples annealing for 0.5 and 30 minutes.

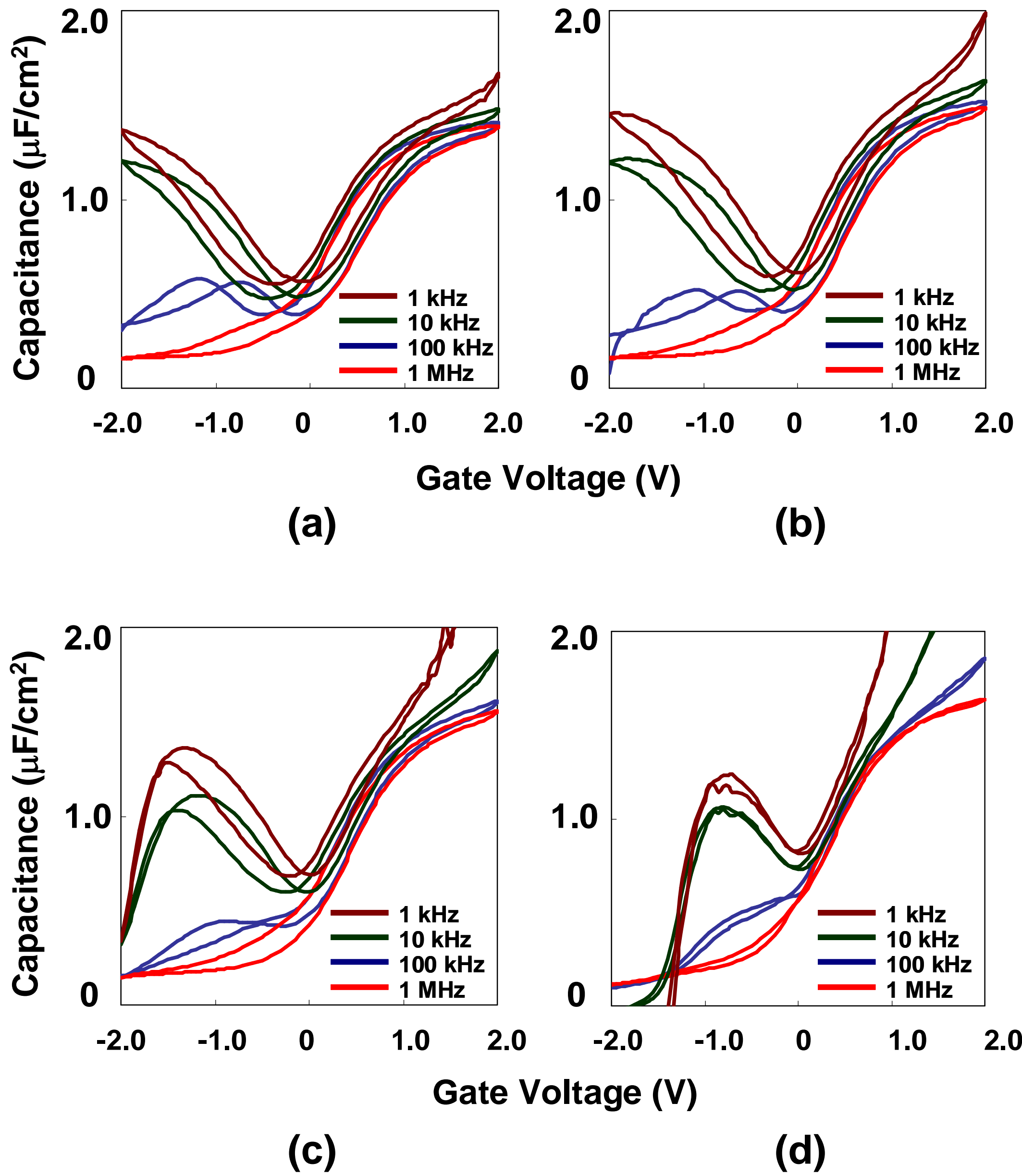


Figure 3.1 *C-V* curves of an 8-nm-thick La_2O_3 layer deposited InGaAs MOS capacitors compared annealing temperature. (a) 300 ^oC, (b) 350 ^oC, (c) 400 ^oC, and (d) 450 ^oC for 5 min in F.G ambient.

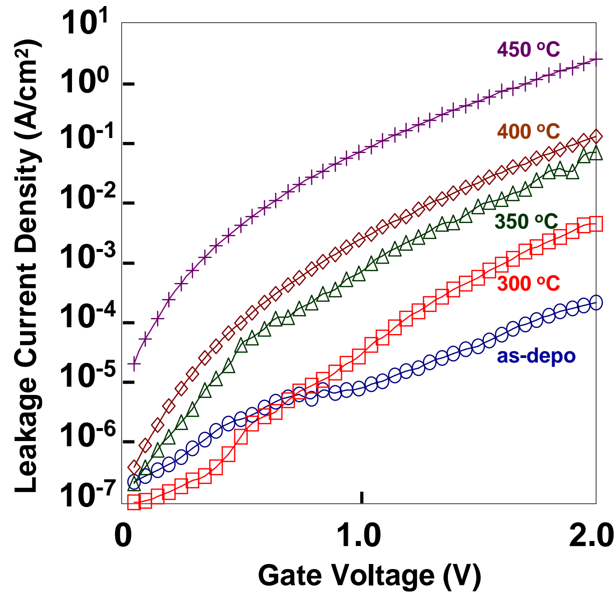


Figure 3.2 Gate leakage currents of an 8-nm-thick La_2O_3 layer deposited InGaAs MOS capacitors with annealing from 300 to 450 °C for 5 min and as-depo.

On the other hand, Fig. 3.3 (a)-(c) shows *C-V* characteristics with annealing duration of 0.5, 5, or 30 minutes at 300 °C, respectively. Large frequency dispersion is shown in Fig. 3.3 (a). The frequency dispersion was improved with annealing for 5 minutes and over. Figure 3.4 is shown gate leakage current of the capacitances. The leakage current is almost independent of the annealing duration. This tendency is contrast with effect on annealing temperature.

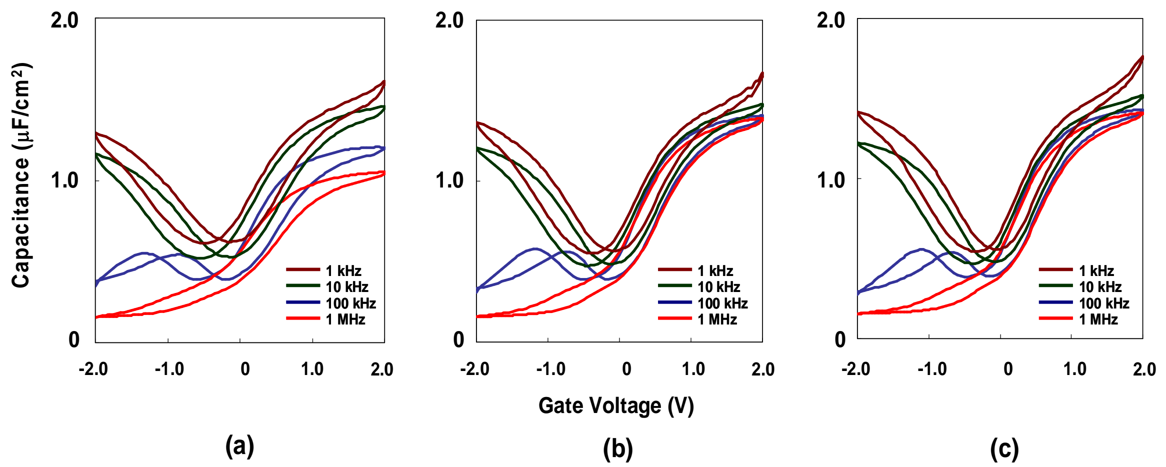


Figure 3.3 *C-V* curves of an 8-nm-thick La_2O_3 layer deposited InGaAs MOS capacitors compared annealing time. (a) 30 sec, (b) 5 min, and (c) 30min at 300 °C in F.G ambient.

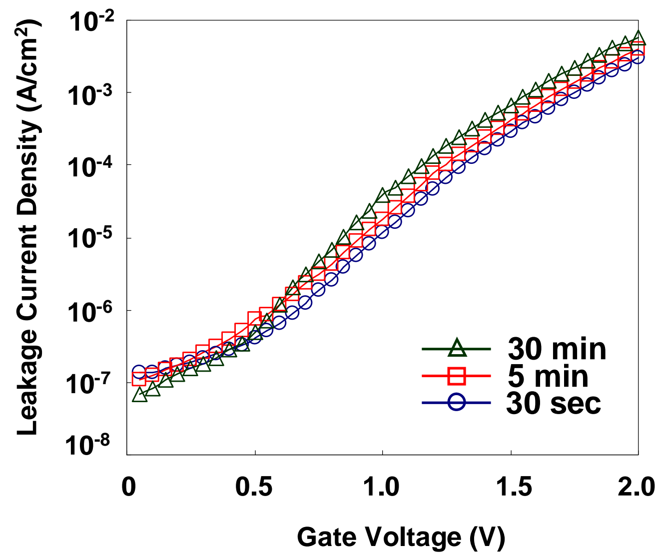


Figure 3.4 Gate leakage currents of an 8-nm-thick La_2O_3 layer deposited InGaAs MOS capacitors with annealing for 30sec, 5 min, and 30 min at 300 °C

3.2.2 La_2O_3 (15 nm)/*n*-type InGaAs MOS capacitors

The 8-nm-thick La_2O_3 layer deposited MOS capacitors were very sensitive to the leakage current because of quite thin layer so that thicker (15-nm-thick) La_2O_3 layer deposited *n*-type InGaAs MOS capacitors were fabricated. Figure 3.5 shows *C-V* curves of the capacitors with annealing in F.G ambient at 300 °C ((a)-(c)) and 450 °C ((d)-(f)) for 0.5, 5, and 30 minutes, respectively. The measured gate voltage range is from -2 to 2.5 V.

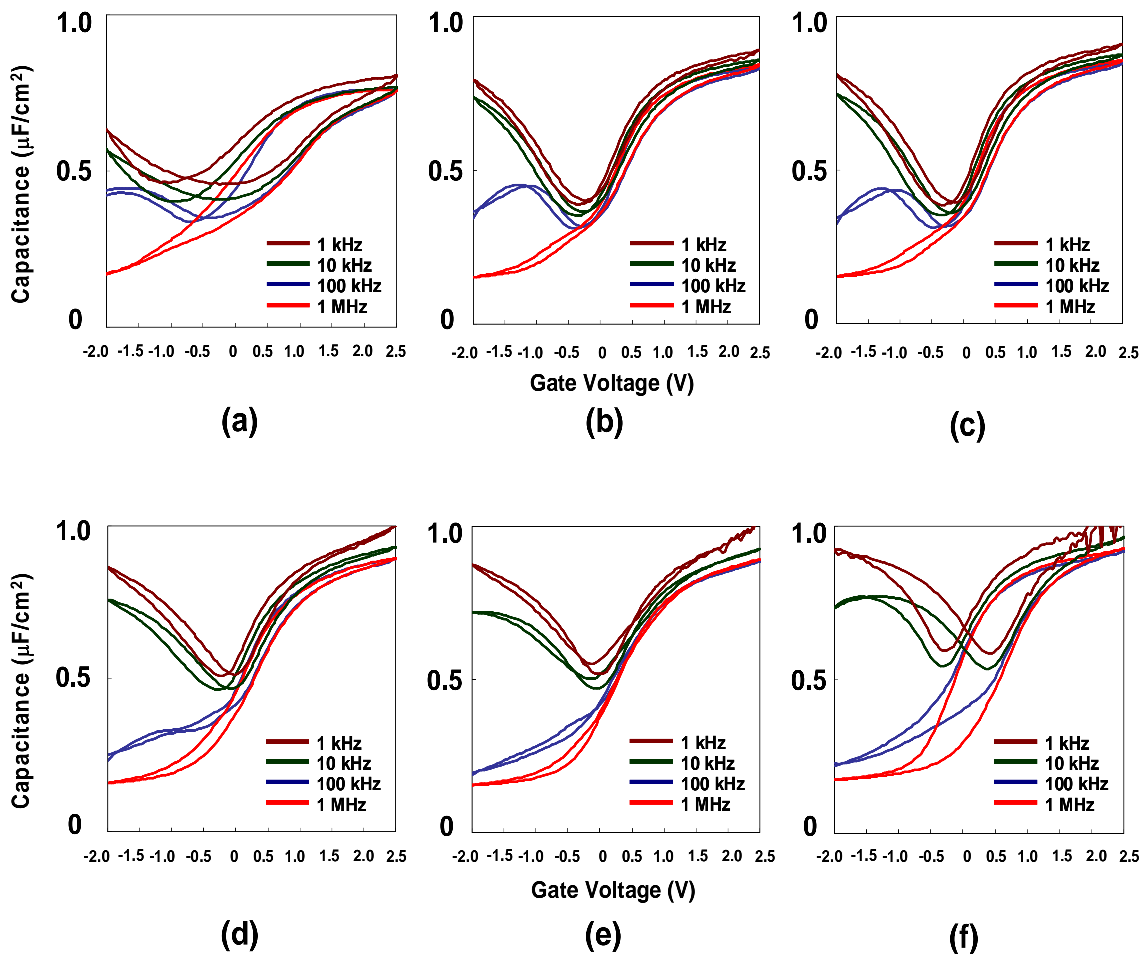


Figure 3.5 *C-V* curves of La_2O_3 (15nm)/InGaAs MOS capacitors compared annealing time.
(a) 0.5 min (b) 5 min (c) 30 min at 300 °C in F.G ambient.
(d) 0.5 min (e) 5 min (f) 30 min at 450 °C in F.G ambient.

In the case the annealing temperature is low (300 °C), large hysteresis was observed for 0.5 minutes annealing (Fig. 3.5 (a)). The hysteresis was improved with annealing for 5 minutes and over (Fig. 3.5 (b),(c)). However, in the case the annealing temperature is high (450 °C), large hysteresis was observed for 30 minutes annealing (Fig. 3.5 (f)). Therefore, the proper characteristics effect on annealing time, are conditional on the annealing temperature.

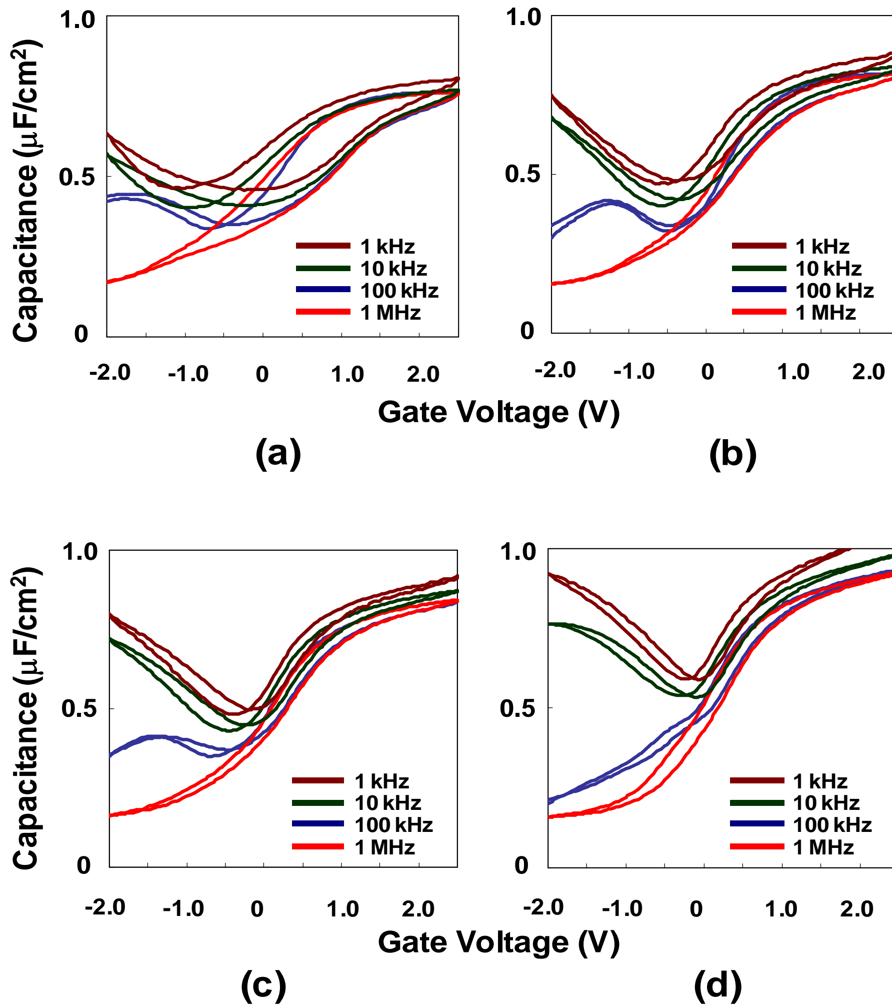
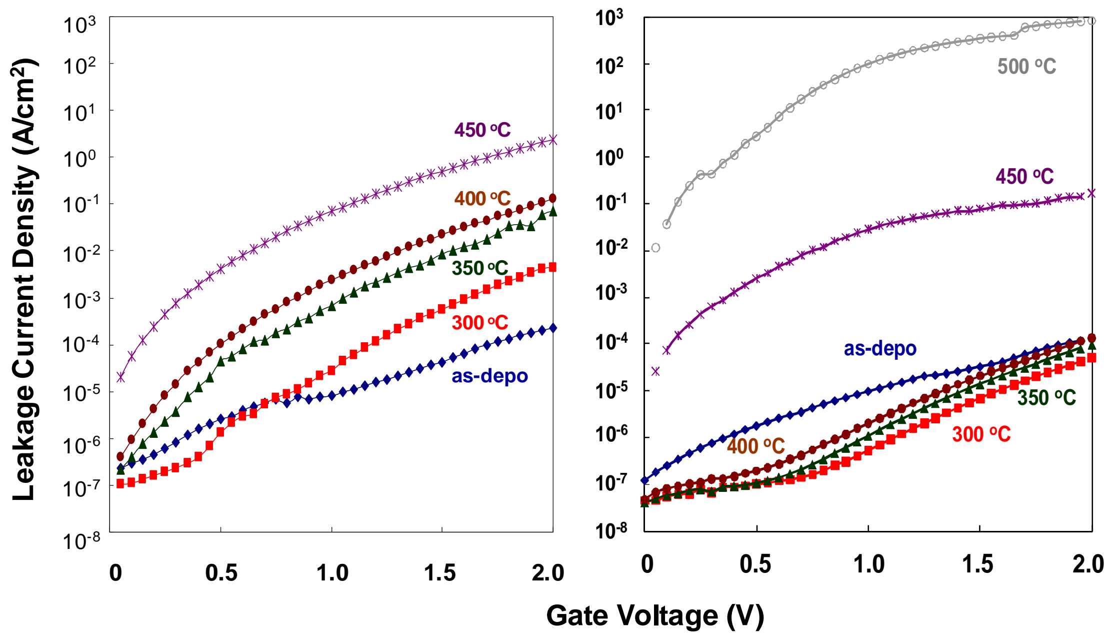


Figure 3.6 *C-V* curves of a 15-nm-thick La_2O_3 layer deposited InGaAs MOS capacitors compared annealing temperature. (a) 300 °C, (b) 350 °C, (c) 400 °C, and (d) 500 °C for 30 sec in F.G ambient.

Figure 3.6 shows *C-V* curves with annealing for 30 seconds. In this annealing time, higher annealing temperature could improve the hysteresis. However, very high annealing temperature (500 °C) caused the effect on leakage current. The effect on leakage current is observed in accumulation at low frequency (1 kHz) in Fig. 3.6 (d). Gate leakage currents on annealing for 30 minutes compared to various thickness of La_2O_3 were shown in Fig.3.7. The leakage current of thinner layer (8 nm) deposited device was dependent on annealing temperature. However, thicker layer (15 or 20 nm) deposited device could suppress the effect on annealing temperature in lower annealing temperature (300 – 400 °C).



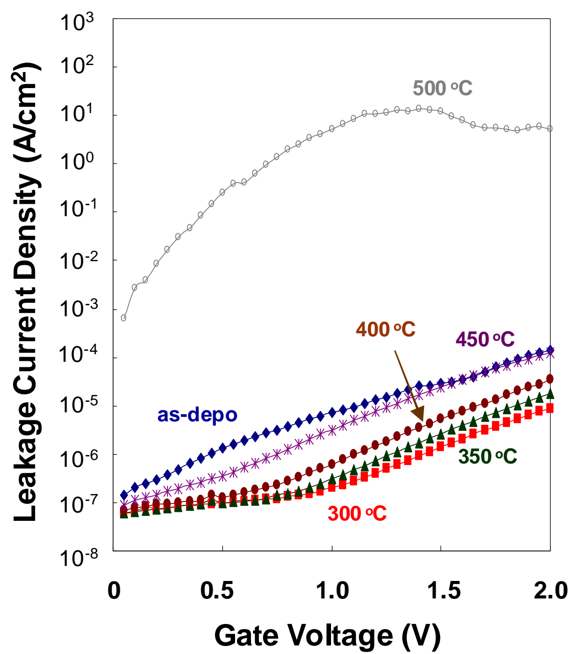


Figure 3.7 Gate leakage currents of (a) 8-nm-thick, (b) 15-nm-thick, and (c) 20-nm-thick La_2O_3 layer deposited InGaAs MOS capacitors compared with annealing temperature for 30 min.

3.2.3 HfO_2 (15 nm)/*n*-type InGaAs MOS capacitors

A 15-nm-thick HfO_2 layer deposited *n*-type InGaAs MOS capacitors were fabricated. Annealing was performed in F.G ambient in the range from 300 to 500 °C for 0.5, 5, or 30 minutes. Figure 3.8 shows *C-V* characteristics with annealing from 300 to 500 °C for 5 minutes, respectively. This insulator thickness might be thinner than 15 nm because the capacitance in accumulation is large. *C-V* characteristics were not improved for increasing annealing temperature. The effect on leakage current is shown at Vg > 1.0 V and Vg < -1.0 V in Fig. 3.8 ((b),(c)). Indeed, the gate leakage current after annealing at the temperature from 300 to 500 °C for 5 minutes as a function of gate voltage increased with increasing annealing temperature (Fig. 3.9).

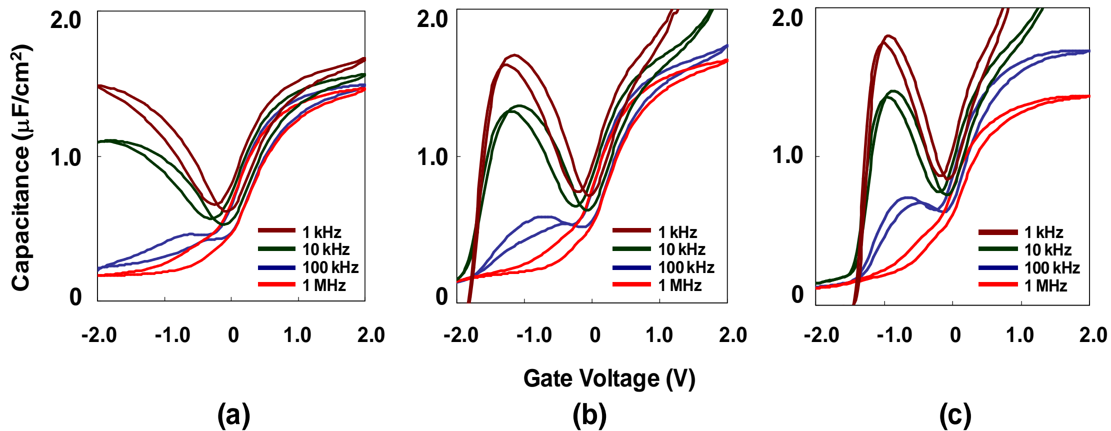


Figure 3.8 *C-V* curves of a 15-nm-thick HfO_2 layer deposited InGaAs MOS capacitors compared annealing temperature. (a) 300 °C, (b) 400 °C, and (c) 500 °C for 5 min in F.G ambient.

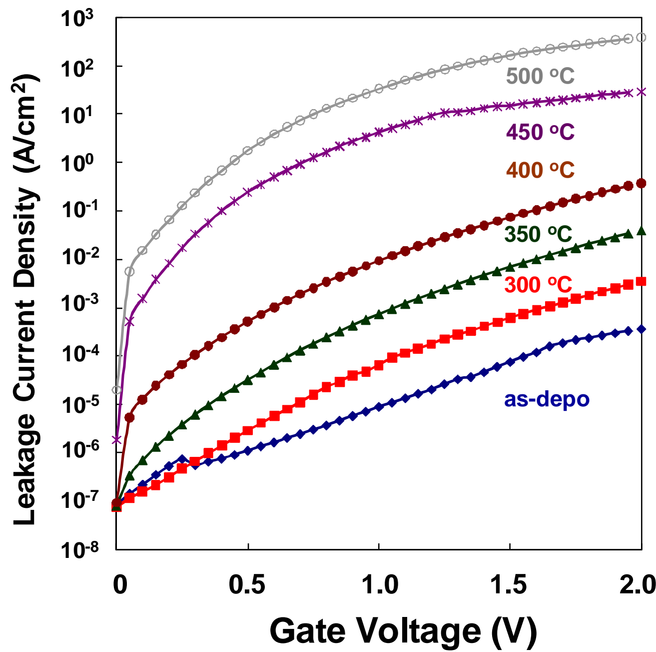


Figure 3.9 Gate leakage currents of a 15-nm-thick HfO_2 layer deposited InGaAs MOS capacitors compared with annealing temperature for 5 min.

On the other hand, an effect of high-*k* layer deposition in O_2 ambient was observed. Figure 3.10 (a)-(b) shows *C*-*V* characteristics of a 15-nm-thick HfO_2 layer deposited in vacuum (~10^{-6} Pa) and in O_2 ambient, respectively. Annealing was performed in F.G ambient at 300 °C for 5 minutes. *C*-*V* characteristics were not improved for deposition in O_2 ambient. Frequency dispersion in Fig 3.10 (b) was larger than that in Fig 3.10 (a). The 1 MHz *C*-*V* curve at $Vg < -1.0$ V in Fig 3.10 (b) was not constant as same as the curve in Fig 3.10 (a). Indeed, interface state densities of deposition in O_2 ambient were higher than that of deposition in vacuum at the annealing range from 300 to 500 °C for 5 minutes (Fig. 3.11).

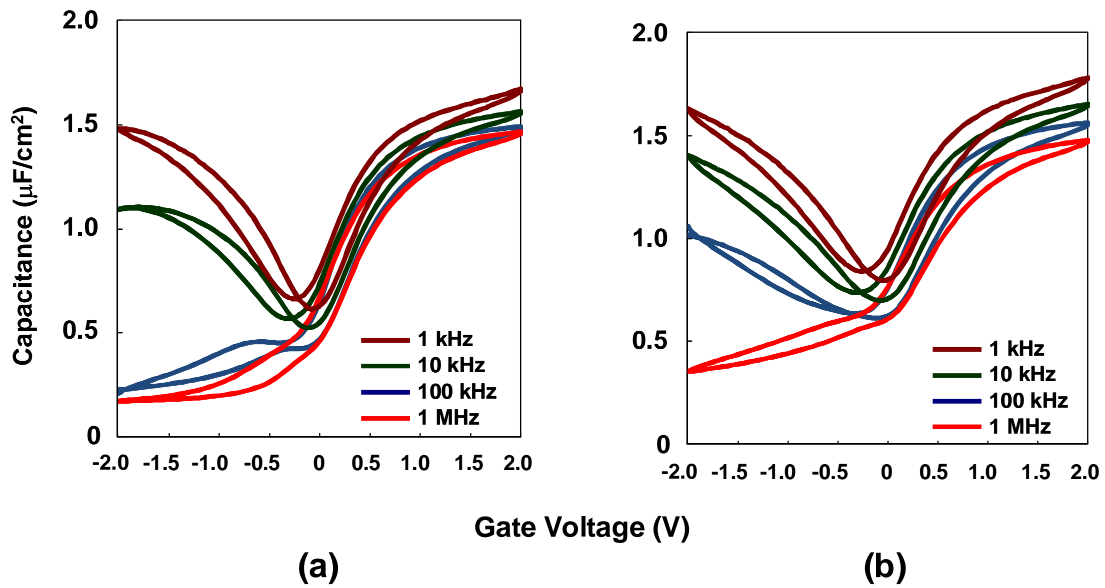


Figure 3.10 *C-V* curves of a 15-nm-thick HfO_2 layer deposited (a) in vacuum (~10^{-6} Pa) (b) in O_2 ambient. Annealing was performed at 300 °C for 5 min in F.G ambient.

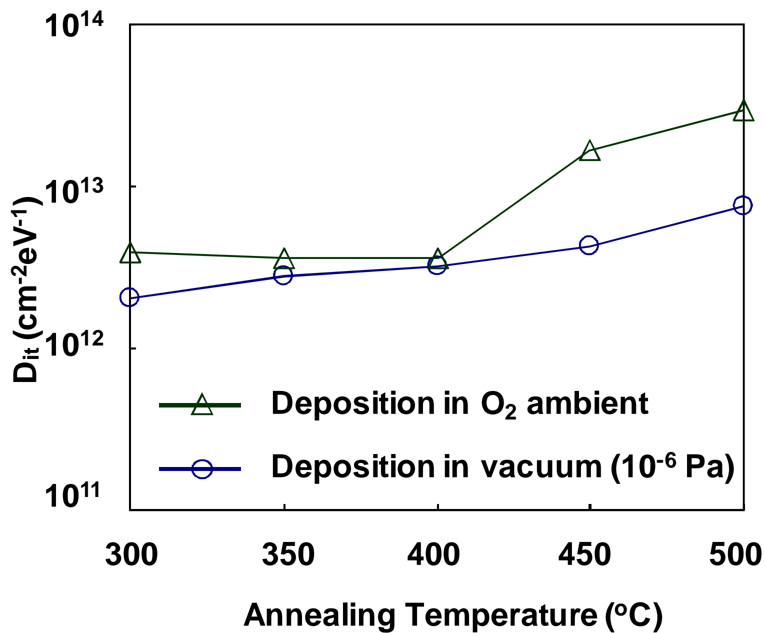


Figure 3.11 Interface state densities of a 15-nm-thick HfO_2 layer deposited in vacuum (~10^{-6} Pa) and in O_2 ambient compared with annealing for 5 min in F.G ambient.

3.2.4 High-*k* (20 nm)/*p*-type InGaAs MOS capacitors

A 20-nm-thick La_2O_3 or HfO_2 layer deposited *p*-type InGaAs MOS capacitors were fabricated. Annealing was performed in F.G ambient in the range from 300 to 500 °C for 0.5, 5, or 30 minutes. Figure 3.12 shows *C-V* characteristics with annealing at 300 and 450 °C for 30 minutes, respectively. The insulator thickness of HfO_2 might be thinner than 20 nm because the capacitance in accumulation is large. Frequency dispersion with HfO_2 as the gate dielectric (Fig. 3.12 (c),(d)) is larger than that with La_2O_3 as the gate dielectric (Fig. 3.12 (a),(b)). The frequency dispersion at higher annealing temperature (Fig. 3.12 (b),(d)) is larger than that at lower annealing temperature (Fig. 3.12 (a),(c)). The *C-V* characteristics of *p*-type InGaAs MOS capacitors with La_2O_3 or HfO_2 as the gate dielectrics is behind in that of *n*-type InGaAs MOS capacitors discussed in section from 3.2.1 to 3.2.3. One of the reasons may be the effect on impurity differences. *N*-type InGaAs was doped Si, on the other hand, *p*-type InGaAs was doped Zn so that the proper annealing condition of *p*-type InGaAs is different from that of *n*-type InGaAs.

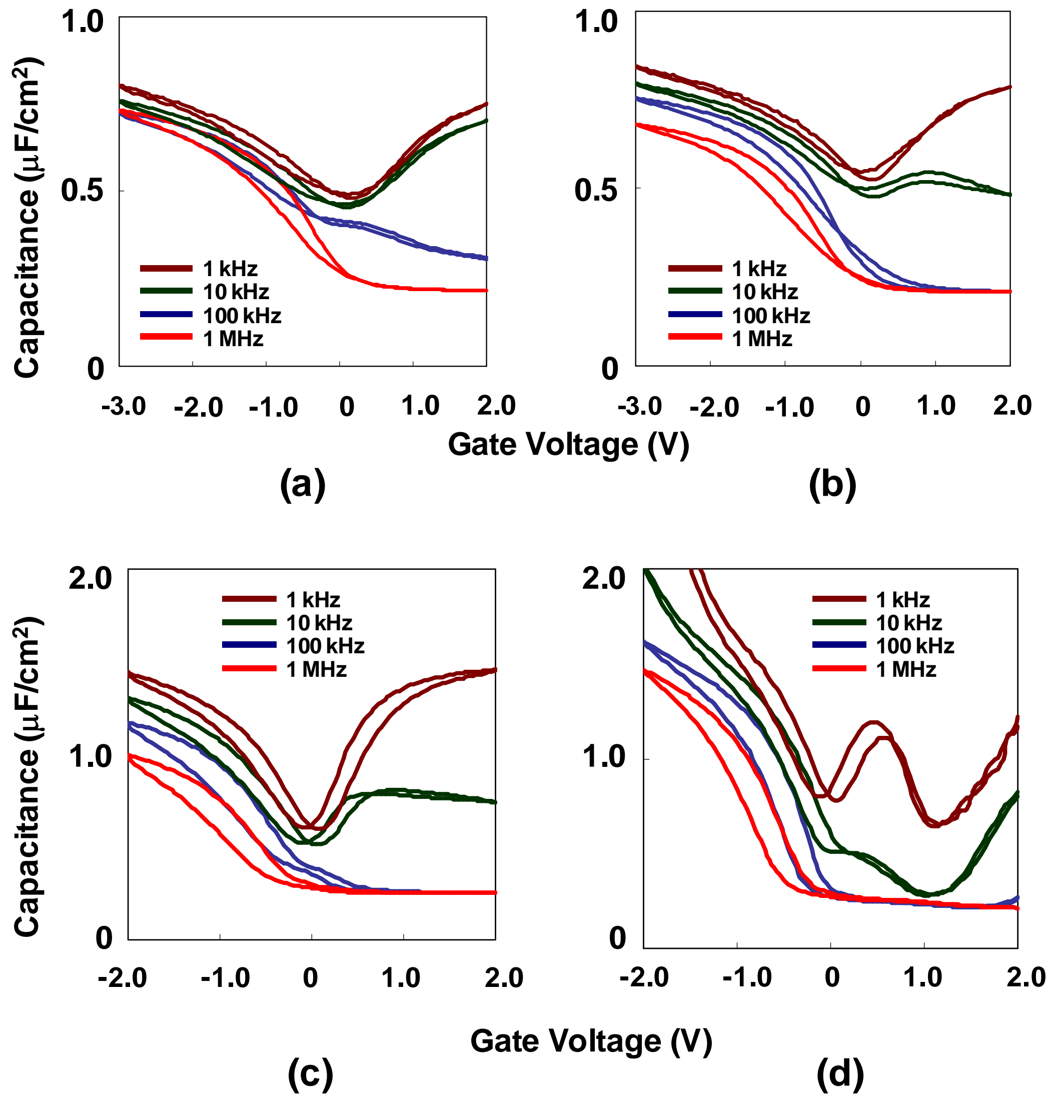


Figure 3.12 *C-V* curves of a 20-nm-thick La_2O_3 or HfO_2 layer deposited InGaAs MOS capacitors compared annealing temperature.
(a) 300 ^oC (b) 450 ^oC for 30 min with La_2O_3
(c) 300 ^oC (d) 450 ^oC for 30 min with HfO_2.

3.2.5 HfO_2 (10 nm)/La_2O_3 (2nm)/ *n*-type InGaAs MOS capacitors

InGaAs MOS capacitors deposited a 10-nm-thick HfO_2 layer and a 2-nm-thick La_2O_3 layer were annealed in F.G from 300 °C to 500 °C for 5 minutes. Figure 3.13 shows *C-V* characteristics after annealing at 400 °C for 5 minutes. Frequency dispersion and influence of leakage current were observed.

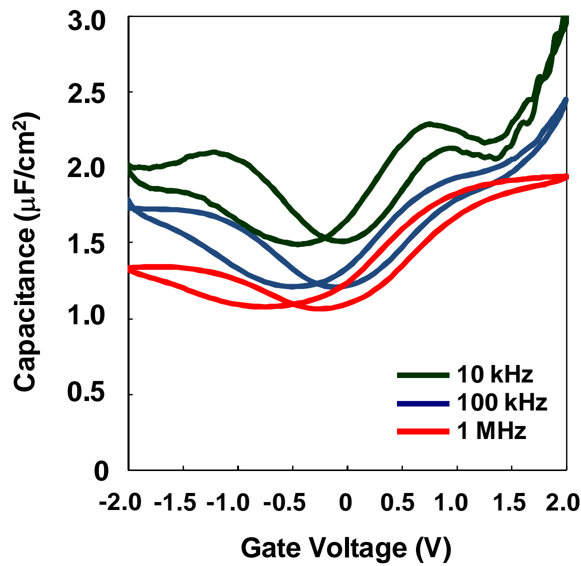


Figure 3.13 *C-V* curves of HfO_2 (10nm)/La_2O_3 (2nm)/InGaAs MOS capacitor after annealing at 400 °C for 5 min in F.G ambient.

3.3 Interface state density (D_{it})

Interface state density (D_{it}) was measured by conductance method discussed in section 2.3.3. The valid energy of measurement by the method is depletion region of MOS capacitors. Variation of total charge density for an *n*-type $In_{0.53}Ga_{0.47}As$ MOS capacitor is shown in Fig. 3.14. Depletion region is from Fermi energy to intrinsic Fermi energy, theoretically.

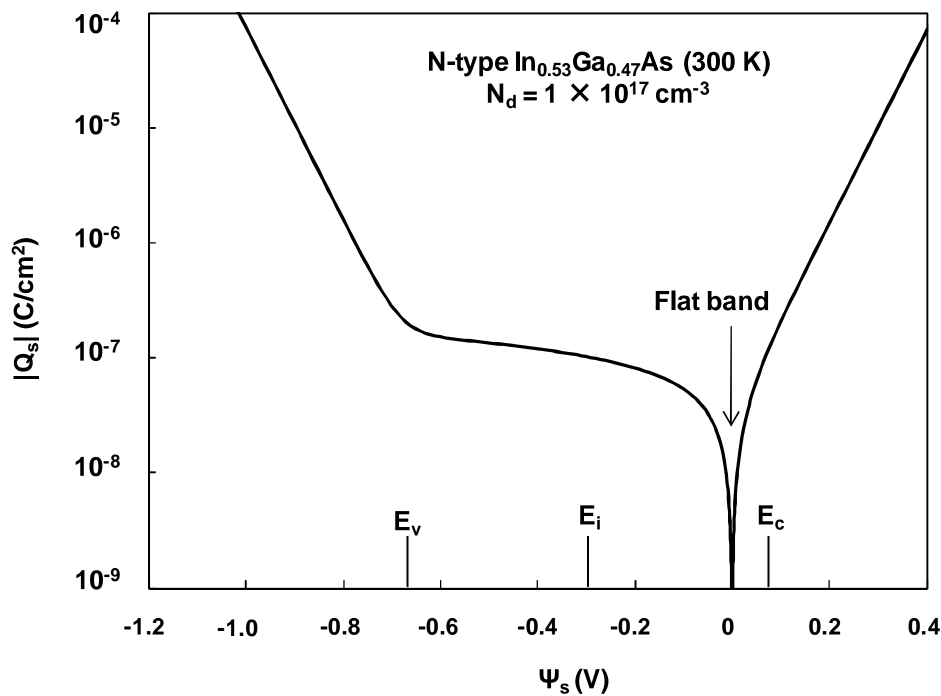


Figure 3.14 Variation of total charge density in $In_{0.53}Ga_{0.47}As$ as a function of surface potential Ψ_s for an *n*-type MOS device.

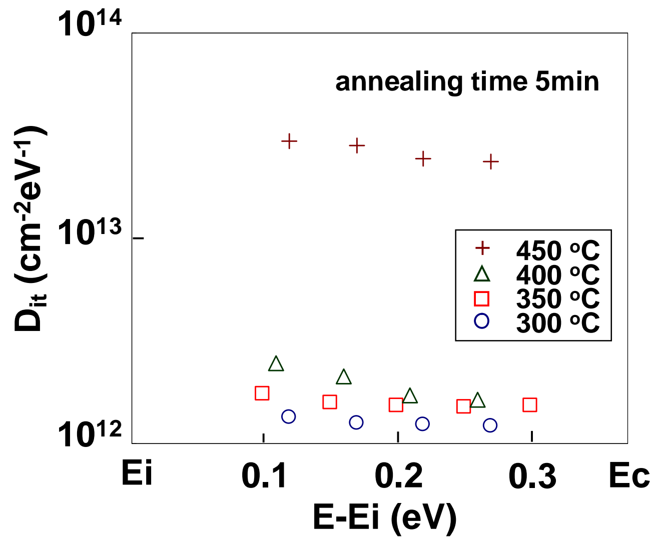


Figure 3.15 Interface state distribution of La_2O_3 (8 nm)/InGaAs MOS capacitors depending on annealing temperature. The annealing were performed in F.G ambient at the range of 300 - 450 °C for 5min.

Figure 3.15 shows distribution of D_{it} for the La_2O_3 (8 nm)/InGaAs MOS capacitor annealed in forming gas at temperature from 300 to 450 °C for 5 minutes. D_{it} was extracted by conductance method. The smallest D_{it} of 10^{12} $cm^{-2}eV^{-1}$ was obtained by annealing at 300 °C. D_{it} gradually increases with increasing the annealing temperature. However, when annealed at 450 °C, D_{it} exhibits a dramatic increase above 10^{13} $cm^{-2}eV^{-1}$. Dependence of D_{it} on annealing temperature and annealing are shown in Fig. 3.16. When the annealing time is longer, lower D_{it} is obtained at 300 °C and 350 °C. D_{it} increases by annealing at 400 °C for 30 minutes. However, the degradation of D_{it} can be suppressed by shortening the annealing time. In summary, low annealing temperature (300 - 350 °C) in addition to long annealing time (30 minutes) is preferable to reduce D_{it}. The smallest value of 1.1×10^{12} $cm^{-2}eV^{-1}$ is obtained by annealing at 300 °C for 30 minutes.

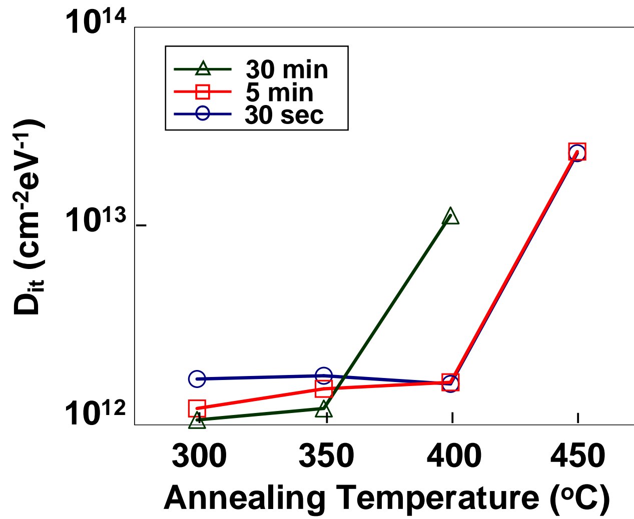


Figure 3.16 Interface state densities of La_2O_3 (8 nm)/InGaAs MOS capacitors depending on annealing temperature and annealing time.

Figure 3.17 (a) and (b) shows values of D_{it} for the InGaAs MOS capacitor with 15-nm-thick La_2O_3 and HfO_2 annealed in forming gas at temperature from 300 to 500 °C, respectively. D_{it} of low annealing temperature (300 – 350 °C) in 5 or 30 minutes were lower than that of high annealing temperature (400 – 500 °C). In addition, D_{it} of short time annealing (30 seconds) was higher than that of long time annealing (5 and 30 minutes). Compared the both graphs, the capacitor with La_2O_3 was obtained lower D_{it} at 300 °C and 350 °C for long time annealing (5 and 30 minutes). Therefore, interface characteristics of the capacitor with La_2O_3 were better than that with HfO_2.

On the other hand, D_{it} of the *p*-type MOS capacitors discussed in section 3.2.4 has not been calculated. *C*-*V* curves in accumulation of the capacitors had large frequency dispersion so that it is hard to calculate the D_{it}, correctly.

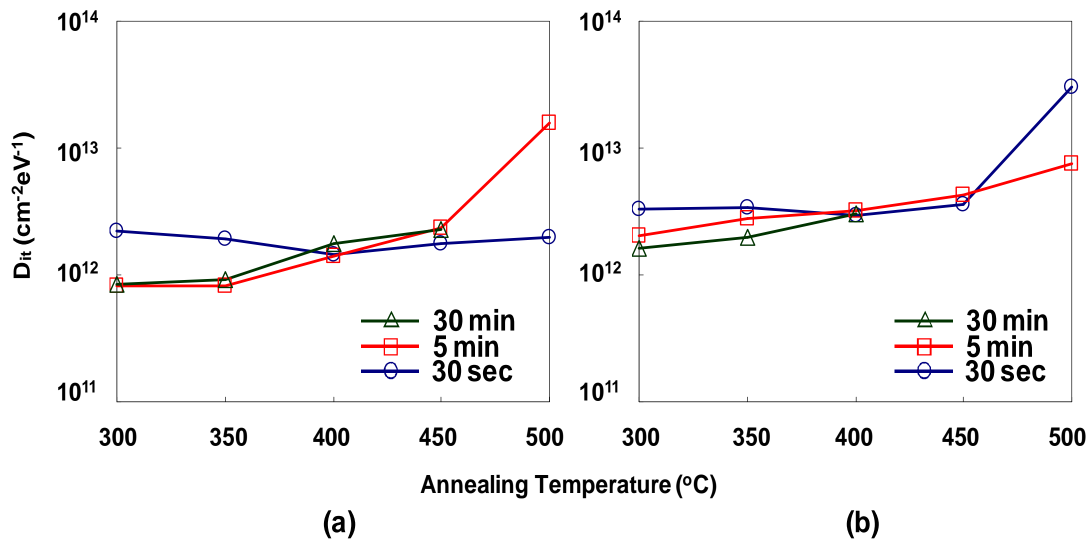


Figure 3.17 Interface state densities of InGaAs MOS capacitors with 15-nm-thick (a) La_2O_3 and (b) HfO_2 as the gate dielectrics depending on annealing temperature and annealing time.

Chapter 4.

Conclusion

4.1 Conclusion of this study

The purpose of this study was to improve interface characteristics of the interface between high-*k* layer and InGaAs substrate. Electrical characteristics (*C*-*V* curves, leakage currents, and interface state densities) of $In_{0.53}Ga_{0.47}As$ MOS capacitors with La_2O_3 and HfO_2 as the gate dielectrics were measured. This study compared various annealing temperature and annealing time. Lower annealing temperature of 300 - 350 °C and long annealing time from 5 to 30 minutes were preferable for reducing D_{it}. In addition, the leakage currents of devices annealing low temperature (300 - 350 °C) were comparatively suppressed, and the leakage currents hardly depend on annealing time at all. Therefore, in the case of higher annealing temperature, hysteresis was improved and capacitance was higher but leakage current was increased. On the other hand, in the case of longer annealing time, *C*-*V* characteristics were improved with suppress leakage current increased. D_{it} of the capacitors with La_2O_3 as the gate dielectrics was better than that with HfO_2 as the gate dielectrics. The fabrication process of the high-*k* layer deposition in O_2 ambient could not improve the interface characteristics.

4.2 Extension of this study

This study was compared annealing temperature and annealing time. The *C-V* curves still had hysteresis and frequency dispersion so that the improvement of them is necessary. The frequency dispersion is very important problem of InGaAs MOS devices. In addition, D_{it} which values were from10^{12} to 10^{13} $cm^{-2}eV^{-1}$ was still high, and it is need to be smaller. New studies such as surface cleaning for $(NH_4)_2S$ on the InGaAs substrate, annealing in other gas ambient, and so on will be necessary in the future.

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