**Doctorial Thesis**

# A Study on High-Frequency Performance in MOSFETs Scaling

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*To my father, a physicist.*

*You inspired my interest in science.*

# Chapter.1

# Introduction

# – Background and Motivation of This Study

## 1.1 Field Effect Transistor Technology

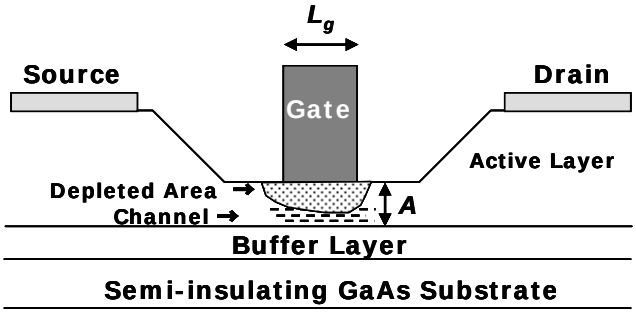
The Si-MOSFET has been traditionally regarded a slow device not suitable for RF applications. The main reason is that the electron mobility in silicon is by nature lower than in III-V compounds devices. In 1990s, the field of RF transistors has been dominated by III-V transistors. The commercially available Si-based RF transistor was the Si-bipolar transistor for application in the lower GHz range. However recent aggressive downsizing of CMOS devices has improved its RF characteristics significantly and some of them have already exceeded some of Si-bipolar and GaAs transistors. The situation changed dramatically and Si-MOSFETs became widely accepted RF devices. [1-1, 1-2, 1-3]

In this section, Field Effect Transistor (FET) is focused and its performance trends are discussed. Figure 1-1 shows the cross-section of three FET devices: a gallium arsenide (GaAs) metal-semiconductor FET (MESFET), a III-V high-electron mobility transistor (HEMT) and a silicon MOSFET. $L_g$ is the gate length and $A$ is the gate-to-channel distance.

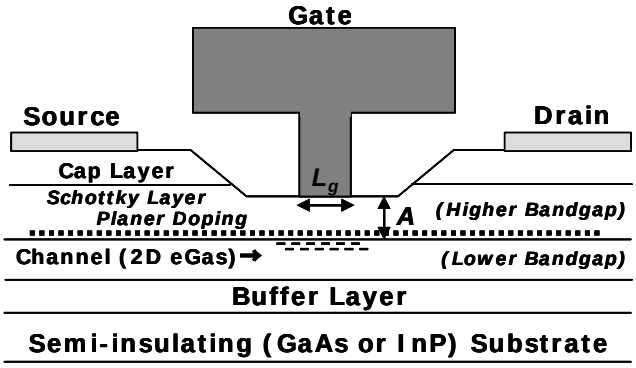
The first FET is the GaAs MESFET, first developed during the 1970s and 1980s. A gate Schottky contact is directly realized on the active channel layer. FET technology continued to improve with the development of III-V HEMT during the early 1980s. In this technology, a heterojunction is built up through the

association of a doped Schottky barrier layer with a channel layer (the Schottky barrier layer has the higher bandgap). This system offers high flexibility in terms of channel engineering; the semi-insulating substrate is either GaAs or indium phosphid (InP). The channel is formed by a two-dimensional electron gas, separated from the ionized doping atoms from which they were released, and electron transport is improved in comparison to the GaAs MESFET.

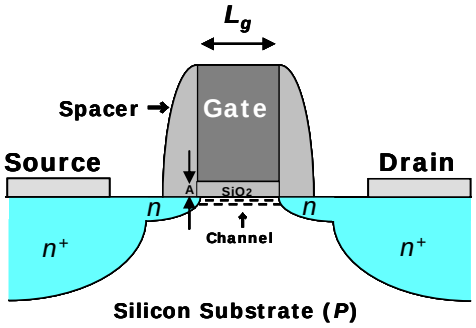
During GaAs MESFET and III-V HEMT technologies have evolved, silicon MOSFET performance also kept improving, with the main focus to digital applications. A silicon MOSFET is fabricated using a self-aligned process: a polysilicon gate is deposited on the oxide ($SiO_2$), followed by the formation of spacers that are used to realize diffused source/drain contacts. The channel charge is formed at the interface oxide/silicon for a DC gate-to-source voltage higher than the threshold voltage, $V_{th}$. [1-4]




(a) GaAs MESFET




(b) III- V HEMT




(c) silicon MOSFET

*Fig.1-1. Cross section for various FET.*

*(a) GaAs MEFET (b) III- V HEMT (c)silicon MOSFET*

## 1.2 Performance Trends of RF transistors

Figure 1-2 shows the reported cutoff frequencies, $f_T$, and maximum frequencies of oscillation, $f_{max}$ of Si MOSFETs and other III-V FETs as a function of time. The $f_T$ and $f_{max}$ data vs. time plots clearly indicate that the frequency limits of the Si-based and of the III-V RF transistor have been enhanced continuously. Sub-100 nm gate MOSFETs showing both cutoff frequencies and maximum frequencies of oscillation well in excess of 100 GHz as well as low noise figures have been reported. Figure 1-3 shows the cutoff frequency; $f_T$ and maximum frequency of oscillation; $f_{max}$ of experimental Si-MOSFETs as a function of gate length. The $f_T$ and $f_{max}$ of GaAs MESFETs, GaAs pHEMTs, and InP HEMT are also included. The best record of $f_T$ and $f_{max}$ at 2010 are:

$f_T$ =628 GHz [1-61] for 30nm-InAs/InP HEMTs and $f_{max}$ =1 THz [1-58] for 50nm-InP HEMTs ,

$f_T$=485 GHz [1-26] and $f_{max}$ =410 GHz [1-31] for 40nm-Si MOSFETs.

Currently GaAs pHEMTs are the most popular commercial GaAs-based RF FETs. They outperform the traditional GaAs MESFETs and AlGaAs/GaAs HEMTs in terms of speed and noise performance. Figure 1-2(b) shows that no clear gate length dependence could be observed. While $f_T$ can be increased by

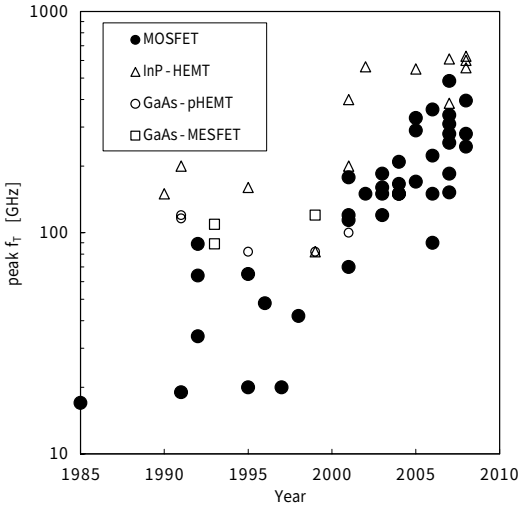
scaling down the gate length, $f_{max}$ depends strongly on not only gate length, but also the parasitic components. So, much work has been done to optimize the design of Si RF-MOSFETs, especially the gate design, and to improve their RF performance. The MOSFET with the highest $f_{max}$ at that time has been a 0.3-μm gate transistor showing an $f_{max}$ of 37 GHz and a rather low $f_T$ of 20 GHz [see chapter 3].

During the past few years, also the noise performance of Si RF MOSFETs has been improved considerably. Figure 1-4 shows the best reported minimum noise figures of Si MOSFETs and other FETs as a function of frequency. It is clear from this plot that the use of low noise GaAs MESFET technology is mainly limited to applications in the centimeter wavelength range ($f_T$ < 30 GHz); the reason for which is closely related to $g_m$ (respectively $f_T$), which limits $NF_{min}$. Note that an excellent result was achieved in [1-38]. Later, during the early 1980s, HEMT technology had been developed, allowing applications in the centimeter/millimeter wavelength range to be addressed; the use of the heterojunction leads to an increase in channel mobility and $f_T$, which can further be improved through channel engineering.

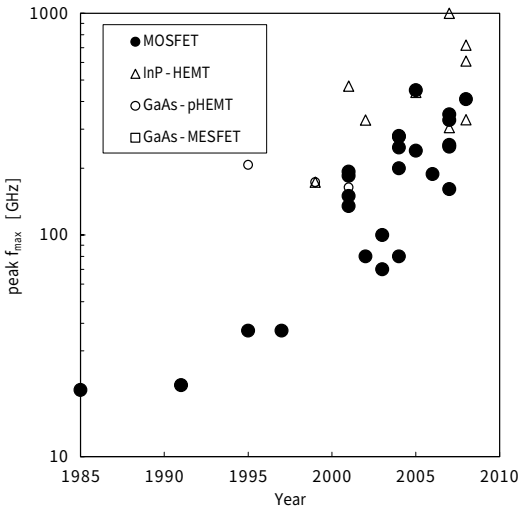
The first heterojunction-based FET (GaAs pHEMT) technology can achieve a $NF_{min}$ around 2.3 dB at 94 GHz [1-39] ($L_g$ =0.1 μm, $f_T$ =120 GHz). To obtain such a performance, gate resistance and source resistance have been optimized, as well as the device aspect ratio $L_g/A$.

Though the $NF_{min}$ of a GaAs pHEMT already enables good low-noise performance, it still too high to address a number of important applications in W(75-110 GHz) and G (140-220 GHz) bands, respectively. For such applications, the best low noise FET technology is InP HEMT, which is also illustrated in Fig.1-4. This technology performs better than GaAs pHEMT technology, achieving $NF_{min}$ of 1.4 dB [1-47] at 95 GHz, and $f_T$ =150 GHz. While $L_g$=0.15 μm in[1-47] is larger than for the GaAs pHEMT [1-39], the technology benefits from higher $f_T$ values. InP HEMT the best low-noise technology currently.

As shown in Fig.1-4, silicon MOSFETs technology features good $NF_{min}$ . The lowest noise figures are below 0.5 dB up to 26 GHz [1-15]. This is sufficiently low for many applications, but does not outperform GaAs pHEMT despite an aggressive gate length downscaling [1-15]. Nevertheless, the enhanced RF performance of Si MOSFETs obtained recently make these devices very attractive for many RF applications in the lower GHz range. Especially in market segments where high-level integration is required, Si MOSFETs are serious competitors to other RF transistors, such as III-V HEMTs. Si RF-MOSFETs are in high-volume production and are widely used in commercial products.

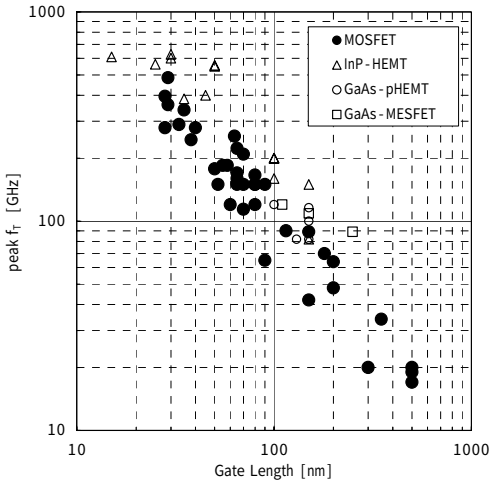



*(a) Cutoff frequency, $f_T$*

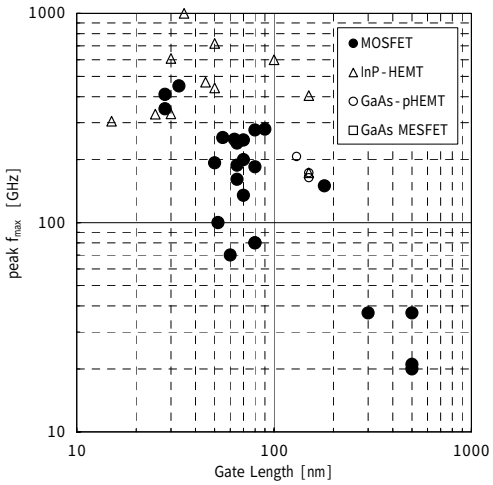



*(b) Maximum frequency of oscillation, $f_{max}$*

*Fig.1-2. Evolution of (a) the cutoff frequency, $f_T$ and (b) the maximum frequency of oscillation, $f_{max}$ of different RF transistor technologies.*




*(a) Cutoff frequencies; $f_T$*




*(b) Maximum frequency of oscillation; $f_{max}$*

*Fig.1-3. Reported (a) cutoff frequencies; $f_T$ and (b)maximum frequency of oscillation; $f_{max}$ for RF Si-MOSFETs, InP-pHEMTs, GaAs-pHEMTs and GaAs-MESFETs as a function of gate length.*

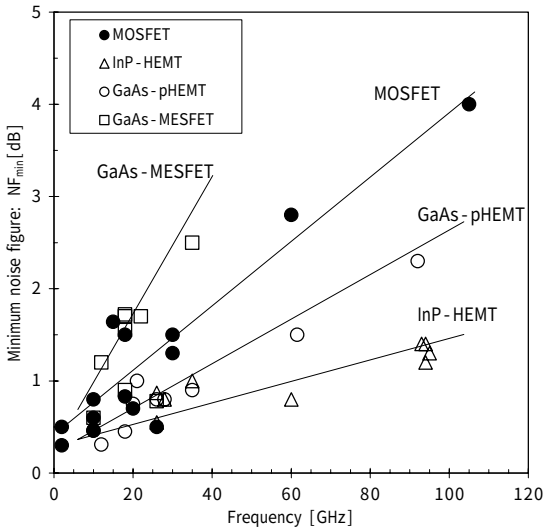



*Fig.1-4. Reported minimum noise figure; $NF_{min}$ for RF Si-MOSFETs, InP-pHEMTs, GaAs-pHEMTs and GaAs-MESFETs as a function of frequency.*

## 1.3. Objective and Organization of This Study

In order to realize the low-cost and high-performance RF mixed signal system-on-chip, a deeper understanding of the scaling effects on RF-MOSFETs is significantly important.

The objective of this study is to investigate the scaling effects on the high frequency performance of MOSFETs.

The thesis consists of seven chapters, as illustrated in Fig.1-5. Following this chapter, chapter 2 described AC S-parameter measurements, high-frequency noise measurements, large-signal measurements, and two-tone intermodulation distortion measurements.

In chapter 3, a novel and practical configuration of MOSFETs to attain remarkable high frequency performance was proposed by using a 0.25 μm CMOS technology and the parasitic effect of Si-MOSFETs for high frequency performance was also discussed.

In chapter 4, it was studied that the scaling effects from the 150 nm node to the 65 nm node on RF CMOS devices which are basically made of logic CMOS process without any change. The purpose of the study is to confirm the suitability of the 65 nm logic CMOS for RF application. In particular, RF characteristics -- such as cut-off frequency ($f_T$), maximum oscillation frequency ($f_{max}$), minimum noise figure ($F_{min}$), intrinsic gain ($g_m/g_{ds}$), peak power-added

efficiency (*PAE*), 1dB compression point ($P_{1dB}$), third order inter-modulation distortion ($IM_3$), and third order intercept point ($IP_3$) -- of the 65 nm RF mixed signal CMOS were compared with those of the 150 nm CMOS. The gate layout dependence on the RF performance has been also investigated.

In chapter 5, The RF noise parameter ($F_{min}$, $R_n$, $\Gamma_{opt}$) of 45 nm node MOSFETs were measured from 5 to 15 GHz. Then, the noise values — the drain channel noise $\overline{i_d^2}$, the induced gate noise $\overline{i_g^2}$ and their correlation noise $\overline{i_g i_d^*}$ — from S-parameters and noise parameters were extracted by using noisy two-port theory. Next, the noise coefficients *P*, *R*, and *C* were extracted by using an extended van der Ziel's model. After that, the extracted noise coefficients of the 45 nm node MOSFETs versus frequency, bias condition, and gate length are presented. Finally, the effect of noise coefficients on noise figure is discussed.

In chapter 6, a novel representation of the thermal noise for equivalent noise temperature was proposed by applying an extended van der Ziel's model. The noise temperatures of the 45 nm node n-MOSFETs versus gate length were extracted. A comparison between the proposed representation and Pospieszalski's model is also performed. Finally, a physical validity of proposed representation for equivalent noise temperature was discussed, especially for drain noise temperature, $T_d$.

Finally, in chapter 7, the studies referred to in this thesis are summarized and their importance is described.

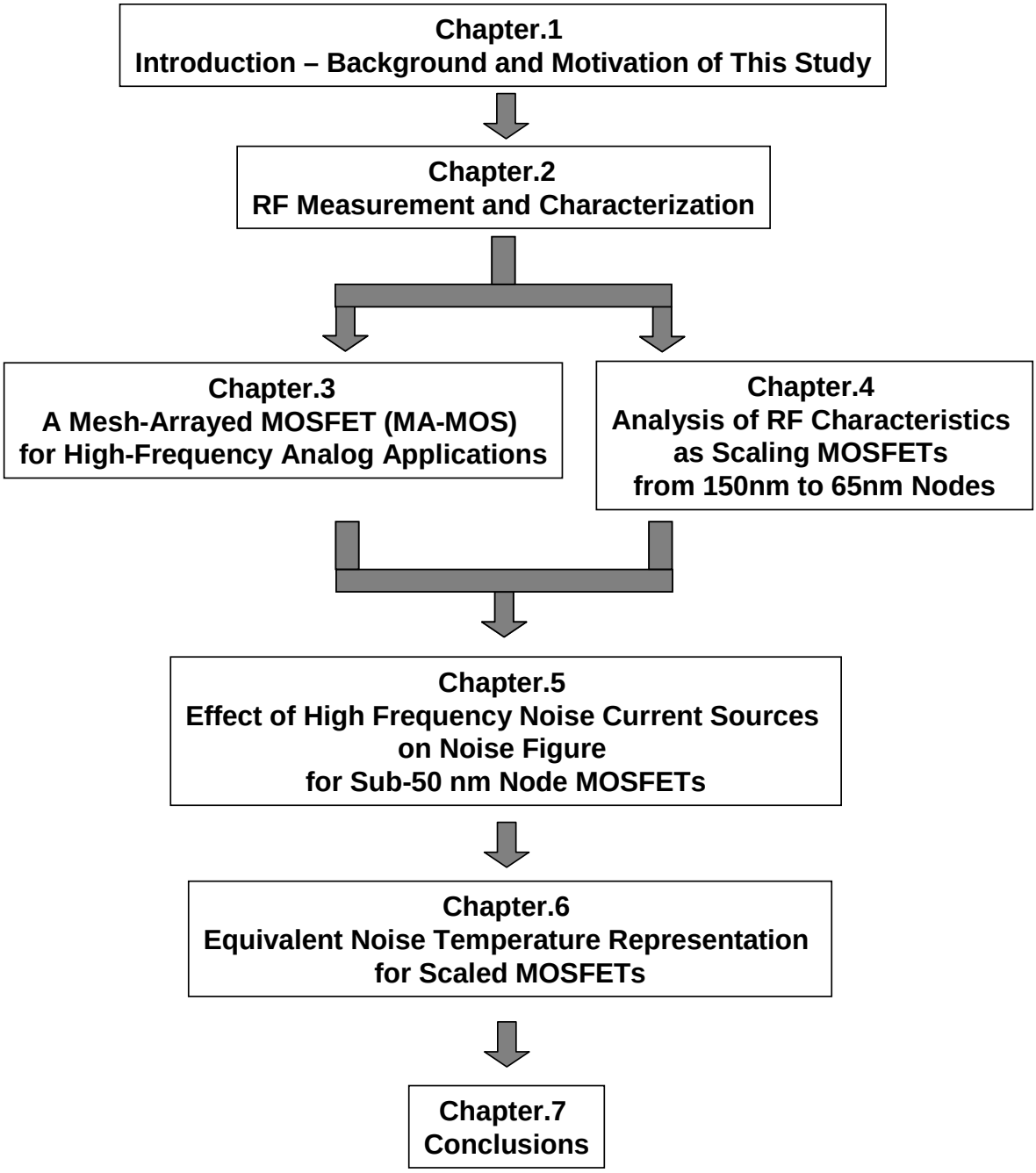



*Fig.1-5. Outline and organization of this study.*

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# Chapter.2

# RF Measurement

# and Characterization

## 2.1 Introduction

RF measurement and characterization are a very important step in the development of device design, characterization and modeling. While the characterization of electronic components in the DC domain only requires a voltmeter and an amperemeter, the frequency performance is affected by magnitude dependence and phase shift of the currents and voltages. In this chapter, AC S-parameter measurements, high-frequency noise measurements, large-signal measurements, and two-tone intermodulation distortion measurements are described.

## 2.2 AC S-parameter Measurements

### 2.2.1 De-embedding Techniques using The OPEN and The SHORT Dummy Device

For on-wafer device characterization, using G-S-G (ground-signal-ground) probes, the test pads degrade the performance of the very inner "DUT" (device-under-test) by their layout specific capacitive and inductive pad parasitics. In order to extend the calibration plane to the inner DUT, these outer parasitics effects have to be stripped off. This is called *de-embedding*. A method to also strip

off the series parasitic influence from the measured data is to de-embed the inner DUT from both the "OPEN" and "SHORT" dummy device. Figure 2-1 indicates the layouts of a DUT and dummy structures used in the method based on the parallel-series configuration. The OPEN dummy structure consists of the signal pads and interconnections without the transistor. The SHORT dummy structure consists of the signal pads and interconnections except with shorted interconnections at the location of the transistor.

The idea behind this method is, that the electrical behavior of the pads around the DUT can be described by a combination of exclusively parallel (OPEN) and exclusively serial (SHORT) circuit elements as described in Fig.2-2(a).

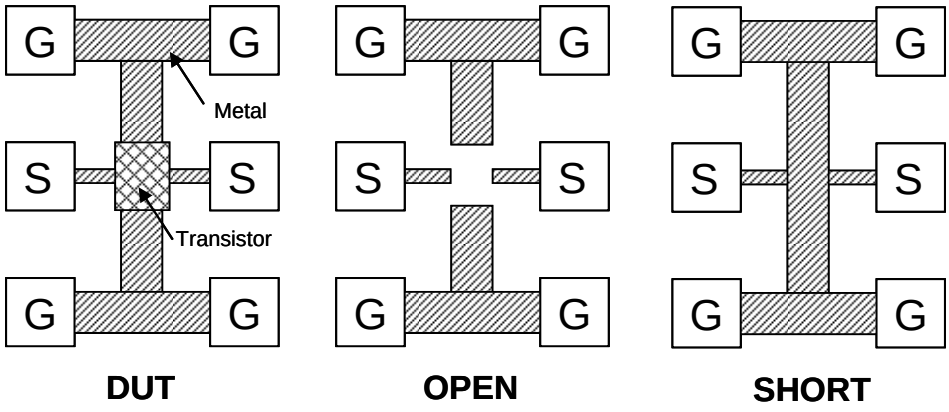
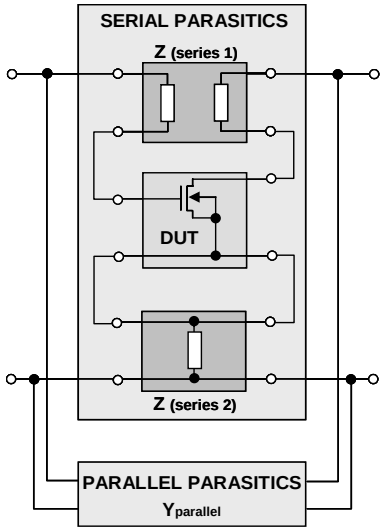
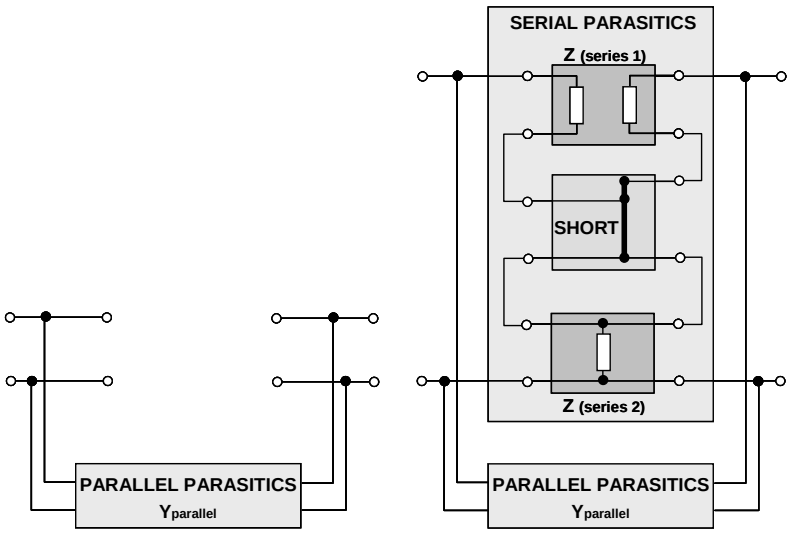



*Fig.2-1. A device-under-test (DUT) and its corresponding "OPEN" and "SHORT" dummy structures for the DUT modeled in the parallel-series configuration.[2-5]*




*(a) Device*




*(b) "OPEN" dummy* *(c)"SHORT" dummy*

*Fig.2-2. For"OPEN" and "SHORT" dummy device de-embedding using Y- and Z-matrix subtraction.[2-5]*

Figure 2-2(b) and (c) indicates Y- and Z-matrix components of the OPEN and the SHORT dummy device. Looking at Fig.2-2(a), the schematic of the SHORT dummy device, how the matrices of the serial and parallel parasitic elements can be determined:

(1) Parallel elements:

The S-to-Y converted S-parameters of the OPEN dummy give the Y-parameters of the parallel elements.

(2) Serial elements:

The Z-parameters of the serial elements can be determined from the SHORT dummy when the Y-parameters of the parallel elements are known and de-embedded.

With this pre-assumption, the de-embedding can be performed following these matrix operations:

De-embed from OPEN:

$$Y_{DUT/Open} = Y_{Total} - Y_{Open}$$
$$Y_{Short/Open} = Y_{Total} - Y_{Open}$$

Convert to Z:

$$Z_{DUT/Open} = Z(Y_{DUT/Open})$$
$$Z_{Short/Open} = Z(Y_{Short/Open})$$

De-embed from SHORT:

$$Z_{DUT} = Z_{DUT/Open} - Z_{Short/Open}$$

Convert to S:

$$S_{DUT} = S(Z_{DUT})$$

In a first step, the influence of the parallel parasitic elements is removed from both the SHORT and DUT. This is done by subtracting the Y-parameters of the OPEN from the Y-parameters of the SHORT and DUT. In the following step, the resulting Y-parameters are converted to Z-parameters and in this representation, the influence of the serial parasitic elements is removed by subtracting the de-embedded Z-parameters of the SHORT from the de-embedded Z-parameters of the DUT. The resulting Z-parameters of the DUT are then finally converted back to S-parameters.

### 2.2.2 Cutoff Frequency, $f_T$

S-parameter measurements are used to calculate two important figures of merit for transistors: the cutoff frequency of the AC-current gain, $f_T$, and the cutoff frequency of the maximum power gain, also called the maximum oscillation of frequency, $f_{max}$.

To calculate $f_T$, the S-parameters are converted to H-parameters and, in graphical terms, the AC current gain, $|H_{21}|$ (in dB), is plotted on a linear scale as a function of frequency on a log scale. The $f_T$ of the transistor is the point at which $|H_{21}|$ crosses the x-axis. The $|H_{21}|$ curve is assumed to have perfect single-pole, 20-dB/decade, roll-off characteristics. The $f_T$ is calculated using the base transit time $\tau_T$, where

$$\tau_T = \left| \frac{\sin \angle H_{21}}{|H_{21}|\omega} \right| . \tag{2-1}$$

Then $f_T$ is given by

$$f_T = \frac{1}{2\pi\tau_T} . \tag{2-2}$$

### 2.2.3 Maximum Oscillation Frequency, $f_{max}$

In 1954, Mason defined a *unilateral power gain* for a linear two-port, and discussed some of its properties [2-3, 2-4]. The unilateral power gain $U$ is the maximum power gain that can be obtained from the two-port, after it has been

made unilateral with the help of a lossless and reciprocal embedding network (which provides the required feedback).

Mason defined the problem as "being the search for device properties that are invariant with respect to transformations as represented by an embedding network" that satisfy the four constraints listed below [2-4].

1.The embedding network is a four-port.

2.The embedding network is linear.

3.The embedding network is lossless.

4.The embedding network is reciprocal.

Mason showed that all transformations that satisfy the above constraints can be accomplished with just three simple transformations performed sequentially. Similarly, this is the same as representing an embedding network by a set of three embedding networks nested within one another. The three mathematical expressions can be seen below.[2-4]

1. Reactance padding: $\left[Z - Z_t\right]$ and $\left[Z + Z^*\right]$

2. Real transformations: and $\left[Z - Z_t\right]\left[Z + Z^*\right]$ and $\dfrac{\det\left[Z - Z_t\right]}{\det\left[Z + Z^*\right]}$

3. Inversion: The magnitudes of the two determinants and the sign of the denominator in the above fraction remain unchanged in the inversion transformation. Consequently, the quantity invariant under all three conditions is:

$$U = \frac{\left|\det\left[Z - Z_t\right]\right|}{\det\left[Z + Z^*\right]} \tag{2-3a}$$

$$= \frac{\left|Z_{12} - Z_{21}\right|^2}{4\left(\Re\left[Z_{11}\right]\Re\left[Z_{22}\right] - \Re\left[Z_{12}\right]\Re\left[Z_{21}\right]\right)} \tag{2-3b}$$

$$= \frac{\left|Y_{21} - Y_{12}\right|^2}{4\left(\Re\left[Y_{11}\right]\Re\left[Y_{22}\right] - \Re\left[Y_{12}\right]\Re\left[Y_{21}\right]\right)} \tag{2-3c}$$

While Mason's unilateral power gain can be used as a figure of merit across all operating frequencies, its value at $f_{max}$ is especially useful. $f_{max}$ is the maximum oscillation frequency of a device, and it is defined when $U(f_{max}) = 1$. This frequency is also the frequency at which the maximum stable gain; *MSG* and the maximum available gain; *MAG* of the device become unity. Consequently, $f_{max}$ is a characteristic of the device, and it has the significance that it is the maximum frequency of oscillation in a circuit where only one active device is present, the device is embedded in a passive network, and only single sinusoidal signals are of interest.

## 2.3 Noise Characterization

Noise De-embedding techniques are based on the noise power matrix first introduced by Haus and Adler [2-1] and letter renamed the noise correlation matrix by Hillbrand and Russer [2-2]. In this section, the commonly used noise de-embedding procedure based on the parallel-series configuration is described. This section also describes a general and systemic procedure for any equivalent noise circuit to extract the noise current of the drain channel noise $\overline{i_d^2}$, the induced gate noise $\overline{i_g^2}$ and their correlation noise $\overline{i_g i_d^*}$.

### 2.3.1 Noise De-embedding Procedure

The RF probe-pad parasitics are de-embedded from the measured noise parameters with the help of "OPEN" and "SHORT" dummy structures. Based on the DUT and dummy structures shown in Fig.2-1, the procedure for the noise parameter de-embedding and extraction are described. [2-5]

1. Measure the scattering parameters $[S^{DUT}]$,$[S^{OPEN}]$,$[S^{SHORT}]$ of a DUT,"OPEN" and "SHORT" dummy pads, and then convert each of them to the Y parameters $[Y^{DUT}]$,$[Y^{OPEN}]$ and $[Y^{SHORT}]$ using the conversion formula

$$[Y]=\frac{\begin{bmatrix}(1-S_{11})(1+S_{11})+S_{12}S_{21} & -2S_{12}\\ -2S_{21} & (1+S_{11})(1-S_{22})+S_{12}S_{21}\end{bmatrix}}{Z_0\cdot[(1+S_{11})(1+S_{22})-S_{12}S_{21}]} \tag{2-4}$$

2. Measure the noise parameters , $NF_{min}{}^{\mathrm{DUT}}$ ,$Y_{opt}{}^{\mathrm{DUT}}$ and $R_n{}^{\mathrm{DUT}}$ of the DUT.

3. Calculate the correlation matrix [$\mathrm{CA}^{\mathrm{DUT}}$] of the DUT from the measured noise parameters using

$$\left[C_A^{DUT}\right]=2kT_0\begin{bmatrix} R_n^{DUT} & \frac{NF_{\min}^{DUT}-1}{2}-R_n^{DUT}(Y_{opt}^{DUT})^*\\ \frac{NF_{\min}^{DUT}-1}{2}-R_n^{DUT}\cdot Y_{opt}^{DUT} & R_n^{DUT}\left|Y_{opt}^{DUT}\right|^2\end{bmatrix} \tag{2-5}$$

where $k$ is Boltzmann's constant, $T_0$ is the standard temperature, and the asterisk denotes the complex conjugate.

4. Convert the [$\mathrm{C_A}^{\mathrm{DUT}}$] matrix to its [$\mathrm{C_Y}^{\mathrm{DUT}}$] correlation matrix using

$$\left[C_Y^{DUT}\right]=\left[T^{DUT}\right]\cdot\left[C_A^{DUT}\right]\cdot\left[T^{DUT}\right]^{\dagger} \tag{2-6}$$

where [$\mathrm{T}^{\mathrm{DUT}}$] is given by

$$\left[T^{DUT}\right]=\begin{bmatrix}-Y_{11}^{DUT} & 1\\ -Y_{21}^{DUT} & 0\end{bmatrix} \tag{2-7}$$

and the $^{\dagger}$ in $[T^{DUT}]$ denotes the Hermitian conjugate.

5. Calculate the correlation matrix $[C^{Y}_{OPEN}]$ of the "OPEN" dummy structure with

$$\left[C_Y^{OPEN}\right] = 2kT\Re\left(\left[Y^{OPEN}\right]\right) \tag{2-8}$$

where $\Re(\ )$ stands for the real part of the elements in the matrix and $T$ is the absolute temperature at which the measurement was made.

6. Subtract parallel parasitics from the $[Y^{DUT}]$ and $[Y^{SHORT}]$ according to

$$\left[Y_I^{DUT}\right] = \left[Y^{DUT}\right] - \left[Y^{OPEN}\right] \text{ and} \tag{2-9}$$

$$\left[Y_I^{SHORT}\right] = \left[Y^{SHORT}\right] - \left[Y^{OPEN}\right] . \tag{2-10}$$

7. De-embed $[C_Y{}^{DUT}]$ from the parallel parasitics using

$$\left[C_{YI}^{DUT}\right] = \left[C_Y^{DUT}\right] - \left[C_Y^{OPEN}\right]. \tag{2-11}$$

8. Convert the $[Y_I{}^{DUT}]$ and $[Y_I{}^{SHORT}]$ to $[Z_I{}^{DUT}]$ and $[Z_I{}^{SHORT}]$ with the conversion formula

$$\left[Z\right] = \frac{1}{Y_{11}Y_{22} - Y_{12}Y_{21}}\begin{bmatrix} Y_{22} & -Y_{12} \\ -Y_{21} & Y_{11} \end{bmatrix} \tag{2-12}$$

9. Convert $[C_{YI}{}^{DUT}]$ to $[C_{ZI}{}^{DUT}]$ with

$$\left[C_{YI}^{DUT}\right] = \left[Z_I^{DUT}\right] \cdot \left[C_{YI}^{DUT}\right] \cdot \left[Z_I^{DUT}\right]^{\dagger} \tag{2-13}$$

10. Calculate the correlation matrix $[C_{ZI}{}^{SHORT}]$ of the "SHORT" test structure after de-embedding the parallel parasitics with

$$\left[C_{ZI}^{SHORT}\right] = 2kT\Re\left(\left[Z_I^{SHORT}\right]\right) \quad . \tag{2-14}$$

11. Subtract series parasitics from the $[Z_I^{DUT}]$ to get the Z parameters $[Z^{TRANS}]$ of the intrinsic transistor using

$$\left[Z^{TRANS}\right] = \left[Z_I^{DUT}\right] - \left[Z_I^{SHORT}\right] \quad . \tag{2-15}$$

12. De-embed $[C_{ZI}^{DUT}]$ from the series parasitics to get the correlation matrix $[C_Z]$ of an intrinsic transistor using

$$\left[C_Z\right] = \left[C_{ZI}^{DUT}\right] - \left[C_{ZI}^{SHORT}\right] \quad . \tag{2-16}$$

13. Convert the $[Z^{TRANS}]$ of the intrinsic transistor to its chain matrix $[A^{TRANS}]$ with the conversion formula

$$\left[A\right] = \frac{1}{Z_{21}}\begin{bmatrix} Z_{11} & Z_{11}Z_{22} - Z_{12}Z_{21} \\ 1 & Z_{22} \end{bmatrix} \tag{2-17}$$

14. Transform $[C_Z]$ to $[C_A]$ with

$$\left[C_A\right] = \left[T_A\right] \cdot \left[C_Z\right] \cdot \left[T_A\right]^{\dagger} \tag{2-18}$$

where $[T_A]$ is given by

$$\left[T_A\right] = \begin{bmatrix} 1 & -A_{11}^{TRANS} \\ 0 & -A_{21}^{TRANS} \end{bmatrix} \quad . \tag{2-19}$$

15. Calculate the noise parameters, $NF_{min}$ , $Y_{opt}$ and $R_n$ of an intrinsic transistor from the noise correlation matrix in chain representation $[C_A]$ using the expressions

$$NF_{\min} = 1 + \frac{1}{kT}\left( \Re\left(C_{12A}\right) + \sqrt{C_{11A} + C_{22A} - \left(\Im\left(C_{12A}\right)\right)^2} \right) , \tag{2-20}$$

$$Y_{opt} = \frac{\sqrt{C_{11A}C_{22A} - \left(\Im\left(C_{12A}\right)\right)^2} + i\Im\left(C_{12A}\right)}{C_{11A}} \tag{2-21}$$

and

$$R_n = \frac{C_{11A}}{2kT} \tag{2-22}$$

where $\Im(\ )$ stands for the imaginary part of the elements in the matrix and $i$ is the imaginary unit.

### 2.3.2 Noise Parameter Extraction Theory [2-5, 2-6, 2-7]

The noise figure, defined as the signal-to-noise ratio at the input port divided by signal-to-noise ratio at the output port, is widely used as a measure of noise performance of a noisy two-port network. It is usually expressed in dB. The noise figure ($F$) is generally affected by two factors - the source (input) impedance at the input port of a network and the noise sources in the two-port network itself.

The noise figure of a two-port network can defined as

$$F = \frac{P_{N,out}}{G_A \cdot P_{N,in}} = \frac{G_A \cdot P_{N,in} + P_{N,N}}{G_A \cdot P_{N,in}} \tag{2-22}$$

where $P_{N,out}$ is the output noise power, $G_A$ is the available gain of the two-port, $P_{N,in}$ is the input noise power, and $P_{N,out}$ is the noise contributed to the output by the two-port.

ln general, $F$ may be written as

$$F = F_{\min} + \frac{r_n}{g_s}\left|y_s - y_{opt}\right|^2 \tag{2-23}$$

where $y_s=g_s+jb_s$ is the source admittance seen by the two-port network, $y_{opt}=g_{opt}+jb_{opt}$ is the optimal source admittance which will result in the minimum noise figure $F_{min}$, and $r_n=R_n/R_o$ is the normalized noise resistance of the two-port. Note, that small letters are used for normalized quantities and capital

letters for actual values. At high frequencies, the admittance parameter $y$ is usually converted to reflection coefficient using $\Gamma = (1 - y)/(1 + y)$ . $F_{min}$, $R_n$, $\Gamma_0$ are called noise parameters of the two-port. A noisy two-port may be represented by a noise-free two-port and two current noise sources as shown in Fig. 2-3(a). These correspond to gate and drain sources in an FET device and are usually correlated. From y-parameters of the two-port and the noise source information, one may evaluate the noise parameters of the two-port. For this purpose, we also represent the noisy two-port with the noise free two-port and a noise current and a noise voltage source at the input side of the two-port, as shown in Fig.2-3(b).

From the y-parameters, of the two-port and the noise currents $i_d$ , $i_g$ , and the correlation term $\overline{i_g i_d^*}$ , we can calculate $i$ and $u$ and the corresponding correlation factor called $Y_{cor}$ as

$$i = i_{un} + uY_{cor}$$

$$\overline{iu^*} = Y_{cor}\overline{u^2} \qquad (2\text{-}24)$$

where $i_{un}$ is the part of noise current in $i$ that is uncorrelated to $u$ and $uY_{cor}$ is the part that is fully correlated to $u$. In addition, the values of $i$, $u$ and $Y_{cor}$ can be calculated from

$$u = -\frac{1}{y_{21}} i_d$$

$$i = i_g - \frac{y_{11}}{y_{21}} i_d$$

$$Y_{cor} = y_{11} - y_{21} \frac{\overline{i_g i_d^*}}{\overline{i_d^2}} = G_{cor} + jB_{cor} \quad , \qquad (2\text{-}25)$$

and the noise power of $i$ and $u$ can be calculated from

$$\overline{u^2} = \frac{\overline{i_d^2}}{\left|y_{21}\right|^2} = 4kT\Delta f \cdot R_u \qquad (2\text{-}26)$$

$$\overline{i^2} = \overline{i_g^2} + \overline{i_d^2}\left|\frac{y_{11}}{y_{21}}\right| - 2\Re\left(\overline{i_g i_d^*}\frac{y_{11}^*}{y_{21}^*}\right)$$

$$= 4kT\Delta f \cdot G_i \qquad (2\text{-}27)$$

where $\Re[\ ]$ denotes the real part of [ ] , $Y_{opt}$ is the optimal source admittance, and $Y_{cor}$ is the correlation factor given by

$$Y_{cor} = \frac{F_{\min} - 1}{2R_n} - Y_{opt} \quad . \qquad (2\text{-}28)$$

From these we can calculate

$$R_n = R_u$$

$$G_{opt} = \sqrt{\frac{G_i}{R_n} - B_{cor}^2}$$

$$B_{opt} = -B_{cor}$$

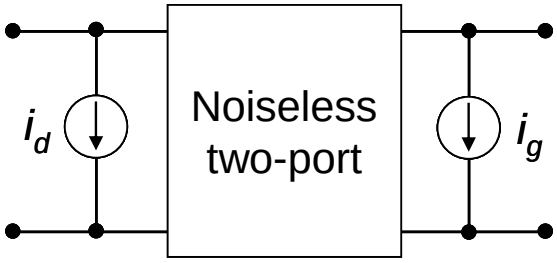
$$F_{\min} = 1 + 2R_n\left(G_{cor} + G_{opt}\right) \quad . \tag{2-29}$$

Finally, we can obtain

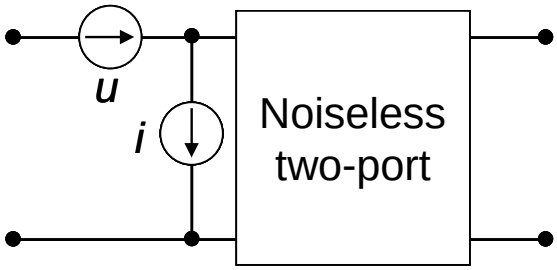
$$\overline{i_d^2} = 4kT_0\Delta f \cdot R_n\left|Y_{21}\right|^2 \tag{2-30}$$

$$\overline{i_g^2} = 4kT_0\Delta f \cdot R_n\left\{\left|Y_{opt}\right|^2 - \left|Y_{11}\right|^2 + 2\Re\left[\left(Y_{11} - Y_{cor}\right)Y_{11}^*\right]\right\} \tag{2-31}$$

$$\overline{i_g i_d^*} = 4kT_0\Delta f\left(Y_{11} - Y_{cor}\right)R_n Y_{21}^* \quad . \tag{2-32}$$




*(a) Admittance representation*




*(b) Chain representation*

*Fig.2-3. Different representations of noise two-port networks*

## 2.4 Large-Signal Measurements

Determining how active devices behave at different power levels is also an important consideration when designing telecommunications systems. Many RF amplifiers are designed to operate in the weakly nonlinear region, where power-added efficiency (*PAE*) peaks. The power-added efficiency is defined as the ratio of the additional power provided by the amplifier to the dc power,

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2-33}$$

Large-signal measurements provide output power, gain, and efficiency information at a given input power level. Figure 2-4 shows the results of large-signal measurements made on a MOSFETs. For these measurements, both the input and output impedance were set to 50 Ω. Figure 2-4 also illustrates the power levels at which the device enters compression and the power-added efficiency; *PAE* in that region. The 1-dB gain compression point, usually given in terms of output power, is an important quantity when considering the dynamic range of the transistor.

In addition to power level considerations, impedance matching throughout the system is an essential aspect of RF circuit design. Thus, it is also important to explore how the input and output impedance presented to each device in the system affect the performance of that device in the circuit. Furthermore, a

designer may want to determine the necessary impedance-matching conditions to achieve a specific desired performance from the device. Once either the desired input or output impedance is determined, contours can be generated for the other termination to illustrate tradeoffs that must be made between, for example, maximum power-added efficiency and maximum output power. [2-8]

## 2.5 Distortion

Many components of telecommunication systems receive numerous signals closely spaced in frequency at their inputs. The nonlinearities inherent in all active devices lead to certain undesirable effects, such as intermodulation and harmonic distortion, which in turn lead to the transfer of power to other frequencies near the frequency of interest. For a device with two signals at its input, one at a frequency $f_1$ and the other at a frequency $f_2$, it is traditionally the third-order (at frequencies $2f_1 - f_2$ and $2f_2 - f_1$) and fifth-order ($3f_1-2f_2$ and $3f_2-2f_1$) intermodulation products that are of most concern, because they are near the two frequencies of interest ($f_1$ and $f2$) and therefore will be the most difficult to filter out of the system. Therefore, RF and telecommunications applications, such as power amplifiers, require devices that exhibit highly linear operating characteristics. Two-tone measurements must be performed on the device offerings in RF-CMOS technologies to fully analyze the linearity of the devices

offered. Use is made of a load-pull system to make these measurements. The third-order and fifth-order intermodulation products are commonly measured, and the third-order intercept point; $IP_3$, an important figure of merit for describing linearity, is obtained. [2-8]

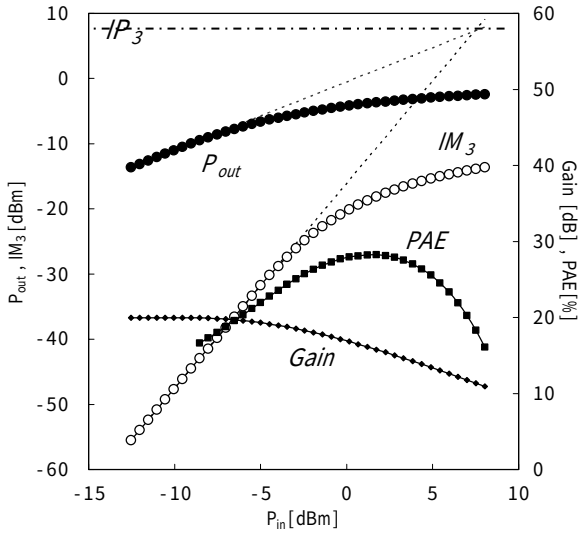



*Fig.2-4. Sample of measured large-signal and intermodulation distortion data for a MOSFET and the determination of $IP_3$ is also illustrated. $P_{out}$ denotes the output power, $IM_3$ denotes the third-order intermodulation product, PAE denotes the power-added efficiency, and $P_{in}$ denotes the input power.*

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# Chapter.3

# A Mesh-Arrayed MOSFET (MA-MOS) for High-Frequency Analog Applications

## 3.1 Introduction

The Si-MOSFET technology is a new candidate for high-level system integration and cost reduction of mobile communication LSIs. Some system integrations for RF and baseband circuits have been currently realized with the Si-MOSFET technology [3-3, 3-4]. The lowest noise figure of 0.6dB at 2GHz operation is reported, using a 0.2μm Ni-salicide CMOS technology [3-5].

In this chapter, a novel and practical configuration of MOSFETs to attain remarkable high frequency performance is proposed by using a 0.25μm CMOS technology and the parasitic effect of Si-MOSFETs for high frequency performance is also discussed.

## 3.2 Device Configuration and Parasitic Components

Figure 3-1 shows a schematic top-view of unit Mesh-Arrayed MOSFET(MA-MOS) with ring-shaped gate electrode. Ring-shaped gate electrode is often used for power devices such as DMOS.

Although the gate electrode of DMOS is arranged around the source area, the ring-shaped gate electrode of MA-MOS surrounds the drain area for the reduction of $R_s$ and $C_{gd}$. Unit gate finger length ($W_f$) of the MA-MOS is 7.0 μm and 28 units are arrayed by mesh, as shown in Fig.3-2. We also fabricated

conventional MOSFETs with the 1 and 2 contact holes at each finger. The finger length ranges from 5 μm to 20 μm with the same total gate width of 200μm to compare the performance, as shown in Fig.3-3.

The equivalent circuit parameters of the conventional n-MOS and n-channel MA-MOS are extracted by measured S-parameters. Figure 3-4 shows a simplified equivalent circuit of MOSFET. It also summarizes equations for high-frequency characteristics: current gain cutoff frequency ($f_T$), noise figure, and maximum oscillation frequency ($f_{max}$) [3.4]. These equations suggest that the reduction of both $R_g$ and $R_s$ is effective in improving $NF_{min}$ and $f_{max}$, and the reduction of $C_{gd}$ is effective in improving $f_{max}$. Figure 3-5 shows the dependence of parasitic components on gate finger length for various n-MOS patterns. MA-MOS can reduce the parasitic components: $R_g$, $R_s$, $C_{gd}$, and $C_{ds}$ successfully owing to ring-shaped gate electrode and mesh layout. In particular, $C_{ds}$ is reduced to be 60% of conventional MOSFET with the gate width of 5 μm.

The MA-MOS configuration was optimized to furthermore reduce $R_g$ and $C_{gs}$. Figure 3-6 shows two types of the MA-MOS configuration. Figure 3-7 shows the dependence of parasitic components on device configuration. The optimized MA-MOS can reduce $R_g$ and $C_{gs}$, which are 50% and 85% of non-optimized MA-MOS, respectively.

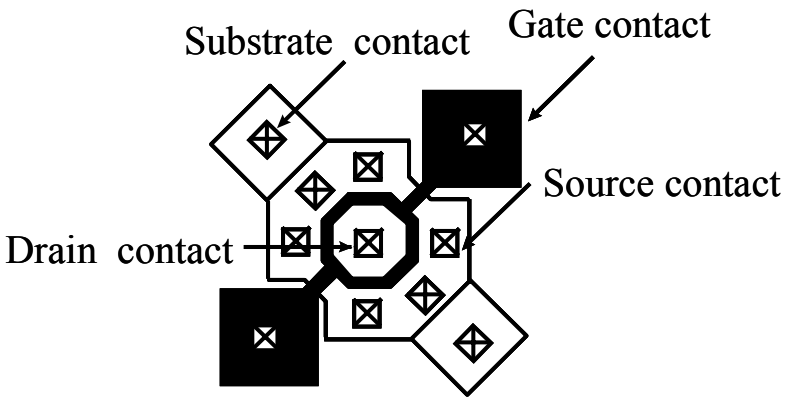



*Fig.3-1. Schematic top view of Mesh-Arrayed MOSFET(MA-MOS) with ring-shaped gate electrode.*

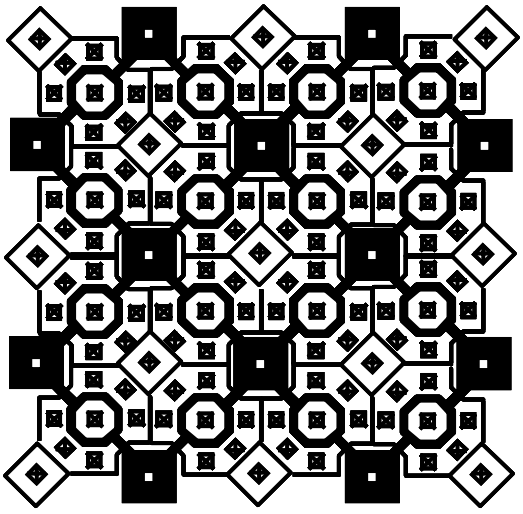


*Fig.3-2. Schematic top view of MA-MOS layout.*

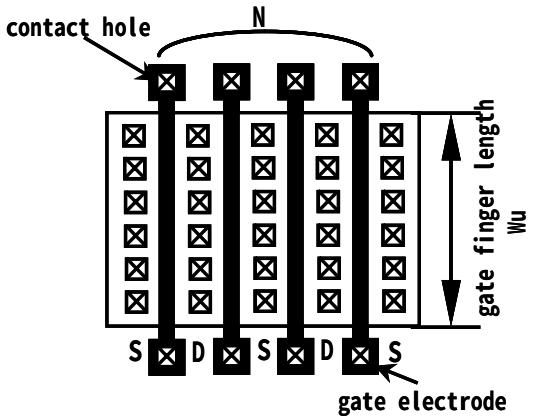
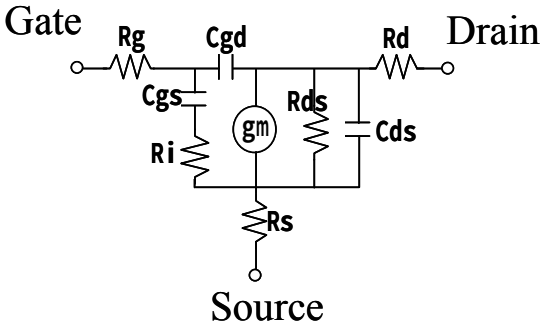



*Fig.3-3. Schematic top view of conventional MOSFET.*

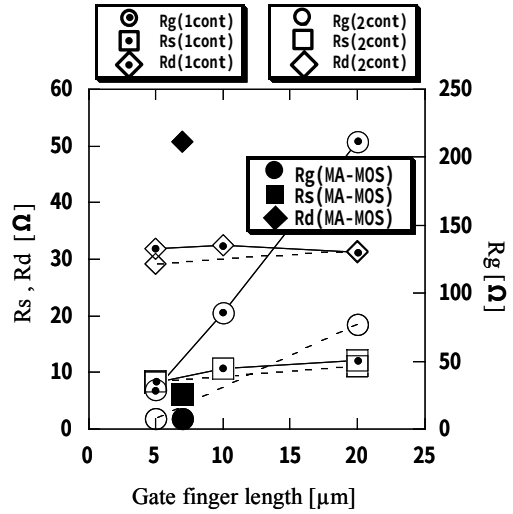



$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

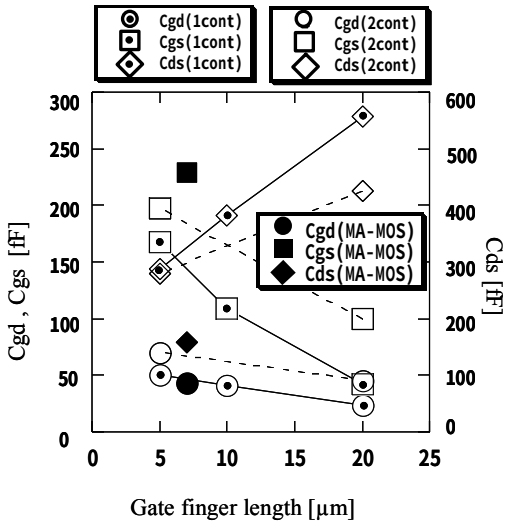
$$F_{\min} = 1 + 2\pi f K C_{gs}\sqrt{\frac{R_g + R_s}{g_m}}$$

$$f_{\max} = \frac{f_T}{2\sqrt{R_g(g_{ds} + 2\pi f_T C_{gd}) + g_{ds}(R_i + R_s)}}$$

*Fig.3-4. Silicon MOSFET small-signal equivalent circuit and equations for high-frequency characteristics.*




*(a) Parasitic resistance*




*(b) Parasitic capacitance*

*Fig.3-5. The dependence of (a) parasitic resistance and (b) parasitic capacitance on gate finger length for various n-MOS patterns.*

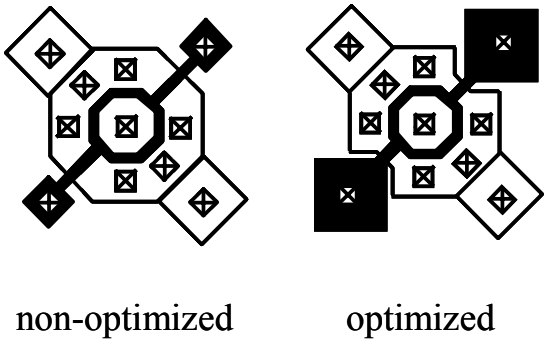
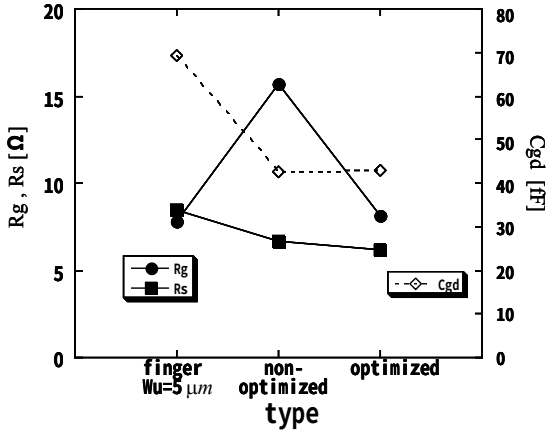
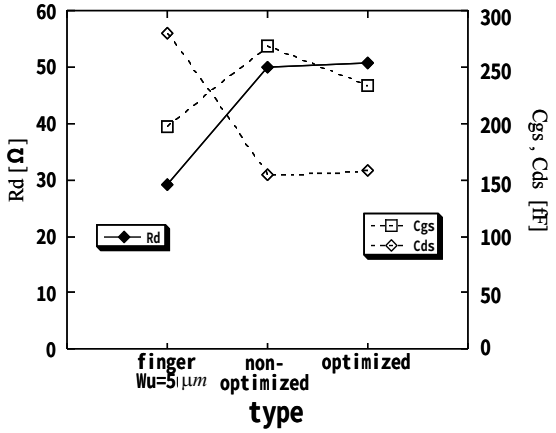



*Fig.3-6. Two type of MA-MOS configuration.*




*(a) $R_g$, $R_s$ and $C_{gd}$ .*




*(b) $R_d$ ,$C_{gs}$ and $C_{ds}$.*

*Fig.3-7. The dependence of parasitic components on device configuration.*

## 3.3 AC Characteristics

High-frequency AC characteristics are measured by an on-wafer measurement system. Current gain cutoff frequencies ($f_T$) for various 0.3 μm n-MOS and n-channel MA-MOS are shown in Fig.3-8. $f_{T\_peak}$ of 35 GHz and 20 GHz are obtained for 0.3 μm conventional n-MOS with $W_f$=20 μm and 0.3 μm n-channel MA-MOS, respectively. Since parasitic gate capacitance increases with the number of gate fingers as shown in Fig.3-5, $f_T$s of the short finger MOS and MA-MOS result in smaller than that of the long finger length MOS.

Figure 3-9 shows the dependence of $NF_{min}$ and associated gain($G_a$) on Wu. $NF_{min}$ of 1.0 dB at 2 GHz with $G_a$ of 20 dB are obtained for the 0.3μm conventional n-MOS with $W_f$=5 μm. MA-MOS realizes sufficient low $NF_{min}$ of 0.6 dB at 2 GHz with $G_a$ of 23 dB, though using non-silicide gate. On the other hand, for non-optimized MA-MOS shown in Fig.3-6, $NF_{min}$ value of 0.9 dB at 2 GHz with $G_a$ of 21 dB are obtained. The result indicates the effectiveness of the optimized device configuration on the $NF_{min}$ and $G_a$.

Moreover, $f_{max}$ of 37 GHz is obtained for optimized MA-MOS by maximum stable gain and maximum available gain (MSG/MAG) plots as shown in Fig.3-10. It is mainly due to the reduction of $R_g$, $R_s$, and $C_{gd}$ by ring-shaped gate electrode and mesh layout.

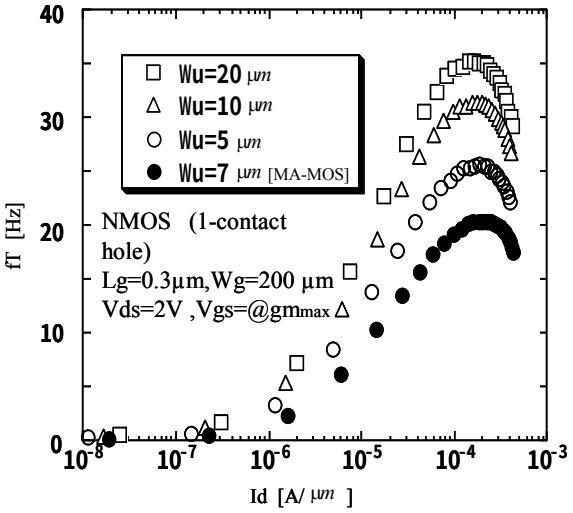



*Fig.3-8. The dependence of Current gain cutoff frequency on drain current.*

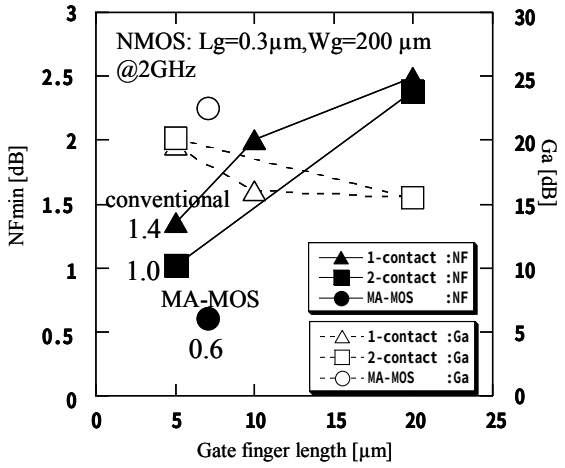



*Fig.3-9. The dependence of $NF_{min}$ and $G_a$ on gate finger length.*

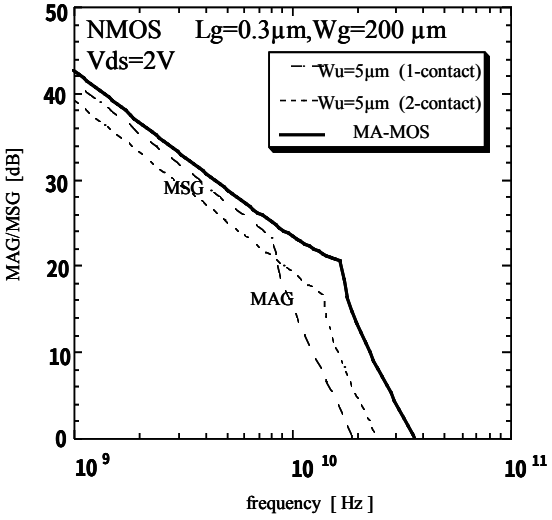



*Fig.3-10. The dependence of maximum stable gain and maximum available gain (MSG/MAG) on frequency.*

## 3.4 Conclusion

A Mesh-Arrayed MOSFET with ring-shaped gate electrode for high-frequency analog application has been developed. The dependence of noise figure and maximum oscillation frequency on parasitic components in MA-MOS configuration has been discussed. The MA-MOS realizes low noise figure of 0.6 dB at 2 GHz and high $f_{max}$ of 37 GHz, using a non-salicide 0.25 μm CMOS technology.

The MA-MOS is the most practical candidate to realize low cost and high performance one-chip RF Baseband CMOS LSI.

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# Chapter.4

# Analysis of RF Characteristics as Scaling MOSFETs from 150 nm to 65 nm Nodes

## 4.1. Introduction

The downscaling of CMOS technology has resulted in strong improvement in RF performance of bulk and SOI MOSFETs. Owing to the progress of the RF performance of smaller geometry MOSFETs, the monolithic integration of both RF front-end and baseband circuits are now possible up to 2 or 5 GHz frequency region with the RF mixed signal CMOS technology. Moreover, in the research level, even millimeter-wave applications can be implemented in pure CMOS process [4-1, 4-2].

In order to realize the low-cost RF mixed signal CMOS system-on-chip, the device structure of the RF CMOS should be the same as that of the logic CMOS so that no additional fabrication process steps are necessary. In other words, basically no change from the logic CMOS is allowed for the RF CMOS device structures except their horizontal layout which can be realized only by mask pattern design change.

Because subtle differences exist in the optimization of logic and RF CMOS device structures, there has been always a concern for every scaled CMOS generation, whether such low-cost RF mixed CMOS devices can satisfy the RF requirements for the high-performance RF application, such as cellular phones. For example, the degradation of the signal to noise ratio under the lower supply voltage in the scaled CMOS and degradation of the matching of pair MOSFET

characteristics in the short-channel deices are big concerns. Also, while cut-off frequency ($f_T$) can be increased by scaling down the gate length, another performance such as maximum oscillation frequency ($f_{max}$), and minimum noise figure ($NF_{min}$) depend strongly on the parasitic components [4-3, 4-4, 4-5].

In this chapter, it was studied that the scaling effects from the 150 nm node to the 65 nm node on RF CMOS devices which are basically made of logic CMOS process without any change. The purpose of the study is to confirm the suitability of the 65 nm logic CMOS for RF application, despite the above concerns. In particular, RF characteristics -- such as cut-off frequency ($f_T$), maximum oscillation frequency ($f_{max}$), minimum noise figure ($F_{min}$), intrinsic gain ($g_m/g_{ds}$), peak power-added efficiency ($PAE$), 1dB compression point ($P_{1dB}$), third order inter-modulation distortion ($IM_3$), and third order intercept point ($IP_3$) -- of the 65 nm RF mixed signal CMOS were compared with those of the 150 nm CMOS. The gate layout dependence on the RF performance has been also investigated.

## 4.2. Methodology and Experimental Procedures

In this chapter, we fabricated multi-finger n-MOSFETs using 65 nm node CMOS technology, as shown in Fig.4-1(a). The gate length is 60nm and unit gate finger length ($W_f$) ranges from 0.32 μm to 8 μm with the same total gate width of 160 μm to compare the performance. The multi-finger n-MOSFETs using 150 nm

node technology are also compared. Gate length is 180 nm and unit gate finger length ($W_f$) ranges from 1 μm to 20 μm with the same total gate width of 160 μm. Device parameters of the n-MOSFETs for 65 nm and 150 nm are shown in Table 4-1. The finger lengths of the n-MOSFETs for the 65 nm and 150 nm are shown in Table 4-2. The optimization of the unit gate finger length is significantly important in order to obtain good RF performance [4-6]. Figure 4-1(b) shows a simplified small-signal equivalent circuit of MOSFET [4-7] which is adopted in this chapter.

The equivalent circuits-parameters including noise factor:$\gamma$. were extracted. Unfortunately, our evaluation structure of 65nm node with different finger lengths do not have sufficiently low interconnect resistance from device to pad. This results high drain and source resistance as shown in Table 4-3, and therefore the lower $I_{ds}$ and $g_m$.

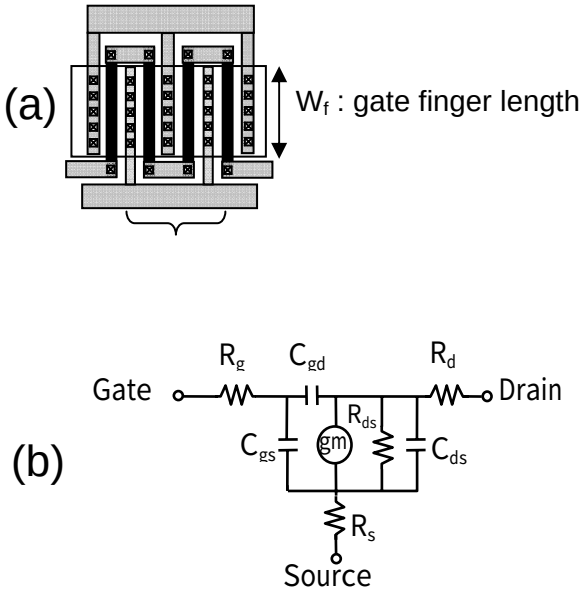



*Fig.4-1. (a) Schematic top view of MOSFETs .$W_f$ is unit gate finger length and $N_f$ is gate finger number. (b) Simplified small-signal equivalent circuit of MOSFET which is adopted in this chapter.*

*Table 4-1 The device parameter for 65nm and 150nm node.*

| Technology | Vdd (V) | Lg (nm) | $t_{ox}$ (nm) | Vth (V) |
|---|---|---|---|---|
| 150nm | 1.5 | 180 | 3.0 | 0.3 |
| 65nm | 1.2 | 60 | 2.2 | 0.28 |

*Table 4-2 The variation of device structures.*

*(a) 65nm node*

*Gate length is 60nm and unit gate finger length ($W_f$) ranges from 0.32μm to 8μm with the same total gate width of 160μm.*

| gate finger length :$W_f$ (μm) | 0.4 | 0.8 | 1 | 1.6 | 2 | 3.2 | 4 |
|---|---|---|---|---|---|---|---|
| gate finger number :$N_f$ | 160 | 80 | 64 | 40 | 32 | 20 | 16 |

*(b) 150nm node*

*Gate length is 180 nm and unit gate finger length ($W_f$) ranges from 1μm to 20 μm with the same total gate width of 160 μm.*

| gate finger length :$W_f$ (μm) | 1 | 1.25 | 2 | 2.5 | 4 | 5 | 8 | 10 | 20 |
|---|---|---|---|---|---|---|---|---|---|
| gate finger number :$N_f$ | 160 | 128 | 80 | 64 | 40 | 32 | 20 | 16 | 8 |

*Table 4-3 The parameter of the evaluation structure of 65nm node.*

| | $W_{total}$ (μm) | $W_f$ (μm) | Rd_wire (Ω) | Rs_wire (Ω) | R_wire total (Ω) |
|---|---|---|---|---|---|
| Evaluation Structure - 1 | 160 | 0.32 - 8 | 0.70 | 2.00 | 2.70 |
| Evaluation Structure - 2 | 128 | 1 | 0.18 | 0.23 | 0.41 |

## 4.3. Small Signal and Noise Characteristics

Small signal and noise characteristics are measured by an on-wafer measurement system.

### 4.3.1 Cut-off Frequency : $f_T$ and Maximum Oscillation Frequency: $f_{max}$

The cut-off frequency ($f_T$) is defined as the frequency where the *current gain* is equal to unity, while the maximum oscillation frequency ($f_{max}$) is defined as the frequency where *power gain* is equal to unity. $f_T$ and $f_{max}$ are given below.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4-1.a}$$

$$\approx \frac{1}{2\pi} \cdot \frac{v_{sat}}{L_g} \tag{4-1.b}$$

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds} \cdot (R_g + R_s) + 2\pi \cdot f_T \cdot R_g \cdot C_{gd}}} \tag{4-2.a}$$

$$\approx \sqrt{\frac{f_T}{8\pi \cdot R_g \cdot C_{gd}}} \tag{4-2.b}$$

where $g_m$ is the transconductance and $C_{gs}$,$C_{gd}$ are the gate-source capacitance and gate-drain capacitance, respectively. $g_{ds}$ is the output conductance and $R_g$ ,$R_s$ are the gate resistance and the source resistance, respectively. $v_{sat}$ is the saturation velocity.

The equation (4-1.b) and (4-2.a) indicate that while $f_T$ can be increased by scaling down the gate length, $f_{max}$ depends strongly on not only $g_m$ and $g_{ds}$ but also the parasitic components.

Figure 4-2 shows the cut-off frequency ($f_T$) of 65nm node as a function of drain current compared with that of the 150 nm node n-MOSFET, which is measured from *Evaluation Stracture-2*. Peak $f_T$ of 146 GHz is obtained for 65nm node, while peak $f_T$ of 55 GHz is obtained for 150 nm node. This is expected value by Eq.(4-1.b) from 150 nm to 65 nm node. Higher $g_m$ value and smaller gate dimension provide the high $f_T$ value, as demonstrated in Eq.(4-1.a). Figure 4-3 shows the maximum oscillation frequency ($f_{max}$) of 65 nm node as a function of

drain current compared with 150 nm node n-MOSFET. Peak $f_{max}$ of 135 GHz is obtained for 65 nm node, while peak $f_{max}$ of 76 GHz is obtained for 150 nm node.

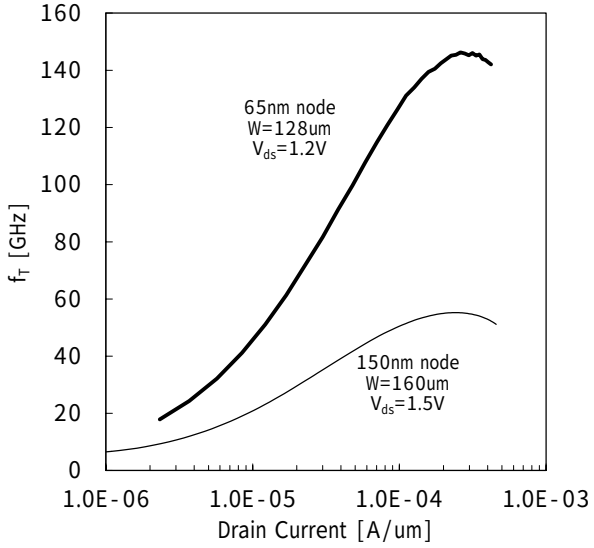



*Fig.4-2. The cut-off frequency ($f_T$) of 65 nm node as a function of drain current compared with 150 nm node n-MOSFET. Peak $f_T$ of 146 GHz is obtained for 65 nm node, while peak $f_T$ of 55 GHz is obtained for 150 nm node.*

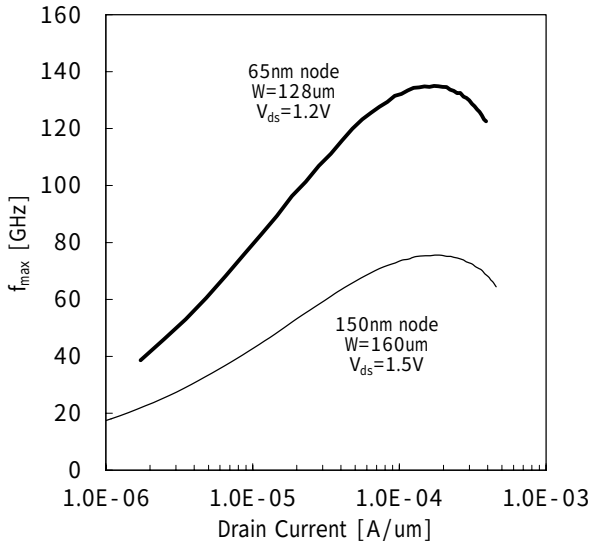



*Fig.4-3. The maximum oscillation frequency ($f_{max}$) of 65 nm node as a function of drain current compared with 150 nm node n-MOSFET. Peak $f_{max}$ of 135 GHz is obtained for 65 nm node, while peak $f_{max}$ of 76 GHz is obtained for 150 nm node.*

The cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) measured at the same bias condition of $NF_{min}$ (see next section) for various n-MOSFET are shown in Fig.4-4. Calculated $f_T$ and $f_{max}$ using extracted component from the s-parameters with eqs.(4-1a) and (4-2a), are also indicated in Fig.4-4. With decreasing of the gate finger length, gate resistance ($R_g$) decreases. However, since the cross-section capacitance of the gate wiring and drain wiring increases, gate capacitance ($C_{gd}$) increases with finger number. Therefore, $f_{max}$ have optimize point at minimum value of these products ($R_g$*$C_{gd}$) around $W_f$=1 to

2 μm, as shown in Fig.4-5 and Eq.(4-2.b). Maximum $f_T$ value of 140 GHz and $f_{max}$ value of 162 GHz are obtained with $W_f$=1μm and $W_f$=3.2μm, respectively. Calculated $f_T$ and $f_{max}$ using extracted component from the s-parameters are also indicated in Fig.4-4. Note that these are not the peak values of $f_T$ and $f_{max}$ .

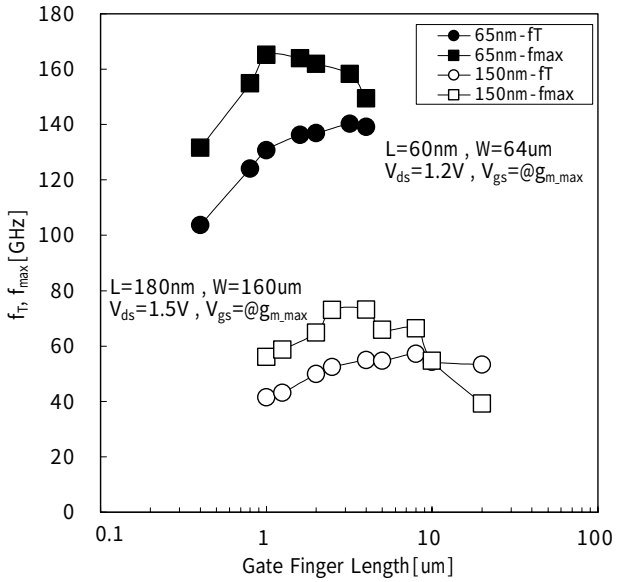



*Fig.4-4. Cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) measured at the same bias condition of $NF_{min}$ for various n-MOSFET.* Calculated $f_T$ and $f_{max}$ using extracted component from the s-parameters is also shown in this figure.

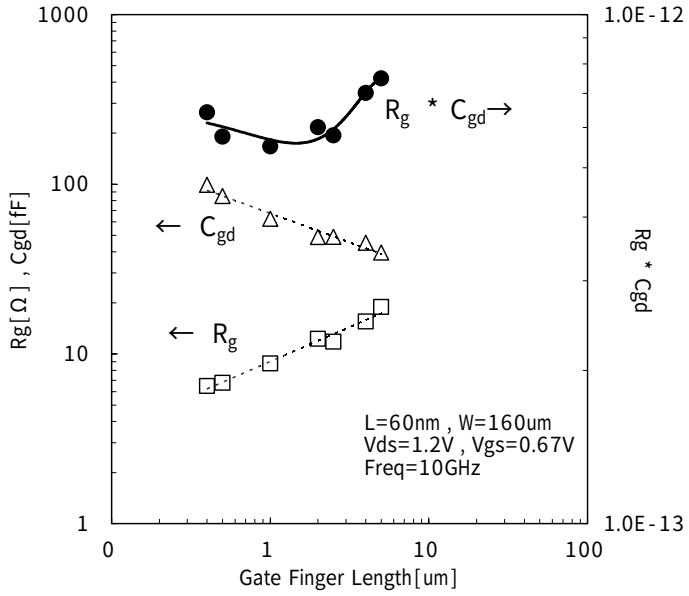



*Fig.4-5. The dependence of extracted gate resistance ($R_g$), gate-drain capacitance ($C_{gd}$) and these products ($R_g$*$C_{gd}$) as a function of gate finger length ($W_f$) . With decreasing of $W_f$, $R_g$ decreases. However, since the cross-section capacitance of the gate wiring and drain wiring increases, $C_{gd}$ increases with finger number.*

### 4.3.2 Noise Figure: $NF_{min}$

Thermal noise is the main noise source of the CMOS device for high frequency performance, and is dominated by the channel noise. In chapter 5, more detail about noise characteristics is described. Here, the drain channel noise is

focused. A figure of merit for the device thermal noise properties is the minimum noise figure ($F_{min}$, $NF_{min}$) ,which are given below.

$$F_{\min} = 1 + 2 \cdot \frac{f}{f_T} \sqrt{\gamma_{gm} \cdot g_m \cdot \left(R_g + R_s\right)} \tag{4-3.a}$$

$$R_n = \frac{\gamma_{gm}}{g_m} \tag{4-3.b}$$

$$NF_{\min} = 10 \cdot \log_{10} F_{\min} \quad \text{[dB]} \tag{4-3.c}$$

$R_n$ is the equivalent noise resistance, and $\gamma_{gm}$ is so-called drain current excess noise factor, and corresponds to noise parameter; $P$ in chapter 5. The power spectral density (PSD) of drain current noise, $\overline{i_d^2}$ in a band-width $\Delta f$ is defined by the equation [4-8],

$$\overline{i_d^2} = 4kT \cdot \gamma_{gm} \cdot g_m \cdot \Delta f \tag{4-4.a}$$

$$= 4kT \cdot \gamma_{gd0} \cdot g_{do} \cdot \Delta f \tag{4-4.b}$$

where $g_{d0}$ is the channel conductance at $V_{ds}$=0. $\gamma_{gm}$ and $\gamma_{gd0}$ are $g_m$ and $g_{d0}$ referenced excess noise factor, respectively. The theoretical long-channel value of $\gamma$ is $\gamma_{gm}$=$\gamma_{gd0}$= 2/3 in the saturation region [4-9]. However the value of $\gamma$ become greater than 2/3 and $\gamma_{gm} \neq \gamma_{gd0}$ with short channel device [4-10] due to channel length modulation [4-11]. In this chapter, $g_m$ referenced excess noise factor; $\gamma_{gm}$ is used. The equation (4-3.b) indicates that $NF_{min}$ also depends strongly on the

parasitic components and $\gamma_{gm}$. Fig.4-6 shows measured $NF_{min}$ versus the gate-to-drain voltage ($V_{gs}$) of $W_{total}$=160 μm at 10 GHz. The de-embedding techniques based on the noise correlation matrix [4-12] was applied to extract intrinsic device characteristics. Minimum $NF_{min}$ value of 1.06dB is obtained at $V_{gs}$=0.67 V for 65 nm node. Therefore, our measurement and analysis both of small and large signal are performed at this bias point. Figure 4-7 shows the $g_m$ referenced excess noise factor; $\gamma_{gm}$ as a function of the $V_{gs}$ compared with 65 nm and 150 nm node. The value of $\gamma_{gm}$=1.59 is obtained at this bias point for 65 nm node, while $\gamma_{gm}$=0.91 for 150 nm node. As scaling continues, the $NF_{min}$ improvement tends to saturate.

Figure 4-8 indicates the dependence of $NF_{min}$ and $R_n$ as a function of gate finger length ($W_f$) at 10 GHz. Devices are biased at $V_{ds}$=1.2 V and $V_{ds}$=0.67 V. Minimum $NF_{min}$ value is obtained with $W_f$=1μm at 10GHz. Fig.4-9 shows the optimized gate finger length in terms of $NF_{min}$ and $f_{max}$ versus technology node. The data from Morifuji's analysis [4-6] are also plotted in the figure.

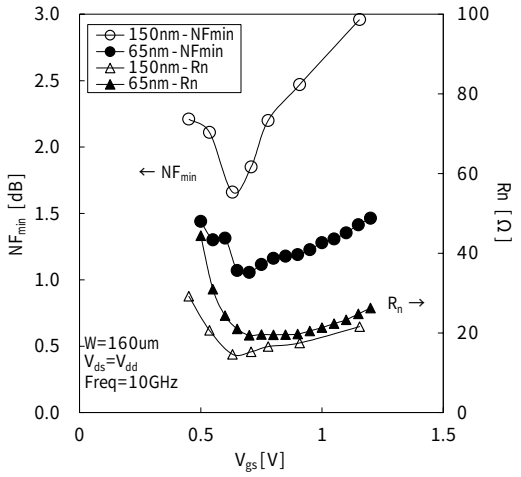



*Fig.4-6. Measured $NF_{min}$ value of 65 nm and 150 nm node as a function of the gate-to-drain voltage ($V_{gs}$) of $W_{total}$=160 μm at 10 GHz. The device shows the minimum value at around $V_{gs}$=0.67 V.*

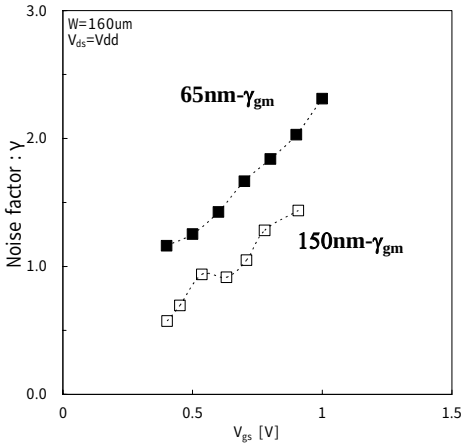



*Fig.4-7. The $g_m$ referenced excess noise factor; $\gamma_{gm}$ as a function of the gate-to-source voltage ($V_{gs}$) compared with 65 nm and 150 nm node. The value of $\gamma_{gm}$=1.59 is obtained at this bias point for 65 nm node, while $\gamma_{gm}$=0.91 for 150 nm node.*

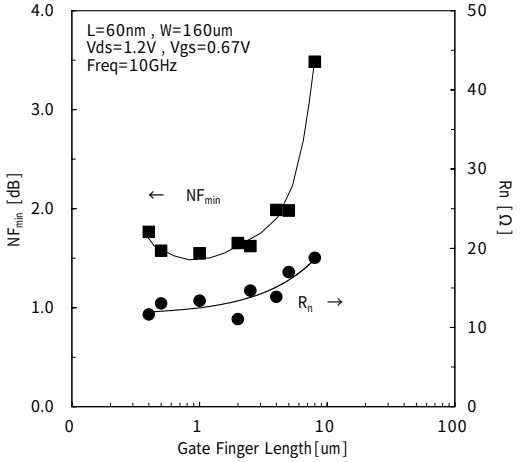



*Fig.4-8. The dependence of $NF_{min}$ and equivalent noise resistance ($R_n$) as a function of gate finger length ($W_f$) at 10 GHz. Devices are biased at $V_{ds}$=1.2 V and $V_{ds}$=0.67 V. Minimum $NF_{min}$ value of 1.55 dB is obtained with $W_f$=1 μm.*

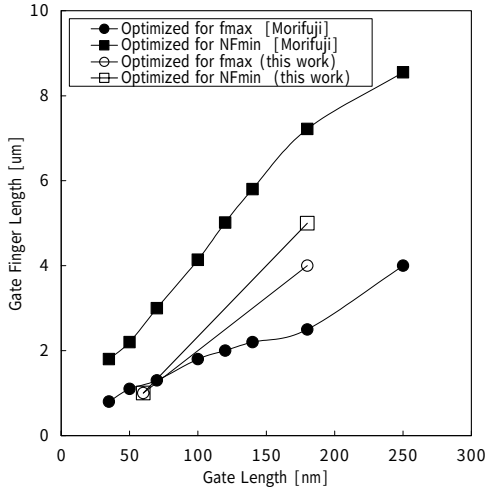



*Fig.4-9. The optimized gate finger length in terms of maximum oscillation frequency ($f_{max}$) and minimum noise figure ($NF_{min}$) versus the technology node. The data from Morifuji's analysis [4-6] are also plotted.*

### 4.3.3 Intrinsic gain: $g_m/g_{ds}$

The intrinsic gain is calculated by dividing transconductance ($g_m$) with output conductance ($g_{ds}$). In the velocity saturation, $g_m$ scales with the inverse of gate oxide thickness ($1/t_{ox}$) as shown in Eq.(4-5.a), while $g_{ds}$ increase as $V_{ds}/L$ increases due to drain induced barrier lowing (DIBL) as shown in Eq.(4-5.b) [4-13]. Therefore, intrinsic gain ($g_m/g_{ds}$) is related to $L/t_{ox}$, as shown in Eq.(4-5.c).

$$g_m \propto W \frac{v_{sat}}{t_{ox}} \tag{4-5.a}$$

$$g_{ds} \propto \frac{V_{ds}}{L} \tag{4-5.b}$$

$$\frac{g_m}{g_{ds}} \propto W \cdot \frac{v_{sat}}{V_{ds}} \cdot \frac{L}{t_{ox}} \tag{4-5.c}$$

Since the scaling of gate oxide thickness: $t_{ox}$ cannot be reduced as that of gate length:$L$, the intrinsic gain:$g_m/g_{ds}$ reduced as scaling continues. Figure 4-10 shows the intrinsic gain obtained from the s-parameter as a function of $V_{gs}$ with comparison between the 65nm and 150 nm nodes at 10 GHz. Peak intrinsic gain of 14.6 is obtained for 150 nm node, while that of 10.4 for the 65nm node.

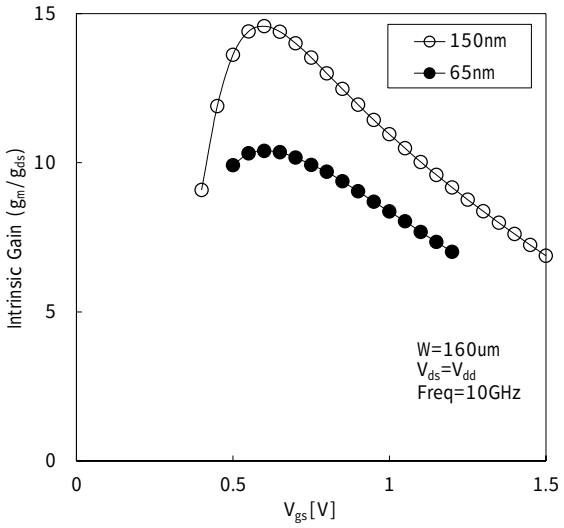



*Fig.4-10. the intrinsic gain as a function of $V_{gs}$ compared with 65 nm and 150 nm at 10GHz. Peak intrinsic gain of 14.6 is obtained for 150 nm node, while that of 10.4 for 65 nm node.*

## 4.4. Large Signal and Distortion Characteristics

Large signal and distortion characteristic are used to describe nonlinearities of analog circuits. The large signal and distortion characteristics were measured by load-pull system.

### 4.4.1. Power-Added Efficiency: *PAE* and Associated Gain: $G_a$

The power-added efficiency (*PAE*) is defined below

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{4-6.a}$$

$$\approx PAE_0 \cdot \left(1 - \frac{1}{G_a}\right) \tag{4-6.b}$$

where $P_{dc}$ is dc power and $G_a$ is associated gain. At the low frequency limit, in which $1/G_a$ approaches 0, *PAE* approaches $PAE_0$. $PAE_0$ is 50% in class A operation and 79% (= π/4) in class B operation. Using large-signal cut-off frequency: $f_{c,ls}$, $G_a$ is defined as follows: [4-14]

$$Ga = \left(\frac{f_{c,ls}}{f}\right)^2 \tag{4-6.c}$$

$$f_{c,ls} \propto f_{\max} \tag{4-6.d}$$

$f_{c,ls}$ is almost 30% of the maximum oscillation frequency ($f_{max}$) in a HEMT device [4-14]. It was also reported that $f_{c,ls}$ is almost 50% of $f_{max}$ in a 65 nm node CMOS device [4-15]. Figure 4-11 shows output power vs. gain and power added gain at 5 GHz for 65n m and 150 nm nodes, which is measured from *Evaluation Structure-2*. The device reveals an output power of 9.3 $dB_m$ and a gain of 11.3 dB at a peak *PAE* of 39.6% for 65 nm node, while an output power of 10.3 $dB_m$ and a gain of 10.2 dB at a peak *PAE* of 40.2% for 150nm node. No big difference was observed between the 65 and 150 nm nodes because the measurement frequency is sufficiently smaller than $f_{max}$. Figure 4-12 indicates the dependence of *PAE* as a function of gate finger length ($W_f$). which are measured at the same bias point in the case of noise and small signal measurement; $V_{ds}$=1.2 V and $V_{ds}$=0.67 V. Since the evaluation structure with different finger lengths (*Evaluation Stracture-1*) have high drain and source resistance, as mentioned before, the lower *PAE*, gain and Pout are obtained as shown in Fig.4-11. Figure 4-12 also indicates the estimated line when reducing the resistance by 15%. The highest peak PAE value is obtained with $W_f$=1 μm. The dependency of *PAE* has a similar trend of $f_{max}$, as shown in Fig.4-12.

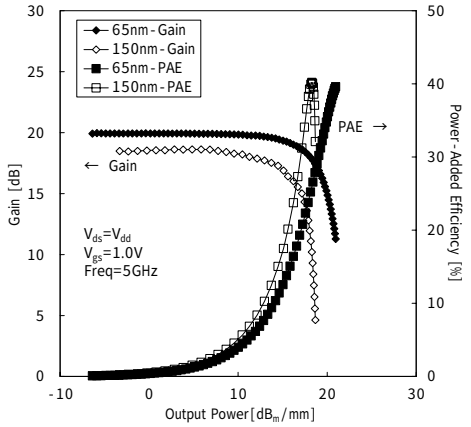



*Fig.4-11. Output power vs. gain and power added gain at 5 GHz for 65 nm and 150 nm nodes. The device reveals an output power of 9.3 dBm and a gain of 11.3 dB at a peak PAE of 39.6% for 65 nm node, while an output power of 10.3 dBm and a gain of 10.2 dB at a peak PAE of 40.2% for 150 nm node.*

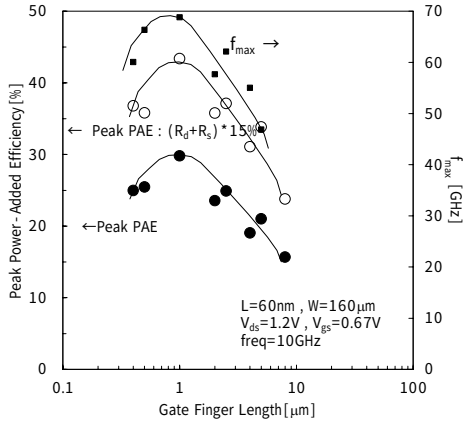



*Fig.4-12. The dependence of peak Power-Added Efficiency (PAE) as a function of unit gate finger length ($W_f$). The highest peak PAE value of 29.8% is obtained with $W_f$=1 μm. The estimated line when reducing the resistance by 15% is also indicated.*

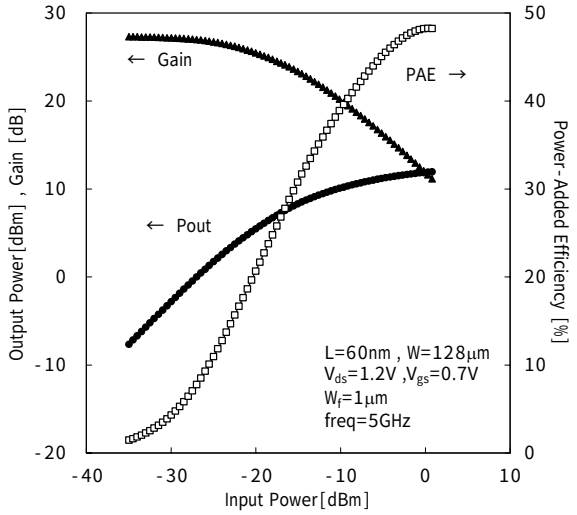
### *4.4.2 1dB compression point: $P_{1dB}$*

The 1dB compression point ($P_{1dB}$) is defined as the power level at which its gain has compressed by 1dB. Output gain is also measured at the $P_{1dB}$ point. The transfer characteristics at 5 and 10 GHz for 65 nm node are indicated in Fig.4-13. $OP_{1dB}$ of 5.1 dBm with gain of 10.7 dB are obtained at 10 GHz, while $OP_{1dB}$ of 3.4 dBm with gain of 26.3 dB at 5 GHz. The $P_{1dB}$ for various gate finger length ($W_f$) was also measured, and the dependency of $W_f$ was not observed.

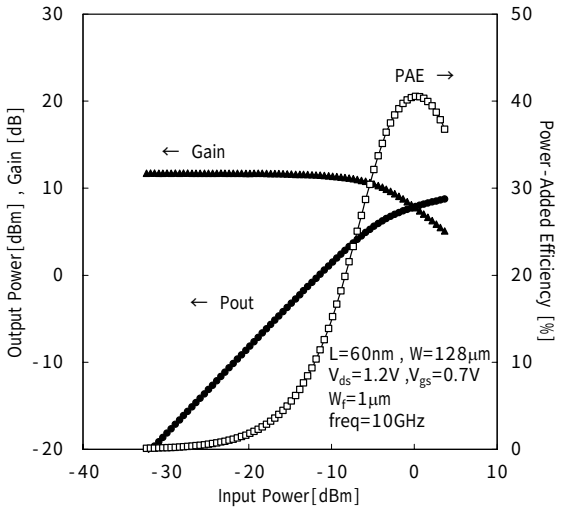
Since $IP_{1dB}$ and third order intercept point :$IP_3$ (See next section) are related by [4-16] ,

$$IP_3 = P_{1dB} + 9.6 \quad \text{[dB]} \tag{4-7}$$

the scaling effect of the distortion characteristics will be discussed in following section.




(a) 5GHz




(b) 10GHz

*Fig.4-13. The transfer characteristics at (a)5 GHz and (b)10 GHz for 65 nm node.*

### 4.4.3 Third Order Intercept Point: $IP_3$

Third order intercept point: $IP_3$ test is extracted from measured two-tone characteristics to describe nonlinearity. Figure 4-14 demonstrates the measured two-tone distortion characteristics for (a)65 nm and (b)150 nm node at 5GHz for $\Delta f$=1 MHz. $IP_3$ also can be input ($IIP_3$) or output referred ($OIP_3$). Third-order intermodulation distortion ($IM_3$) measured by a two-tone test expresses the degree of non-linearity of the device, and is given in units of $dB_c$. For low distortion operation, $IP_3$ should be as high as possible, and $IM_3$ should be as low as possible. $OIP_3$ of 12.8 dBm with $IM_3$ of 12.0 $dB_c$ for 65 nm node and 13.4 dBm with 11.5 $dB_c$ for 150 nm node are obtained at 5 GHz.

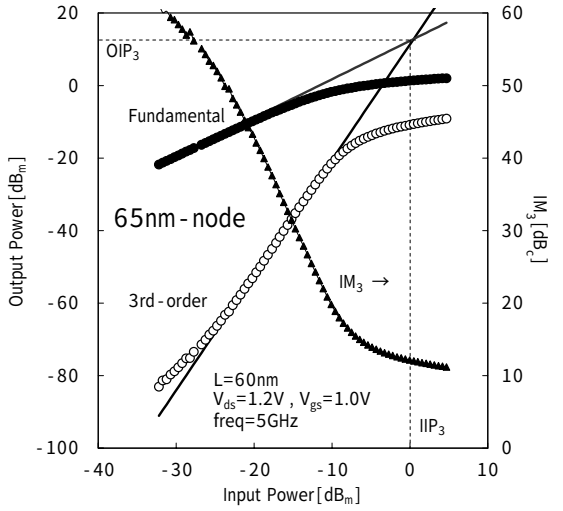
In addition, the third harmonic intercept voltage; $V_{IP3}$ was measured, which are given below.

$$V_{IP3i} = \frac{1}{\sqrt{3}} V_{IP3h} = \frac{1}{\sqrt{3}} \sqrt{24 \cdot \frac{g_m}{g_{m3}}} = \sqrt{8 \cdot \frac{g_m}{g_{m3}}} \quad \text{[V]} \qquad (4\text{-}8.a)$$

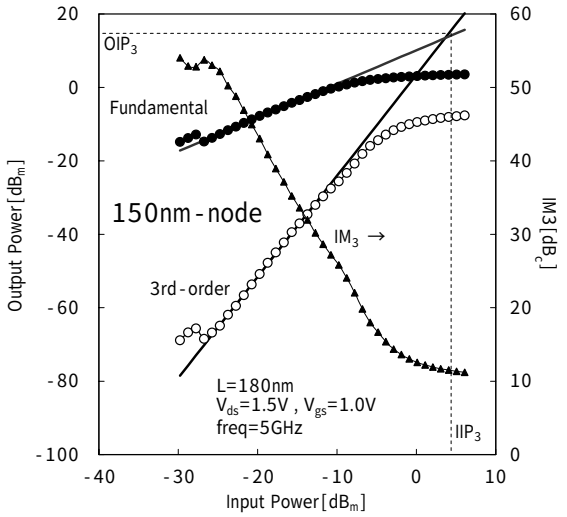
$$\text{where,} \quad g_{m3} = \frac{\partial^3 I_{ds}}{\partial^3 V_{gs}} \qquad (4\text{-}8.b)$$

$V_{IP3}$ is often used to measure the linearity, because it can be easily done with DC measurement. The index i of $V_{IP3i}$ is add in order to make a distinction with $V_{IP3h}$,

the 3-rd order intercept point for *harmonics* [4-17]. Figure 4-15 shows measured $V_{IP3}$ for 65nm and 150nm as a function of $V_{gs}$-$V_{th}$. Measured $OIP_3$ by load-pull system in Fig.4-14 is also indicated. Since $g_{m3}$ increases in a faster rate than $g_m$, the value of $V_{IP3}$ degrades as technology scaling down as shown in Fig.4-15 [4-18, 4-19].




(a) 65 nm node




(b) 150 nm node

*Fig.4-14. Measured two-tone distortion characteristics for (a)65 nm and (b)150nm node at 5 GHz for Δf=1 MHz.*

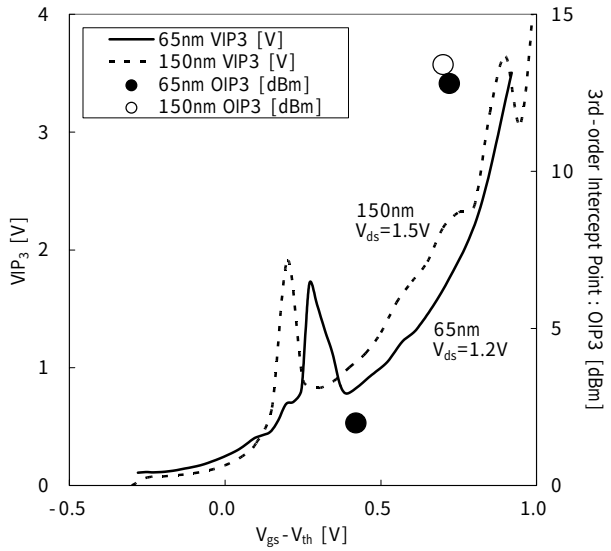



*Fig.4-15. Measured $VIP_3$ for 65 nm and 150 nm as a function of $V_{gs}$-$V_{th}$. Measured $OIP_3$ by load-pull system in Fig.4-14 is also indicated. Since $g_{m3}$ increases in a faster rate than $g_m$, the value of $VIP_3$ degrades as technology scaling down.*

## 4.5. Conclusion

The scaling effect of RF characteristics of the 65nm CMOS technology compatible with logic CMOS was investigated and compared with that of 150nm CMOS. The gate layout effect for the RF performance has been also investigated. To better understand the gate layout effect of RF performance, our analysis is performed at the same bias condition both of small and large signal measurement.

The Summary of RF Characteristics is summarized in Table 4-4.

As scaling continues, cut-off frequency ($f_T$) can be increased by scaling down the gate length, while maximum oscillation frequency ($f_{max}$) and minimum noise figure ($NF_{min}$) depend strongly on the parasitic components. $f_T$, $f_{max}$ and $NF_{min}$ have the dependency of gate finger length ($W_f$). Since the scaling of gate oxide thickness: $t_{ox}$ cannot be reduced as that of gate length:$L$, the intrinsic gain:$g_m/g_{ds}$ reduced as scaling continues. 1dB compression point ($P_{1dB}$) and third order intercept point ($IP_3$ ) degrade as technology scaling down, and the dependency of $W_f$ was not observed.

The results confirm the scaling effect of a comprehensive RF characteristics from 150 nm node to 65 nm node CMOS technology.

*Table 4-4 Summary of RF Characteristics*

| parameter | | unit | 150nm | 65nm | Finger length sensitivity |
|---|---|---|---|---|---|
| $f_T$ | cut-off frequency | GHz | 55 | 146 | v |
| $f_{max}$ | maximum oscillation frequency | GHz | 76 | 135 | v |
| $NF_{min}$ | minimum noise figure(@10GHz) | dB | 1.66 | 1.06 | v |
| $\gamma_{gm}$ | $g_m$ referenced excess noise factor | | 0.91 | 1.59 | - |
| $g_m/g_{ds}$ | Intrinsic gain(@10GHz) | | 14.6 | 10.4 | - |
| PAE | power-added efficiency(@5GHz) | % | 40.2 | 39.6 | v |
| $G_a$ | associated gain(@5GHz) | dB | 10.2 | 11.3 | - |
| $P_{1dB}$ | 1dB compression point(@5GHz) | dBm | - | 5.1 | - |
| $IP_3$ | 3rd-order intercept point(@5GHz) | dBm | 13.4 | 12.8 | - |

v : sensitive for gete layout optimizing
—: not sensitive

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# Chapter.5

# Effect of High Frequency Noise Current Sources on Noise Figure for Sub-50 nm node MOSFETs

## 5.1. Introduction

The downscaling of CMOS technology has resulted in strong improvement in RF performance of bulk and SOI MOSFETs [5-1, 5-2]. Owing to the progress of the RF performance of smaller geometry MOSFETs, the monolithic integration of both RF front-end and baseband circuits is now possible up to 2 or 5 GHz frequency regions with the RF mixed signal CMOS technology. Moreover, in the research level, even millimeter-wave applications can be implemented in pure CMOS process [5-3, 5-4, 5-5].

In order to realize a low-noise RF circuit, a deeper understanding of the noise performance for MOSFETs is required. Thermal noise is the main noise source of the CMOS device for high frequency performance, and is dominated by the drain channel noise, the induced gate noise, and their correlation noise. Because MOSFETs and MESFETs are very similar in their small-signal equivalent noise model, one can apply the results of historical studies of high-frequency noise behavior of the MESFETs to MOSFETs.

In this chapter, the RF noise parameter ($F_{min}$, $R_n$, $\Gamma_{opt}$) of 45 nm node MOSFETs were measured from 5 to 15 GHz. Then, The noise values — the drain channel noise $\overline{i_d^2}$, the induced gate noise $\overline{i_g^2}$ and their correlation noise $\overline{i_g i_d^*}$ —from S-parameters and noise parameters were extracted by using noisy

two-port theory. Next, the noise coefficients *P*, *R*, and *C* were extracted by using an extended van der Ziel's model. After that, the extracted noise coefficients of the 45 nm node MOSFETs versus frequency, bias condition, and gate length are presented. Finally, the effect of noise coefficients on noise figure is discussed.

## 5.2. Noise Theory

### 5.2.1. Van der Ziel model

Van der Ziel, in his pioneering work, first analyzed noise in field-effect transistors and formulated the equation of the drain channel noise $\overline{i_d^2}$ , the induced gate noise $\overline{i_g^2}$ , and their correlation noise $\overline{i_g i_d^*}$ [5-6],[5-7]. The noise equivalent circuit of an FET is illustrated in Fig.5-1(a). Baechtold expressed the van der Ziel model using drain noise coefficient; *P*, induced gate noise coefficient; *R*, and their correlation coefficient; *C* [5-8].

$$\overline{i_d^2} = 4kT_0\Delta f \cdot g_m \cdot P \tag{5-1}$$

$$\overline{i_g^2} = 4kT_0\Delta f \cdot (\omega^2 C_{gs}^2 / g_m) \cdot R \tag{5-2}$$

$$\overline{i_g i_d^*} = j \cdot C\sqrt{\overline{i_g^2}}\sqrt{\overline{i_d^2}} = j \cdot 4kT_0\Delta f \cdot \omega\, C_{gs} \cdot C\sqrt{PR} \tag{5-3}$$

where $k$ is the Boltzmann constant, $T_0$ is the lattice temperature, $\Delta f$ is the bandwidth, $g_m$ is the transconductance, $C_{gs}$ is the gate-source capacitance, $j$ is the imaginary unit and the asterisk defines the complex conjugate.

The van der Ziel model shows two important features.

1) The power spectral density of the drain noise current source, $\overline{i_d^2}$ is frequency-independent. Indeed at high frequency, the noise in FET is diffusion noise of the conducting channel and the power spectrum of such a noise is “white” in the commonly used operating frequencies.

2) The real part of the correlation between the gate and drain current noise sources, $\overline{i_g i_d^*}$ is small as compared with the imaginary part. Therefore the complex correlation coefficient is mainly imaginary.

These specific features show that FET is a particular noisy two-port; its high-frequency noise properties can be calculated using simplified noise models.

5.2.2. Pucel's Noise Model

According to Pucel's analysis, the minimum noise figure $F_{min}$ and other noise parameters of the FET can be given as below [5-9].

$$F_{\min} = 1 + 2\sqrt{P + R - 2C\sqrt{PR}} \cdot \frac{f}{f_C} \cdot \sqrt{g_m\left(R_g + R_s\right) + \frac{PR(1-C^2)}{P + R - 2C\sqrt{PR}}} \quad \text{(5-4.a)}$$

$$g_n = g_m\left(\frac{f}{f_c}\right)^2 \cdot \sqrt{P + R - 2C\sqrt{PR}} \quad \text{(5-4.b)}$$

$$Z_{opt} = \sqrt{\frac{g_m\left(R_s + R_g\right) + \frac{PR\left(1-C^2\right)}{P + R - 2C\sqrt{PR}}}{P + R - 2C\sqrt{PR}}} \cdot \frac{1}{C_{gs}\omega} + \frac{1}{jC_{gs}\omega} \cdot \left(\frac{P - C\sqrt{PR}}{P + R - 2C\sqrt{PR}}\right) \quad \text{(5-4.c)}$$

where $R_g$, $R_s$ are the gate resistance and the source resistance, respectively. $f_c$ is the intrinsic cut-off frequency ($f_c = g_m/2\pi C_{gs}$), $g_n$ is the noise conductance, $Z_{\text{opt}}$ is

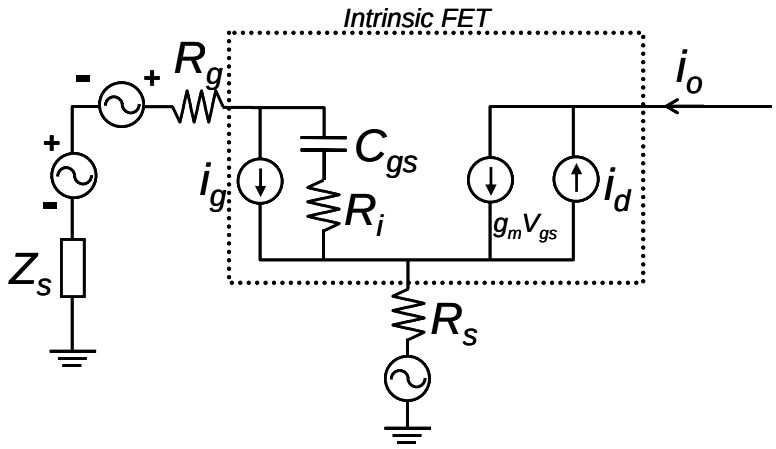
the optimum input impedance. If access resistance $R_g$+$R_s$ tends to zero, Eq.(5-4.a) can be simplified as

$$F_{\min} = 1 + 2\frac{f}{f_C}\sqrt{PR(1-C^2)} \tag{5-5}$$

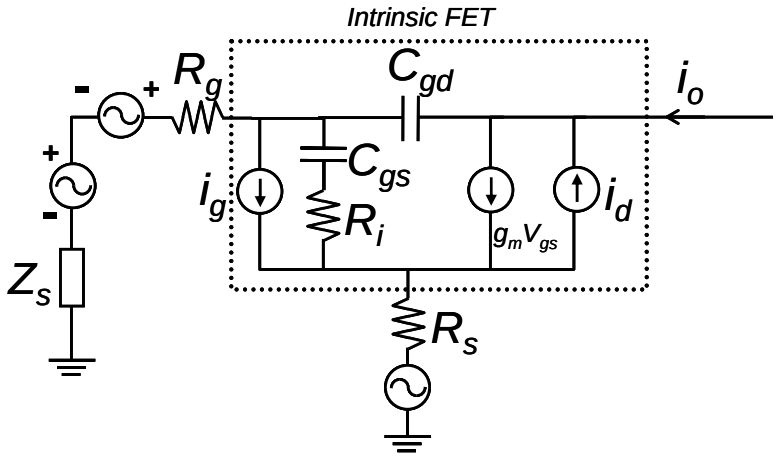
The so-called "Fukui's equation" is obtained by neglecting induced gate noise ($R$=0), and assuming a correlation coefficient close to unity in Eq.(5-4.a) [5-10, 5-11, 5-12].

$$F_{\min} = 1 + K_f \cdot \frac{f}{f_C}\sqrt{g_m(R_g + R_S)}, \qquad K_f = 2\sqrt{P} \tag{5-6}$$

This equation involves an empirical Fukui's noise figure coefficient $K_f$, which corresponds to $2\sqrt{P}$. Since Fukui's equation is simple and suggestive, it has been widely used in interpretation and modeling of noise properties of GaAs MESFETs and more recently in MOSFETs.




*(a) Simplified equivalent noise circuit*




*(b) Complete equivalent noise circuit*

*Fig.5-1. Noise equivalent circuits for FETs.*

## 5.3. Methodology and Experimental Procedures

In this chapter, we fabricated multi-finger n-MOSFETs using 45 nm node CMOS technology. The gate length ranges from 40 nm to 480 nm and unit gate finger length ($W_f$) is 1 μm with the total gate width of 128 μm to compare the noise performance.

First, the van der Ziel model is extended to be applicable to short channel devices. Figure 5-2 illustrates a gate-source capacitance; $C_{gs}$ and a gate-drain capacitance; $C_{gd}$, as a function of gate length for the n-MOSFETs with gate width $W$=128 μm and gate length $L$ = 480 nm, 160 nm, 70 nm and 40 nm, respectively. When the gate length decreases, the gate-source capacitance decreases as the gate area decreases. On the other hand, gate-drain capacitance, which contains the overlap capacitance of the 'gate to lightly doped drain (LDD)' region and the outer/inner fringing capacitance of the 'gate to drain' region, is less affected by the gate scaling, and a $C_{gd}$ is comparable with a $C_{gs}$ for sub-50 nm device. Since the induced gate noise is due to capacitance coupling of drain noise onto the gate electrode, one should not neglect the gate-drain capacitance; $C_{gd}$.

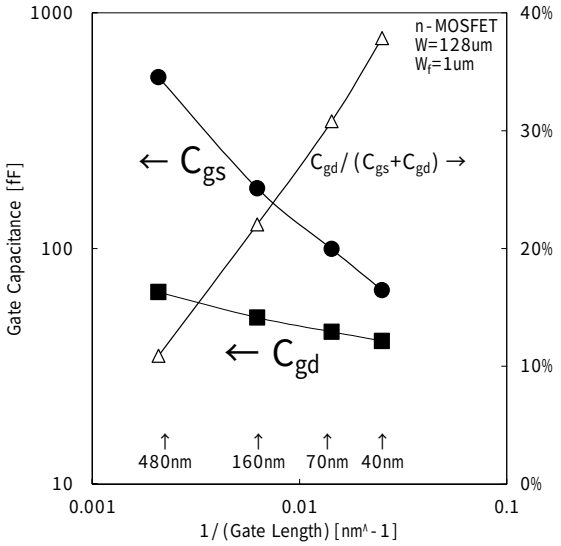



*Fig.5-2. The gate-source capacitance; $C_{gs}$ and the gate-drain capacitance; $C_{gd}$, as a function of gate length for the n-MOSFETs with gate width W=128 μm and gate length L = 480 nm, 160 nm, 70 nm and 40 nm, respectively.*

We can apply the same sort of van der Ziel theory is applied to the complete noise equivalent circuit in Fig.5-1(b), and obtain "extended van der Ziel model" as below.

$$\overline{i_d^2} = 4kT_0\Delta f \cdot g_m \cdot P \tag{5-7}$$

$$\overline{i_g^2} = 4kT_0\Delta f \cdot g_m \cdot R \cdot \left(\frac{f}{f_T}\right)^2 \tag{5-8}$$

$$\overline{i_g i_d^*} = j \cdot 4kT_0\Delta f \cdot g_m \cdot C\sqrt{PR} \cdot \left(\frac{f}{f_T}\right) \tag{5-9}$$

where $f_T$ is cut-off frequency : $f_T=g_m/2\pi(C_{gs}+C_{gd})$. We can also apply the noise parameters: $P$, $R$, and $C$ to Eqs.(5-4.a) and (5-5). When $C_{gd} << C_{gs}$, $f_C = f_T$ and the Eqs.(5-7)-(5-9) corresponds to Eqs.(5-1)-(5-3).

Next, the RF noise parameter (minimum noise figure $F_{min}$, equivalent noise resistance $R_n$, and the optimized source reflection coefficient $\Gamma_{opt}$) were measured from 5 to 15 GHz and the de-embedding techniques based on the noise correlation matrix [5-13],[5-14] were applied to extract intrinsic device characteristics. These noise parameters were extracted from fitting noise circles to the measured NF values of at least 5 mechanical-tuner positions, each of 64 points averaging. After the noise parameters of two-port devices are specified, the drain channel noise $\overline{i_d^2}$, the induced gate noise $\overline{i_g^2}$ and their correlation noise $\overline{i_g i_d^*}$ are obtained as follows [15],[16] ;

$$\overline{i_d^2} = 4kT_0\Delta f \cdot R_n \left|Y_{21}\right|^2 \tag{5-10}$$

$$\overline{i_g^2} = 4kT_0\Delta f \cdot R_n \left\{ \left|Y_{opt}\right|^2 - \left|Y_{11}\right|^2 + 2\Re\left[\left(Y_{11} - Y_{cor}\right)Y_{11}^*\right]\right\} \tag{5-11}$$

$$\overline{i_g i_d^*} = 4kT_0\Delta f \left(Y_{11} - Y_{cor}\right)R_n Y_{21}^* \quad . \tag{5-12}$$

where $\Re$ [ ] denotes the real part of [ ] , $Y_{opt}$ is the optimal source admittance, and $Y_{cor}$ is the correlation factor given by

$$Y_{cor} = \frac{F_{\min} - 1}{2R_n} - Y_{opt} \tag{5-13}$$

Next, the noise coefficients *P*, *R*, and *C* were extracted by comparing equations with (5-10)-(5-12) and extended van der Ziel's model (5-7)-(5-9). After that, the extracted noise coefficients of the 45 nm node n-MOSFETs versus frequency, bias condition, and gate length are presented and the effect of noise coefficients on the noise figure is discussed.

## 5.4. Experimental Results and Discussions

Figure 5-3 shows the extracted drain noise $\overline{i_d^2}$, gate induced noise $\overline{i_g^2}$, and their correlation noise $\overline{i_g i_d^*}$ versus frequency characteristics for n-MOSFETs with gate width *W*=128 μm and gate lengths *L*=40 nm biased at $V_{ds}$=1.2 V and $V_{gs}$=1.0 V. It was confirmed that $\overline{i_d^2}$ is independent of frequency, that $\overline{i_g^2}$ increases in proportion to frequency-squared, and that $\overline{i_g i_d^*}$ increases in proportion to frequency, as van der Ziel model described. Therefore, the dominant component of the $\overline{i_g^2}$ can be considered as the noise due to the gate resistance and the shot noise induced by the gate leakage current can be negligible within the measured frequency range.

Figure 5-4 indicates the $\overline{i_d^2}$, $\overline{i_g^2}$, and $\overline{i_g i_d^*}$ as a function of gate length for the n-MOSFETs with gate width $W$=128 μm and gate length $L$ = 480 nm, 160 nm, 70 nm and 40 nm, respectively, biased at $V_{ds}$ = 1.2 V and $V_{gs}$=1.0 V at 10 GHz. It is shown that the drain channel noise increases when the gate length decreases. When the gate length decreases, both the induced gate noise and the correlation noise also decrease from $L$=480 nm to 160 nm.

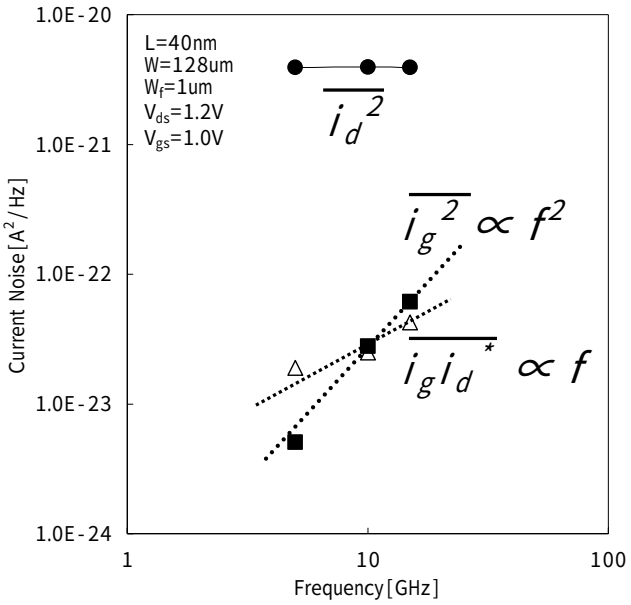



*Fig.5-3. The extracted drain noise* $\overline{i_d^2}$ *, gate induced noise* $\overline{i_g^2}$ *, and their correlation noise* $\overline{i_g i_d^*}$ *versus frequency characteristics for n-MOSFETs with gate width W=128 μm and gate lengths L=40 nm biased at* $V_{ds}$*=1.2 V and* $V_{gs}$*=1.0 V.*

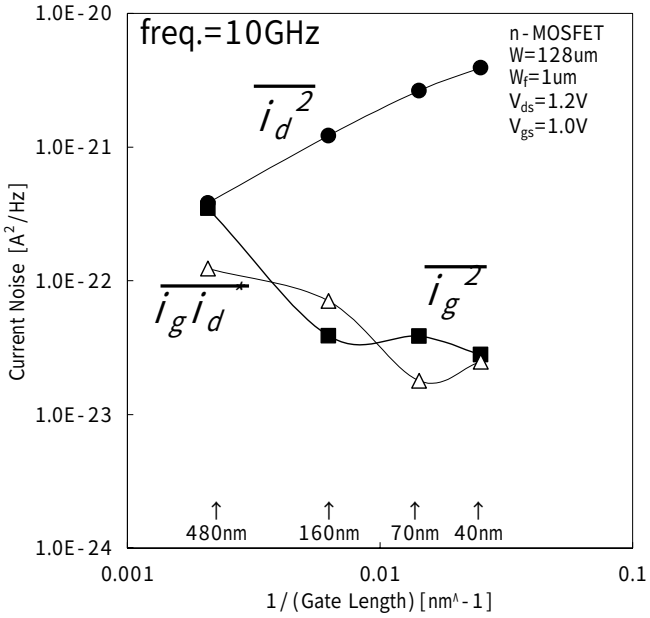



*Fig.5-4. The* $\overline{i_d^2}$ , $\overline{i_g^2}$ , *and* $\overline{i_g i_d^*}$ *as a function of gate length for the n-MOSFETs with gate width W=128 μm and gate length L = 480 nm, 160 nm, 70 nm and 40 nm, respectively, biased at* $V_{ds}$ *= 1.2 V and* $V_{gs}$*=1.0 V at 10 GHz.*

This trend is in agreement with the measurement results of *L*=970 nm to 180 nm for 0.18 μm CMOS in [5-17], and *L*=250 nm to 70 nm in [5-18]. On the other hand, it is noted that $\overline{i_g^2}$ is saturated and $\overline{i_g i_d^*}$ increases when the gate length decreases from *L*=70 nm to 40 nm, as can be seen in Fig.5-4. Since it was confirmed that noise coefficients are independent of frequency, the details of frequency dependence were not indicated hereafter.

Figure 5-5 indicates the noise coefficients *P*, *R*, and *C*, which are extracted by Eqs (5-7)-(5-9) and (5-10)-(5-12), as a function of gate length for the same device parameters as for Fig.5-4, biased at $V_{ds}$ =1.2 V at 10 GHz. In fact, several papers have reported that the correlation noise coefficient *C* is a positive value, and decreases when the gate length is reduced [5-17, 5-19]. It was found, for the first time, that *C* decreases *from positive to negative values* when the gate length is reduced continuously, and it thus follows that the gate length dependence of the correlation noise $\overline{i_g i_d^*}$ has an inflection point around *L*=70 nm, as can be seen in Fig.5-4. In addition, this trend can be explained by the simulation results that the absolute value of *C* increases when the gate length is reduced [5-19, 5-20]. Let $Lc_0$ be the gate length where the correlation noise coefficient *C* equals zero. It seems that $Lc_0$ of 45 nm node n-MOSFETs exists within 70 nm to 40 nm, as can be seen in Fig.5-5.

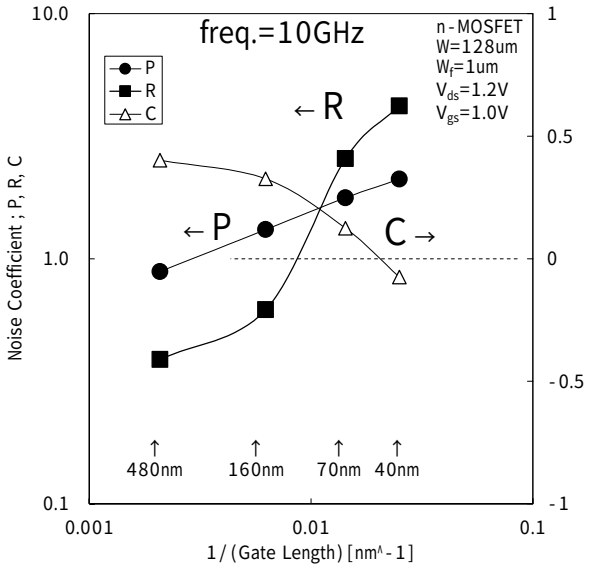
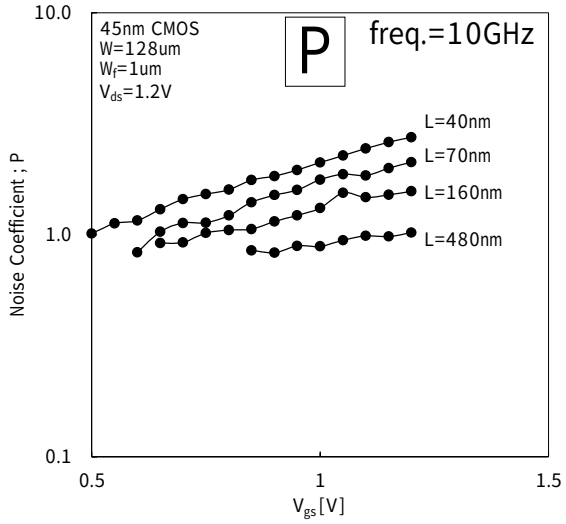


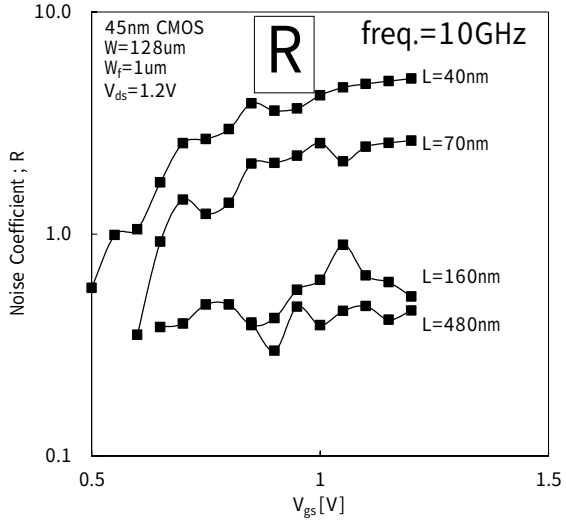

*Fig.5-5. The noise coefficients P, R, and C ,which are extracted by Eqs. (5-7)-(5-9) and (5-10)-(5-12), as a function of gate length for the same device parameters as for Fig.5-4 at 10 GHz.*

The gate noise coefficient *R* increases sharply when the gate length is reduced. While the induced gate noise $\overline{i_g^2}$ is two orders of magnitude lower than that of drain channel noise $\overline{i_d^2}$ for *L*=40 nm, the gate noise coefficient *R* is obtained two times as large as the drain noise coefficient *P*. Since the cut-off frequency: $f_T$ is around 200 GHz , the value of $(f/f_T)^2$ is around 1/400 at *f*=10 GHz in Eq.(5-8). This is because *R* is comparable with *P*. Therefore, it is obvious that

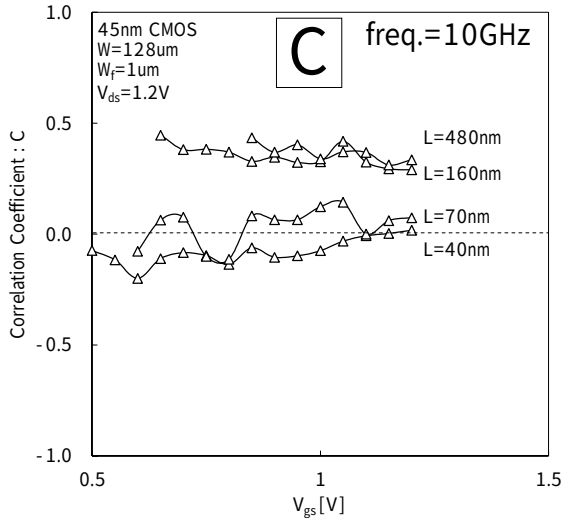
one should not neglect the gate noise and the correlation noise in short-channel MOSFET noise analysis.




*(a) The drain noise coefficient; P.*




*(b) The induced gate noise coefficient; R.*




*(c) The correlation coefficient; C.*

*Fig.5-6. The noise coefficients P, R, and C as a function of $V_{gs}$ for the same device parameters as for Fig.5-4, biased at $V_{ds}$ = 1.2 V at 10 GHz .*

Figure 5-6 shows the noise coefficients *P*, *R*, and *C* as a function of gate-to-source voltage $V_{gs}$ for the same device parameters as for Fig.5-4. It is shown that the induced gate noise coefficient *R* has a strong bias dependence, especially in the case of *L*=40 nm, but the drain noise coefficient *P* and the correlation noise coefficient *C* have a weak bias dependence. *C* decreases, namely the absolute value of *C* increases where the pinch-off region accounts for a big part of the channel at low currents[5-21], especially in the case of *L*=40 nm and 70 nm.

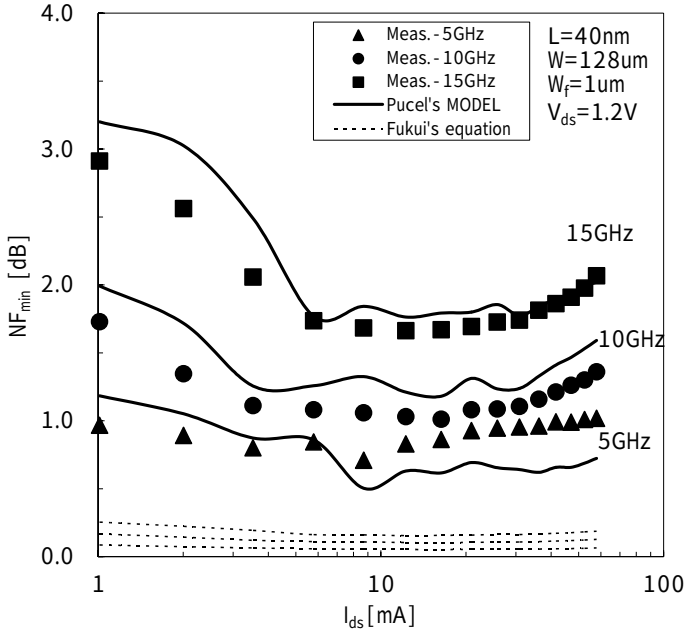



*Fig.5-7. The minimum noise figure measured and calculated from noise coefficients P, R, and C versus the drain current with gate width W=128 μm and gate lengths L=40 nm biased at $V_{ds}$ =1.2 V at 5,10,15 GHz, respectively.*

A comparison between noise figure measured and calculated from noise coefficients versus drain current is shown in Fig.5-7, with gate width *W*=128 μm and gate lengths *L*=40 nm under bias conditions at $V_{ds}$ = 1.2 V at 5, 10, and 15 GHz, respectively. The Fukui's equation predicts lower noise figure than the data measured due to neglecting induced gate noise, and access resistance, $R_g$+$R_s$, close to zero for 45 nm node n-MOSFET.

It was confirmed that Pucel's equation (5-4.a), using noise coefficients *P*, *R*, and *C* from extended van der Ziel model, can be considered a good approximation even for sub-50 nm MOSFETs.

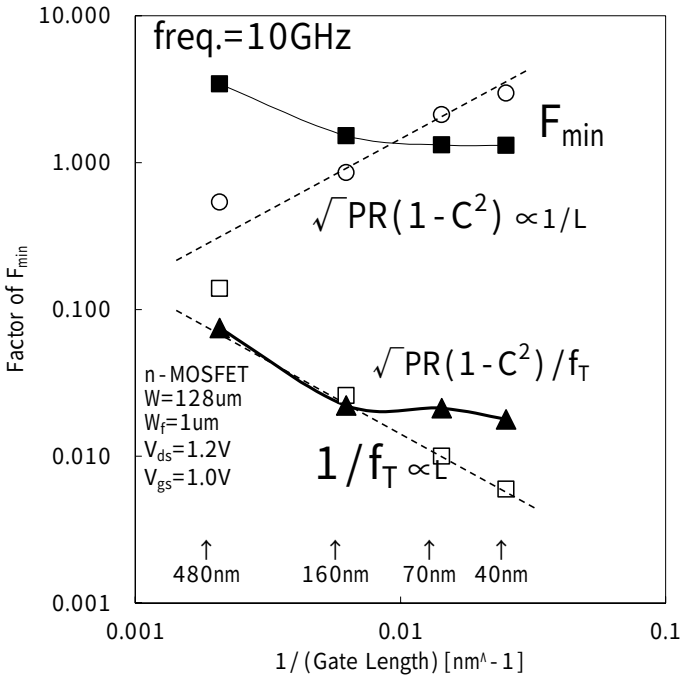



*Fig.5-8. The factors of noise figure for Eq.(5-5).*

In addition, the influence of noise coefficients *P*, *R*, and *C* on the minimum noise figure is examined. Figure 5-8 shows the factors of noise figure for Eq.(5-5). Since $f_T$ and the factor $\sqrt{PR(1-C^2)}$ is proportional to $1/L$ when $Lc_0 > L$ , the factor $\sqrt{PR(1-C^2)}/f_T$ is saturated. $Lc_0$ also indicates the saturation point of minimum noise figure.

It was confirmed that $Lc_0$ plays a very important role in the determination of the saturation point of minimum noise figure at fixed bias point, as shown in Fig.5-8.

## 5.5. Scaling Effect on the Minimum Noise Figure

Recently, several approaches have been presented to formulate an analytical expression for thermal noise in short-channel MOSFETs [5-22～5-25]. Triantis' noise model is based on the consideration that the channel of MOSFETs is separated into two consecutive regions; a gradual channel approximation region and a velocity saturation region [5-22, 5-23]. This approach is phenomenologically equivalent in [5-26]. Triantis' model is expressed by only DC parameters. In this section, the detail of Triantis' model is explained and a scaling effect of the noise coefficients is discussed, especially the correlation noise coefficient *C* on the minimum noise figure.

### 5.5.1 Triantis' Noise Model

Triantis' approach that has been followed for the analytical modeling of the thermal noise, is based on the consideration that two consecutive regions exist between the source and drain of a saturated short-channel MOSFET ,as shown in Fig.5-9. These regions are as follows:

*Region-1*: a gradual channel approximation region

*Region-2*: a velocity saturation region

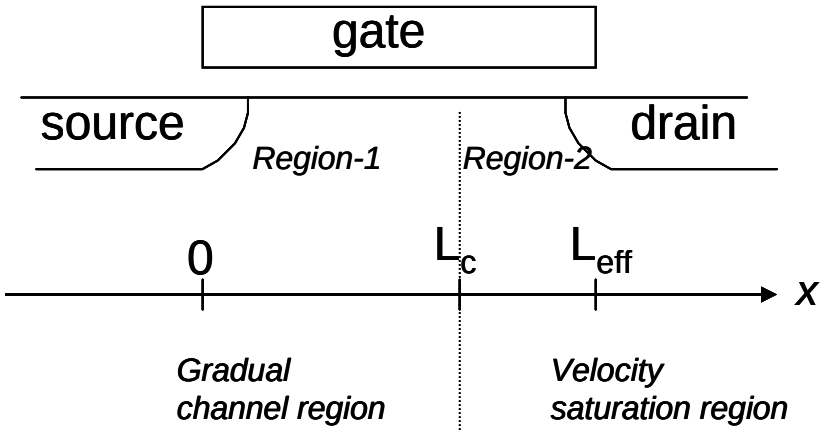



*Fig.5-9. Schematic representation of the channel separation of a submicron MOSFET into a gradual channel approximation region-1 and a velocity saturation region-2*

(1) The drain current

According to [5-22] and [5-23], the thermal noise of the drain current of a short channel MOSFET is efficiently calculated, as follows.

$$\overline{i_d^2} = \frac{4k_B T_0}{\alpha I_{ds}} \times \left( \frac{2}{3} P_{D1} \cosh^2(AL_{SAT}) + \frac{\alpha E_C}{A} P_{D2} \right) g_{ds}^2 \cdot \Delta f \tag{5-14}$$

where $A$ is a function of the gate oxide thickness and the substrate doping [see Eq.(5-25)], $L_{SAT}$ is the length of the velocity saturation region, which is so-called "pinch-off length", $i_{ds}$ is the drain current, $g_{ds}$ is the channel's conductance,

$\alpha$ is a constant near unity and accounts for the channel charge effect on the threshold voltage [5-27].

The polynomial $P_{D1}$ of the drain current noise originating in *region-1* is;

$$P_{D1} = \frac{1}{4V_0}\left[4\alpha V_0 E_C L_C - V_1^2 - 3\delta V_0^2 + \frac{V_1^3 + 3\delta V_0^2 V_1}{V_0}\right], \tag{5-15}$$

while $P_{D2}$ for *region-2* noise is

$$P_{D2} = 2\left[P_0 \sinh\left(AL_{SAT}\right) - P_1 AL_{SAT} \cosh\left(AL_{SAT}\right)\right], \tag{5-16}$$

where $P_0$ and $P_1$ are given by Taylor series form and the first four terms taken into consideration, as follows.

$$P_0 = e^{\lambda}\left(p_{01} + A^2 L_{SAT}^2 p_{02} + A^4 L_{SAT}^4 p_{03} + A^6 L_{SAT}^6 p_{04}\right) \tag{5-17}$$

$$p_{01} = 1 + 3\lambda + 18\lambda^2 + 15\lambda^3$$

$$p_{02} = 1.5\lambda + 9\lambda^2 + 7.5\lambda^3$$

$$p_{03} = 0.75\lambda^2 + 0.62\lambda^3$$

$$p_{04} = 0.02\left(\lambda^2 + \lambda^3\right)$$

$$P_1 = \lambda e^{\lambda}\left(p_{11} + A^2 L_{SAT}^2 p_{12} + A^4 L_{SAT}^4 p_{13}\right) \tag{5-18}$$

$$p_{11} = 3 + 18\lambda + 15\lambda^2$$

$$p_{12} = 0.33 + 3\lambda + 2.5\lambda^2$$

$$p_{13} = 1 + 0.125\lambda + 0.125\lambda^2$$

$\delta$ is an empirical constant which turn out to be in the range of 5 - 20 for values of *Ec* in the range of 2-4 V/μm . Parameters $\delta$ and $\lambda$ are not independent but they follow the relation $\delta = 2e^{\lambda} - 1$.

(2) The gate noise current

According to [5-23], the total gate noise current caused by *region-1* and *region-2* is

$$\overline{i_g^2} = \frac{\omega^2 W^2 C_{ox}^2 k_B T_0}{3\alpha^3 I_{ds}^3} \times \left( \frac{P_{G1} \cosh^2(AL_{SAT})}{2} + \frac{P_{G2} E_C}{A} \right) g_{ds}^2 \cdot \Delta f \tag{5-19}$$

where the quantity $P_{G1}$ is primarily a function of $V_{GT}=V_{GS}$ - $V_{TH}$ .

$P_{G1}$ is calculated as;

$$P_{G1} = P_3^2 I_{G11} + \beta^2 L_C^2 I_{G12} + 2\beta L_C P_3 I_{G13} \tag{5-20}$$

$$P_3 = \frac{V_0 V_3^2 - V_1^3}{6\alpha V_0 E_C} + 2\alpha V_0 L_{SAT} \tag{5-21}$$

$$I_{G11} = \frac{V_1^3 - V_0^3 + 3\delta V_0^2 (V_1 - V_0)}{6\alpha V_0^3 E_C}$$

$$I_{G12}=\frac{1}{6\alpha V_0 E_C}\left[\frac{3V_1^5}{5V_0^2}+V_1^3(1+\delta)+3\delta V_1 V_0^2-6\alpha V_0^2 E_C L_C\left(1+\frac{V_1^2}{V_0^2}\right)-4\delta V_0^3-12\delta\alpha V_0^2 E_C L_C-\frac{8}{5}V_0^3\right]$$

$$I_{G13}=\frac{1}{6\alpha V_0^3 E_C}\left[6\alpha E_C L_C V_0\left(V_1^2+\delta V_0^2\right)+V_0^4(1+3\delta)-3V_1V_0^3-V_1^3V_0-12\alpha^2E_C^2L_C^2V_0^2\right]$$

where $W$ is channel width , $C_{ox}$ is the gate capacitance per unit area, $L_c$ is the length of *region-1*: $L_C=L_{eff}-L_{SAT}$ , $\beta$ accounts for the potential at the end of *region-1* , *Ec* is the electric field at $x=L_C$ . The quantities $V_0$, $V_1$, $V_3$ are respectively: $V_0=V_{GT}-\alpha V_C$ , $V_1=V_{GT}+\alpha V_C$ , and $V_3=\sqrt{V_1^2+2\alpha V_0 E_C L_C}$ with $V_{GT}=V_{GS}-V_{TH}$ .

The quantity $P_{G2}$ is equal to $P_{G2}=\alpha P_1^2 P_{D2}$ where $P_{D2}$ is a component of the noise originating in *region-2* and is given below.

(3) The cross correlation coefficient

The cross correlation coefficient for $\overline{i_d^2}$ ,and $\overline{i_g^2}$ is given by:

$$C = \frac{\left( \frac{P_{GD1}\cosh^2(AL_{SAT})}{3\alpha E_C^2} + \frac{2E_C P_{GD2}}{A} \right)}{\left( \frac{P_{G1}\cosh^2(AL_{SAT})}{2} + \frac{E_C P_{G2}}{A} \right)^{\frac{1}{2}} \cdot \left( \frac{2}{3} P_{D1}\cosh^2(AL_{SAT}) + \frac{\alpha E_C}{A} P_{D2} \right)^{\frac{1}{2}}} \tag{5-22}$$

The quantity $P_{GD1}$ is calculated as

$$P_{GD1} = k_3 V_1^3 + \beta L_C^2 V_1^2 + k_1 V_1 + k_0 \tag{5-23}$$

$$k_3 = P_1 - \beta L_C V_0 \quad , \quad k_1 = 3\delta V_0^2 \left( P_1 - \beta L_C V_0 \right)$$

$$k_0 = \beta L_C V_0^4 \left( 3\delta + 1 \right) - V_0^3 (3\delta P_1 - 6\delta\beta\alpha L_C^2 E_C + P_1) - 12\beta\alpha^2 V_0^2 E_C^2 L_C^3$$

and finally, $P_{GD2} = P_1 P_{D2}$ .

5.5.2. Scaling Effect on the Correlation Noise Coefficient

The gate induced noise $\overline{i_g^2}$, and correlation noise $\overline{i_g i_d^*}$ from measurement DC data of 45 nm node n-MOSFETs were calculated using Triantis' model. A comparison between noise sources measured and calculated from Triantis' model versus gate length is shown in Fig.5-10. While the data measured and calculated show a large deviation, it was confirmed that $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ have the inflection points both of measurement data and Triantis' model at the same gate length.

An influence of each factor for Triantis' model is examined, and it turned out that the parameter in the velocity saturation region, named $P_{D2}$, plays an important role in the determination of inflection points.

$$P_{D2} = 2\left[ P_0 \sinh\left( \frac{L_{SAT}}{l_t} \right) - P_1 \frac{L_{SAT}}{l_t} \cosh\left( \frac{L_{SAT}}{l_t} \right) \right] \tag{5-24}$$

When $P_{D2}$=0 in Eq.(5-24), both of $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ reach the inflection points, and the correlation coefficient $C$=0. Figure 5-10 indicates the dependence of $L_{SAT}$ as a function of gate length for the n-MOSFETs with gate width $W$=128 μm and gate length $L$= 480 nm, 230 nm, 160 nm, 110 nm, 70 nm and 40 nm, respectively, biased at $V_{ds}$ = 1.2 V and $V_{gs}$=1.0 V. When the gate length is reduced, $L_{SAT}$ is also reduced, and the ratio of $L_{SAT}$ ($L_{SAT}/L_g$) increases conversely. The pinch-off length accounts for 22% of the gate length with $L$=40 nm, as shown in Fig.5-11. $P_0$ and

$P_1$ are the quantities with respect to the noise temperature given in [5-23], and less relevance to technology node.

On the other hand, the parameter $l_t$ has strong relevance to technology node as follows [5-28] ;

$$l_t = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO2}} \cdot x_j \cdot t_{ox}} \tag{5-25}$$

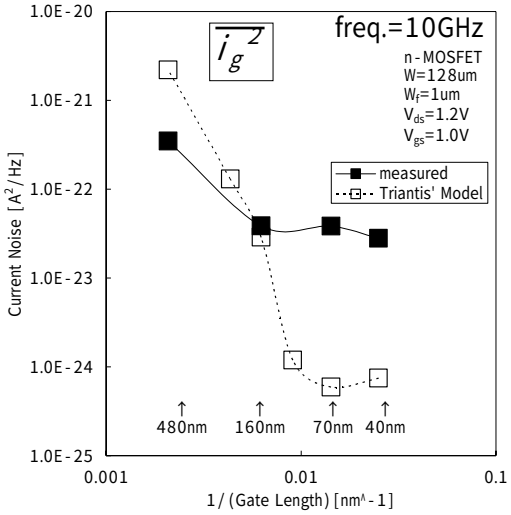
$$A = \frac{1}{l_t}$$

where $x_j$ is the junction depth, $t_{ox}$ is gate-oxide thickness ,$\varepsilon_{ox}$ and $\varepsilon_{sio2}$ is dielectric permittivity of $SiO_2$ and Si , respectively.

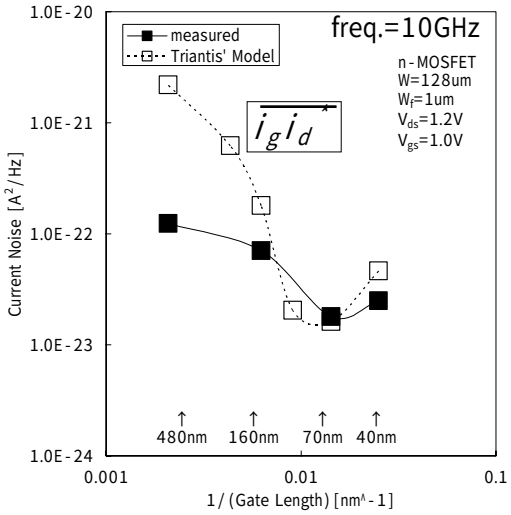
Substituting $P_{D2}$ for zero in Eq.(5-24), we can obtain

$$\frac{P_0}{P_1} \cdot \left( \frac{l_t}{L_{SAT}} \right) \tanh \left( \frac{L_{SAT}}{l_t} \right) = 1 \ . \tag{5-26}$$

Figure 5-11 shows the left terms of Eq.(5-26) for 45 nm and 65 nm node CMOS, biased at $V_{ds}$=1.2 V and $V_{gs}$=1.0 V. The value of $Lc_0$, which is the gate length where the correlation noise coefficient $C$ equals zero, can be determined by the left term equals to 1. The left term is strongly relevance to technology node due to the parameter $l_t$. As scaling continues, $Lc_0$ is reduced as can be seen in Fig.5-12.




*(a) Induced gate noise :* $\overline{i_g^2}$




*(b) Correlation noise :* $\overline{i_g i_d^*}$

*Fig.5-10. A comparison between noise sources measured and calculated from Triantis' model versus gate length: (a) Induced gate noise :* $\overline{i_g^2}$ *(b) Correlation noise :* $\overline{i_g i_d^*}$ .

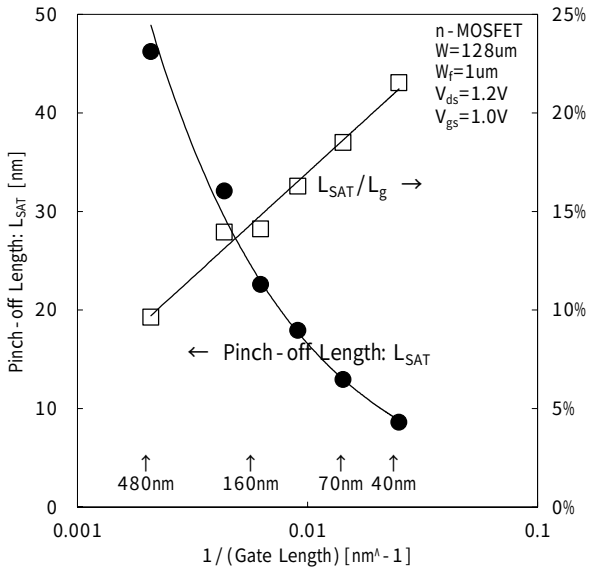



*Fig.5-11. The dependence of pinch-off length $L_{SAT}$ and the ratio of $L_{SAT}$ ($L_{SAT}/L_g$) as a function of gate length for the n-MOSFETs with gate width W=128 μm and gate length L = 480 nm, 230 nm, 160 nm, 110 nm, 70 nm and 40 nm, respectively, biased at $V_{ds}$ = 1.2 V and $V_{gs}$=1.0 V.*

The values of $L_{C0}$ are estimated as 70 and 120 nm for 45 and 65 nm nodes, respectively. It was pointed out in the previous section that $Lc_0$ indicates the saturation point of minimum noise figure. In the case of sub-micron technology node which has the positive correlation coefficient *C*, the minimum allowed gate length $L_{min}$ is larger than $Lc_0$, and the lowest value of the minimum noise figure is obtained at $L_{min}$. On the other hand, for sub-100nm node, since the correlation

coefficient $C$ reaches zero before the gate length is larger than $L_{min}$, it does not necessarily follow that the lowest value of the minimum noise figure is obtained at $L_{min}$. One should have a careful attention for selection of device geometries to design low noise amplifier and maximize noise performance.

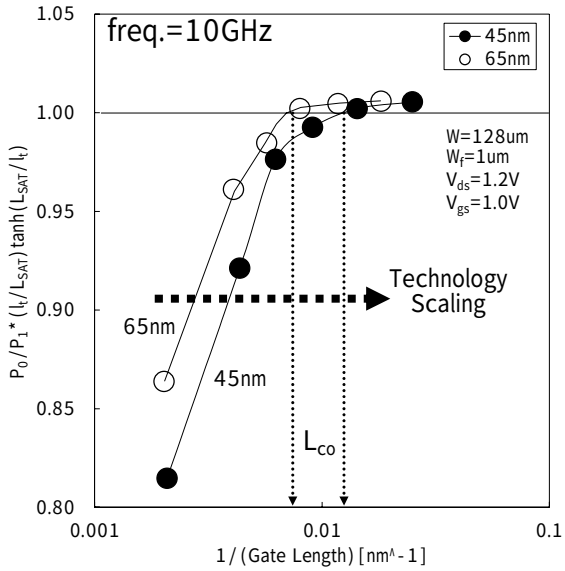



*Fig.5-12. The left term of Eq.(5-26) for 45 nm and 65 nm node CMOS, biased at $V_{ds}$=1.2 V and $V_{gs}$=1.0 V. $Lc_0$, which is the gate length where the correlation noise coefficient C equals zero, can be determined by the left term equals to 1.*

## 5.6. Conclusion

In this chapter, the RF noise parameter ($F_{min}$, $R_n$, $\Gamma_{opt}$) of 45 nm node MOSFETs were measured from 5 to 15 GHz and extracted noise sources and noise coefficients *P*, *R*, and *C* by using an extended van der Ziel's model. It was found, for the first time, that correlation coefficient *C* decreases *from positive to negative values* when the gate length is reduced continuously with the gate length of sub-100nm. It was confirmed that Pucel's noise figure model, using noise coefficients *P*, *R*, and *C*, can be considered a good approximation even for sub-50 nm MOSFETs. A scaling effect of the noise coefficients is also discussed, especially the correlation noise coefficient *C* on the minimum noise figure. It was confirmed that $Lc_0$, which is the gate length where the correlation noise coefficient *C* equals zero, indicates the saturation point of minimum noise figure.

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# Chapter.6

# Equivalent Noise Temperature Representation for Scaled MOSFETs

## 6.1. Introduction

The downscaling of CMOS technology has resulted in strong improvement in RF performance of MOSFETs. In order to realize a low-noise RF circuit, a deeper understanding of the noise performance for MOSFETs is required. Thermal noise is the main noise source of the CMOS device for high frequency performance, and is dominated by the drain channel noise, the induced gate noise, and their correlation noise. Since the minimum noise figure is small value in unit of dB for the sub-50nm device, the equivalent noise temperature representation can be useful to evaluate the noise performance.

In this chapter, a novel representation of the thermal noise for equivalent noise temperature was proposed by applying an extended van der Ziel's model. The noise temperatures of the 45 nm node n-MOSFETs versus gate length were extracted. A comparison between the proposed representation and Pospieszalski's model is also performed. Finally, a physical validity of proposed representation for equivalent noise temperature are discussed, especially for drain noise temperature, $T_d$.

## 6.2. Equivalent Noise Temperature Model

Van der Ziel, in his pioneering work, first analyzed noise in field-effect transistors and formulated the equation of the drain channel noise $\overline{i_d^2}$ , the induced gate noise $\overline{i_g^2}$ , and their correlation noise $\overline{i_g i_d^*}$ [6-1, 6-2]. In chapter 5 [6-3], the van der Ziel model have been extended to be able to apply it to short channel devices. In this chapter, a novel representation for equivalent noise temperatures is proposed by corresponding to the "extended van der Ziel model" and the Nyquist theorem .

### 6.2.1 Equivalent noise temperature

The noise temperature is a means for specifying noise in terms of an equivalent temperature. Note that the equivalent noise temperature $T_n$ is not the physical temperature of the device, but rather a theoretical construct that is an *equivalent* temperature that produces that amount of noise power. The noise temperature is related to the noise factor by: [6-6],

$$T_n = T_0\left(F_{\min} - 1\right) \tag{6-1.a}$$

We can also define noise factor and noise figure in terms of noise temperature:

$$F_{\min} = \frac{T_n}{T_0} + 1 \tag{6-1.b}$$

6.2.2 Nyquist theorem

According to Nyquist theorem [6-4], thermal noise current of a conductance $g$ at the absolute temperature $T_0$ in a frequency interval $\Delta f$ can be represented as below.

$$\overline{i^2} = 4kT_0 \Delta f \cdot g \cdot p(f) \tag{6-2}$$

Equation (6-2) is the generalized Nyquist theorem, and $p(f)$ is the quantum correction factor at frequency given by

$$p(f) = \frac{hf}{kT} \frac{1}{\exp(hf/kT) - 1} \tag{6-3}$$

Even $f$= 1THz in Eq.(6-3), $hf/kT \ll 1$. Therefore the quantum correction factor $p(f)$ is about equal to unity at the microwave and millimeter wave region, as below.

$$\overline{i^2} = 4kT_0 \Delta f \cdot g \tag{6-4}$$

### 6.2.3 Pospieszalski's model

Pospieszalski has proposed two-parameter-noise model, in which it was assumed that the gate noise voltage source was not correlated with the drain noise current source [6-7, 6-8]. The noise equivalent circuit of Pospieszalski's model is illustrated in Fig.6-1(b). Pospieszalski's model is described by two equivalent noise temperatures, which are frequency independent constant, as below.

$$\overline{e_g^2} = 4kT_{g,p} \cdot R_i \cdot \Delta f \tag{6-5}$$

$$\overline{i_d^2} = 4kT_{d,p} \cdot g_{ds} \cdot \Delta f \tag{6-6}$$

$$\overline{e_g i_d^*} = 0 \tag{6-7}$$

where $\overline{e_g^2}$ is the gate noise voltage source, $\overline{i_d^2}$ is the drain noise current source, $R_i$ is the effective channel resistance, $g_{ds}$ is the output conductance. $T_{d,p}$ and $T_{g,p}$ are the drain and the gate equivalent temperature, respectively. The equivalent noise temperature for Pospieszalski's model is given by

$$T_{\min,\,p} = 2\frac{f}{f_T}\sqrt{T_{d,p} \cdot T_{g,p} \cdot g_{ds} \cdot R_i} \quad . \tag{6-8}$$

This model shows a good agreement over a wide frequency range between the measured noise parameters and those predicted for HEMT and MESFET.

### 6.2.4 Novel Representation for Equivalent Noise Temperatures

In this chapter, a novel representation for equivalent noise temperatures was proposed by corresponding to the "extended van der Ziel model" (5-7)-(5-9) and the Nyquist theorem (6-4) , as follows.

$$\overline{i_d^2} = 4kT_d \cdot \Delta f \cdot g_m \tag{6-9}$$

$$\overline{i_g^2} = 4kT_g \cdot \Delta f \cdot g_m \tag{6-10}$$

$$\overline{i_g i_d^*} = j \cdot 4k \cdot \Delta T_{gd} \cdot \Delta f \cdot g_m \tag{6-11}$$

where $k$ is the Boltzmann constant, $\Delta f$ is the bandwidth, $g_m$ is the transconductance, $j$ is the imaginary unit and the asterisk defines the complex conjugate. $T_d$ is equivalent drain noise temperature, $T_g$ is equivalent gate noise temperature and $\Delta T_{gd}$ is their correlation noise temperature, which defined by

$$T_d = P \cdot T_0 \tag{6-12}$$

$$T_g = R \cdot T_0 \cdot \left( \frac{f}{f_T} \right)^2 \tag{6-13}$$

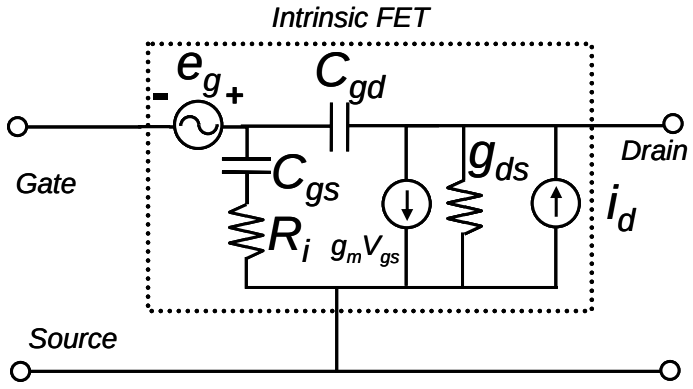
$$\Delta T_{gd} = C\sqrt{PR} \cdot T_0 \cdot \left( \frac{f}{f_T} \right) \quad , \tag{6-14}$$

where $P$ is drain noise coefficient, $R$ is induced gate noise coefficient, $C$ is their correlation coefficient, $T_0$ is the lattice temperature and $f_T$ is cut-off frequency. It has been found that $C$ decreases from positive to negative values when the gate

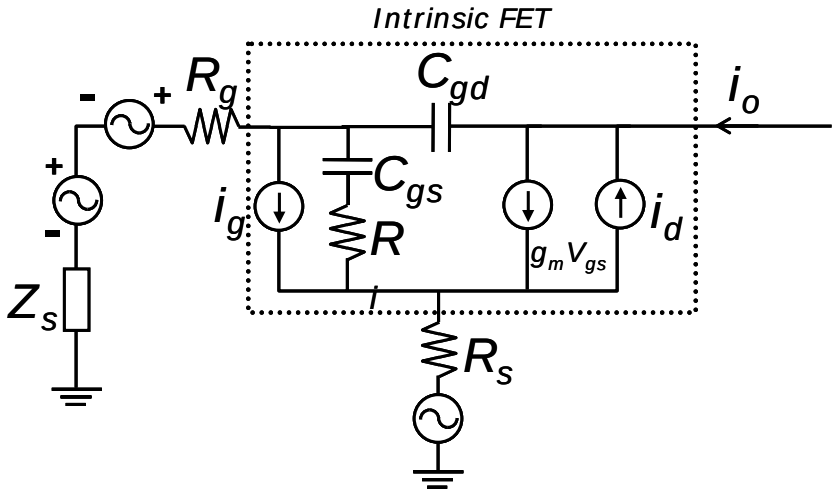
length is reduced continuously to sub-100nm [6-3]. This is because the correlation noise temperature is expressed "$\Delta T_{gd}$". According to Pucel's analysis [6-5] and the representation of the noise temperature [6-6], we can obtain equivalent noise temperature, $T_{min}$, as below.

$$T_{\min} = 2\sqrt{T_d \cdot T_g - \left(\Delta T_{gd}\right)^2} \tag{6-15}$$

Equation (6-15) is a novel representation for equivalent noise temperature, which is useful to understand the contribution of each noise source.




(a) *Equivalent noise circuit for Pucel's model*




*(b) Equivalent noise circuit for Pospieszalski's model*

*Fig.6-1. Noise equivalent circuits for FETs.*

## 6.3. Experimental Procedures and Results

In this chapter, we fabricated multi-finger n-MOSFETs using 45 nm node CMOS technology. The gate length ranges from 40 nm to 480 nm and unit gate finger length ($W_f$) is 1 μm with the total gate width of 128 μm to compare the noise performance. Next, the RF noise parameter (minimum noise figure $F_{min}$, equivalent noise resistance $R_n$, and the optimized source reflection coefficient $\Gamma_{opt}$) were measured from 5 to 15 GHz at $T_0$=300 K and extracted noise temperature $T_d$, $T_g$, $\Delta T_{gd}$ and $T_{min}$ from Eqs.(6-12)- (6-15).

Figure 6-2 shows the extracted $T_d$ and $T_g$ versus frequency characteristics for n-MOSFETs biased at $V_{ds}$=1.2 V and $V_{gs}$=1.0 V. It was confirmed that $T_d$ is independent of frequency, and that $T_g$ increases in proportion to frequency-squared, as Eqs.(6-12) and (6-13).

Figure 6-3(a) indicates the extracted $T_d$, $T_g$, and $T_{min}$ from Eqs.(6-12),(6-13), and (6-15) with measured $T_{min}$ as a function of gate length for the n-MOSFETs biased at $V_{ds}$ = 1.2 V and $V_{gs}$=1.0 V at 10 GHz. It is shown that $T_d$ increases and $T_g$ decreases when the gate length decreases. $T_g$ of 225 K was obtained for $L$= 480 nm, and $T_g$ of 4 K was obtained for $L$= 40 nm, which was a very "cold" temperature due to a factor of $(f/f_T)^2$ in Eq.(6-13). Figure 6-3(a) also indicates the extracted $T_{d,p}$, $T_{g,p}$, and $T_{min,p}$ from Pospieszalski's model. It is noted that both $T_{d,p}$ and $T_{g,p}$ of this model increase when the gate length decreases, and

that $T_{d,p}$ is an order of magnitude higher than that of the proposed $T_d$. In the case of $L$= 40nm, $T_d$ of 634 K was obtained for our representation, while $T_{d,p}$ of 13,000 K was obtained for Pospieszalski's model. Figure 6-3(b) indicates the extracted $\Delta T_{gd}$ from Eq.(6-14). $\Delta T_{gd}$ decreases from positive to negative values when the gate length is reduced, corresponding to the correlation coefficient; $C$.

To our best knowledge, the noise temperature of MOSFETs by Pospieszalski's model has not been reported. It was confirmed that the Eq.(6-15) can be considered a good approximation even for sub-100nm, while the Pospieszalski model predicts a deviation from the data measured.

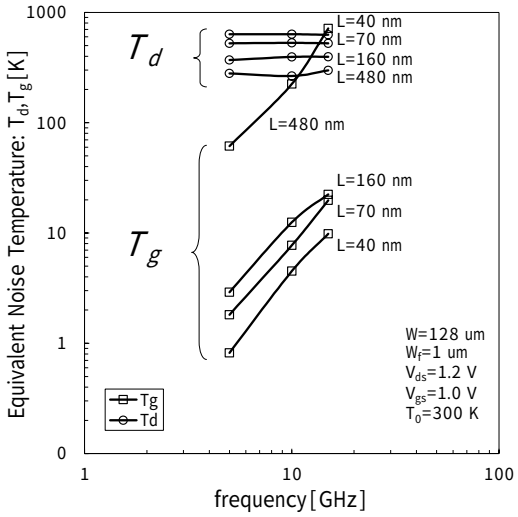
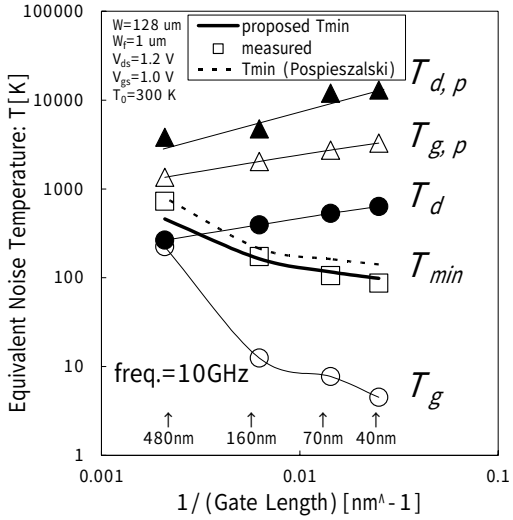
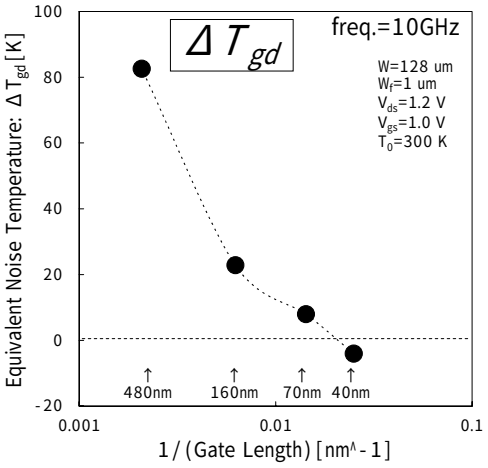



*Fig.6-2. The extracted drain noise temperature, $T_d$ and gate noise temperature, $T_g$ from Eqs.(6-12)-(6-13) versus frequency characteristics for n-MOSFETs with gate width W=128 μm and gate length L = 480 nm, 160 nm, 70 nm and 40 nm, respectively, biased at $V_{ds}$=1.2 V and $V_{gs}$=1.0 V.*




(a)




(b)

*Fig.6-3. (a) The extracted $T_d$, $T_g$, and $T_{min}$ from Eqs.(6-12),(6-13), and (6-15) with measured $T_{min}$ as a function of gate length for the n-MOSFETs biased at $V_{ds}$ = 1.2 V and $V_{gs}$=1.0 V at 10 GHz. It also indicates the extracted $T_{d,p}$, $T_{g,p}$ and $T_{min,p}$ from Pospieszalski's model. (b) The extracted $\Delta T_{dg}$ from Eq.(6-14) with measured $T_{min}$ as a function of gate length for the n-MOSFETs with gate width W=128 μm.*

### 6.4. Discussions

Here, a physical validity of our representation for equivalent noise temperature is discussed, especially for the drain channel noise temperature, $T_d$. Recently several studies have reported full 2-D noise simulation results in a drift-diffusion (DD) and a hydrodynamic (HD) based device simulator [6-9～6-12]. It is demonstrated that channel thermal noise in MOSFETs is mainly due to cold or warm electrons in a gradual channel region, and that the contribution of hot electrons in a velocity saturation region is found to be negligible. At high electric field in short channel MOSFETs, the electron temperature, $T_e$ depends on the electric field along the channel, as below [6-6].

$$T_e = T_0\left(1+\frac{E(x)}{Ec}\right)^2 \tag{6-16}$$

where $E_c$ is a critical field, $E(x)$ is an electric field at channel position; $x$ ,as below[6-13].

$$E(x) = \frac{V_0 \cdot E_C}{\sqrt{2\left[\left(V_{gs}-V_{th}\right)-V_0\right]^2 - 4aV_0E_cx}} \tag{6-17}$$

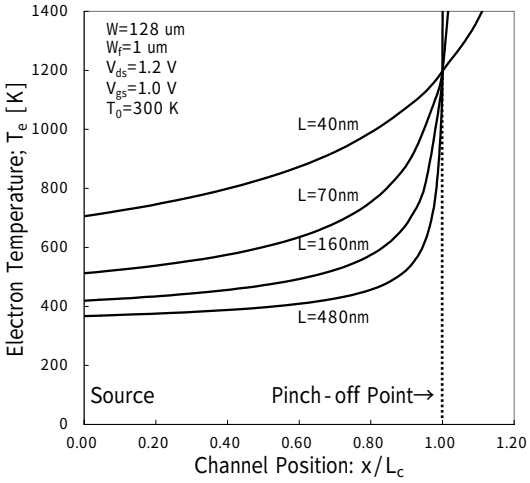
$$V_0 = \left(V_{gs}-V_{th}\right)-a\cdot V_{sat}$$

Figure 6-4(a) indicates the electron temperature, $T_e$ as obtained by the data measured and Eq.(6-16), where the gate begins at source and ends at pinch-off point; $L_c$. It was confirmed that the representation (6-12) of $T_d$ corresponds to the

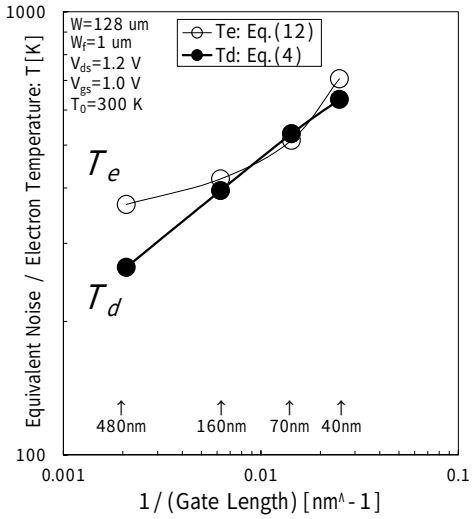
electron temperature in a gradual channel region, as shown in Fig.6-4(b). It calls for further investigation that the physical validities of equivalent gate noise temperature (6-13) and the correlation noise temperature (6-14) by DD and HD simulations.

## 6.5. Conclusion

In this chapter, a novel representation for equivalent noise temperature was proposed, which is useful to understand the contribution of each noise source. A comparison between the proposed representation and Pospieszalski's model is also performed. It was confirmed that the representation of drain noise temperature, $T_d$ corresponds to the electron temperature in a gradual channel region.




(a)




(b)

*Fig.6-4. (a)The electron temperature as obtained by the data measured and Eq.(6-16), where the gate begins at source and ends at $L_c$. (b)The drain noise temperature, $T_d$ for Eq.(6-12) and the electron temperature, $T_e$ at the source end.*

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# Chapter.7

# Conclusions

In Chapter 7, the studies referred to in this thesis are summarized and their importance is described.

*1) Proposal of Layout optimization for RF-MOSFETs*

In Chapter 3, a Mesh-Arrayed MOSFET with ring-shaped gate electrode for high-frequency analog application has been described. The dependence of noise figure and maximum oscillation frequency on parasitic components in MA-MOS configuration has been discussed. The MA-MOS realizes low noise figure of 0.6 dB at 2 GHz and high $f_{max}$ of 37 GHz, using a non-salicide 0.25 μm CMOS technology.

The MA-MOS is the most practical candidate to realize low cost and high performance one-chip RF Baseband CMOS LSI.

*2) Scaling effect of a comprehensive RF characteristics from 150nm node to 65nm node CMOS technology*

In Chapter 4, the scaling effect of RF characteristics of the 65nm CMOS technology compatible with logic CMOS was investigated and compared with that of 150nm CMOS The gate layout effect for the RF performance has also been investigated. To better understand the gate layout effect of RF performance, our

analysis is performed at the same bias condition both of small and large signal measurement.

As scaling continues, cut-off frequency ($f_T$) can be increased by scaling down the gate length, while maximum oscillation frequency ($f_{max}$) and minimum noise figure ($NF_{min}$) depend strongly on the parasitic components. $f_T$, $f_{max}$ and $NF_{min}$ have the dependency of gate finger length ($W_f$).

Since the scaling of gate oxide thickness: $t_{ox}$ cannot be reduced as that of gate length:$L$, the intrinsic gain:$g_m/g_{ds}$ reduced as scaling continues.

1dB compression point ($P_{1dB}$) and third order intercept point ($IP_3$) degrade as technology scaling down, and the dependency of $W_f$ was not observed.

The results confirm the scaling effect of a comprehensive RF characteristics from 150nm node to 65nm node CMOS technology.

*3) Scaling effect of noise sources of 45nm node MOSFETs*

In Chapter 5, the RF noise parameter ($F_{min}$, $R_n$, $\Gamma_{opt}$) of 45 nm node MOSFETs were measured from 5 to 15 GHz and the noise sources and noise coefficients $P$, $R$, and $C$ were extracted by using an extended van der Ziel's model. It was found, for the first time, that correlation coefficient $C$ decreases *from positive to negative values* when the gate length is reduced continuously with the gate length of sub-100 nm. It was confirmed that Pucel's noise figure model,

using noise coefficients $P$, $R$, and $C$, can be considered a good approximation even for sub-50 nm MOSFETs. A scaling effect of the noise coefficients is also discussed, especially the correlation noise coefficient $C$ on the minimum noise figure. It was confirmed that $Lc_0$, which is the gate length where the correlation noise coefficient $C$ equals zero, indicates the saturation point of minimum noise figure.

*4) Proposal of a novel representation for equivalent noise temperature*

In Chapter 6, a novel representation for equivalent noise temperature was proposed, which is useful to understand the contribution of each noise source. A comparison between the proposed representation and Pospieszalski's model is also performed. It was confirmed that the representation of drain noise temperature, $T_d$ corresponds to the electron temperature in a gradual channel region.

In conclusion, the studies referred to in this thesis were useful in the progress of RF-MOSFET technology, and they are also expected to contribute to the future progress of MOSFETs technology for high-level integration and high frequency commercial products.

# Publications and Presentations

## Publications

[1] H.Shimomura, K.Kakushima, and H.Iwai, "Effect of High Frequency Noise Current Sources on Noise Figure for Sub-50 nm node MOSFETs," IEICE Transactions on Electronics, Vol.E93-C, No.5, pp. 678-684, May. 2010.

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# International Presentations

[1] H.Shimomura, A Matsuzawa, H.Kimura, G.Hayashi, T.Hirai, and A.Kanda, "A mesh-arrayed MOSFET (MA-MOS) for high-frequency analog applications," IEEE 1997 Symposium on VLSI Technology, Digest of Technical Papers, pp. 73-74.

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# Books

[1] H.Shimomura, "Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications," (edited by T.Sakurai, A.Matsuzawa, and T.Douseki), Chapter.3.9, pp. 114-122, 1st ed.; Springer: New York, 2006.

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