Doctoral Thesis

A Study on Electrical Characteristics of Silicon Nanowire Field Effect Transistors

A dissertation submitted to the department of electronics and applied physics,
interdisciplinary graduate school of science and engineering,
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Abstract

Silicon nanowire (SiNW) metal-oxide-semiconductor field-effect transistor (MOSFET) is a promising candidate of future CMOS device for further scaling. As the cross-sectional dimensions of SiNW channel is very small, cross-sectional shapes should affect electrical characteristics of SiNW FETs. In this work, effects of cross-sectional shapes of gate stack formation on (*i*) fabrication feasibility of SiNW FET; (*ii*) carrier transport properties including on-current, effective carrier mobility and inversion charge density; (*iii*) electrostatic controllability are investigated.

A novel device structure, semi gate-around structure is proposed in this work, which is similar to tri-gate structure. Silicon nitride sidewalls are filled at the pedestal of the tri-gate structure, which reduces steepness of three-dimensional structure. Therefore, over-etching step time during gate patterning process is reduced. As a result, SiNW FET is successfully fabricated using conventional bulk CMOS fabrication facilities.

To establish design guideline of cross-sectional shapes of SiNW FET to achieve high on-current (I_{ON}), SiNW FETs with various cross-sectional shapes are fabricated and characterized. Among rectangular, half-circular, tear-like, and tall rectangular cross-sections, SiNW FET with rectangular cross-section exhibits highest on-current for nFET at the channel height of 12 nm and width of 19 nm. Ratio of on-current around corners is larger that the on-current of flat-surface component, which suggest importance of corners in SiNW cross-section for enhancement of I_{ON}.

For analysis of transport properties, effective carrier mobility (μ_{eff}) and inversion charge density (Q_{inv}) are evaluated. Q_{inv} of rectangular cross-section is increased because of high-density inversion carrier regions around corners compared with planar SOI nFET. μ_{eff} is also enhanced compared with that of planar SOI FET. The product of Q_{inv} and μ_{eff} of rectangular cross-section is highest, which coincides with the largest I_{ON}.

Although the ratio of corner current is large, the corner effect is not observed in this work. This is due to low doping concentration (~10^{17} cm^{-3}) according to theoretical calculation and results of computer simulation using three-dimensional device simulator.

SiNW pFETs with rectangular cross-section and different gate oxide thickness is characterized, and it is shown that oxide thickness scaling is valid down to 1.5 nm.

Design guidelines of SiNW channel cross-section for enhancement of electrical characteristics are proposed in this work. Rectangular cross-sectional shape is suitable for enhancement of electrical performance of SiNW nFET.

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Abbreviations

Symbol	Description	Unit
μ_{eff}	Effective carrier mobility	cm^2/Vs
μ_{elec}	Effective electron mobility	cm^2/Vs
μ_{hole}	Effective hole mobility	cm^2/Vs
μ_{ph}	Phonon-scattering-limited mobility	cm^2/Vs
μ_{surf}	Surface-roughness-scattering-limited mobility	cm^2/Vs
C_{BOX}	Buried oxide layer capacitance	F/cm^2
C_{dm}	Maximum depletion layer capacitance	$\mu F/cm^2$
C_{flat}	oxide capacitance along flat-surface	$\mu F/cm^2$
C_{gc}	gate-to-channel capacitance	$\mu F/cm^2$
C_{it}	Interfacial state capacitance	$\mu F/cm^2$
C_L	Total load capacitance of all gates	F
C_{OX}	Oxide capacitance	$\mu F/cm^2$
CV/I	Intrinsic delay time	sec
E_i	Intrinsic Fermi level	eV
E_F	Fermi level	eV
EOT	Equivalent oxide thickness	nm
F	Operation frequency	Hz
h_{NW}	Nanowire channel height	nm
I_{corner}	Corner component of on-current	A
I_{flat}	Flat surface component of on-current	A
I_{OFF}	Off-state leakage current	A
I_{ON}	On-current	A
K	Boltzmann constant	J/K
L_g	Gate length	nm
Ψ_B	Difference between E_i and E_F	eV
P	Total power consumption	W
Q	Elemental charge	C
Q_{inv}	Inversion charge density	$\mu C/cm^2$
m	Body constant	
n_i	Intrinsic carrier concentration	cm^{-3}

N_a	Acceptor concentration	cm^{-3}
N_d	Donor concentration	cm^{-3}
N_S	Inversion carrier density	cm^{-2}
R_{SD}	Source/drain parasitic resistance	Ω
τ	Intrinsic delay time	sec
T	Measurement temperature	K
t_{Si}	Thickness of silicon-on-insulator layer	nm
T_{OX}	Gate oxide thickness	nm
v_{sat}	Saturation velocity	
V_1	Terminal voltage of V_1	V
V_2	Terminal voltage of V_2	V
V_{DD}	Power supply voltage	V
V_{fb}	Flat-band voltage	V
V_g	Gate voltage	V
V_d	Drain voltage	V
V_{OV}	Overdrive gate voltage	V
V_{supply}	Power supply voltage	V
V_{th}	Threshold voltage	V
w_{NW}	Nanowire channel width	nm
W	Channel width	nm

Chapter 1

Introduction

1.1. Evolution of integrated circuits with scaling technology

Since the Intel 4004 microprocessor appeared in 1971, the number of metal-oxide-silicon (MOS) field-effect transistors (FETs) integrated in the integrated circuits has increased evolutionally as Gordon Moore, the co-founder of Intel said "*The number of transistors incorporated in a chip will approximately double every 24 months."* By the downsizing of the MOSFET, the number of transistors integrated on a integrated circuit increased, which resulted in a more highly functional devices [1.1]. In addition, the electrical performance of each MOSFET also has increased by downsizing. These phenomena can be explained using scaling theories.

1.1.1. Scaling theory

Silicon device has evolved with scaling technology. In 1974, *Dennard et al.* proposed the constant-field scaling theory [1.2]. **Tab. 1.1** shows details of his constant-field scaling theory.

Dennard et al. designed MOSFET so that the electric field in MOSFET is constant. By downscaling using the constant-field theory, the electrical performance of MOSFET will not be degraded because degradation because of high electrical field is negligible. In addition, as the device dimension decreases, the delay time per circuit decrease,

Table 1.1 Scaling factors of the constant-field scaling theory proposed by Dennard et al. in 1974 [1.2].

	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance	$1/\kappa$
Delay time per circuit	$1/\kappa$
Power dissipersion per circuit	$1/\kappa^2$
Power density	1

, which results in a high-speed operation. The number of MOSFETs on an integrated circuit also increases, and the integrated circuits become more functional. However, the power density is constant. This means that there is no problem about cooling of the integrated circuits.

Actually, the scaling of CMOS did not follow the constant-field scaling theory precisely because of non-scaling factors. The most prominent factor is the threshold voltage of MOSFET (V_{th}). As the subthreshold current has the exponential dependence on the gate voltage, the threshold voltage cannot be scaled down significantly without causing a substantial increase in the off-current. The threshold voltage limitation made it difficult to reduce the power supply voltage (V_{DD}). This restriction caused device degradation by high-field effects.

1.1.2. Power consumption of CMOS logic circuits

In the complementary metal-oxide-silicon (CMOS) circuits as shown in **Fig. 1.1**, we use both pMOSFET and nMOSFET complementarily. At the steady state, one of them is off-state and the other is at the on-state. Therefore, at steady state, only off-state leakage current is effective. When an input logic state of a MOSFET changes, the total load capacitance of next stage (C_L) is charged. Therefore, for reduction of waiting power consumption, a reduction of off-state leakage current is very important. **Fig. 1.2** shows increase of power density of integrated circuits [1.3]. Total power consumption has been increasing and the power density is reaching to the same amount on the Sun's surface.

Details of power consumption of integrated circuits are shown in **Fig. 1.3** [1.4]. As the production year increased, the gate length of MOSFET shrieked. The clock frequency of integrated circuits also increased. As a result, dynamic power consumption has been increasing. Details are shown in below. On the other hand, sub-threshold leakage current and gate-oxide leakage current exponentially has been exponentially increasing. Oxide leakage current is due to thinning of gate oxide thickness for enhancement of electrostatic controllability of gate electrode. A solution of the oxide leakage current is to introduce of high permittivity material as a gate oxide material, and

to increase gate oxide thickness and reduce gate leakage current. Sub-threshold leakage current is due to short channel effect. A solution is introduction of three-dimensional device structure to enhance electrostatic controllability of gate electrode.

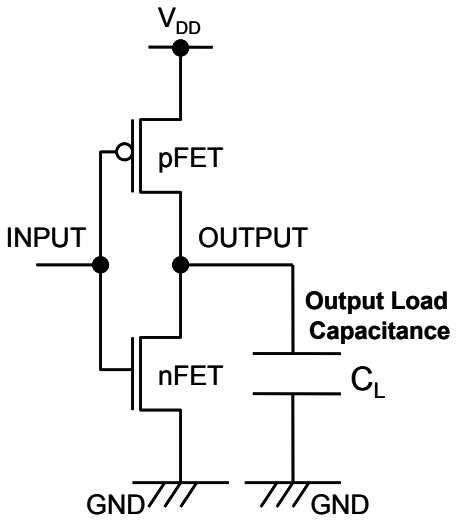


Figure 1.1 A schematic illustration of CMOS inverter circuit and output load capacitance (C_L).

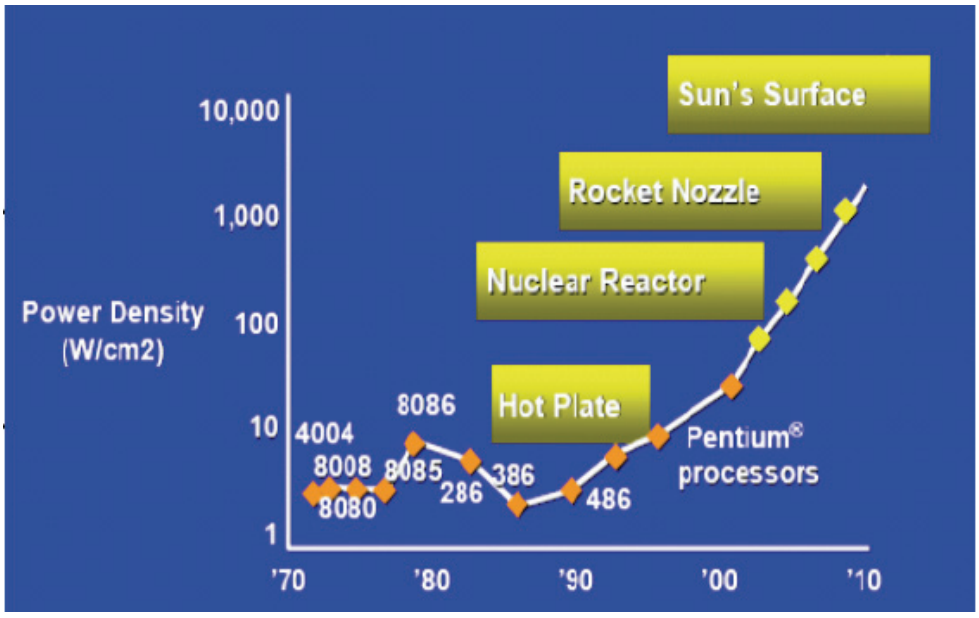


Figure 1.2 Increase of power density of integrated circuits as a function of product year [1.3].

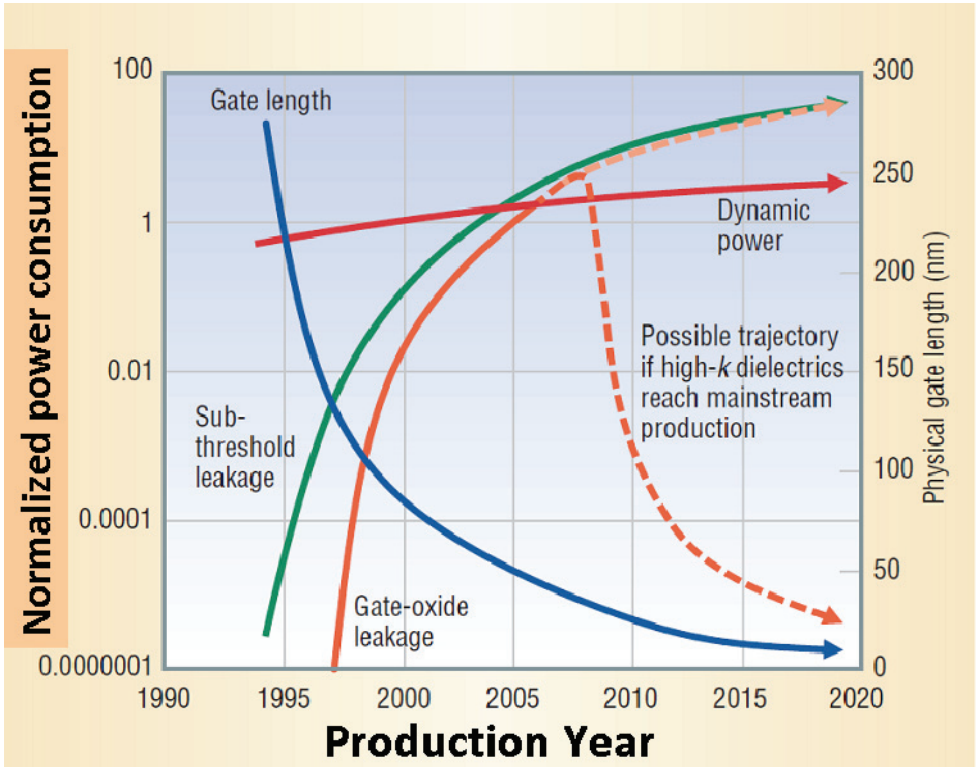


Figure 1.3 Details of power consumption of integrated circuits [1.4]

1.1.2.1. Operating frequency and power supply voltage of logic circuits [1.4]

An operating frequency (f) depends on power supply voltage (V_{supply}) as follows;

$$f \propto \left(V_{\sup ply} - V_{th}\right)^{\alpha} / V_{\sup ply} \qquad (1.1)$$

, where V_{th} is the threshold voltage of MOSFET, and α is approximately 1.3. Using this equation, an equation about a variability of power supply voltage and operation frequency can be derived as follows;

$$V_{norm} = \beta_1 + \beta_2 \cdot f_{norm} \qquad (1.2)$$

, where $V_{norm} = V_{supply}/V_{max}$, $b_1=V_{th}/V_{max}$, $b_2=1-b_1$, $f_{norm} = f/f_{max}$, and V_{max} is the maximum operating voltage. If we assume b1 = 0.3, reduction of the operating frequency results in reduction of the operating voltage by 35 %.

1.1.2.2. Power consumption of the logic circuits [1.4]

Total power consumption (P) is the sum of dynamic and static power:

$$P = AC_L V_{\sup ply}^2 f + V_{\sup ply} I_{leak} \qquad (1.3)$$

, where A is the fraction of gates actively switching, and C_L is the total capacitance load of all gates. The first term is related to dynamic power consumption and the second term is related to static power consumption.

The leakage current is the sum of the subthreshold leakage current I_{sub} and gate oxide leakage current $I_{ox.}$ Therefore, reduction of the subthreshold leakage currnet Isub is important for reduction of the power consumption.

1.1.3 Problems of off-state leakage current

1.1.3.1 The short channel effect

The short channel effect (SCE) appears as the gate length of MOSFET decreases. Threshold voltage of MOSFET decrease as the gate length decreases, which is a roll-off of the threshold voltage. Subthreshold swing of MOSFET also degrades as the gate

length decrease because of SCE.

Yau et al. proposed the charge share model for explanation of the roll-off of the threshold voltage of MOSFET [1.5]. The amount of the depletion charge terminated by the electric field from source and drain is remains. Whereas, the amount of the depletion charge terminated by the electric field from gate electrode decreases. Therefore, as the gate length decrease, a ratio of depletion charge terminated by the electric field from gate electrode decreases. As a result, short-channel MOSFETs can turn on at the lower gate voltage than the threshold voltage of long-channel MOSFET.

Degradation of the subthreshold slope can be explained by the penetration of the electric field from source and drain electrode [1.6]. In the uniformly doped concentration N_a, Poisson's equation can be written as follows:

$$\frac{\partial E_x}{\partial x}+\frac{\partial E_y}{\partial y}=\frac{\rho}{\varepsilon_{si}}=-\frac{qN_a}{\varepsilon_{si}} \qquad (1.4)$$

Where E_x is the electric field in the vertical direction controlled by the gate electrode, and E_y is the electric field in the lateral direction controlled by source and drain electrodes. In a long-channel device, lateral electric field is negligible. However, in a short-channel device, lateral electric field is not negligible, and the amount of depletion charge controlled by the lateral electric field increases. Therefore the depletion charge controlled by channel can be written as follows:

$$\varepsilon_{Si}\frac{\partial E_x}{\partial x}=\rho-\varepsilon_{Si}\frac{\partial E_y}{\partial y} \qquad (1.5)$$

This increased charge controlled by the source and drain suggests penetration of the electric field from source and drain. The penetration of the electric field from source and drain leads to undesired source-drain leakage current, which results in the degradation of the subthreshold drain current.

1.1.3.2 Drain induced barrier lowering

Drain induced barrier lowering is induced by penetration of the electric field from source and drain. The barrier height of channel is lowered even more by high drain bias

voltage. This results in further reduction of the threshold voltage. Eventually, the device reaches the punch-through condition when gate totally loses control of the channel and high drain current persists independent of gate voltage.

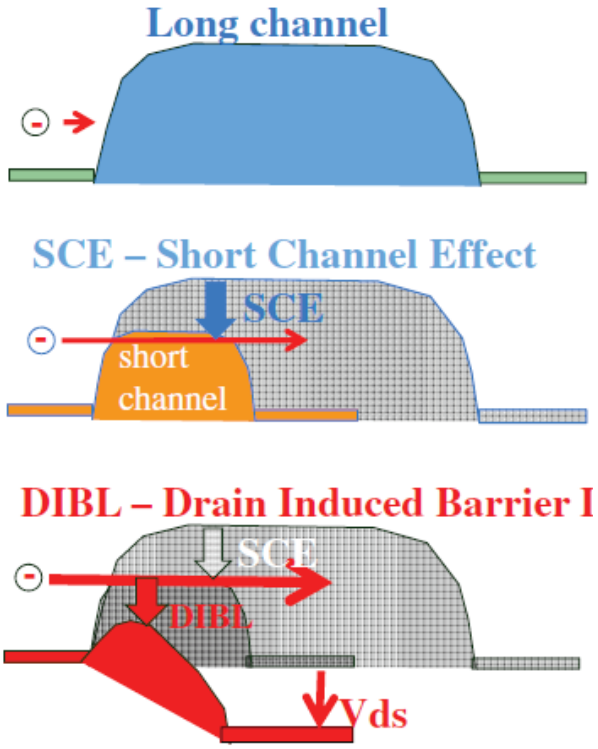


Figure 1.4 Schematic illustrations for explanation of the short channel effect and the drain induced barrier lowering [1.6].

The solution to the SS degradation, Vth roll-off and DIBL is the enhancement of the electrostatic controllability of channel.

There are some solutions: (i) increase of the gate capacitance of MOSFET. (ii) enhancement of the effective carrier mobility while gate length is retained (iii) adoption of three-dimensional structure. The solution (i) is the thinning of the gate oxide thickness and introduction of high permittivity (high-κ) gate oxide materials. The solution (iii) is the introduction of stressors for enhancement of the effective carrier mobility. However, the scaling of the gate length is the most important for enhancement of integration density of MOSFETs. Therefore, as the gate length decreases the solutions (i) and (iii) reach the limit. Therefore the solution (ii) is the last solution for enhancement of integrated circuits.

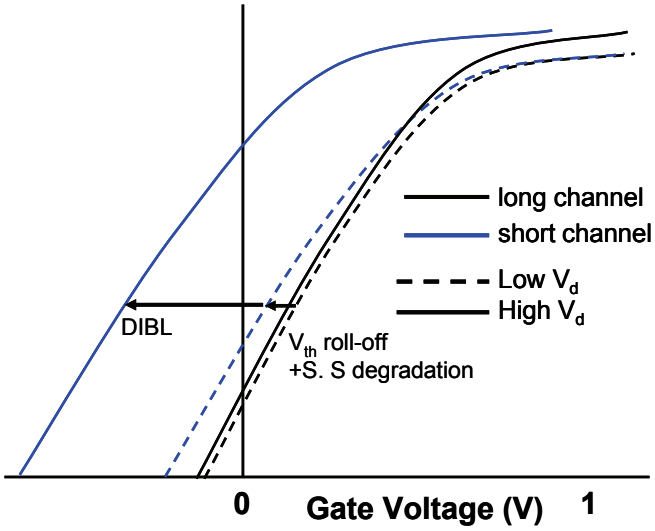


Figure 1.5 A schematic illustration for explanation of off-characteristics degradation because of the short channel effect and drain induced barrier lowering.

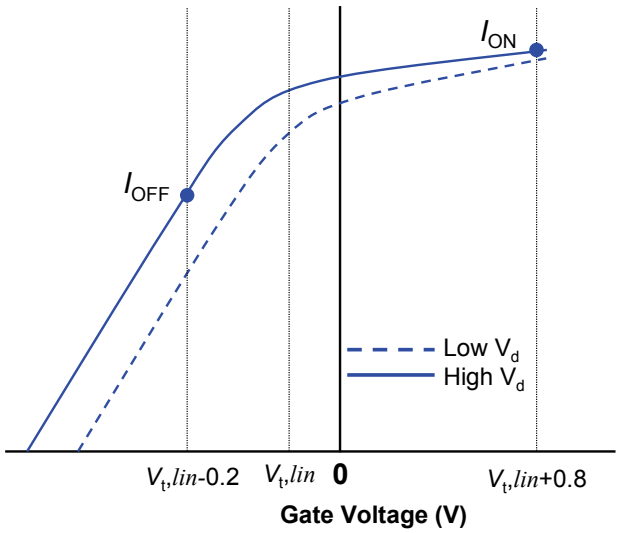


Figure 1.6 Definition of the on-current and off-current in case of improper threshold voltage of nMOSFET.

1.1.4. Requirements for On-current

When the input is inverted, nMOSFET and pMOSFET switch to the reverse state. For fast transfer of the input information to the output, which can be modeled as a capacitance, large on-current is important for fast circuit operation. Therefore high I_{ON} and low I_{OFF} is ideal. However, there are problems in reality.

On-current is important for reduction of delay time because circuit operation is determined by the charging time of the next stage capacitance. Therefore high on-current is important for high speed circuit. Intrinsic delay is defined as follows.

$$\tau = \frac{CV}{I} \qquad (1.6)$$

, where τ is the intrinsic delay, C is the gate capacitance, V is the power supply voltage, and I is the drain current [1.7]. As the intrinsic delay determines the maximum operation frequency of the logic circuit, the intrinsic delay is one of the important parameter of MOSFET. Figure 1.x shows the expected delay time in future [1.8].

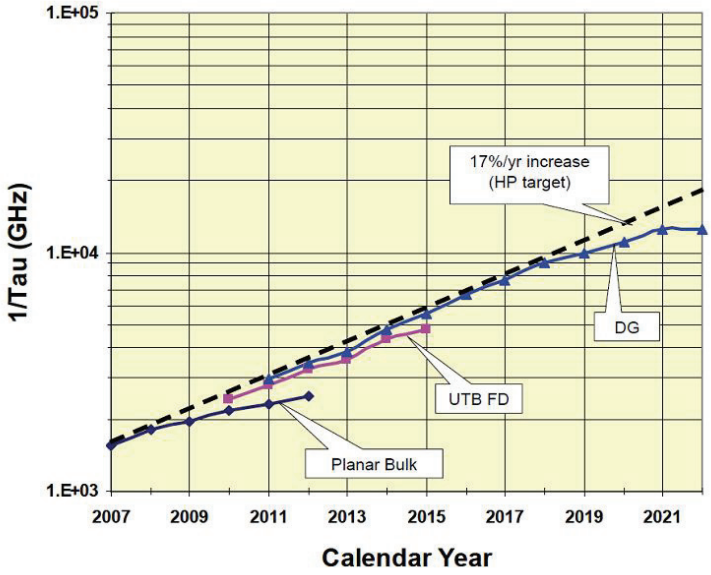


Figure 1.7 Transition of requirements for intrinsic delay time described in the International Technology Roadmap for Semiconductor 2007 [1.8].

Figure 1.7 shows an inverter with the output load capacitance. Actually interconnect affects the delay time of integrated circuits [1.9]. Interconnect resistance *R* and interconnect capacitance *C* dominates as the device dimensions shrink. Therefore, the delay time is also determined by the resistance R and total output load capacitance C_L. Therefore, for high operation frequency high I, which is the on-current I_{ON}, is necessary.

1.2. Introduction of multi-gate FETs

1.2.1. Fully depleted SOI device

Fully depleted SOI CMOS device has advantages over bulk CMOS devices:

- Low source/drain junction capacitance
- Low source/drain junction leakage current
- Steep subthreshold slope

SOI CMOS devices are fabricated on Buried Oxide layer. Bulk CMOS device has depletion region under source/drain junctions. However, SOI CMOS has BOX layer under source/drain region. Therefore junction capacitance of SOI CMOS is reduced as shown in **figure 1.8**. This leads to reduction of load capacitance and high frequency CMOS device.

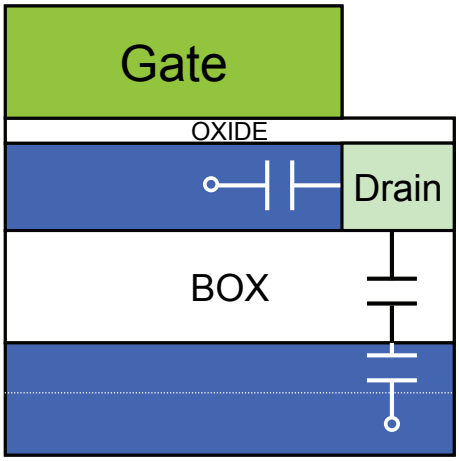


Figure 1.8 A schematic illustration for junction capacitance and substrate capacitance of SOI devices.

The junction interface exists at the side of source/drain junctions. Therefore, area of source/drain junction is smaller than the junction area of source/drain in bulk CMOS devices. This leads to reduction of junction leakage current of SOI CMOS devices and is advantageous for reduction of off-state leakage current.

As the fully depleted SOI CMOS has series capacitance of BOX layer. Therefore, the total substrate capacitance is

$$C_{SOI} = \frac{C_B \cdot C_{BOX}}{C_B + C_{BOX}} \qquad (1.5)$$

Subthreshold swing is

$$S.S. = \ln 10 \frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \qquad (1.6)$$

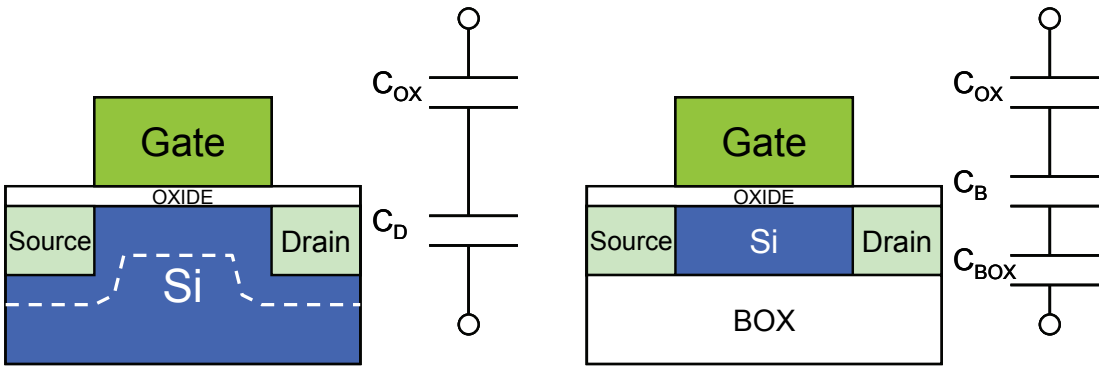


Figure 1.9 Schematic illustrations of the gate capacitance of bulk silicon FET and SOI FET.

Therefore, steeper subthreshold slope is expected for fully-depleted SOI CMOS device. However, too thick BOX layer is not favorable because the electric field from drain penetrates BOX layer and affects channel potential [1.12]. Too thin BOX layer is also not favorable for extremely scaled SOI CMOS device with the gate length of 10 nm [1.13]. Therefore, multi-gate structure is necessary for reduction of the short channel effect.

1.2.2. Double-gate and Multi-gate devices

In the double-gate MOSFET, another gate stack is formed at the bottom of the SOI layer of SOI MOFSET. Therefore, electrostatic controllability of channel is enhanced compared with either single gate bulk MOSFET or SOI MOSFET. Using narrow SOI channel instead of SOI layer results in formation of multi-gate MOSFET as shown in **Fig. 1.11**. In double-gate and multi-gate structure, electrostatic controllability of gate is enhanced, and lightly doped silicon channel can be used. This results in higher carrier mobility.

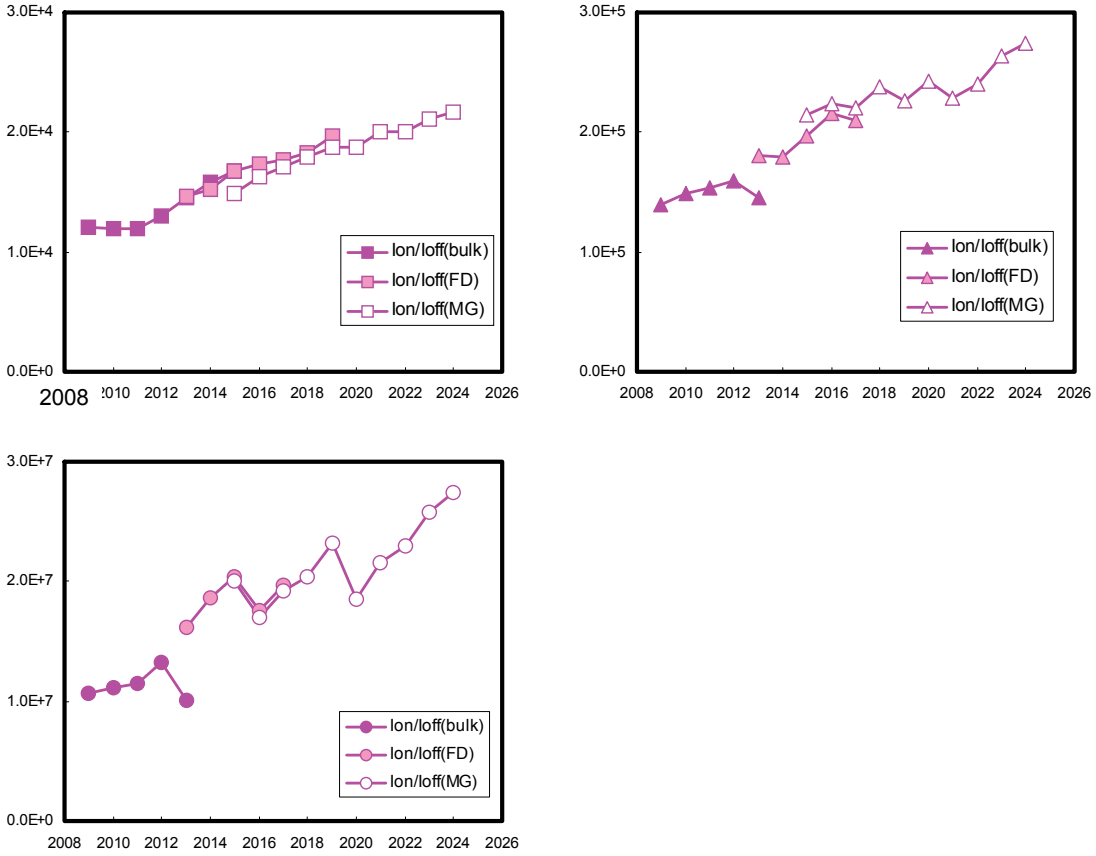


Figure 1.10 I_{ON}/I_{OFF} characteristics on the international technology roadmap for semiconductor 2009 of different purposes.

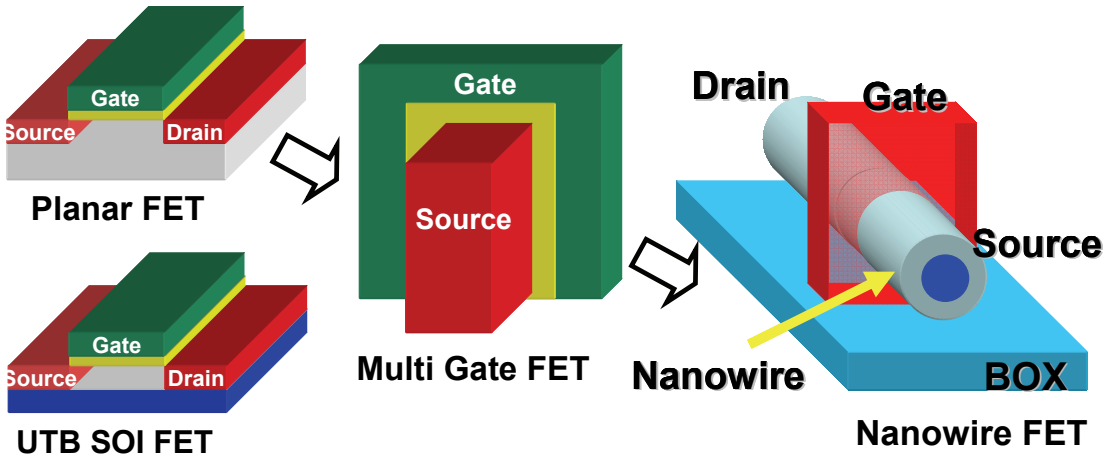


Figure 1.11 Transition of the device structure for enhancement of electrostatic controllability of the gate electrode on the channel.

1.3. Expectations of electrical performance of the silicon nanowire FET

1.3.1. Off-characteristics

Silicon nanowire FET employs narrow silicon channel for enhancement of electrostatic controllability on its channel. Therefore, superior off-characteristics are expected. **Figure 1.12** shows the criterions for achieve subthreshold swing less than 75 mV/dec. and drain-induced barrier lowering less than 50 mV/V. The Gate all around (GAA) structure achieves the criterion using the smallest gate length at the same silicon thickness. On the other hand, the largest silicon body thickness is allowed to achieve the criterion at the same gate length. Therefore the immunity of the GAA structure for the short channel effect is the largest. **Figure 1.12** also shows that as the silicon body thickness decreases the smaller gate length is allowed for the criterion. Therefore the SiNW FET, which has small diameter of silicon channel, has the largest advantage.

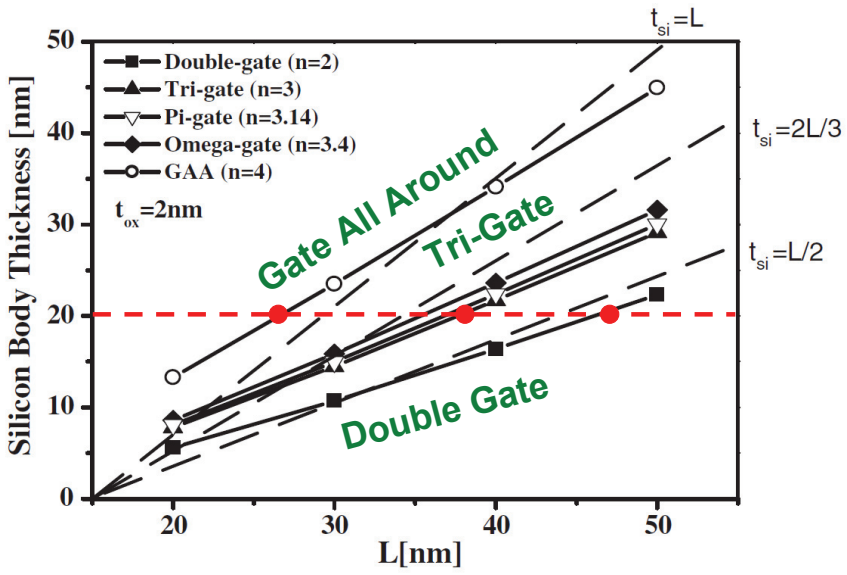


Figure 1.12 Criterions for achieve subthreshold swing less than 75 mV/dec. and drain-induced barrier lowering less than 50 mV/V [1.10].

1.3.2. Effective carrier mobility

i. Experimental approach

Investigations about the electrical characteristics have been performed. In 2000, *Y. Cui et al.* demonstrated the carrier mobility of the SiNW FET experimentally [1.15]. The SiNWs were synthesized using the laser-assisted catalytic growth, which is one of the bottom-up approaches. They calculated carrier mobility with the transfer characteristics and resulted in 3.17 cm^2/Vs with boron-doped SiNW channel with the diameter of 150 nm. In 2003, they improved the carrier mobility with defect passivation [1.16]. The peak mobility of their SiNW FET was 560 to 1350 cm^2/Vs at room temperature with the diameter of 5 nm. Their work suggests the possibility of high carrier mobility of the SiNW FET.

ii. Theory and simulation

H. Sakaki presented the probability of high mobility of the SiNW FET because of the scattering suppression in one-dimensional carrier transport in 1980 [1.17]. It has been reported that silicon nanowire FET has high effective carrier mobility. A. K. Buin et al. has been reported that significant enhancement of hole mobility was obtained using $sp^3d^5s^*$ tight binding calculation.

1.3.3. Gate capacitance of SiNW FET

Gate capacitance of the gate around structure is different from the capacitance of planar FETs. We can calculate C_{ox} in the previous literature as follows. We assume that the channel is a cylindrical conductor with the radius of t_{Si} and the gate oxide thickness is t_{ox} with dielectric constant of ε_{ox}. The gate electrode rounding the gate oxide is also assumed to be a conductor.

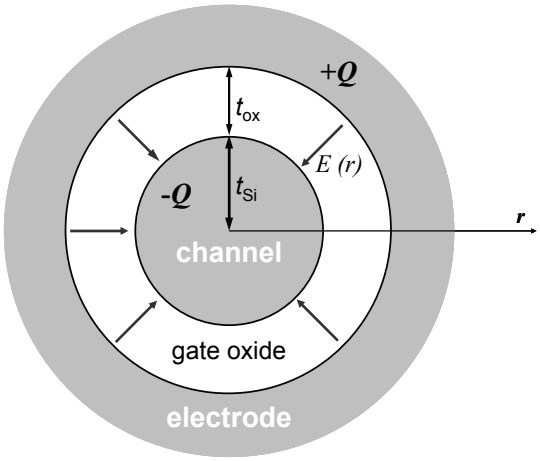


Figure 1.13 A model for calculation of the capacitance of the silicon nanowire structure using cylindrical conductor with insulator.

Using the gauss's law,

$$E(r)\cdot 2\pi r = \frac{Q}{\varepsilon_0 \varepsilon_{Si}} \qquad (1)$$

Voltage of the outer electrode is the integral of electric field and,

$$V = \int_{t_{Si}}^{t_{Si}+t_{ox}} \frac{Q}{2\pi r \varepsilon_{ox} \varepsilon_0 r} dr \quad (2)$$

Therefore the capacitance C and the capacitance normalized by the peripheral length of the channel C_{nor} are respectively,

$$C = \frac{Q}{V} = \frac{2\pi\varepsilon_0\varepsilon_{ox}}{\ln\left(1+\frac{t_{ox}}{t_{Si}}\right)}, \quad C_{nor} = \frac{\varepsilon_0\varepsilon_{ox}}{t_{Si}\cdot\ln\left(1+\frac{t_{ox}}{t_{Si}}\right)} \qquad (3)$$

Therefore we can speculate the enhancement of the gate capacitance rather than that of planar FETs at the same overdrive voltage. The larger gate capacitance results in enlargement of inversion charge density of the SiNW FET compared with that of planar FETs.

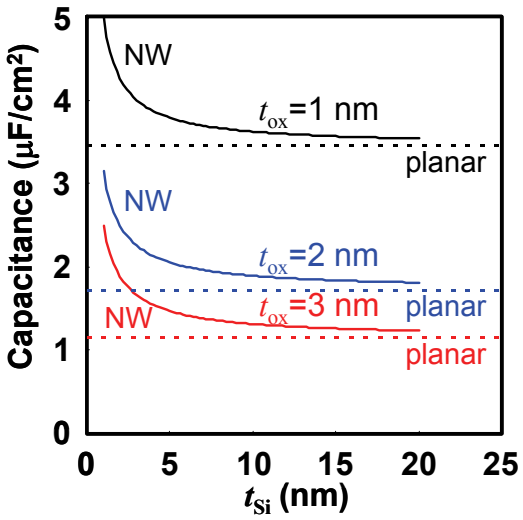


Figure 1.14 Capacitance calculated using cylindrical conductor model.

1.4. Previous researches of SiNW FET

1.4.1 Channel size dependence

S. D. Suk *et al.* in Samsung Electronics reported size dependency on the SiNW FET from channel width w_{NW} of 2 to 11 nm [1.18]. They obtained the highest normalized on-current around 4 nm. S. Bangsaruntip *et al.* in IBM reported systematic investigation on size dependency of electrical characteristics from channel width w_{NW} of 5.0 nm to 20 nm, mainly electrostatic controllability of SiNW FET [1.19].

1.4.2 Channel cross-sectional shapes

Electrical characteristics of triangular [1.20, 1.21], circular [1.22], ellipsoidal [1.23], and rectangular [1.24] cross-sections have been reported. The effects of the various cross-sectional shapes of the SiNW FETs on their electrical properties have been reported, for example, the gate capacitance [1.25], the on-current I_{ON} [12], the threshold voltage (V_{th}) [1.26], the effective carrier mobility (μ_{eff}) [1.27], and the interfacial state density (Dit) [1.28].

Although a lot of efforts were paid for investigation of electrical characteristics of SiNW FETs, guidelines of cross-sectional shapes for high electrical performance of SiNW FET have not been established well.

1.5. Purpose of this work

The purpose of this work is (*i*) to fabricate the SiNW FET with conventional process facilities and examine the electrical performance of the SiNW FET with experiments and (*ii*) to establish design guidelines for high-performance SiNW FET. First I will design device structure of the SiNW FET so that the SiNW can be fabricated as easily as possible. One of the main concerns is the over-etching of gate pattering process. Process condition of the SiNW channel is also investigated by experiments. Then I will investigate the dc-characteristics of the SiNW FET, especially on and off characteristics of the SiNW FET. In chapter 4, the effective carrier mobility of the SiNW FET is investigated. In chapter 5, corner effect of the SiNW FET is investigated. In chapter 6, effect of the gate oxide thickness of the SiNW FET is investigated. In chapter 7, the SiNW FET with four-terminal geometry is investigated. Finally I conclude my study on electrical characteristics of the SiNW FET.

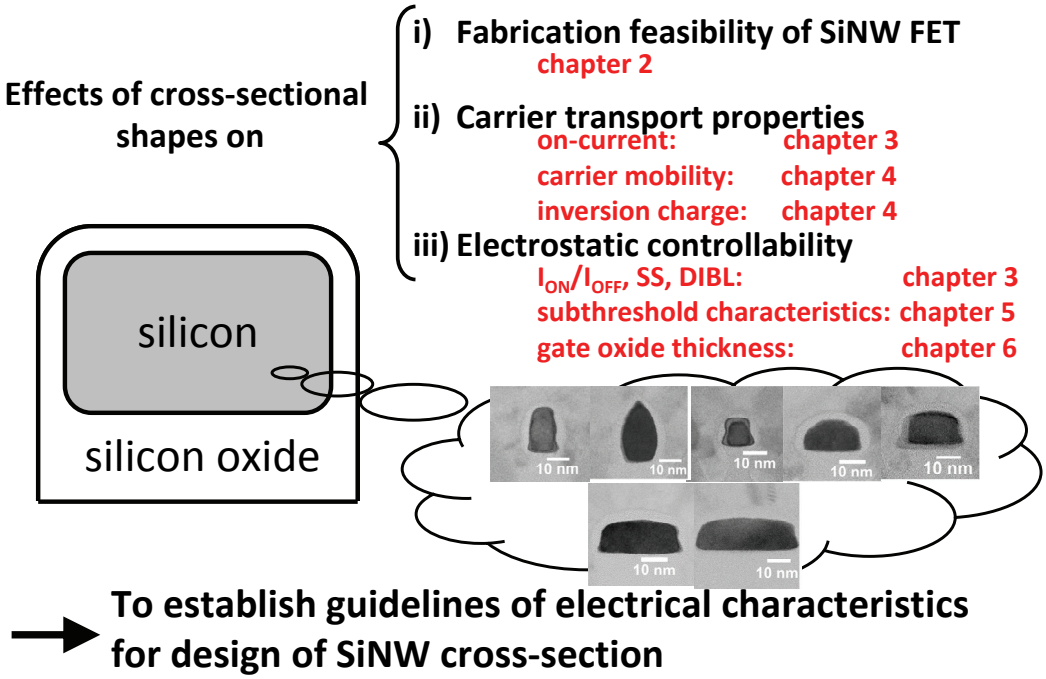


Figure 1.15 Purpose of this study.

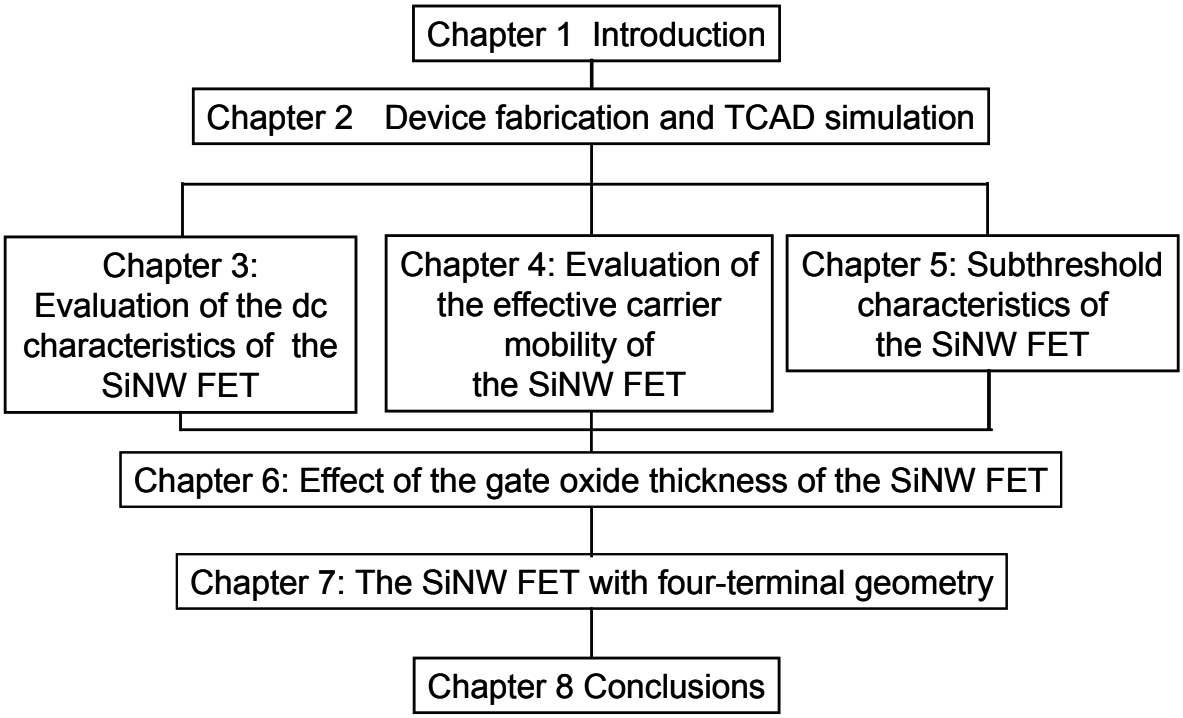


Figure 1.16 Diagram of my study on the electrical characteristics of the SiNW FET.

References

[1.1] H. Iwai. CMOS technology –year 2010 and beyond. *IEEE J. Solid-State Cirucits.* **34** (1999) 357.

[1.2] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc. Design of ion-implanted MOSFETs with very small physical dimensions. *IEEE. J. Solid-State Circuits.*

[1.3] P. P. Gelsinger. Microprocessors for the New Millennium: Challanges, Opportunities, and Nwe Frontiers. *IEEE Int'l Solid-State Circuits Conf. 2001.*

[1.4] N. S. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J. S. Hu, M. J. Irwin, M. Kandemir, and V. Narayanan. Leakage current: Moore's law meets static power. Computer.

[1.5] L. D. Yau. A simple theory to predict the threshold voltage of short-channel IGFETs. *Solid-State Electron.* **17** 1059.

[1.6] T. N. Nguyen and J. D. Plummer. Physical mechanisms responsible for short hcannel effects in MOS devices. Int'l Electron Deivces Meet. 1981. 596-599.

[1.7] T. Skotnicki, CMOS Technologies- Trends, Scaling and Issues. IEDM 2010 short cournce.

[1.8] R. R. Troutman. VLSI limitations from drain-induced barrier loweing. IEEE J. Solid-State Circuits. **14** (1979) 383-391.

[1.9] Y. Taur and T. H. Ning. Fundamentals of modern VLSI devices.

[1.10] International Technology Roadmap for Semiconductor 2007, Process Integration, Device and Structures.

[1.11] K. C. Saraswat and F. Mohammadi. Effect of scaling of interconnections on the time delay of VLSI circuits. *IEEE J. Solid-Satte Circ.* **SC-17** (1982) 275.

[1.12] T. Tsuchiya, T. Ohno, and T. Kado. Proc. Int'l Symp. SOI Technology and Devices. 1994. 401.

[1.13] T. Shimatani, S. Pidin, and M. Koyanagi. Ext. Abst. Solid-State Device Meet. 1996. 949.

[1.14] C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge. Device design guidelines for nano-scale MuGFETs. *Solid-State Elecron.* **51** (2007) 505-510.

[1.15] Y. Cui, X. Duan, J. Hu, and C. M. Lieber. Doping and electrical transport in silicon nanowires. *J. Phys. Chem B*. **104** (2000) 5213.

[1.16] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber. High performance silicon nanowire field-effect transistors. *Nano Lett.* **3** (2003) 149.

[1.17] H. Sakaki. Scattering suppression and high-mobility effect of size-quantized electrons in ultrafine semiconductor wire strutures. *Jpn. J. Appl. Phys.* **19** (1980) L735.

[1.18] S. D. Suk. Investigation of nanowire size dependency on TSNWFET. *Proc. Int'l Electron Device Meet. 2007.*

[1.19] S. Bangsaruntip. High performance and high uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling. *Proc. Int'l Electron Device Meet. 2009.*

[1.20] N Singh., F. Y. Lim, W. W. Fang, S. C. Rustagi, Bera L. K., Agarwal A., Tung C. H., Hoe K. M., Omampuliyur S. R., Tripathi D., Adeyeye A. O., Lo G. Q., Balasubramanian N., Kwong D. L. Ultra-narrow silicon nanowire gate-all-around CMOS devices: impact of diameter, channel-orientation and low temperature on device performance. *Tech. Dig. of Int'l Electron Device Meet. 2006:1-4.*

[1.21] Moselund K. E., Dobrosz P., Olsen S., Pott V., De Michielis L., Tsamados D., Bouvet D., O'Neill A., Ionescu A. M. Bended Gate-All-Around Nanowire MOSFET: a device with enhanced carrier mobility due to oxidation-induced tensile stress. *Tech. Dig. of Int'l Electron Device Meet. 2007:191-194.*

[1.22] Li M., Yeo K. H., Suk S. D., Yeoh Y. Y., Kim D-W., Chung T. Y., Oh K. S., Lee W-S. Sub-10 nm gate-all-around CMOS nanowire transistors on bulk Si substrate. *Tech. Dig. Symp. of VLSI Tech. 2009: 94-95.*

[1.23] Suk S. D., Yeoh Y. Y., Li M., Yeo H. Y., Kim S. H., Kim D. W., Park D., Lee W. S. TSNWFET for SRAM cell application: Performance variation and process dependency. *Tech. Dig. Symp. of VLSI Tech. 2008:38-39.*

[1.24] Bidal G., Boeuf F., Denorme S., Loubet N., Huguenin J. L., Perreau P., Fleury D., Leverd F., Lagrasta S., Barnola S., Salvetat T., Orlando B., Beneyton R., Clement L., Pantel R., Monfray S., Ghibaudo G., Skotnicki T. High velocity Si-nanodot: a candidate for SRAM applications at 16 nm node and below. *Tech. Dig. Symp. of VLSI Symp*. 2009:240-241.

[1.25] Wunnicke O. Gate capacitance of back-gated nanowire field-effect transistors. *Appl. Phys. Lett.* 2006;89(8):083102.

[1.26] Giacomini R., Martino J. A. Trapezoidal cross-section influence on FinFET threshold voltage and corner effects. *J. Electrochem. Soc*. 2008;155(4):213-217.

[1.27] Chen J., Saraya T., Miyaji K., Shimizu K., Hiramoto T. Electron mobility in silicon gate-all-around [100]- and [110]- directed nanowire metal-oxide-semiconductor field-effect transistors on (100)-oriented silicon-on-insulator substra 399 te extracted by improved split capacitance-voltage method. *Jpn. J. Appl. Phys.* 2009;48(1):011205.

[1.28] Cassé M., Tachi K., Thiele S., Ernst T. Spectroscopic charge pumping in Si nanowire transistors with ah high-k/metal gate. *Appl. Phys. Lett.* 2010;96(12):123506.

[1.29] T. Tezuka. Observation of mobility enhancement in strained Si and SiGe tri-gate MOSFEts with multi-nanowire channels trimmed by hydrogen thermal etching. *Proc. Int'l Electron Device Meet. 2007.*

Chapter 2

Device fabrication and TCAD simulation

2.1 Introduction

2.2 Device structure of SiNW FET already reported

2.3 Device design of the silicon nanowire FET

2.4 Pre-experiments for fabrication of the silicon nanowire channel

2.5 Fabrication of the silicon nanowire FETs

2.6 TCAD simulation

2.7 Conclusions

2.1. Introduction

For a fabrication of silicon nanowire (SiNW) field-effect metal-oxide-silicon transistors (MOSFETs) with conventional bulk complementary MOS (CMOS) fabrication facilities, newly proposed device structure is necessary. In this chapter, I reviewed fabrication process of SiNW FETs and describe the device design guidelines in this work. To fulfill the guideline, new device structure was proposed and fabricated. Using technology computer aided design (T-CAD) software, inversion charge distribution across SiNW cross-section and inversion charge density of SiNW FET was investigated for prediction of contribution of inversion charge to drain current.

2.2. Device structure of the SiNW FETs already reported

I classified the device structure of the SiNW FET already reported; stack structure and damascene structure. I listed features of these two structures:

Stack structure:

- Similar to conventional gate-first process flow
- Relatively short fabrication steps
- Difficulty at the gate etching process due to three dimensional structure
- Not completely uniform channel width

Damascene structure:

- Similar to gate-last process of conventional CMOS process flow
- Relatively sophisticated process flow
- Uniform channel width
- Elimination of concerns at lithograph and etching process of gate patterning

SiNW FETs fabricated by institute of microelectronics, Singapore is one of the stacking structures. Twin SiNW FETs fabricated by Samsung electronics is one of the representative damascene structures.

2.3. Device design of the SiNW FET

2.3.1. Design guideline of the SiNW FET

Device structures of SiNW FET in this work were designed with guidelines. SiNW FET is a promising candidate for future CMOS technology. For realization of SiNW FET as the device structure at the end of the CMOS scaling technology, it is necessary to be able to fabricate the SiNW FET with the conventional bulk CMOS technology. This is because the special technology, for example Si epitaxial growth facility, is not familiar to all the semiconductor factories. Therefore, the device structure of the SiNW FET in this work was designed to be fabricated as easily as possible with conventional bulk CMOS technology.

2.3.2. Starting material

I used 300 mm diameter silicon-on-insulator (SOI) wafers fabricated by Soitech using Smart-Cut Technology™ for device fabrication of the SiNW FETs and planar SOI FETs in this work. A SOI layer is on a buried oxide (BOX) layer, and SOI layer was electrically separated from a handle wafer. There are some merits to use SOI wafer:

(i) It is easy to electrically separate each elemental device on the SOI wafer. Device isolation is necessary to prevent current leakage between each adjacent device. Using SOI wafer, each device is automatically electrically isolated after a pattering process of the first device dimension definition process. For the fabrication of integrated circuits using bulk silicon wafers, the shallow trench isolation (STI) process is necessary for electrical separation of each device. STI process is much complicated compared with the simple pattering process for SOI wafer. STI process includes lithography, dry-etching and cleaning, thick dielectric film deposition with chemical-vapor-deposition method, long time thermal annealing, and chemical-mechanical polishing processes.

(ii) It is easier to fabricate three-dimensional device on SOI wafer. Parasitic bottom channel could exist under the main channels using bulk silicon wafer. For the prevention of the parasitic bottom channel, ion implantation process is necessary so that the parasitic channel should not be inverted.

2.3.3. Semi gate around Structure

As the three-dimensional device is the promising candidate of future device, etching process becomes more channeling. After isotropic dry-etching process of gate electrode of the device, we must perform significant over-etching process so that stringers do not remain at the bottom of the pattern [2.1]. After the gate etching of the three-dimensional devices, the stringers tend to be more residual and enormous over-etching step is required. High selectivity against base gate dielectric, for example silicon oxynitride firm of high-k dielectric film, is required and very challenging. One of the smart ways is to reduce the amount of the over-etching step by filling the hump of the fabricating device. Therefore, I proposed a semi gate-around structure, as shown in **Fig. 2.1**, for the reduction of the hump of the SiNW FET in this work.

The semi gate-around structure is similar to the tri-gate structure [2.2]. Improved point is the silicon nitride sidewall at the side of the stem-like silicon dioxide support. The SiN sidewall was formed using chemical-vapor-deposition (CVD) process of silicon nitride firm and post etches back process using dry-etching. The sidewall reduced the hump and hence the amount of the over-etching was reduced. The reduction of the amount of over-etching is effective not only for the endurance of base gate dielectric film, but also for avoidance of the gate electrode deformation. **Figure 2.17 (b)** shows the cracked gate electrode because of the large amount of the gate over etching process. One reason is the previous bottom anti-reflective coating (BARC) etching and TEOS hard mask pattering process. During the TEOS hard mask pattering process, the thickness of the TEOS hard mask at the head of the gate electrode was reduced because of the un-uniformity of BARC thickness. Excessive over-etching process reduced the

TEOS mask and the head of the gate electrode was cracked. By reduction of the amount of the over-etching process, the cracking was avoided.

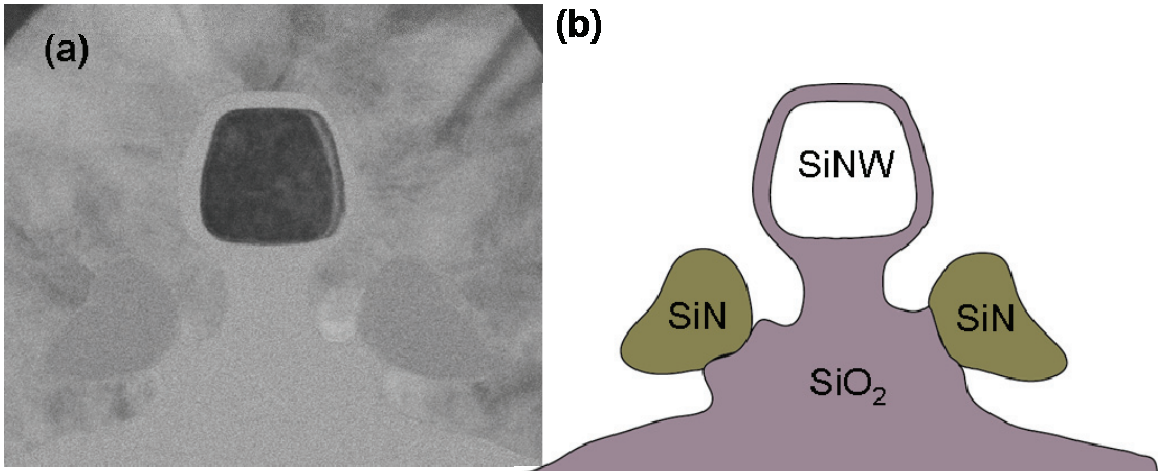


Figure 2.1 (a) Transmission electron microscope image of cross-section of semi gate-around structure (b) schematic illustration of the semi gate-around structure.

2.3.4. Device structure

To fabricate the SiNW FET with conventional CMOS fabrication facilities, I adopted the structure show in **Fig. 2.1**. I designed to form the SiNW FET with four mask layers as shown in **Fig. 2.2 (a)**. The first mask (OD) was used for the patterning of the fin structure with embedded source/drain pads. Formation of narrow source/drain (S/D) structure is out of the scope of this study. Therefore I adopted wide S/D pad for easy contact formation. Silicon fin was formed between S/D pads as shown in **Fig 2.2 (b)**.

I had a concern that the thickness the SOI layer of S/D region would be reduced by the sacrificial oxidation process for the formation of the SiNW channel. Therefore, I designed the formation process of the fin structure using SiN hard mask. After the patterning of the fin structure using SiN hard mask, the SiN layer prevents the oxidation of the S/D region. This process is similar to the local oxidation of silicon (LOCOS) process.

After the formation of the gate structure, the gate electrode was patterned with lithography and dry-etching process using the second mask (PO). Expected challenge is the gate patterning process because gate electrode was formed on the hump (the SiNW channel) as mentioned before. Planarization processes of the poly-Si layer using the chemical-mechanical polishing processes were also considered. Finally, the gate electrode was successfully fabricated with semi gate around structure.

I designed to form spacers after the gate pattering process. I planned to use nickel self-align silicidation process for reduction of parasitic series resistance of source/drain. However, early investigation shows that nickel silicide intrude into channel [kamimura]. Therefore, spaces were necessary to avoid excessive nickel silicidation of the SiNW channels.

After contact hole formation with CON-SOI mask, tungsten was deposited using CVD process. Finally, tungsten was pattered using M1 mask.

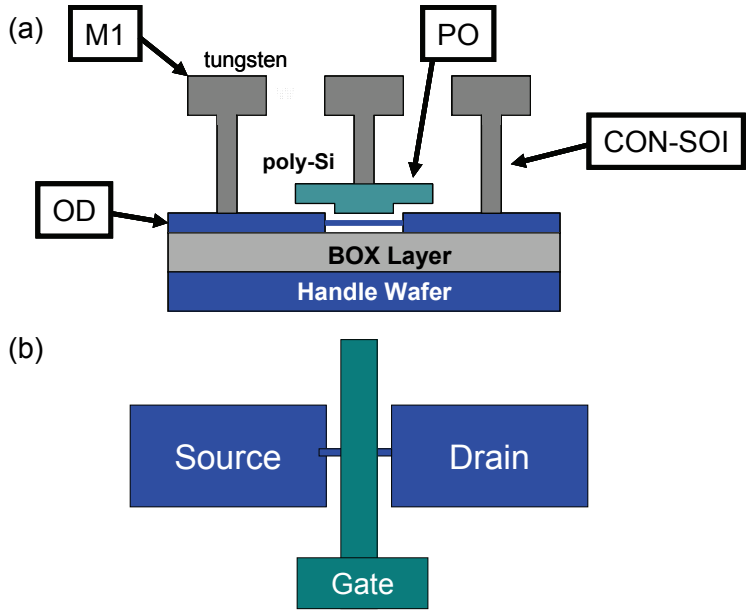


Figure 2.2 A schematic structure of the SiNW FET fabricated in this work.

2.3.5. Specifications of the mask set

- Chip size: 24.80 (mm) x 29.76 (mm)
- Four layers

Table 2.1 Specifications of the mask set: AL01-2.

Name	Roles	Type	Posi/Nega	Machine	Meas. Width (nm)	Minimum width (nm)
AL01-2- OD	Isolation	Bin	Posi	ArF	100	80
↓ PO	Gate	↓	↓	ArF	100	40
↓ CON-SOI	Contact	HfT	Nega	ArF	120	80
↓ M1 -02	Wiring	Bin	Posi	KrF	300	300

2.3.6. Specifications of mask pattern

I designed a chip with 25 sub-chips. In this section, I will describe details of the sub-chips. The chip consists of the SiNW FET with a channel, the SiNW FET with parallel multi-channels, the SiNW FET with four-terminal geometry, and the line and space patterns for cross-sectional secondary electron microscope and transmission electron microscope observations. Two large blank pattern for the measurement of the film thickness using spectroscopic ellipsometry or cross-sectional electron microscope observation. I also designed planar SOI FET with other SiNW FETs.

i. the SiNW FET with a single channel

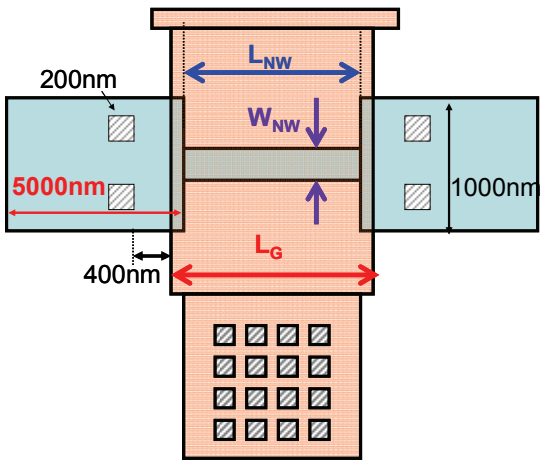


Figure 2.3 A schematic illustration of the single-channel SiNW FET.

Table 2.2 Specifications of the single-channel SiNW FET.

L_{NW}	**40, 50, 60, 70, 80, 90, 100, 120, 140, 160, 180, 200, 250, 300, 400, 500**	**16 types**
L_G	**80, 100, L_{NW}-10, L_{NW}, L_{NW}+50, L_{NW}+100**	**6 types**
W_{NW}	**90,100,110,120**	**4 types**

ii. SiNW FET with multi-channel

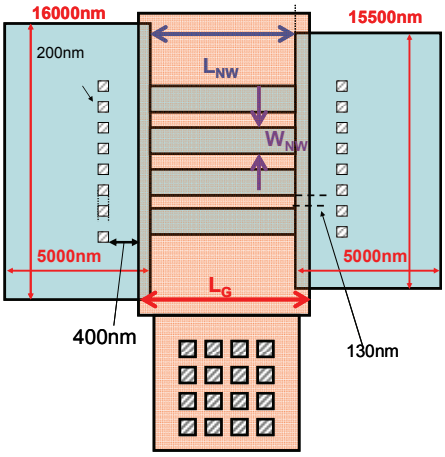


Figure 2.4 A schematic illustration of the multi-channel SiNW FET.

Table 2.3 Specifications of the multi-channel SiNW FET.

L_{NW}	**80, 100, 120, 140, 160, 180, 200, 500**	**8 types**
L_G	**L_{NW}-10, L_{NW}, L_{NW}+50, L_{NW}+100**	**4 types**
N_{NW}	**4, 16, 64**	**3 types**

iii. planar SOI FET

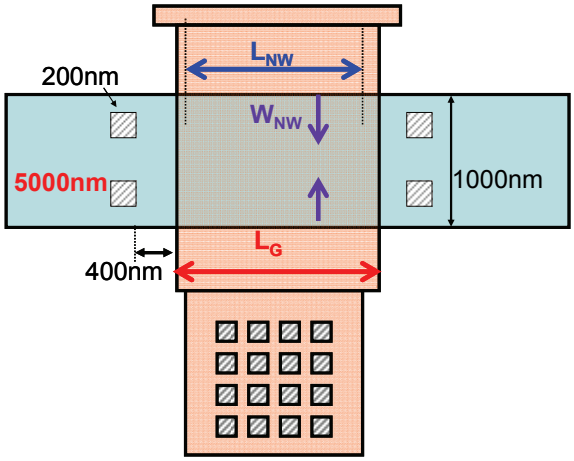


Figure 2.5 A schematic illustration of the SOI planar FET.

iv. SiNW FET with four-terminal geometry

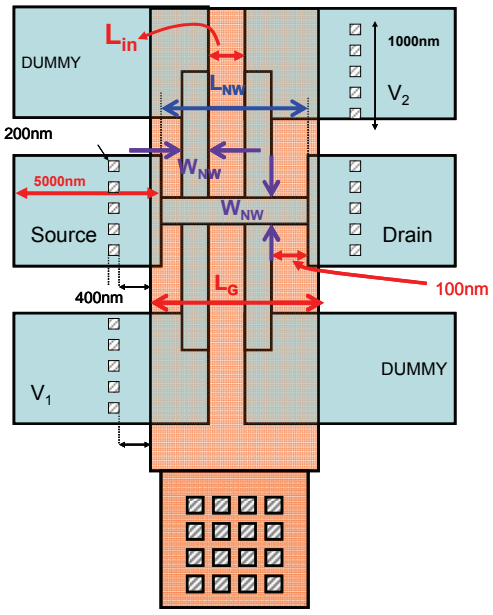


Figure 2.6 A schematic illustration of the SiNW FET with four-terminal geometry.

2.4. Pre-experiments for fabrication of the silicon nanowire channel

For fabrication of silicon nanowire (SiNW) field-effect transistors (FETs), fabrication process of the SiNW channel is one of the key processes. As the width of silicon nanowire channel is less than the limit of modern lithography technology, additional processes are necessary for fabrication of silicon nanowire channel. The SiNW with the width of 3 nm has already been successfully fabricated [2.3]. The width of the SiNW is narrower than the line width realized by the state-of-the-art lithography technology. For comparison, the half of the center-to-center pitch of metal interconnect is 22 nm and the width of the resist pattern for pattering of the gate electrode is 15 nm at the 22 nm technology node [2.4].

Many institutes employ the thermal oxidation process to reduce the width of the SiNW. The reason is that the interface between silicon and silicon dioxide formed by the thermal oxidation process is the most stable. On the other hand, reactive ion etching process induces surface roughness of silicon fin structure and plasma damage also should be considered. There damages might degrade electrical performance of the SiNW FET.

This is based on the self-limiting oxidation process [2.5]. Oxidation rate of the original silicon fin is decreased by additional stress from silicon dioxide during thermal oxidation because of the expansion of the volume of silicon dioxide [2.6]. I used the thermal oxidation process for the reduction of cross-sectional dimensions of the silicon fin structure. A reason is that I planed to fabricate the SiNW FET using silicon-on-insulator (SOI) wafer with the diameter of 300 mm at a pilot fabrication line. However, I thought that it costs a lot of SOI wafers to determine the fabrication condition of the SiNW FET in the pilot line because an experiment requires several SOI wafers per a experiment. I also thought that it costs a lot of time because I cannot exclusively use fabrication facilities, for example a thermal oxidation apparatus.

Therefore, I explored unit process conditions for fabrication of FET using chip-sized samples. Experiments using chip-sized samples are efficient with respect to cost and

time. This is because channel cross-section of silicon nanowire FET strongly depends on fabrication process. Therefore a lot of experiments are necessary for exploration of fabrication conditions. As the cross-sectional shape of the SiNW FET also strongly affects the electrical characteristics of the SiNW FET, electrical characteristics dependence on the cross-sectional shapes also should be investigated. In this chapter, I explore reports for fabrication of nanowire channel. I also examine fabrication process condition of silicon nanowire FET. Using technical computer-aided (TCAD) design software, I also investigated electrical characteristics of the SiNW FET.

2.4.1. Pattern dependent oxidation (PADOX)

Initial structural size and shape of a pattern on SOI substrates strongly affects oxidation process. Therefore, it is called the PAttern Dependent OXidation (PADOX). This is due to the stress and strain induced by the volume expansion of silicon dioxide formed during thermal oxidation process as shown in **Fig. 2.6** [2.6]. The viscosity of silicon dioxide around the SiNW depends on the temperature. As the temperature increase, the viscosity also increases, which results in the relief of localized stress by the oxide around the SiNW. It has been reported that the corner rounding depends on the oxidation temperature [2.7].

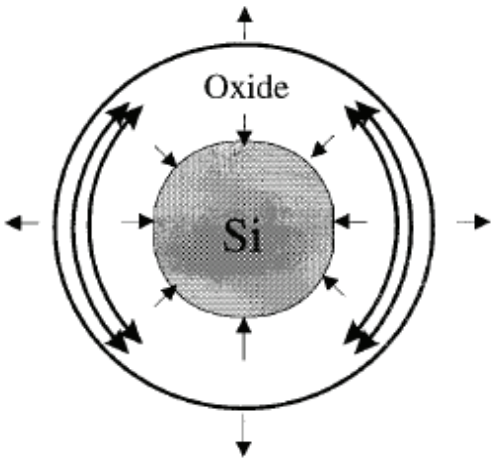


Figure 2.6 A schematic illustration of stress and strain induced by the volume expansion of oxide [2.6].

2.4.2. Experiments for fabrication of silicon nanowire channel

For exploring process condition of silicon nanowire, I first used silicon-on-insulator substrates with line and space patterns. A cross-sectional secondary electron microscope image of the substrate with line and space patterns with different fin width is shown in **Fig. 2.7**. The width of silicon fins on buried oxide (BOX) layer was determined by the dry ArF lithography process and post dry etching processes. The height of the fin was determined by the thickness of the silicon-on-insulator wafer. This is useful for experiments for exploring oxidation condition for fabrication of silicon nanowire.

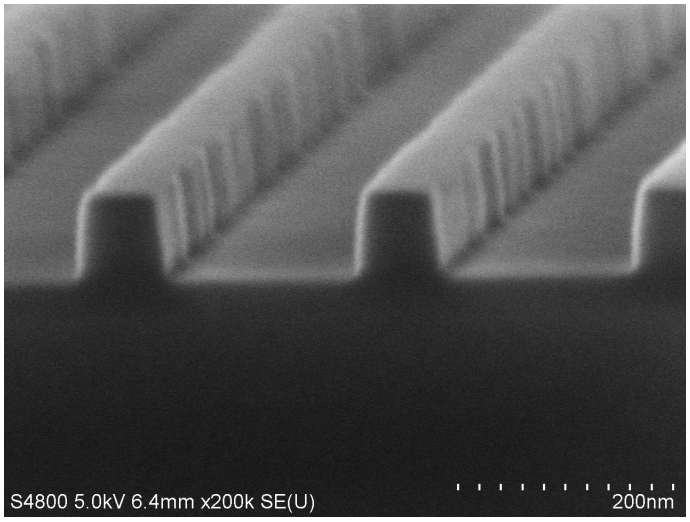


Figure 2.7 Cross-sectional secondary electron microscope image of line and space pattern using silicon-on-insulator wafer.

First, I investigated the aspect ratio of SiNW channel after thermal oxidation process. Cross-sectional dimensions were observed and measured using secondary electron microscope. **Fig. 2.8** shows the relationship of the aspect ratio before and after thermal oxidation process. As we can see, the square cross section was obtained with the square fin structure.

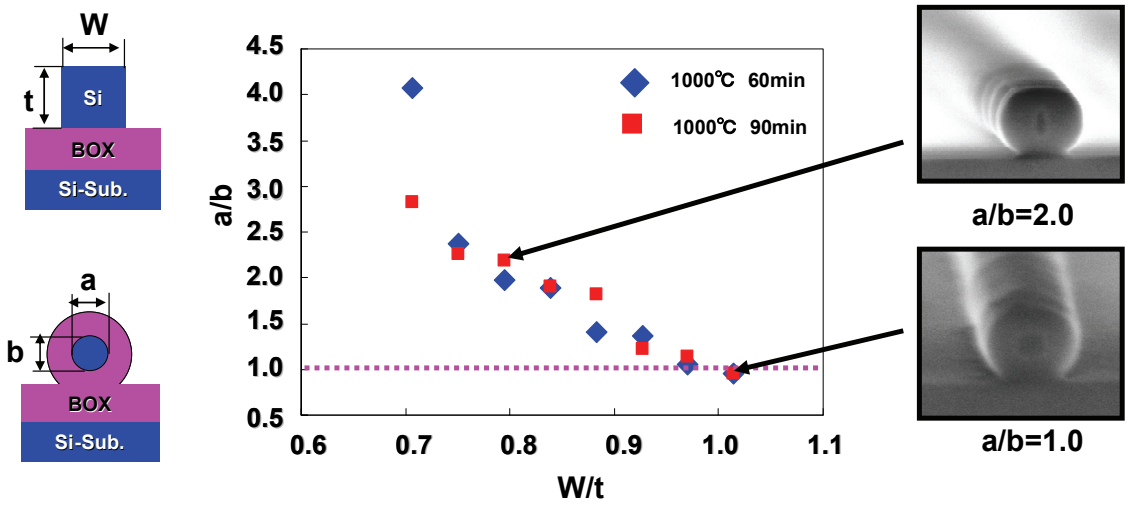


Figure 2.8 Aspect ratio of silicon nanowire before and after thermal oxidation process in dry oxygen ambient at 1000 °C for 60 minutes and 90 minutes.

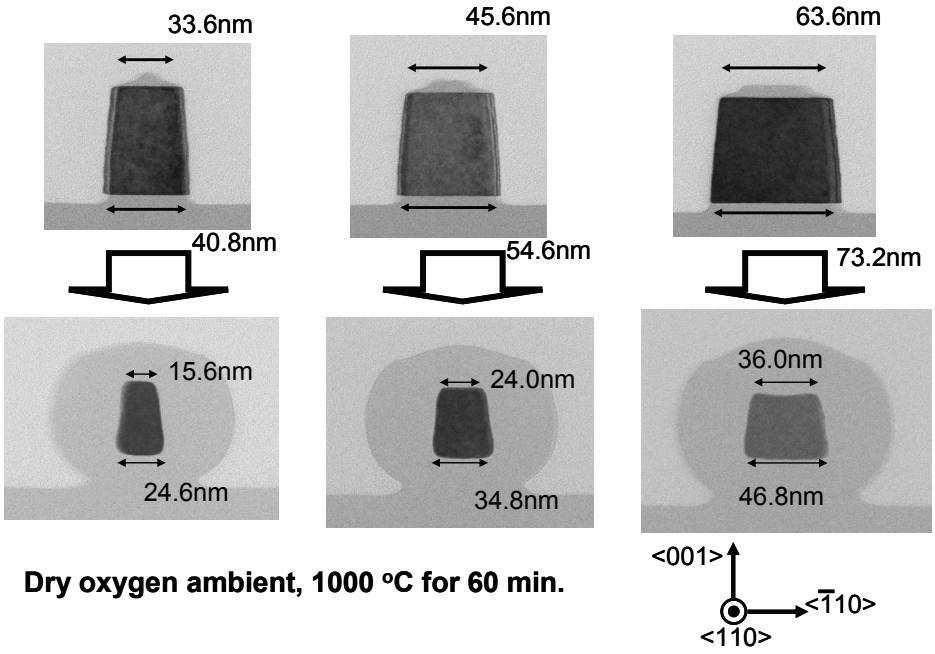


Figure 2.9 Cross-sectional transmission electron microscope images of silicon fins before and after thermal oxidation process in dry oxygen ambient at 1000 °C for 1 hour.

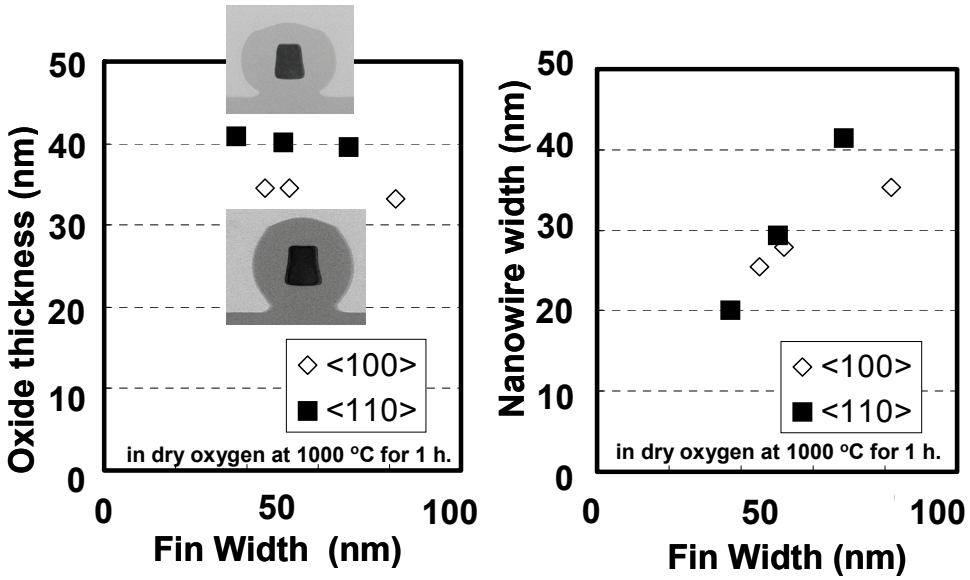


Figure 2.10 Oxide thickness and nanowire width as a function of the fin width oxidized in dry oxygen ambient at 1000 °C for 1 hour.

After sulfuric-peroxide mixture (SPM) cleaning and diluted-HF (DHF) cleaning, a substrate chip with line and space patterns were oxidized in dry oxygen ambient at 1000 ^{o}C. As shown in **Fig. 2.9**, silicon nanowires with rectangular or trapezoidal cross-section with rounded corners were formed. The initial fin width and the thickness of silicon dioxide are shown in **Fig. 2.10**.

As we can see, the oxide thickness depends on the direction of silicon nanowire. On the other hand, the nanowire width seems to be independent of the fin width. First, I consider the direction of the silicon nanowire and the fin structure, and their surface orientations. The <110>-directed fin structure has (100)-oriented surface at the top of the fin and (110)-oriented surfaces at the left and right sides. Whereas the <100>-directed fin structure has (100)-oriented surfaces around the fin structure. It has been reported that the oxidation rate of (110)-oriented silicon substrate was 1.7 nm/min. On the other hand, the oxidation rate of (100)-oriented silicon substrate was 0.80 nm/min [5]. Therefore the oxide thickness of the <110>-directed silicon fin seems to be larger than that of the <100>-directed silicon fin structure.

The young modulus of (100)-oriented surface is 169 G Pa and the young modulus of (110)-oriented surface is 130 G Pa. Therefore the oxidation rate of (110)-oriented surface might be larger than that of (100)-oriented surface.

The experimental results in **Fig. 2.12** show that the oxidation rate of (110)-oriented surface is larger than that of (100)-oriented surface. This result suggests the oxidation rate dependence on the surface orientation is more effective than the young modulus.

For the optimization of cross-sectional shape, I observed the height and width of silicon nanowires using secondary electron microscope as shown in **Fig. 2.9**. If the temperature during thermal oxidation is lower than 1000 ^{o}C, I speculate that the corners will be sharp so as to induce a concentration of electric field near corners. Higher temperature than 1000 ^{o}C might result in more rounded cross-sections. However, for industrial use, less than 1000 ^{o}C is better because thermal oxidation with the temperature more than 1000 ^{o}C is a special process.

Oxidation rate of silicon depends on the surface orientation. As the oxidation rate also depends on the stress of silicon, young modulus also affects the oxidation rate.

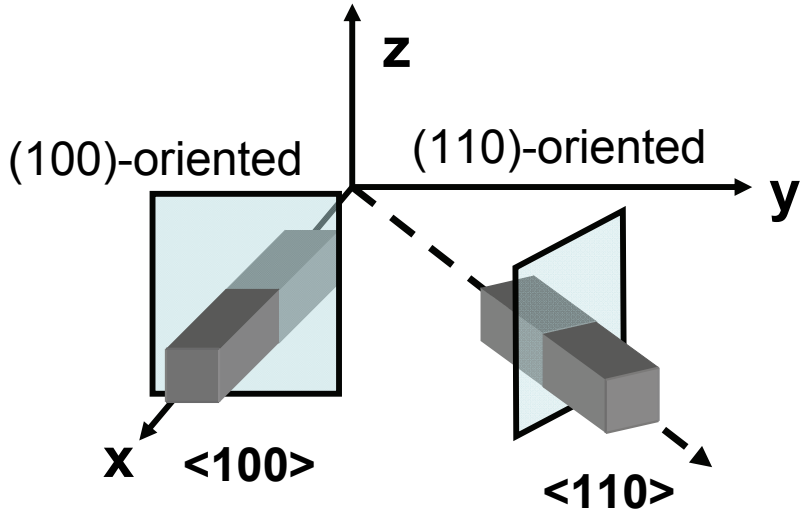


Figure 2.11 Channel directions and surface orientations of silicon fins used for experiment.

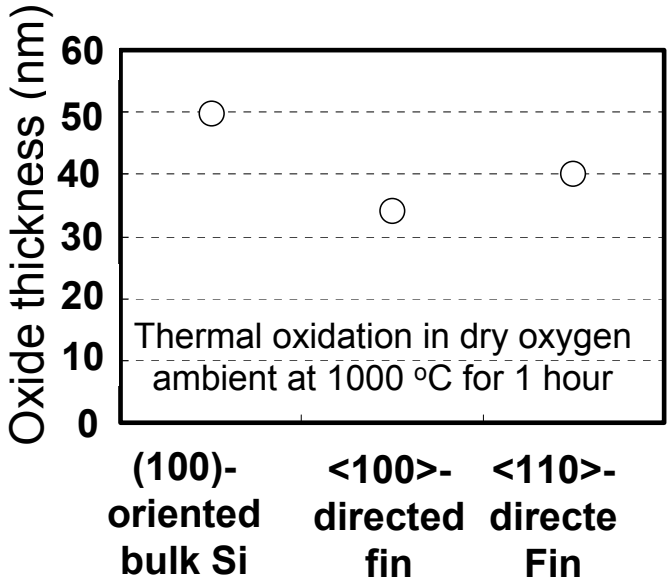


Figure 2.12 Oxide thickness of (100)-oriented bulk silicon chip and <100> and <110>-directed silicon fin.

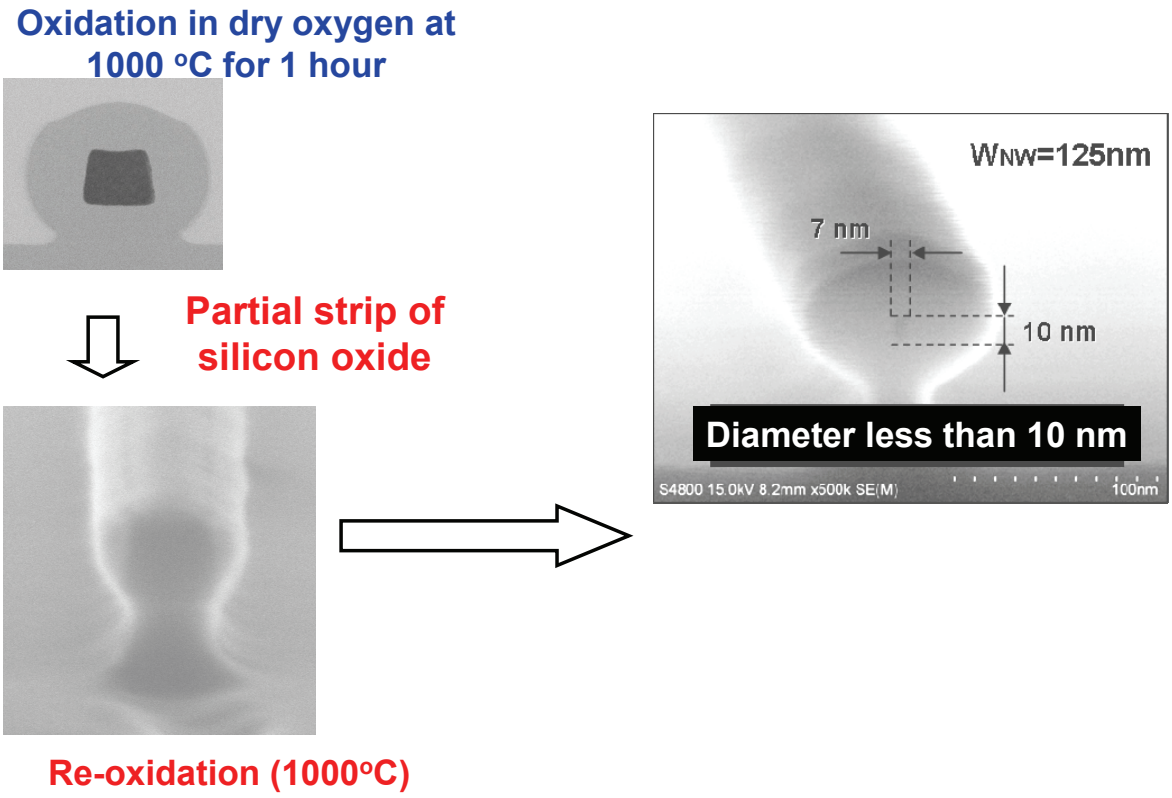


Figure 2.13 cross-sectional transmission electron microscope image and secondary electron microscope images after first sacrificial oxidation, partial strip of silicon dioxide, and after second sacrificial oxidation process. After the second sacrificial oxidation process, SiNW channel with the diameter less than 10 nm was formed.

I examined second time oxidation process as shown in **Fig. 2.13**. As mentioned above, oxidation rate of silicon nanowire decreases as the oxide thickness increases because of the stress in silicon nanowire by volume expansion of silicon dioxide. Diffusion of oxygen atom from atmosphere into silicon nanowire also decreases as the oxide thickness increase. Therefore etching of silicon dioxide around silicon nanowire seems to be an effective way for accelerate oxidation of silicon nanowire.

Wet oxidations relief stress in oxide induced by volume expansion because of viscosity of oxide. Therefore, the wet oxidation is a candidate for formation of silicon nanowire channel. Doping of phosphorus is another method for fabrication of silicon nanowire with rounded cross-sectional shape.

2.5. Fabrication process of the silicon nanowire FETs

A process flow of SiNW FET was constructed so that the SiNW FET could be fabricated with facilities with ASKA II line in Selete, Tsukuba, which had fabrication facilities that are enough to fabricate bulk CMOS devices. Fabrication process flow was shown in the below. Channel height (h_{NW}) and channel width (w_{NW}) was determined by SOI layer thickness and fin width.

2.5.1. Formation of silicon fin structure

The SOI wafer was cleaned with surfer peroxide mixture (SPM), ammonia peroxide mixture (APM) and finally diluted-HF (DHF) cleaning. For a reduction of a thickness of SOI layer, the wafers were subjected to thermal oxidation process. After a removal of the prior sacrificial oxide layer by HF dipping, silicon oxide or silicon nitride (SiN) was formed with chemical vapor deposition (CVD) process with tetraethoxysilane (TEOS) or dichlorosilane (DCS). Before the deposition of SiN, thermal oxide of 7 nm was formed as pad layer. The SiN layer was intended to protect source/drain region from a following sacrificial oxidation process.

After lithography process with dry ArF scanner with coating of resist and bottom anti-reflective coating (BARC) and development, hard mask was patterned with dry etching process. After dry ashing, SOI layer was patterned with dry etching process with chlorine chemistry. A review-SEM image of the fin structure after the etching of SOI layer is shown in **Fig. 2.14**.

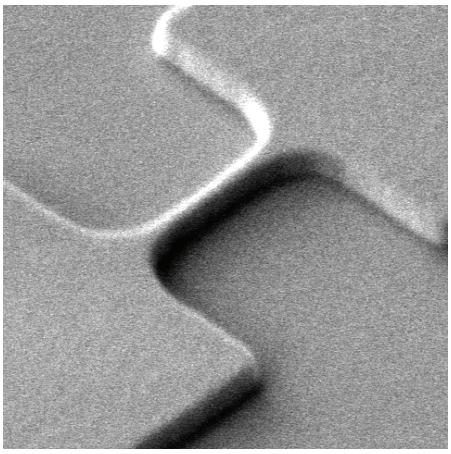


Figure 2.14 Fin structure after formation of Si fin structure.

2.5.2. Sacrificial oxidation process

For fabrication of narrow silicon nanowire channel whose width is less than the limit of lithography process, a sacrificial oxidation process was employed. Cross-sectional TEM images of the Si fin before and after the sacrificial oxidation are shown in **Fig. 2.9**. SiN layer was removed with hot phosphoric acid batch system. A fin structure after the removal of SiN layer is shown in **Fig. 2.15**. A cross-sectional TEM image combined with SEM image along channel direction is also shown in **Fig. 2.16**. Handle wafer below SiNW channel was oxidized, and silicon dioxide formed by thermal oxidation push up SiNW channel.

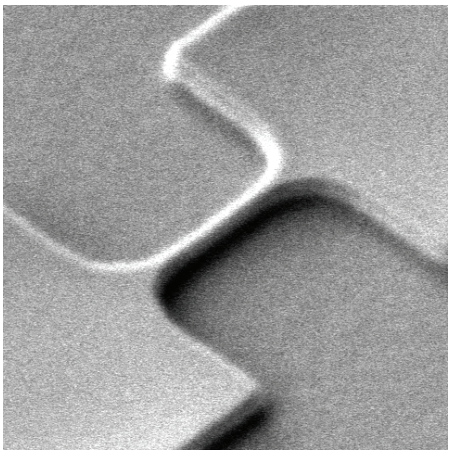


Figure 2.15 Secondary electron microscope image of a fin structure after a removal of silicon nitride layer.

Sacrificial oxidation process tends to employ self-limiting oxidation. This phenomenon was by stress in silicon dioxide during thermal oxidation process as mentioned in **chapter 2**. However, it seems that thermal oxidation in dry oxygen ambient at 1000 oC for 1 hour is previous to the self-limiting region and there is a room for thinning of the diameter of silicon nanowire.

Figure 2.16 shows a mixed picture of transmission electron microscope image and secondary electron microscope image. As we can see, the thickness of silicon-on-insulator layer of source and drain region was larger than the height of silicon nanowire channel. This is due to silicon nitride hard mask on the source and drain

region of the silicon nanowire FET. In addition, silicon nanowire channel was bended up by buried oxide layer thickened by the prior thermal oxidation process.

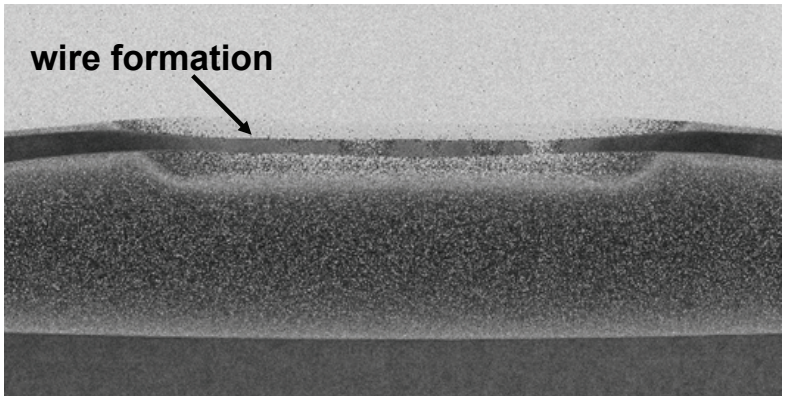


Figure 2.16 A mixed image of transmission electron microscope and secondary electron microscope images of the cross-section of silicon nanowire FET before formation of gate electrode.

2.5.3. Formation of semi gate-around structure

As mentioned in device design section, I fabricated SiNW FET with a channel that is fixed to BOX layer of SOI wafer. I will write fabrication processes to form a gate semi-around structure.

After partial removal of sacrificial oxide, silicon nitride sidewall was formed with the deposition of silicon nitride film of 50 nm using DCS and the etch-back process. Then the residual sacrificial oxide was removed and SiNW channel was exposed. The gate oxide with a thickness between 1.5 and 5 nm was formed with rapid thermal process facility and polycrystalline silicon (Poly-Si) was deposited as gate electrode. After ion implantation process into the gate electrode (phosphorus for nFET and boron for pFETs), silicon oxide hard mask of 30 nm using TEOS was deposited. The gate electrode pattern was formed with dry ArF lithography process, and the resist pattern was transferred to the TEOS hard mask. After a dry ashing process, poly-Si electrode was formed using dry-etching process.

As the SiNW FET is three-dimensional structure, an improvement has to be made at gate etching process as shown in **Fig. 2.17**. Because the gate pattern protrudes over the

source, drain, and channel pattern, over-etching is necessary for gate pattering. There were some difficulties about this process. That is the top of gate electrode was broken at the edge of the wafer by over etching process. In order to solve the problem, a height of SiNW channel was reduced and the amount of over-etching was also diminished. By reduction of the height, gate electrode was formed successfully.

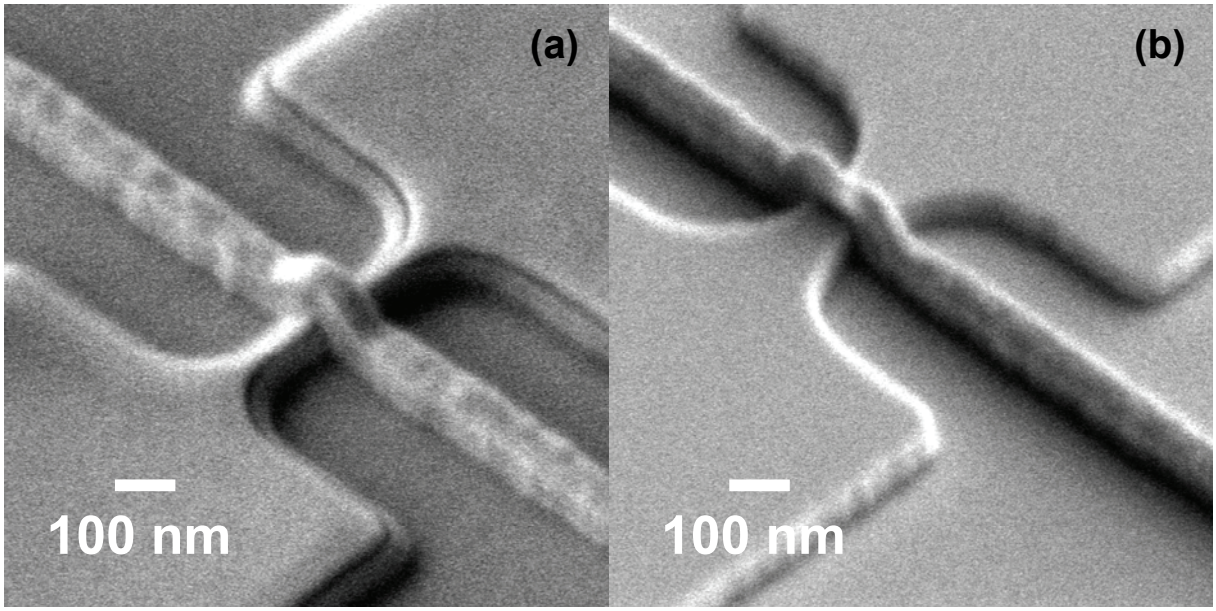


Figure 2.17 (a) Polycrystalline silicon gate electrode was successfully fabricated with semi gate-around structure by reduction of the over-etching step time (b) defective poly-Si gate because of the large over-etching time step.

2.5.4. Spacer formation and ion implantation process

After gate pattering process, gate sidewall was formed. After deposition of TEOS of 2 nm, SiN layer of 5nm was formed using hexachlorodisilane (HCD), which was followed by dry etch-back process. The TEOS layer was inserted as the etch-stop layer of the etch-back process of the HCD silicon nitride film. Dopant ions were implanted into source/drain region with low acceleration energy ion implantation facilities (SEN co. ltd, SHX). Silicon oxide film of 5 nm and silicon nitride film of 50 nm were

deposited and etch-backed again for the formation of the second spacer. Dopant ions were again implanted. After cleaning process, the wafers were subjected to rapid thermal process facilities (Applied Materials, Radiance) for spike annealing aiming at 1000 ^{o}C.

2.5.5. Nickel self-align silicidation process

For reduction of parasitic series resistance of the SiNW FETs and the planar SOI FETs, self-align nickel silicidation (SALICIDE) process was employed. After removal of residual silicon oxide on source/drain by wet etching process, nickel (Ni) of 9 nm and titanium nitride (TiN) of 10 nm was deposited using physical vapor deposition (PVD) method. Then the wafers were subjected to annealing at 435 ^{o}C for 60 seconds for silicidation. It has been reported that there are concerns on encroachment of nickel silicide between source and drain. However, the encroachment was not observed by cross-sectional transmission microscope images in this work. Anomalous nickel diffusion was observed with some transistors. Cross-sectional transmission electron microscope image was shown in **Fig. 2.18**. We can see anomalous nickel diffusion into whole SOI layer from high angle annular dark field scanning TEM (HAADF-STEM) images.

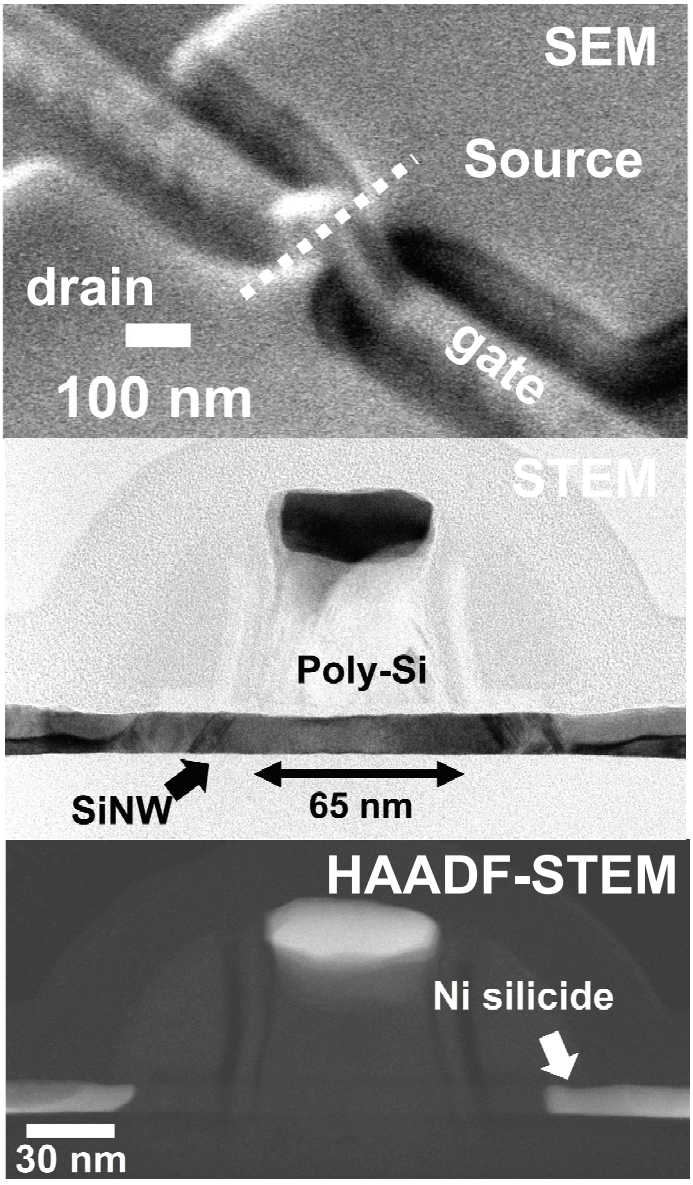


Figure 2.18 (a) A review secondary electron microscope image of the SiNW FET (b) cross-sectional transmission electron microscope image along the SiNW channel (c) High Angular Annular Dark Field Scanning TEM image of the SiNW FET along the SiNW channel.

2.5.6. Back-end process

After deposition of contact etch-stop liner (CESL) of HCD-SiN at 450 ^{o}C, and post metallization dielectric layer of high density plasma chemical vapor deposition silicon oxide (HDP-SiO_2) of 470 nm was deposited. Contact hole patterns were formed with dry ArF lithography process using CON mask. Contact hole was opened and nickel silicide layer was used as an etch-stop layer. After plasma sputtering for cleaning, tungsten electrode was deposited with CVD process. Wiring pattern was formed with KrF lithography process. Finally wiring was formed by dry etching as shown in **Fig. 2.19**. After the cleaning, wafers were subjected to sintering process.

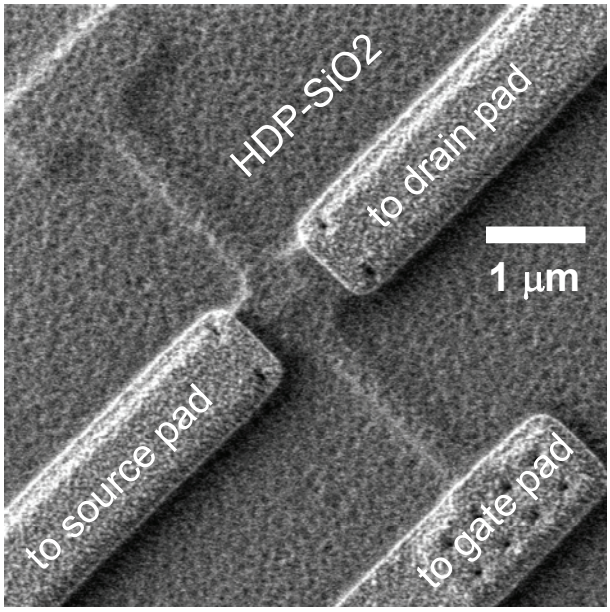


Figure 2.19 A review secondary electron microscope image of the SiNW FET after patterning process of tungsten wiring.

2.6. TCAD simulation

As mentioned in the chapter 1, a cylindrical conductor model predicts that the gate capacitance of nanowire structure is larger than the gate capacitance of the planar FETs. To confirm the increase of gate capacitance of MOS structure, inversion charge distribution and gate capacitance was calculated using technical computer aided design (TCAD) software.

2.6.1. Computer simulation scheme

I used the Technical computer aided design (T-CAD) software tools for expectation of the electrical characteristics of the SiNW FET. I used Taurus-MEDICI by Synopsys for two-dimensional simulation and design of channel cross-section. For three-dimensional simulation, I used Taurus-DAVINCE. Electrical characteristics, for example capacitance-voltage C-V characteristic, transfer and output characteristics are evaluated using Taurus-DAVINCI.

First, computation mesh was generated by Taurus-MEDICI. Auto-boundary condition (ABC) mesh generator was used for precise and effective mesh generation. A typical cross-section with mesh division is shown in **Fig. 2.20**. Then, three-dimensional structure was designed using the two-dimensional generated mesh by Taurus-DAVINCI. Typical physical parameters of n-doped polycrystalline silicon of n-doped poly-Si were used for gate electrode. Dopant concentration of source/drain regions was set to 10^{20} cm^{-3}. The abrupt junction between both source/channel and drain/channel was employed. The gate oxide thickness of the SiNW FET was designed to be uniform around the SiNW channel.

The Gate-to-channel capacitance of the MOSFETs was calculated using quasi-static like computation scheme as shown in **Eq. 2.1**.

$$C = \frac{dQ_{gate}}{dV_{gate}} \qquad (2.1)$$

As we have to take account the quantum-mechanical effects, modified local density approximation (MLDA) method [2.9, 2.10] was used.

2.6.2. Inversion charge distribution

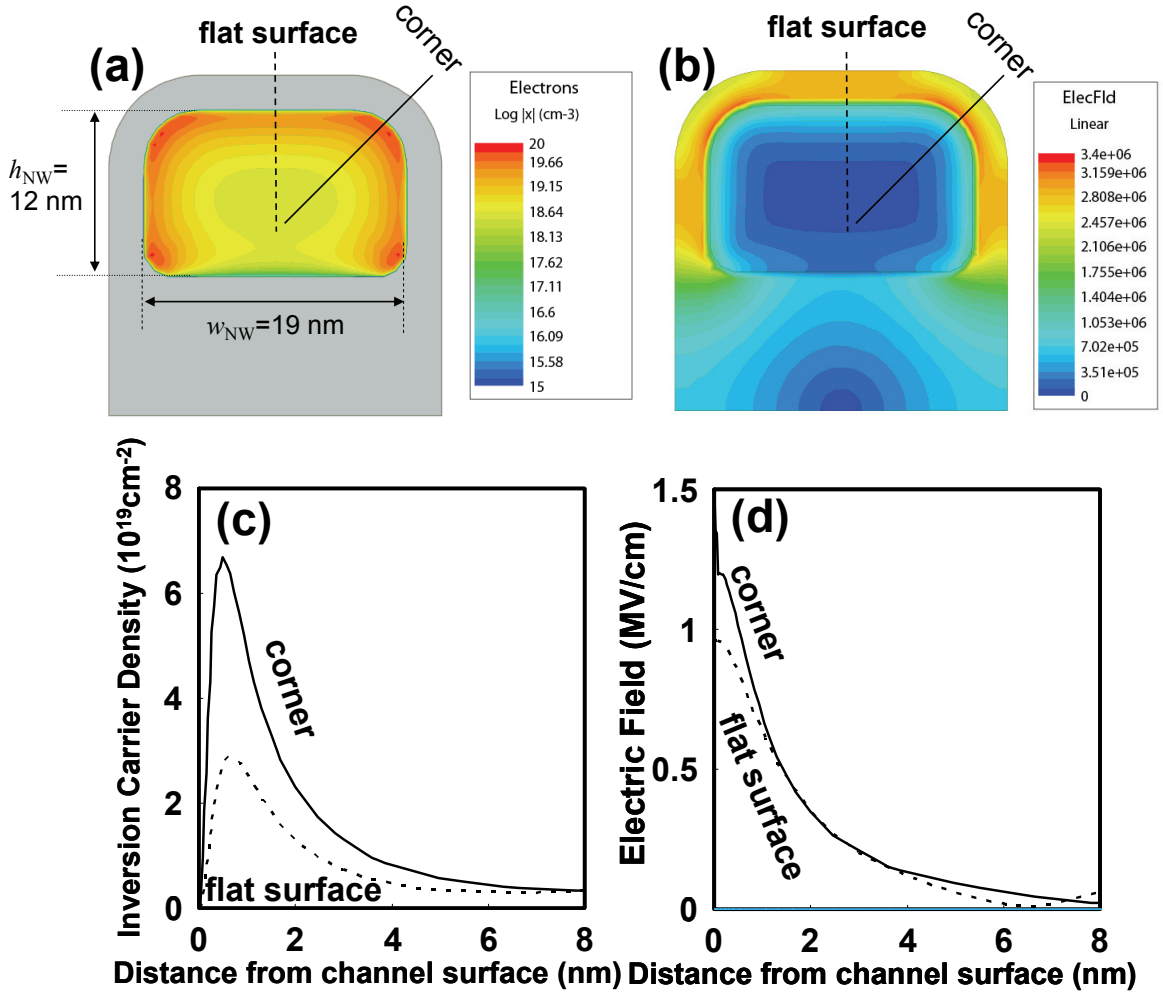


Figure 2.20 (a) Inversion charge distribution and (b) magnitude of electric field across the SiNW channel at the overdrive voltage of 1.0 V at the center and corners of the SiNW channel.

We can see in **Fig. 2.20** higher electric field around corners than the electric field along flat surface. The higher electric field at corners leads to higher inversion carrier density around the corners, which is equal to a reduction of the equivalent oxide thickness around corners. **Fig. 2.21 (a)** shows inversion charge density of SiNW nFETs with rectangular cross-section. The channel width w_{NW} and the channel height h_{NW} were 19 and 12 nm, respectively, with different corner radii. We examined effects of corner radii on the

gate capacitance. **Fig. 2.21 (a)** suggests that the inversion charge density is almost consistent with different corner radii. We evaluated the peak inversion carrier density around the corners, and as the corner radius increased the peak carrier density decreased as shown in **Fig. 2.21 (b)**. On the other hand, an area in the SiNW channel that has inversion carrier density more than 3.2×10^{19} cm^{-2} increased as the corner radius increased as shown in **Fig. 2.21 (b)**. We speculate that a trade-off relationship between the peak inversion carrier density and the area of high inversion carrier region resulted in the consistent inversion charge density with different corner radii. We can also observe this trade-off relationship in **Fig. 2.21 (d), (e), and (f).**

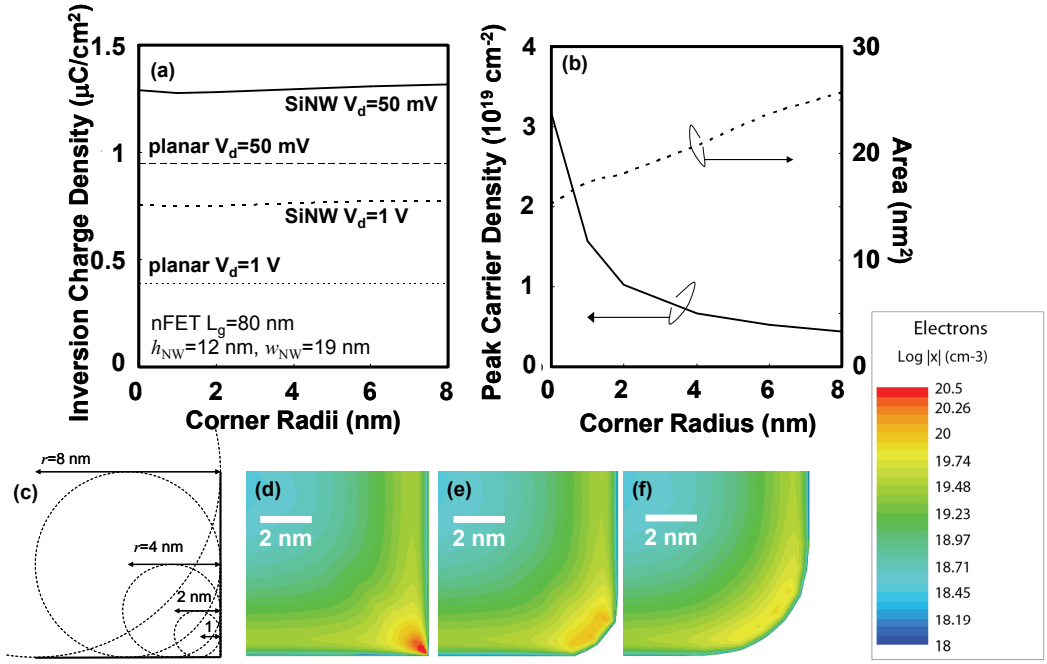


Figure 2.21 (a) Inversion charge density as a function of corner radius. (b) Peak inversion carrier density and area with inversion carrier density over 3.2×1019 cm-2. (c) Schematic illustration of corner radius (r). Contour plot of inversion carrier density with corner radii of (d) 0, (e) 2 and (f) 4 nm at the upper-corner of the SiNW channel.

2.6.3. Inversion charge density

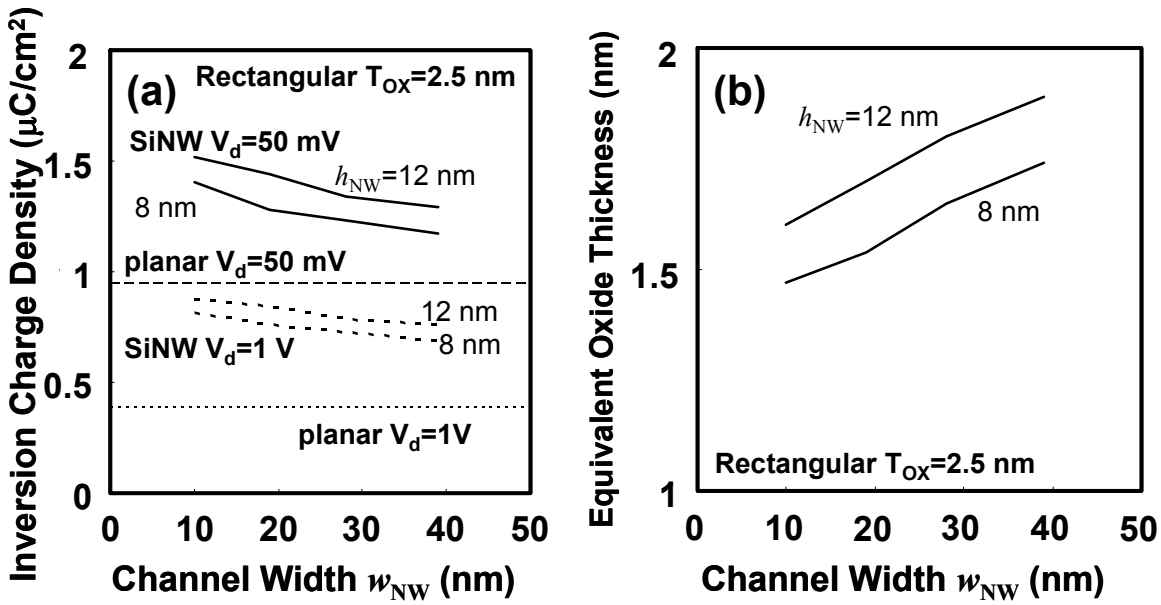


Figure 2.22 (a) Inversion charge density of SiNW nFETs with rectangular cross-sections (hNW=8 and 12 nm) and the upper-corner radius of 4 nm. (b) Equivalent oxide thickness of SiNW nFETs with rectangular cross-sections (hNW=8 and 12 nm) and the upper-corner radius of 4 nm.

Next, we investigated inversion charge density and equivalent oxide thickness of SiNW FET with rectangular cross-section as a function of channel width w_{NW}. **Fig. 2.22 (a)** shows inversion charge density at the overdrive voltage of 1.0 V. As w_{NW} decrease, inversion charge density at both low and high drain bias voltage increased. Equivalent oxide thickness (EOT) of SiNW nFETs are shown in **Fig. 2.22 (b)**. Higher EOT was obtained with smaller w_{NW}. We speculated the higher EOT with smaller w_{NW} was due to high inversion carrier region around the corners of channel cross-section. **Fig. 2.23 (a)** shows inversion carrier distribution and **Fig. 2.23 (b)** shows inversion carrier density of SiNW nFETs with triangular channel cross-sectional shapes. Corner angle θ is the upper corner angle of triangular cross-section. Channel height h_{NW} is 12 and 16 nm. As the corner angle decreased, inversion charge density increased and equivalent oxide thickness decreased. We speculate that a higher peak inversion carrier density with a smaller corner angle θ is the main reason.

Although lower corner angles of triangular cross-section decrease as the upper corner angle increases, contributions of the upper corner are larger than the contributions of lower corners because of the gate semi-around structure as shown in **Fig. 2.23 (a)**.

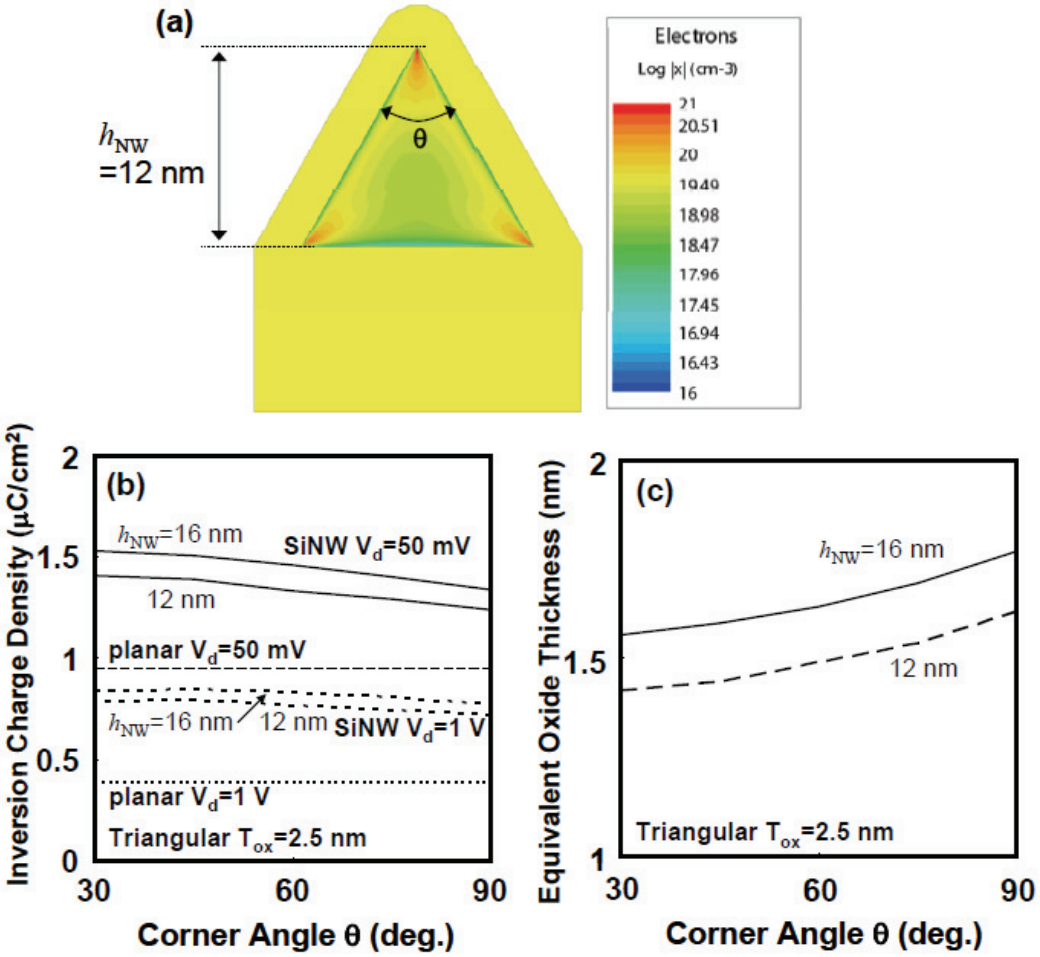


Figure 2.23. (a) Inversion carrier distribution and (b) inversion charge density of SiNW nFETs with triangular cross-sections. (b) Equivalent oxide thickness of SiNW nFETs with triangular cross-sections.

2.7. Conclusions

In this chapter, fabrication of the SiNW FET with conventional bulk CMOS process was demonstrated. SiNW FETs with semi gate structure were fabricated without special processes, for example silicon epitaxial growth facilities. The semi gate-around structure was effective for reduction of the amount of over-etching during gate pattering process. The silicon nitride layer on source/drain regions prevented thermal oxidation of the source/drain regions, which lead to successful fabrication of the SiNW FET with the diameter down to 10 nm.

Using T-CAD software, the inversion charge distribution and inversion charge density of the SiNW FET was investigated. High concentration regions around the corners of the cross-sections were confirmed, which was due to the concentration of electric field around the corners. These results coincide to theoretical prediction in **chapter 1**. I observed the high inversion charge density around corners both at low drain bias voltage and high drain bias voltage, which suggest that the increase of inversion charge density can contribute to enhancement of on-current of the SiNW FET.

References

[2.1] D. Yost, T. Forte, M. Fritze, D. Astolfi, V. Suntharalingam, C. K. Chen, and S. Cann. Dry etching of amorphous-Si gates for deep sub-100 nm silicon-on-insulator complementary metal-oxide-semiconductor. *J. Vac. Sci. Technol. B.* **20** (2002) 191-196.

[2.2] S. Sato, H. Kamimura., H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Yamada, and H. Iwai. Electrical characterization of Si nanowire field-effect transistors with semi gate-around structure suitable for integration. Solid-State Electron. 2010;54(9):925-928.

[2.3] M. C. Lemme, T. Mollenhauer, H. Gottlob, W. Henschel, J. Efavi, C. Welch and H. Kurz. High selective HBr etch process for fabrication of triple-gate nano-scale SOI-MOSFETs. *Microelec. Eng.* **73-74** (2004) 346-350.

[2.4] N. Singh, F. Y. Lim, W. Fang S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi1, A. O. Adeyeye1, G. Q. Lo, N. Balasubramanian, and D. L. Kwong. Ultra-narrow silicon nanowire gate-all-around CMOS devices: Impact of diameter, channel-orientation and low temperature on device performance. Int'l Electron Device Meet. 2006. 1-4.

[2.5] R. F. Pease, and S. Y. Chou. Lithography and other patterning technique for future electronics. Proceedings of the IEEE. **96** (2008) 248.

[2.6] H. I. Liu, D. K. Biegelesen, F. A. Ponce, N. M. Johnson, and R. F. W. Pease. Self-limiting oxidation for fabrication sub-5 nm silicon nanowires. Appl. Phys. Lett. 64(11)1994, 1383.

[2.7] J. Kedzierski, J. Bokor, and C. Kisielowski. Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation. J. Vac. Sci. Technol. B **15** (1997) 2825.

[2.8] M. Uematsu, H. Kageshima, K. Shiraishi, M. Nagase, S. Horiguchi, Y. Takahashi. Two-dimensional simulation of pattern-dependent oxidation of silicon nanostructures on silicon-on-insulator substrates. Soslid-State electron. **48** (2004) 1073.

[2.9] Taurus-MEDICI user guide. Version D-2010.03. Synopsys. March 2010.

[2.10] Taurus-DAVINCI user guide. Version D-2010. Synopsys. March 2010.

Chapter 3

Evaluation of Dc characteristics of SiNW FET

3.1 Introduction

3.2 Characterization methods

3.3 Transfer and output characteristics

3.4 On-current

3.5 Parasitic source/drain resistance

3.6 I_{ON}/I_{OFF} characteristics

3.7 Structural advantage of the SiNW FET

3.8 Separation of the on-current

3.9 Conclusions

References

3.1.Introduction

High on-current of MOSFET in integrated circuits is necessary because a reduction of total delay time has been required for high speed circuits. **Fig. 3.1** shows the on-current-per-wire that has already been reported. The cross-sectional dimensions are also depicted in **Fig. 3.1**. It is difficult to extract trends from this figure. This is because cross-sectional dimensions and shapes of SiNW channels, and structures of source and drain regions of SiNW FETs are different, which stems from the fact that many institutes fabricated their SiNW FET with their own processes. Therefore, it is very important to find guideline for design of cross-sectional shape and dimensions that is suitable for the high performance SiNW FET by comparing SiNW FETs with different cross-sectional shapes and same source and drain structures.

The purpose of this chapter is to establish the guideline for design of channel cross-section aiming at high on-current.

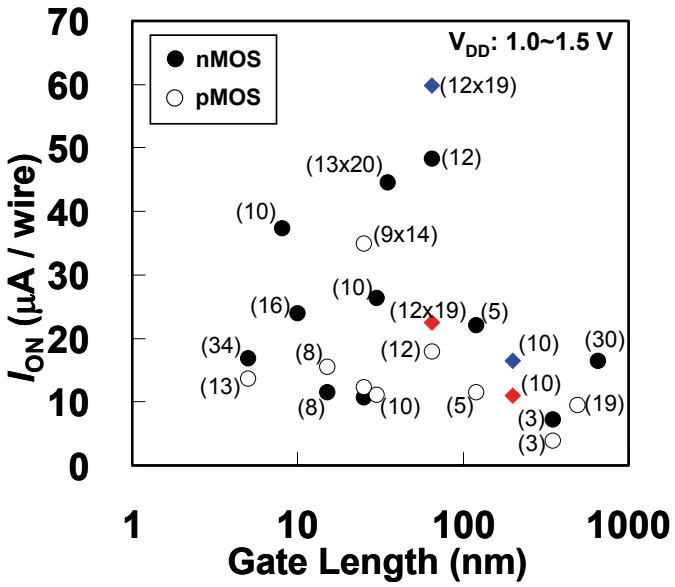


Figure 3.1 On-current per wire of the SiNW FETs already reported.

3.2 Characterization methods

3.2.1. Normalization of the electrical characteristics of the SiNW FET

As SiNW FET has different cross-sectional shape, channel height (h_{NW}) and channel width (w_{NW}), normalization of electrical characteristics is necessary for comparison of electrical characteristics among different devices.

In this research field, there are two ways for normalization of electrical characteristics: (*i*) normalization by the peripheral length; (*ii*) normalization by the device width, or foot-print. As the peripheral length is the sum of the channel height and width, the peripheral length strongly depends on the cross-sectional shape. Therefore the normalization by the peripheral length is advantageous for discussion of structural effect on carrier transport of the SiNW FET.

On the other hand, normalization by the foot-print is advantageous for comparison with different structure devices for discussion of electrical performance, for example bulk silicon devices and planar SOI FETs. In the integrated circuits, foot-print is important for device integration. For high speed operation, high on-current per width is required. On this view point, normalization by the foot-print is important.

In this work, the normalization by the peripheral length is used for comparison of the electrical transport properties of the SiNW FET and planar SOI FET for discussion of the structural effects of the SiNW FET. The normalization by the foot-print is used for benchmark of the on-current of the SiNW FET in this work with MOSFET with any structure.

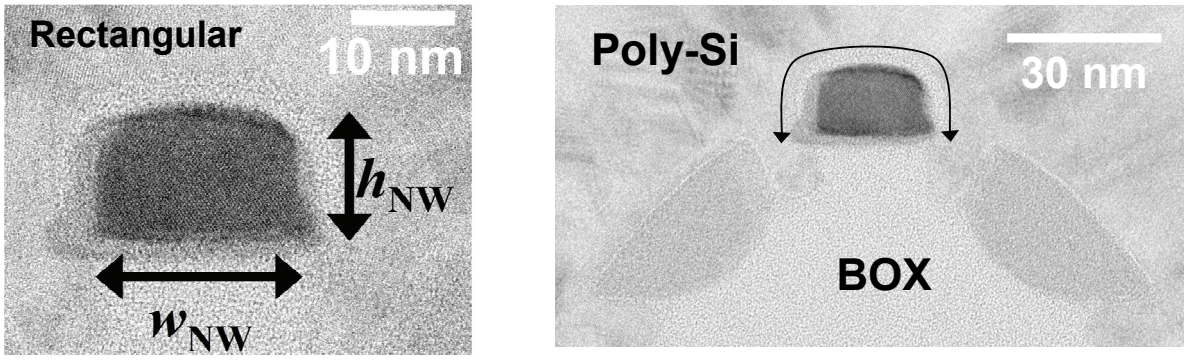


Figure 3.2 A schematic illustration for the normalization method by the peripheral length of channel cross-section of the SiNW FET.

3.2.2. Chern's channel resistance method [3.1]

For extraction of effective gate length (L_{eff}) and parasitic source/drain series resistance (R_{SD}), Chern's resistance method was employed. Effective gate length is largely different from the gate length described on the reticules for lithography process. Reasons are (*i*) condition of the lithography process; (*ii*) the width of resist pattern shrinks after trimming process; (*iii*) dopant diffusion from source and drain regions.

More than three devices with different mask gate length (L_{mask}) are used for CRM. The total resistance of MOSFET (R_{tot}) at the different gate bias voltage is also used. R_{tot} is plotted as a function of the L_{mask}. Three lines shrink at a point, which indicates the difference between mask gate length and effective gate length (ΔL), and R_{SD} as shown in **Fig. 3.3**.

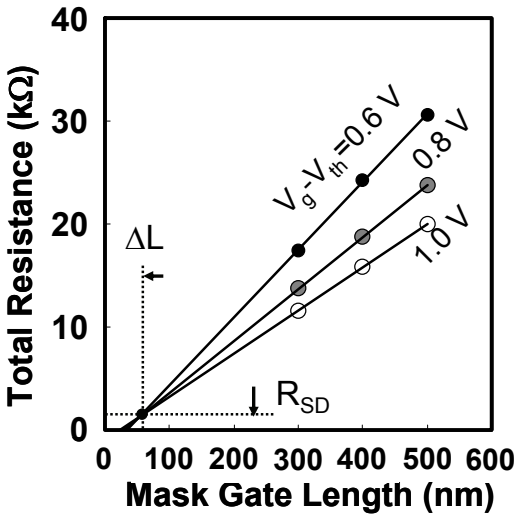


Figure 3.3 Extraction of the difference between gate mask length and electrical gate length (ΔL) and parasitic series resistance (R_{SD}) of nFETs using Chern's channel resistance method.

3.2.3. Extraction of on-current without R_{SD}

Parasitic series source/drain resistance (R_{SD}) is one of the degradation factors of drain current of MOSFET. It is expected that R_{SD} of SiNW FET depends on their cross-sectional dimensions. For evaluation of intrinsic electrical performance of SiNW FET is necessary. Therefore, I used simple calculation for evaluation of intrinsic drain current. **Fig. 3.4** shows schematic illustration of MOSFET with R_{SD}. Drain voltage applied to intrinsic transistor is degraded because of R_{SD}, and effective drain voltage is

$$V_{ds}' = V_{ds} - 2RI_{ds} \qquad (3.1)$$

Gate bias voltage is also degraded because of source resistance and effective gate voltage is

$$V_{gs}' = V_{gs} - RI_{ds} \qquad (3.2)$$

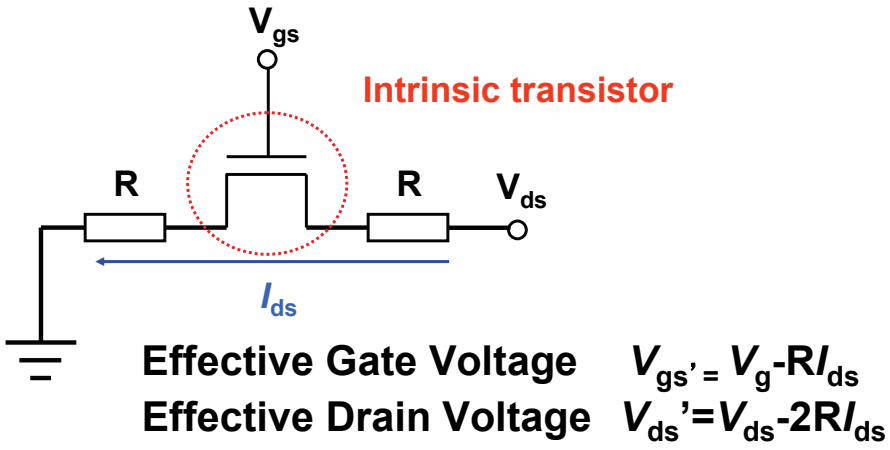


Figure 3.4 A summary of the method to extract intrinsic on-current of MOSFET. R is constant in this method.

3.3. Transfer and output characteristics

3.3.1. Typical transfer and output characteristics

Typical output and transfer characteristics of the SiNW FETs are shown in **Fig. 3.5.** The gate length is 65 nm, the channel height h_{NW} is 12 nm, and the channel width w_{NW} is 19 nm with rectangular cross-section. The SiNW FETs fabricated in this work operates as MOSFET properly.

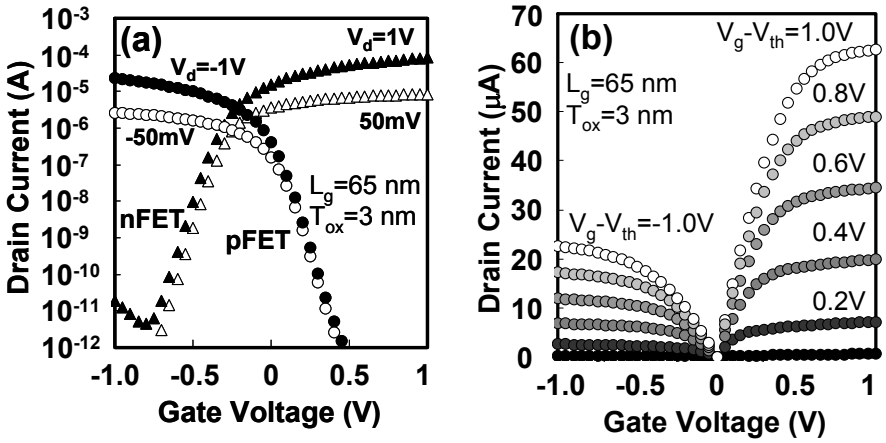


Figure 3.5 Typical (a) transfer and (b) output characteristics of the SiNW FETs with the gate length of 65 nm. Cross-sectional dimensions are channel width w_{NW} of 19 nm and channel height h_{NW} of 12 nm.

3.3.2. Subthreshold swing (*SS*)

Subthreshold swing (*SS*) as a function of the gate length (L_g) is shown in **Fig. 3.6**. The SiNW nFETs and the planar SOI nFETs were fabricated on the same wafer. One can see that *SS* of the SiNW FETs is superior to *SS* of planar SOI nFETs fabricated on the same wafer. This result suggests the superiority of the SiNW FETs to the planar FET on the point of electrostatic controllability on channel. At the gate length L_g of 65 nm, the superior *SS* was achieved with narrower w_{NW}. This result suggests that electrostatic controllability of the SiNW FET on channel with narrower w_{NW} is superior to that of wider w_{NW}.

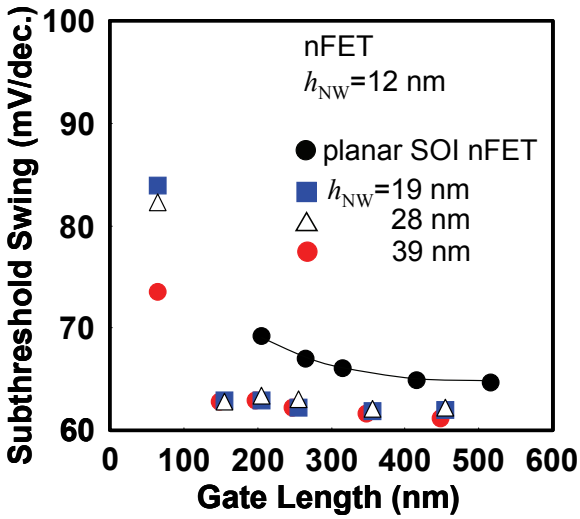


Figure 3.6 Subthreshold swings of the SiNW nFETs and planar SOI nFETs fabricated on the same wafer. I implanted phosphorus ions for extension at the dose of 10^{15} cm^{-2} and acceleration energy of 5 keV, and for source/drain at the dose of 5×10^{15} cm^{-2} and 5keV.

3.3.3. Drain induced barrier lowering (DIBL)

Drain induced barrier lowering (DIBL) of SiNW nFETs and planar SOI nFETs were characterized as shown in **Fig. 3.7**. DIBL of SiNW nFETs were smaller than that of planar SOI nFETs. This result suggests that superior electrostatic controllability on channel of SiNW FET to planar SOI FET.

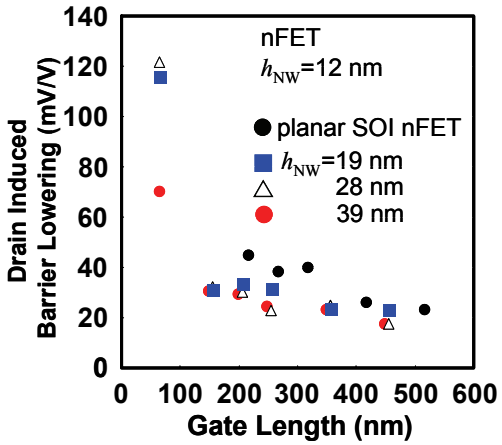


Figure 3.7 Drain-induced barrier lowering of the SiNW nFETs and planar SOI nFETs fabricated on the same wafer.

3.3.4. Effects of channel edge shapes on off-characteristics

Effects of channel cross-sectional dimensions on *SS* and DIBL have been discussed. In addition, channel edge shapes also could affect off-characteristics because uniform channel cannot be always expected because of optical proximity effects during lithography process. In this subsection, effects of channel edge shapes on off-characteristics will be discussed.

Figure 3.8 shows secondary electron microscope images with the almost same gate width and different gate edge width. The gate edge width was modulated by a distance between source and drain pads, which is called the nanowire length.

As the gate edge width increased, subthreshold swing also increased as shown in **Fig. 3.9**, and DIBL also increased as shown in **Fig. 3.10**. One reason might be the penetration of drain field. As show in the latter sections, as the channel width increased,

channel resistance also increased. Considering the result, channel resistance near widened area might be decreased and that drain field concentrated on the narrow channel at the center of SiNW FET. Therefore, off-characteristics were degraded as the channel edge width increased.

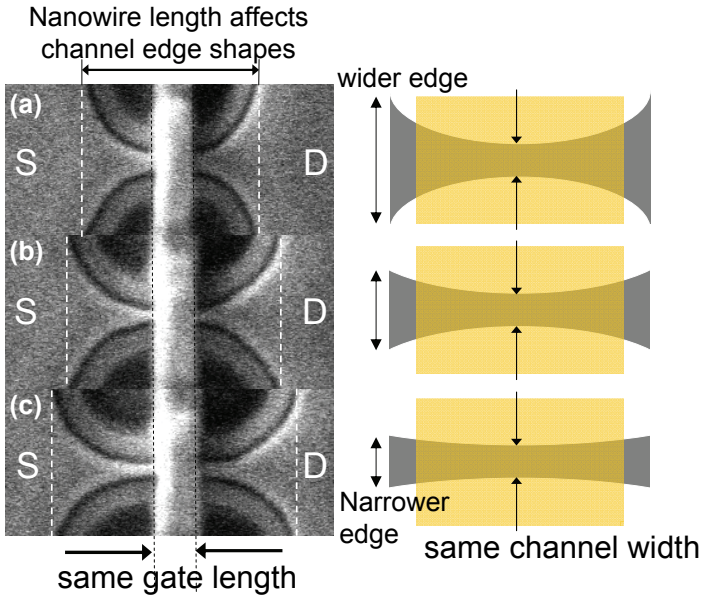


Figure 3.8 Secondary electron microscope images of SiNW nFETs with the same gate length and different channel edge width. Schematic illustrations for widening of gate edge are also shown.

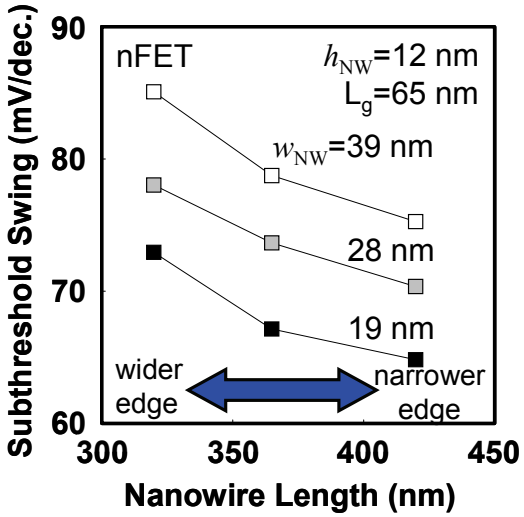


Figure 3.9 Subthreshold swing of the different channel edge width and the same gate length fabricated on the same wafer.

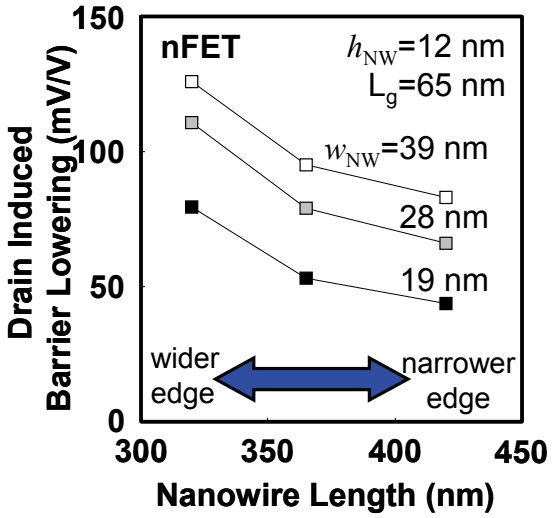


Figure 3.10 Drain induced barrier lowering of different channel edge width and the same gate length fabricated on the same wafer.

3.4 On-current

3.4.1. On-current of SiNW nFET with large rectangular cross-section

First, SiNW nFETs with relatively large cross-sectional dimensions were characterized. Cross-sectional scanning electron microscope image of SiNW channel is shown in **Fig. 3.11**. **Figure 3.12** shows the on-current of the SiNW nFET with the channel height h_{NW} of 35 nm and the channel with w_{NW} of 25, 35 and 45 nm at each gate length. As the channel width w_{NW} increase, on-current-per-wire also increased. However, the on-current normalized by peripheral length of the SiNW channel was almost same with each other. This result suggests that there is no structural effect induced by the reduction of the channel width w_{NW}.

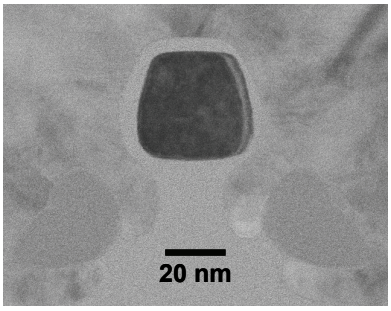


Figure 3.11 Cross-sectional scanning secondary electron microscope images of SiNW nFET with channel width of 35 nm and channel height of 35 nm.

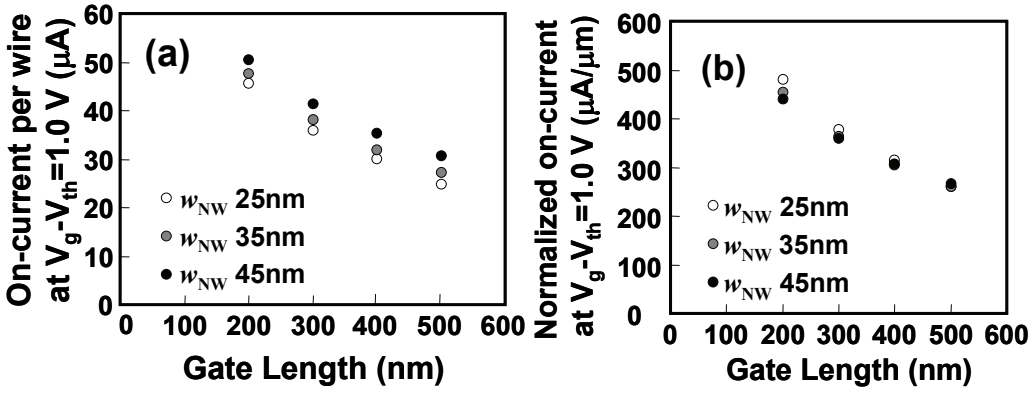


Figure 3.12 On-current-per-wire and normalized on-current of the SiNW nFETs with large cross-sectional dimensions (h_{NW}=35 nm, w_{NW}=25, 35, and 45 nm).

3.4.2. Rectangular cross-sections

SiNW FETs with smaller channel cross-sectional dimensions are characterized in this section. Secondary electron microscope images and transmission electron microscope images of SiNW FETs are shown in **Fig. 3.13**. **Figure 3.14** shows on-current per wire and the on-current normalized by the peripheral length. The SiNW FETs and the planar SOI FETs were fabricated on the same wafer. The channel height h_{NW} is 12 nm for all the SiNW FETs. As the channel width w_{NW} increased, the on-current per wire also increased. On the other hand, normalized on-current of SiNW nFET with smaller w_{NW} was the largest. This is due to structural advantages of rectangular cross-section. Similar trend can be observed for SiNW pFETs with rectangular cross-sections.

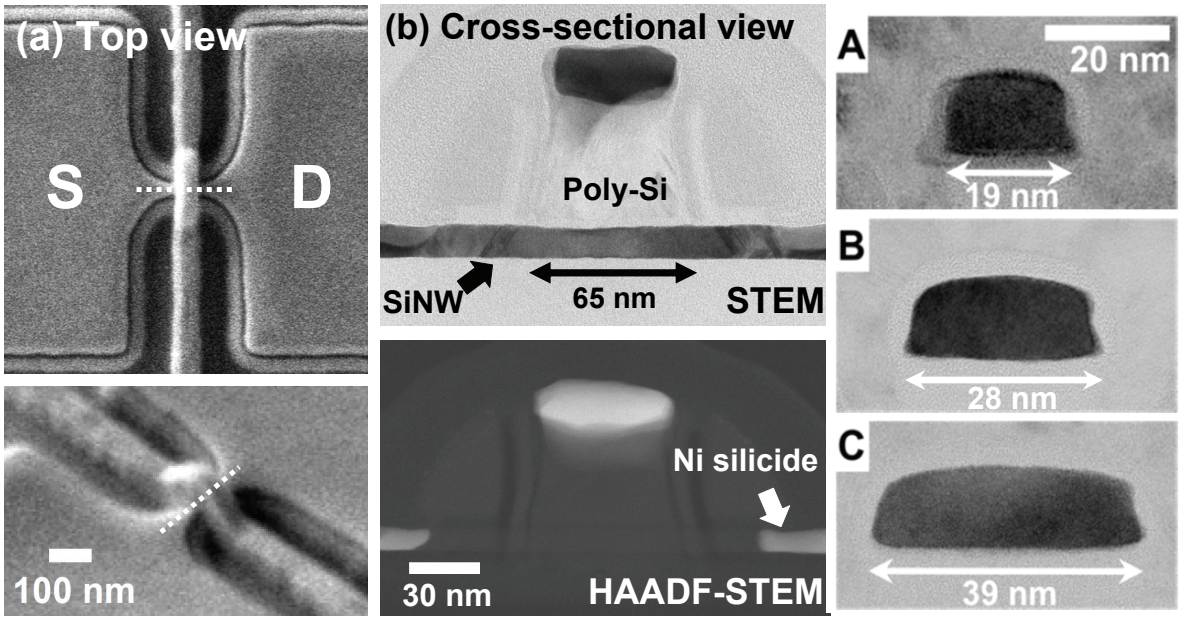


Figure 3.13 (a) Plan-view secondary electron microscope image of SiNW FET. (b) Cross-sectional scanning transmission electron microscope image and high angular annular dark field STEM image of SiNW FET. Cross-sectional SEM image of SiNW channel with rectangular cross-sections are also shown.

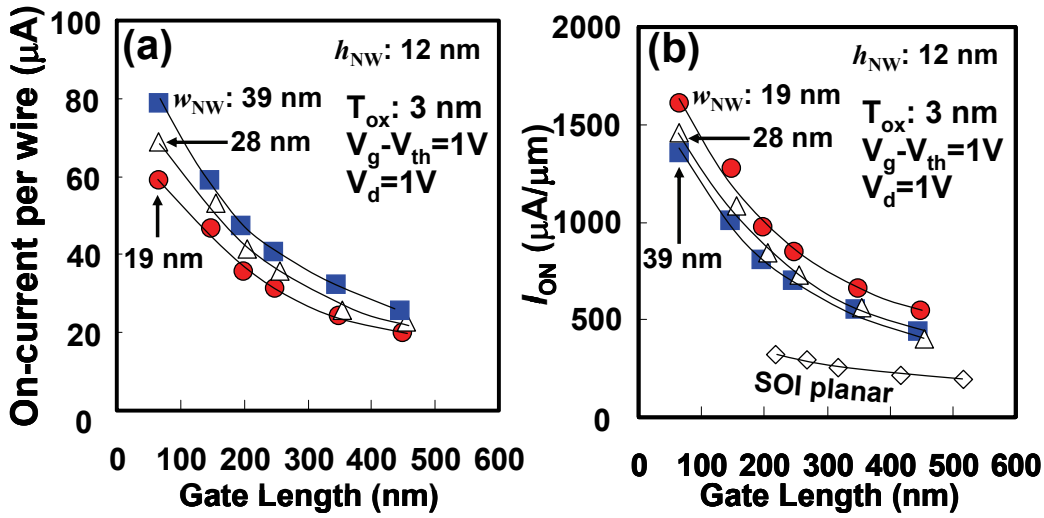


Figure 3.14 (a) On-current-per-wire and (b) the normalized on-current of the SiNW nFETs on the same wafer as a function of the gate length.

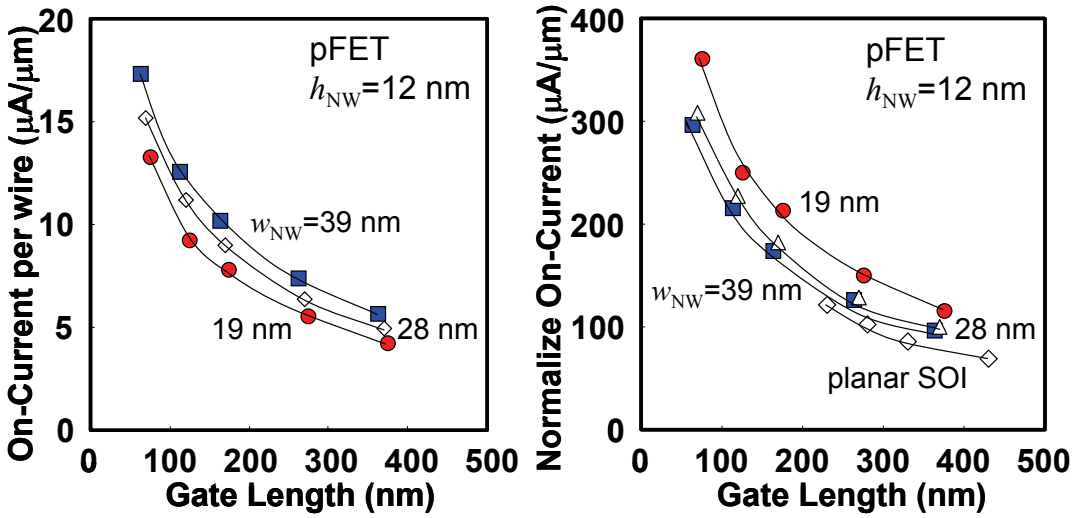


Figure 3.15 (a) On-current-per-wire and the normalized on-current of the SiNW pFETs on the same wafer as a function of the gate length.

3.4.3 Tall-rectangular cross-section

On-current per wire and normalized on-current of SiNW FETs with tall rectangular channel cross-sections with channel height h_{NW} of 20 nm and channel width w_{NW} of 12 and 22 nm were evaluated as shown in **Fig. 3.17**. Channel widths are also shown the figure. As the channel height decrease, normalized on-current increased for SiNW nFETs.

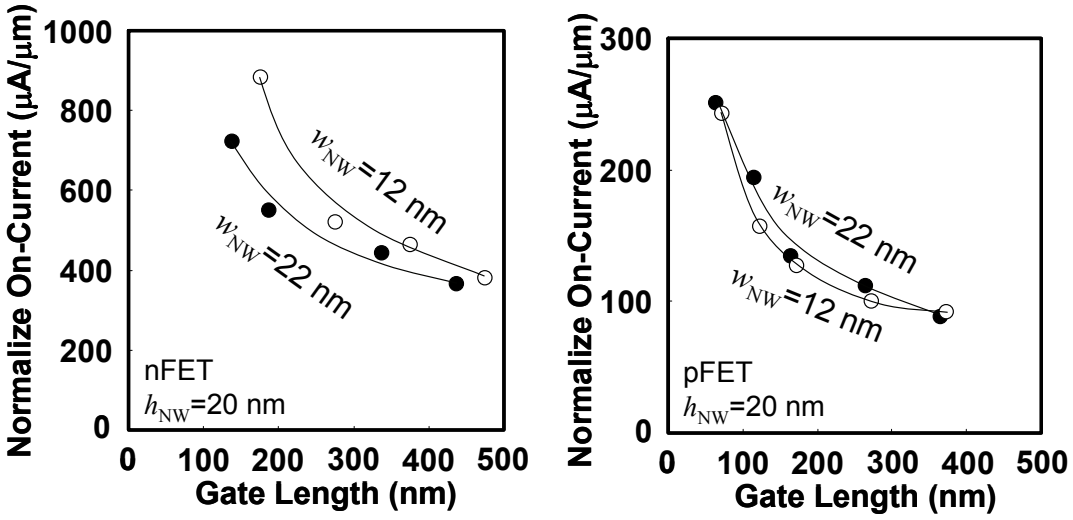


Figure 3.16 Normalized on-current of SiNW (a) nFETs and (b) pFETs fabricated on the same wafer.

3.4.3. Tear-like and half circular cross-section

In this subsection, I characterized on-current of half-circular and tear-like cross-section. Cross-sectional scanning transmission electron microscope images of channel cross-sections are shown in **Fig. 3.17**. Normalized on-current are shown in **Fig. 3.18**.

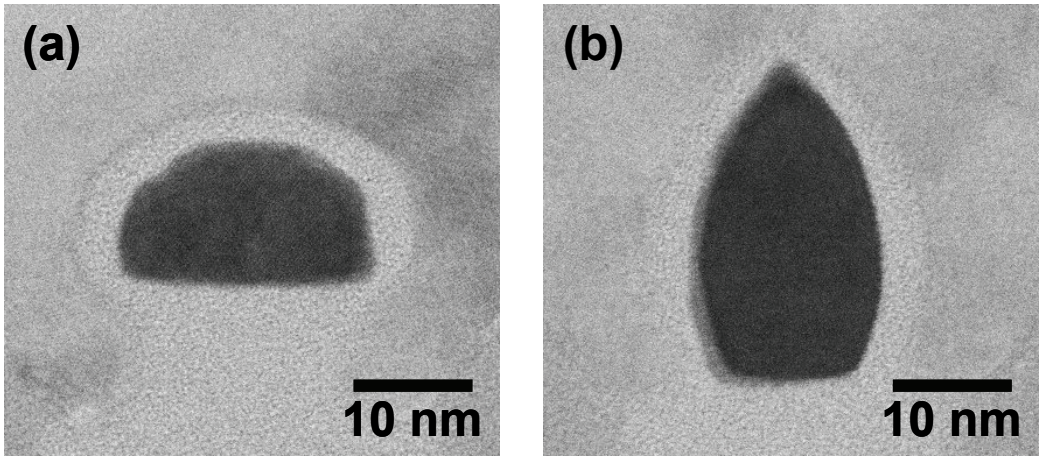


Figure 3.17 Cross-sectional transmission microscope images of the SiNW nFETs with (a) half-circular cross-section and (b) tear-like cross-section.

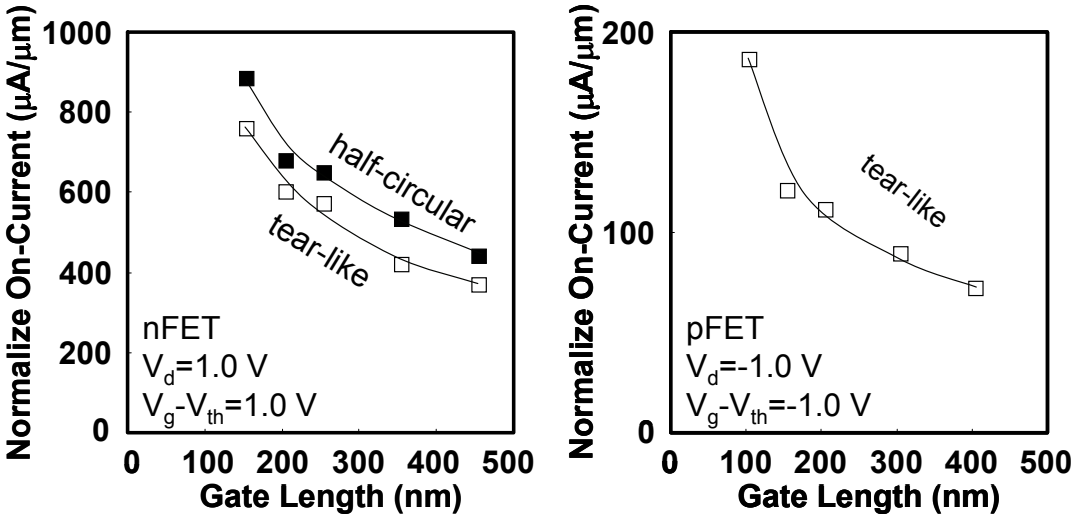
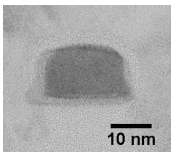
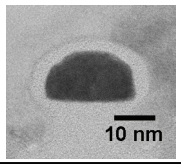
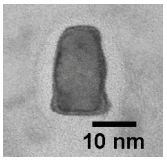
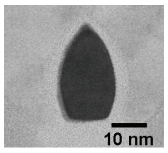


Figure 3.18 Normalized on-current of SiNW FETs with half-circular and tear-like cross-sectional shapes.

3.4.5. Comparison of various cross-sectional shape

On-current of SiNW FETs with various cross-sectional shapes has been investigated. In this section, I compare normalized on-current of different cross-sectional shapes. The parasitic source/drain resistance R_{SD} of SiNW nFET strongly depended on the species of ions implanted into source/drain regions as shown in the previous subsection. Therefore, in this subsection, on-current was extracted with elimination of the degradation of on-current because of R_{SD}.

Table 3.1 Comparison of normalized on-current of SiNW nFETs with rectangular, half-circular, and tear-like cross-sectional shapes.

Cross-sectional shape				
Size (h_{NW} x w_{NW}) (nm)	12 x 19	12 x 21	20 x 12	27 x 16
On-Current (μA/μm)	1277	893	861	780
On-Current w/o R_{SD} (μA/μm)	1361	1073	1051	834
R_{SD} (kΩ)	~1.3	~8.2	~7.4	~2.2

3.5 Parasitic source/drain series resistance

3.5.1 Parasitic source/drain resistance of planar SOI FETs

Planar-type SOI FETs were fabricated simultaneously on the same wafer with SiNW FETs. In this subsection, R_{SD} of planar-type SOI FETs were characterized.

Parasitic series resistance (R_{SD}) of SiNW FETs was calculated using Chern's channel resistance method [3.1] in this work. **Figure 3.19** shows extracted R_{SD} of planar-type SOI FETs in which boron ions were implanted and phosphorous ions were implantations. R_{SD} of <110>- and <100>-directed phosphorus-implanted planar SOI nFET were 284 and 275 Ω μm, respectively. R_{SD} of boron-implanted <110>- and <100>-directed planar SOI pFET were 414 and 357 Ω μm, respectively. Required R_{SD} in ITRS 2009 roadmap [3.2] for high-performance use in 2010 is 200 Ω μm. Compared with the value in ITRS 2009 roadmap, the extracted R_{SD} of planar-type SOI FETs were appropriate values because process conditions for formation of source/drain junction were not fully optimized for planar SOI FETs.

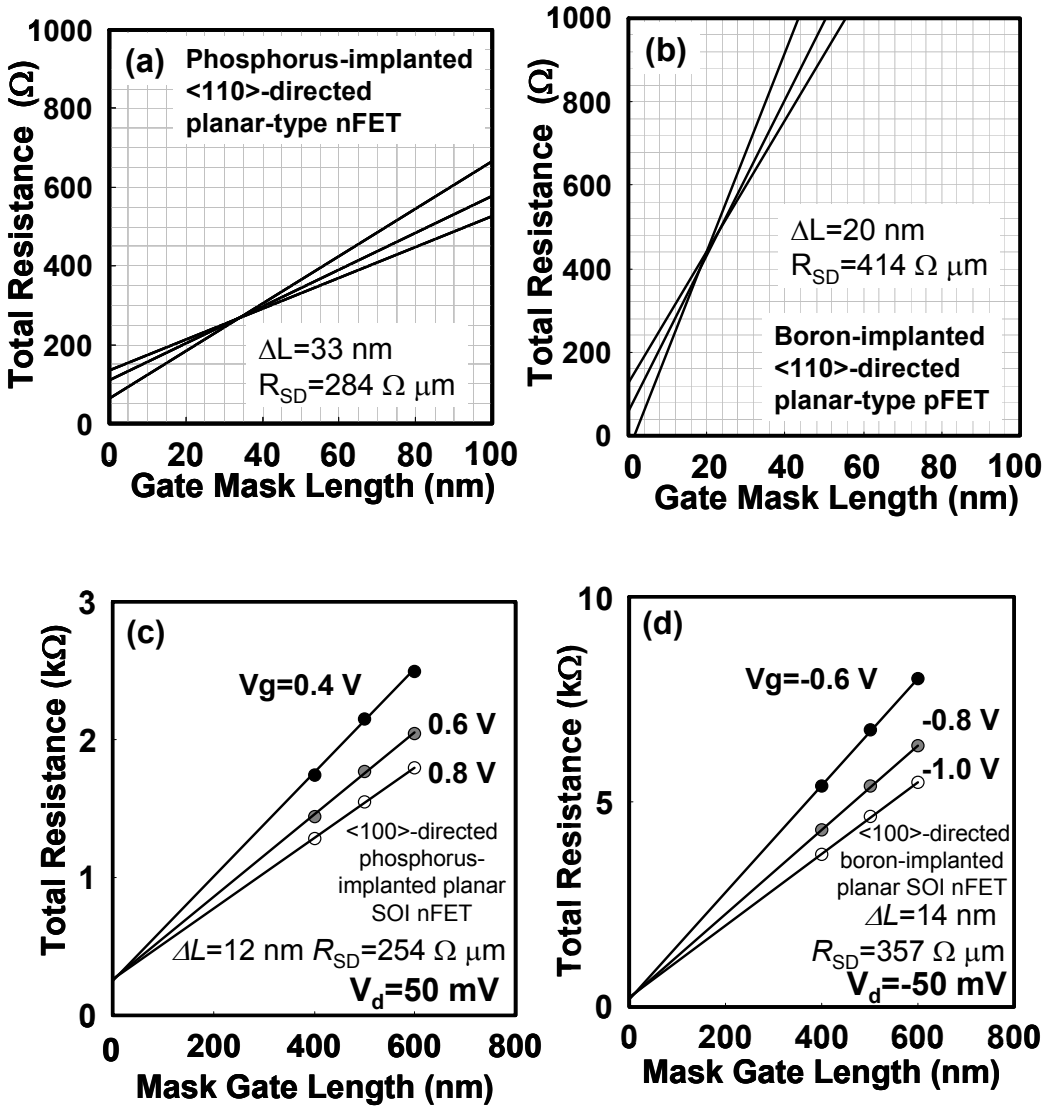


Figure 3.19 Extracted source/drain parasitic resistance of planar-type SOI FETs. Thickness of SOI layer was 28 nm using Chern's channel resistance method. (a) Phosphorus-implanted and (b) boron-implanted <110>-directed SOI FETs. (c) Phosphorus-implanted and (d) boron-implanted <100>-directed SOI FETs.

On the other hand, R_{SD} of arsenic-implanted planar SOI nFETs is much larger than R_{SD} of boron-implanted and phosphorus-implanted planar SOI FETs, and depended on the thickness of SOI layer. R_{SD} of 2.1 kΩ of planar nFET with SOI layer thickness of 28 nm, and 739 Ω μm for 45 nm were obtained. **Fig. 3.20** shows cross-sectional scanning electron microscope (STEM) images and high angular annular dark field (HAADF) STEM images of source/drain regions of arsenic-implanted FETs. White regions in HAADF-STEM images corresponded with nickel, which indicate that nickel diffused into the whole regions of embedded source/drain regions. One possible cause is that amorphous SOI layer was formed after arsenic ion-implantation process because arsenic ion is heavier than phosphorus and boron ions. As a result, the amorphous SOI layer did not recovered to the single crystal phase during dopant activation annealing processes.

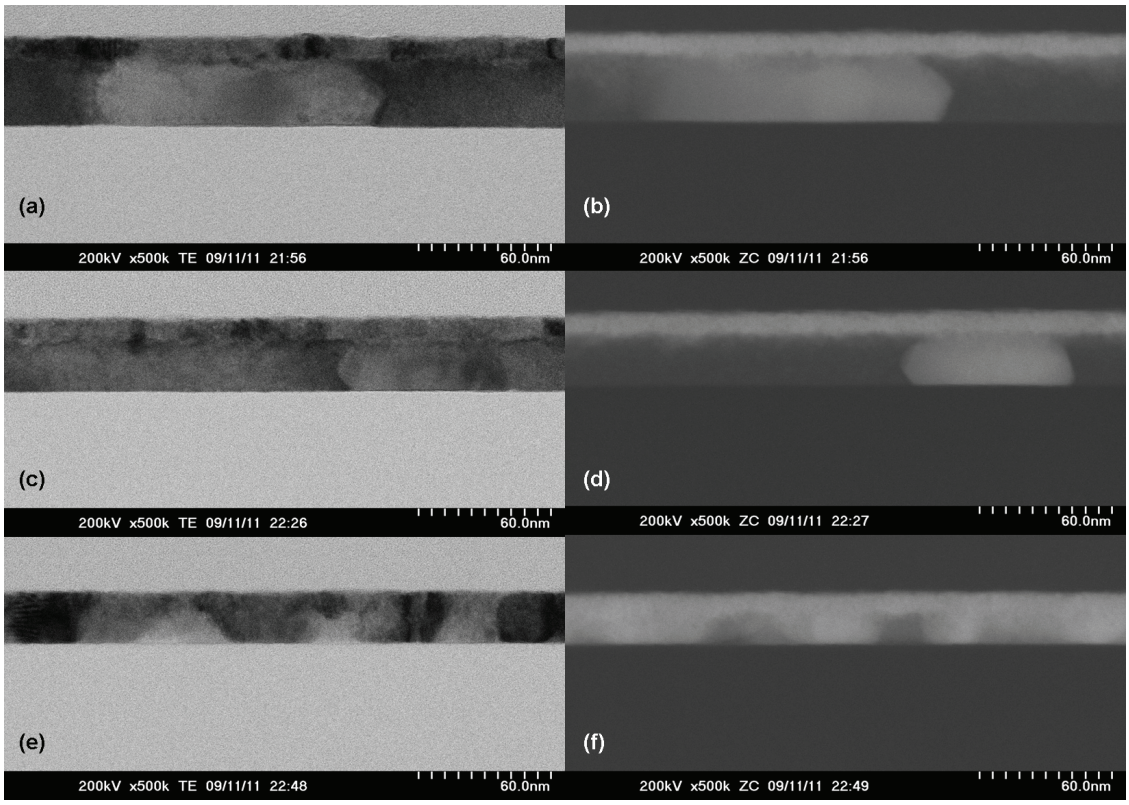


Figure 3.20 (a)(c)(e) Cross-sectional scanning transmission electron microscope (STEM) images and (b)(d)(f) high angular annular dark field STEM images of source and drain regions of SiNW nFETs with different SOI layer thicknesses.

3.5.2. Parasitic source/drain resistance of SiNW FETs

R_{SD} of SiNW nFETs strongly depended on the species of ions implanted into source and drain regions. R_{SD} of SiNW nFETs using phosphorus ions for implantation into source/drain regions was smaller than R_{SD} of SiNW nFETs using arsenic ions. R_{SD} of SiNW nFETs using arsenic ions also strongly depended on the channel cross-sectional dimensions.

Fig. 3.21 shows cross-sectional high angular annular dark field scanning transmission electron microscope (HAADF-STEM) image of source/drain regions near gate electrode along the channel directions of SiNW nFET with arsenic ions. One can see that nickel diffused in the whole source and drain regions. Near the junction of source/drain and channel under gate electrode, nickel diffused into the whole region. I speculate that this is one of the reasons of high parasitic source and drain resistance. It has been reported that full silicidation of SOI layer leads to high series resistance [3.3], which is schematically illustrated in **Fig. 3.22**. R_{SD} of SiNW nFETs with arsenic implanted source drain regions are show in **Fig 3.23**.

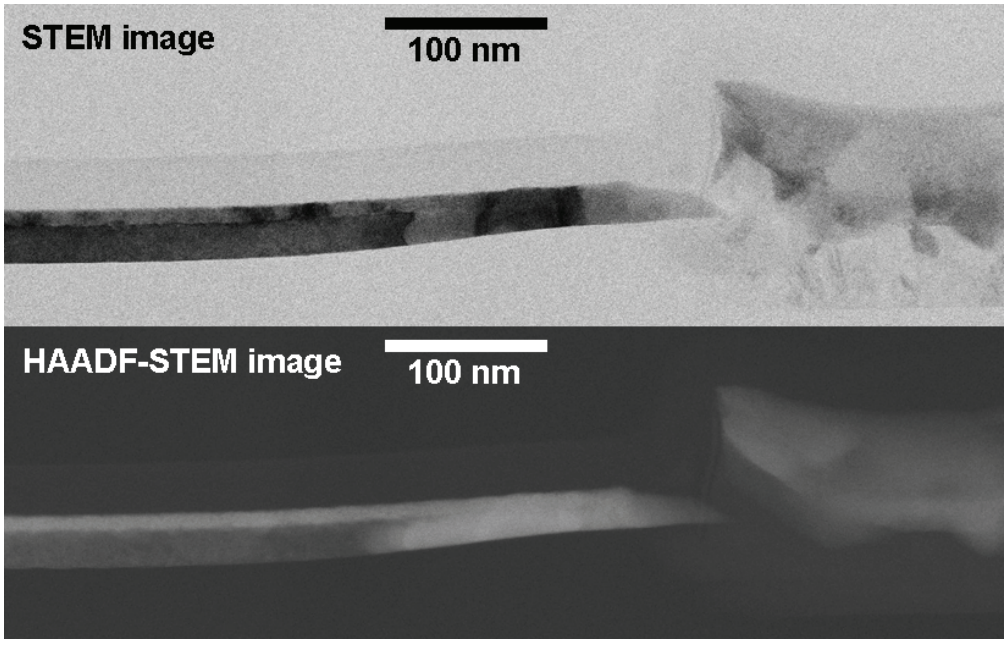


Figure 3.21 Scanning transmission electron microscope (STEM) image and high angular annular dark field STEM image of SiNW nFET using arsenic ions for ion-implantation process into source and drain regions.

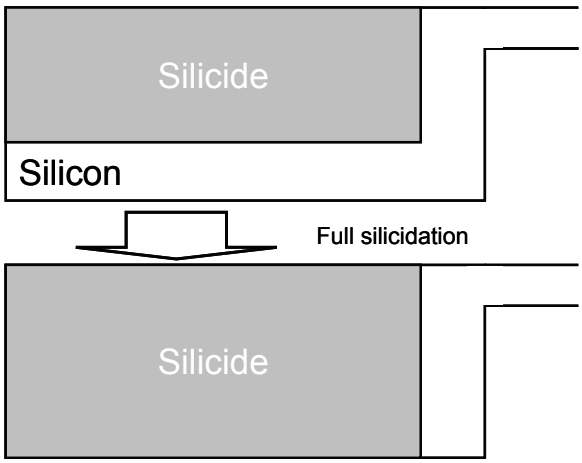


Figure 3.22 A schematic illustration of increase of parasitic source/drain resistance because of full-silicidation of source/drain SOI layer. [3.3]

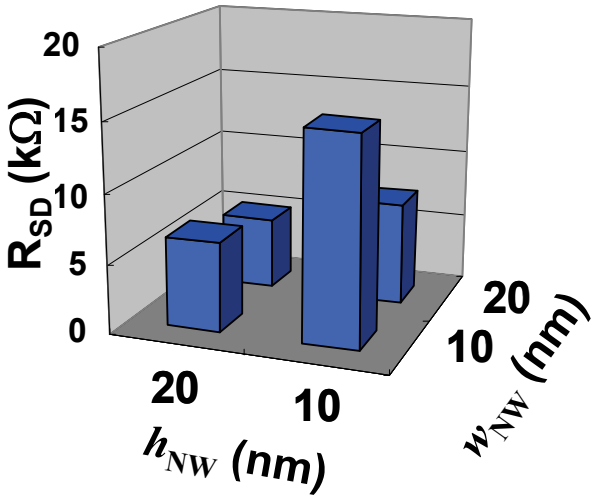


Figure 3.23 R_{SD} of SiNW nFETs with arsenic ion implantation processes.

R_{SD} of SiNW nFETs with phosphorus ion implantations into source/drain regions were lower than R_{SD} of SiNW nFETs with arsenic ion implantation as shown in **Fig. 3.24**. It can be speculated that full-silicidation of source/drain regions did not occur. Parasitic resistance normalized by the peripheral length of <110>-directed SiNW channel was lower than the normalized parasitic resistance of planar-type SOI nFET fabricated on the same wafer. The low R_{SD} of SiNW nFETs with phosphorous implanted source drain regions contribute to high on-current of SiNW nFET.

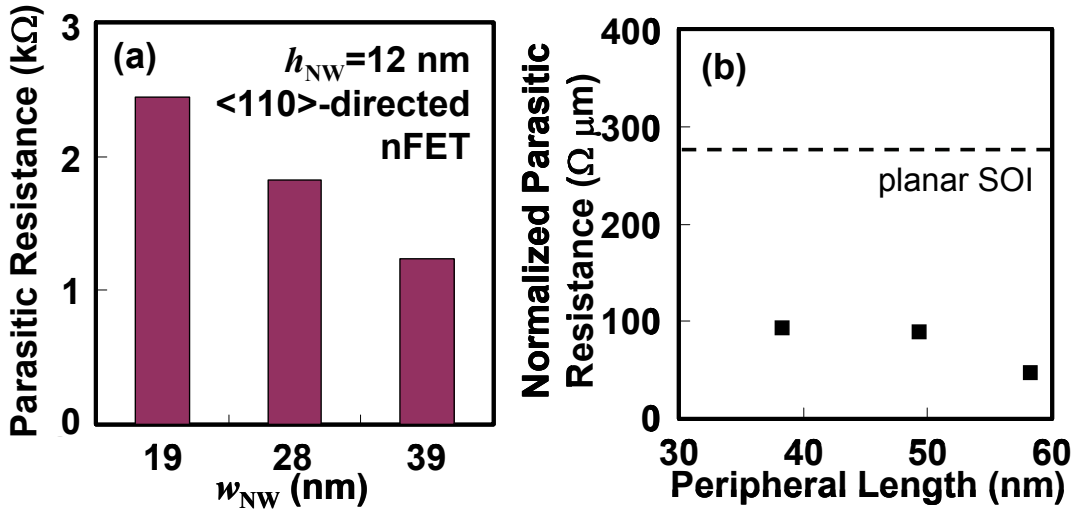


Figure 3.24 Parasitic series resistance of SiNW nFETs with phosphorous ion implantation processes.

R_{SD} of <110>-directed SiNW pFETs were relatively high compared with R_{SD} of nFETs as shown in **Fig. 3.25**. R_{SD} of pFETs exhibited less dependence on cross-sectional dimensions of SiNW channel. One possible reason is that full silicidation of source drain regions did not occur. R_{SD} of <110>-directed pFETs was much larger than R_{SD} of <100>-directed pFETs as shown in **Fig. 3.26**. This is because the ΔL of <110>-directed SiNW pFET is larger than that of <100>-directed SiNW pFETs.

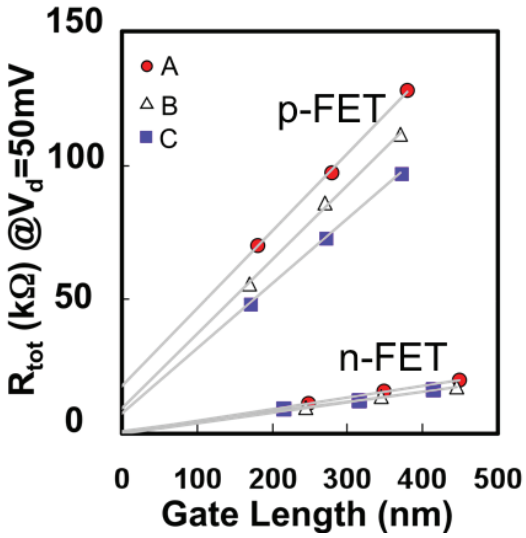


Figure 3.25 Parasitic resistance of <110>-directed SiNW FET extracted using Chern's channel resistance method.

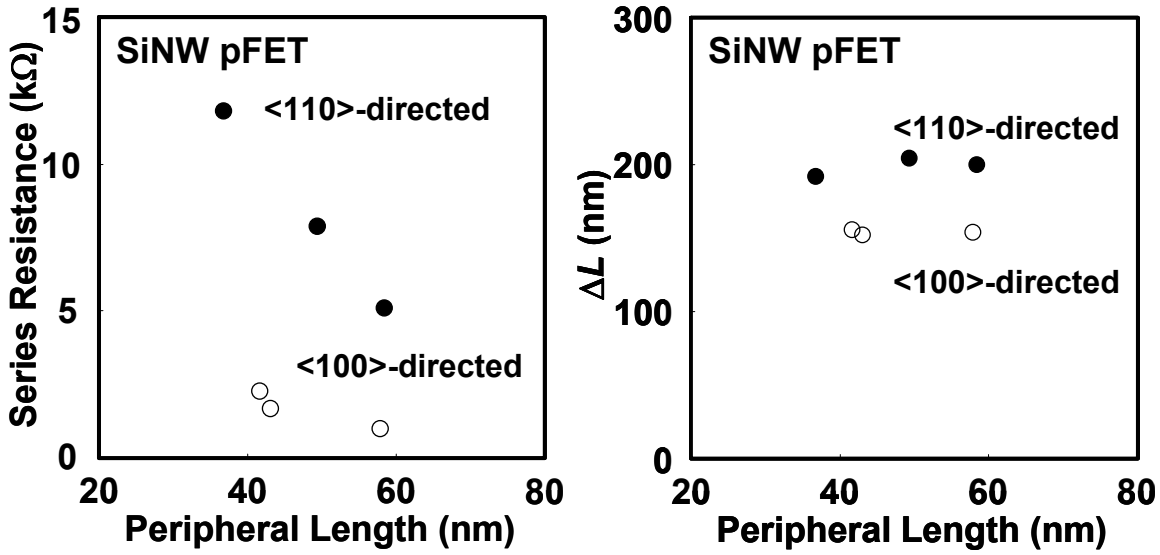


Figure 3.26 R_{SD} of <110>- and <100>-directed SiNW pFETs and DL obtained by Chern's channel resistance method.

3.6 I_{ON}/I_{OFF} characteristics

I_{ON}/I_{OFF} characteristics of the SiNW nFETs with rectangular cross-sections (w_{NW} of (a) 19, (b) 28 and (c) 39 nm) are shown in **Fig. 3.27.** I_{ON}/I_{OFF} characteristics without normalization were similar to each other. As the w_{NW} decreased, I_{ON}/I_{OFF} characteristics of SiNW nFETs improved because of superior electrostatic channel controllability. ION/IOFF characteristics of SiNW nFETs with w_{NW} of 19 nm and h_{NW} of 12 nm were compared with those of planar bulk FETs, SiNW FETs and FinFETs as shown in **Fig. 3.28**. Comparable characteristics were achieved with SiNW nFETs fabricated in this work none the less of relatively thick gate oxide with thickness of 3 nm.

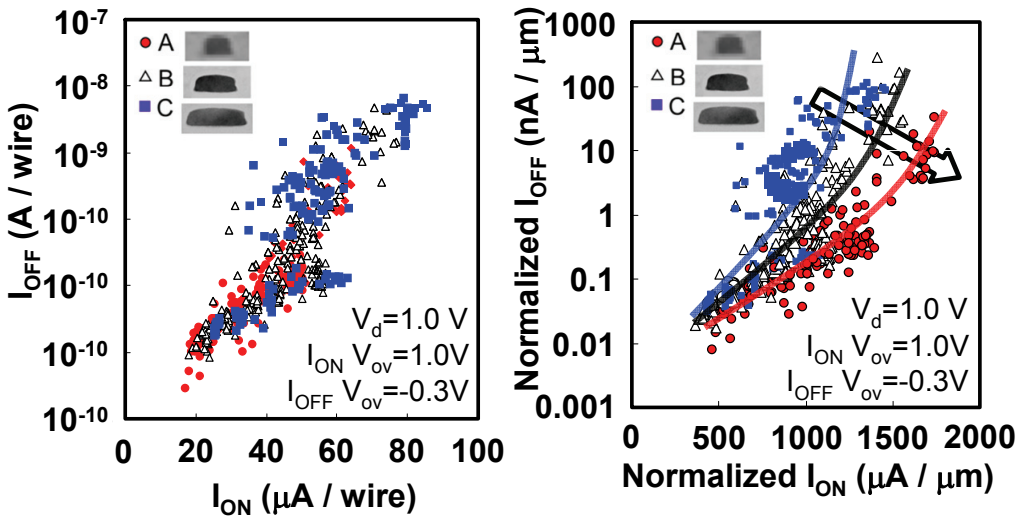


Figure 3.27 I_{ON}/I_{OFF} characteristics of the SiNW nFETs. On-current and off-current were normalized by the peripheral length.

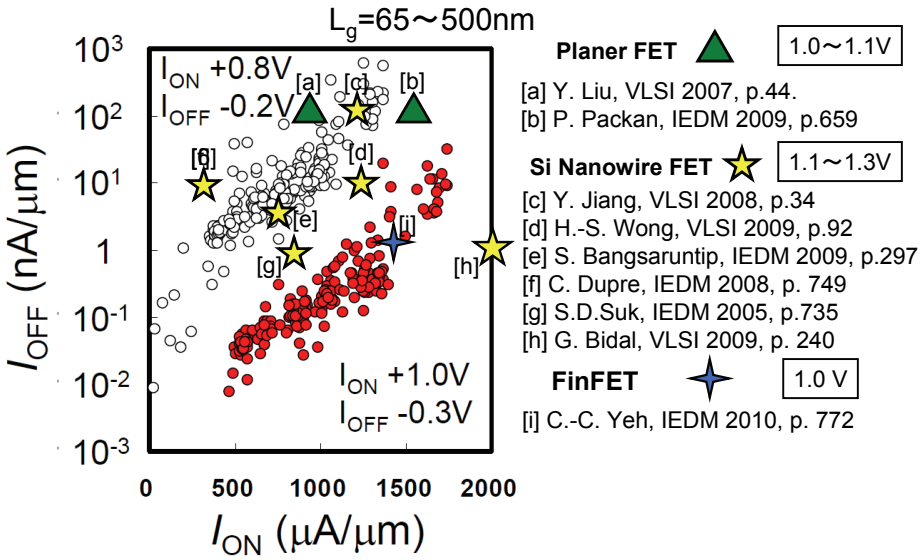


Figure 3.28 I_{ON}/I_{OFF} characteristics of the SiNW nFET with w_{NW} of 19 nm and h_{NW} of 12 nm and planar bulk FETs SiNW FETs and FinFETs reported.

I_{ON}/I_{OFF} characteristics can be discussed from another view point; normalization by foot print of SiNW FET. Compared with the normalization by the peripheral length of SiNW channel, the normalization by the foot print is practical-oriented, that is, on-current normalized by the foot print (I_{ON}*) indicates actual current density in integrated circuits. I_{ON}* of SiNW *n*FETs with h_{NW} of 12 nm and w_{NW} of 19, 28 and 39 nm were 3.12, 2.46, and 2.03 mA/μm, respectively, at the gate overdrive voltage of 1.0 V. These values are much larger than required I_{ON} for planar FET, which suggests superiority of SiNW structure.

It should be noted that SiNW structure requires gap distance between parallel SiNW channels as shown in **Fig. 3.29**. The gap distance is restricted by the lithography process technology and related to the minimum pitch of M1. The number of SiNWs within a unit width (1 mm) is equal to the number of the M1 metal interconnect with width of half-pitch. **Figure 3.30** shows the number of SiNWs within a unit width based on international roadmap for semiconductor (*ITRS*) 2010 update. It is expected that 13 wires/μm can be achieved in 2011, which results in I_{ON}* of 780 μA/μm of SiNW *n*FET with w_{NW} of 19 nm. In 2019, 37 wires/μm is expected, which results in I_{ON}* of

2220 μA/μm with w_{NW} of 19 nm as shown in **Fig. 3.31**. These expectations suggests increase of I_{ON}* of SiNW FETs also strongly depends on the improvement of lithography technology.

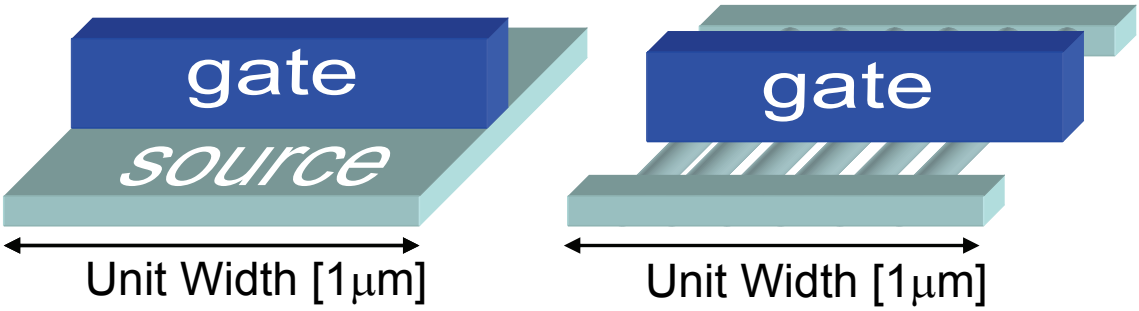


Figure 3.29 Schematic illustrations of planar-type FET and multi-channel SiNW FET.

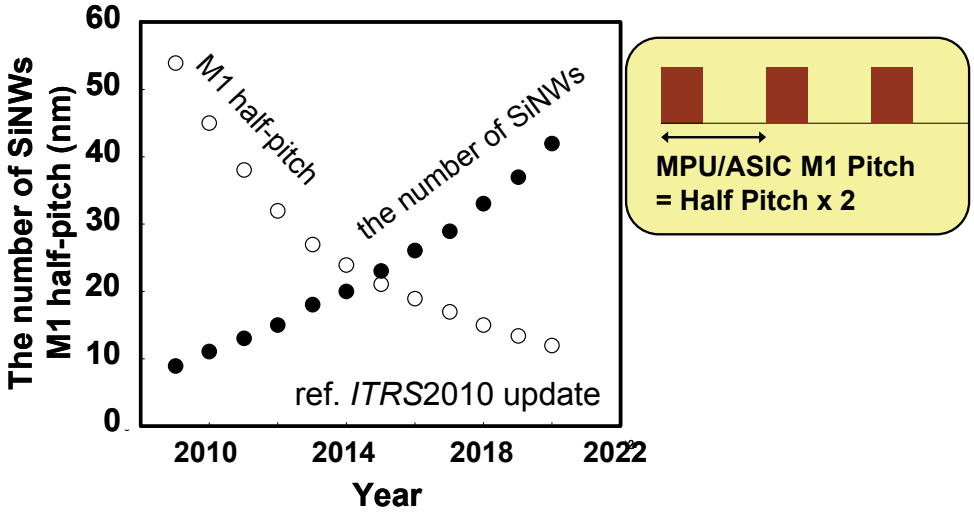


Figure 3.30 The number of SiNWs that can be integrated within a unit width (1 μm) with illustrations based on ITRS 2010 for high-performance.

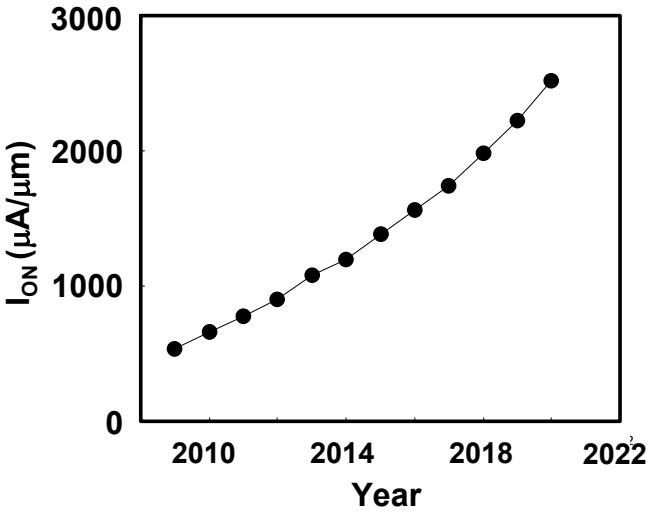


Figure 3.31 Increase of I_{ON} due to the improvement of lithography technology. On-current-per-wire of 60 μA is estimated for the prediction.

3.7 Structural advantage of the SiNW FET

In this chapter, the normalized on-current as a function of the channel width w_{NW} was evaluated. As w_{NW} decreased, I_{ON} increased as shown in **Fig. 3 29**. Compared with the planar SOI nFETs fabricated on the same wafer, the gain also increased. This is due to the structural advantage of the rectangular cross-sectional dimensions of the SiNW FETs.

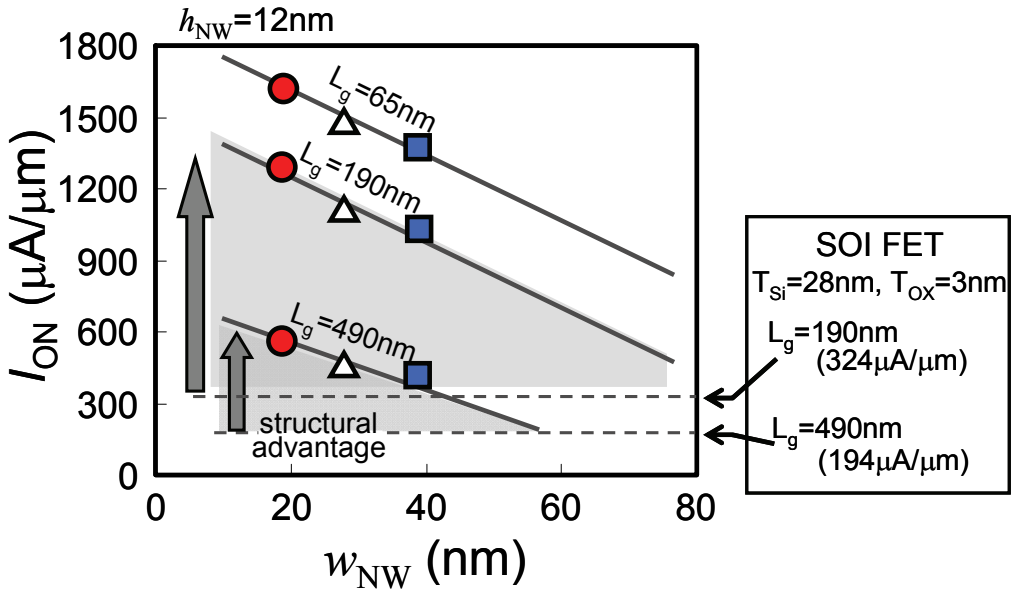


Figure 3.32 Structural advantages of the SiNW nFETs with rectangular-like cross-section over planar SOI nFETs, which increase as the w_{NW} decrease.

3.8 Separation of the on-current of the silicon nanowire field-effect transistors

In the previous section, the structural advantages of w_{NW} on the I_{ON} of the SiNW FET were investigated. The advantages could be explained by the effects of corners in the rectangular-like cross-section. In this section, we attempt to separate on-current of corner component (I_{corner}) and on-current along flat surface (I_{flat}) of the SiNW nFETs for the determination of contributions of the corners in **Fig. 3.30**. The on-current along flat surface I_{flat} and the on-current of the corner component I_{corner} were calculated as follows. First we subtracted the on-current per wire of the SiNW FET with smaller w_{NW} from an on-current per wire of the SiNW FET with larger w_{NW}. Then we normalized the difference of the on-current per wire with the difference of w_{NW} between each SiNW FET. We obtained the normalized on-current along flat surface of (*i*) 1069, (*ii*) 932, and (*iii*) 994 μA/μm using the SiNW nFET with w_{NW} of (*i*) 19 and 28 nm, (*ii*) 28 and 39 nm, and (*iii*) 19 and 39 nm. The averaged normalized on-current along flat surface was 998 μA/μm. Next, we calculated the on-current along flat surface I_{flat}. We assumed that the normalized on-current of side-surface is the same as that of the top-surface. The peripheral length of upper corners were measured based on cross-sectional TEM images and the rest of the peripheral length was that of the flat surface as mentioned in section 2. We multiplied the normalized on-current of the flat surface by the peripheral length of the flat surface and obtained the on-current along flat surface I_{flat}. The rest is the on current of corner component I_{corner}. Separated I_{corner} and I_{flat} is summarized in **Fig. 3.31** and about 60 % of the I_{ON} of the SiNW FET (w_{NW}=19 nm and h_{NW}=12 nm) was attributed to the corners.

On-current was also separated with the devices with different gate length. The result was shown in **Fig. 3.32**. As the gate length decreased, the component of the corner also decreased. This result suggests that the carrier transport of corner and the flat surface is different.

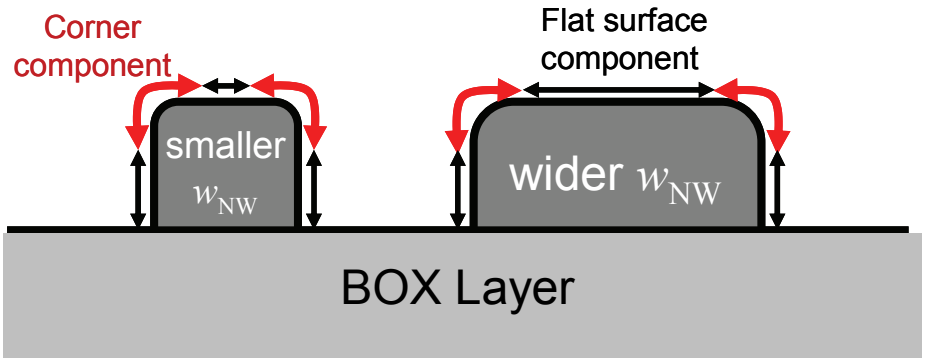


Figure 3.33 Assumptions for calculation and extraction of I_{ON} of the fraction of corners and those of flat surface. W_c is assumed to be 4 nm considering cross-sectional transmission electron microscope images.

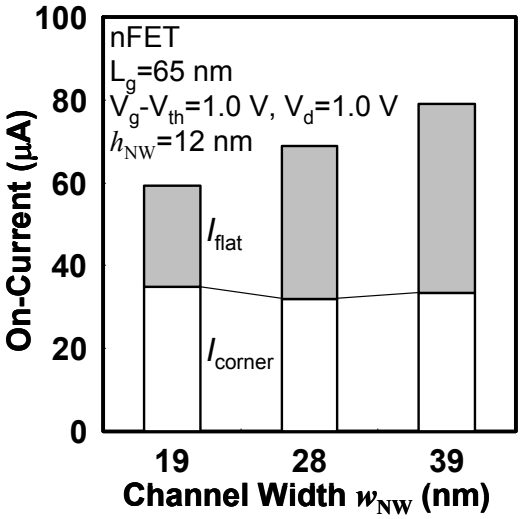


Figure 3.34 Extracted on-current of the corner component and the flat surface component of the SiNW nFETs with the L_g of 65 nm.

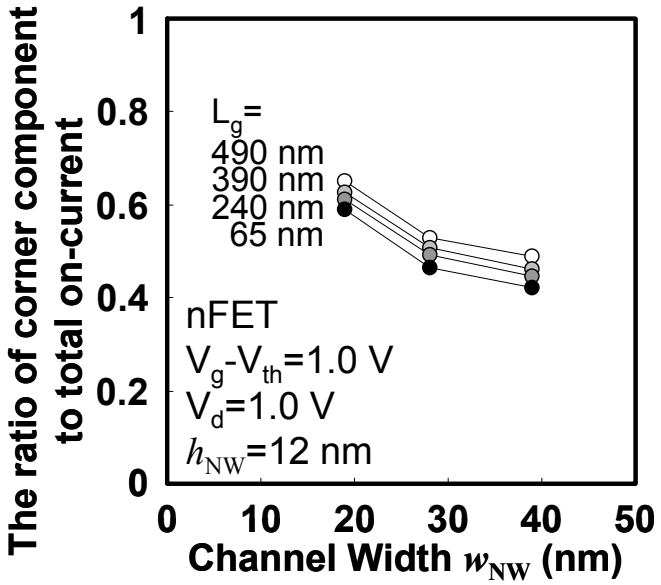


Figure 3.35 The ratio of corner component to the total on-current of the SiNW nFET with each gate length.

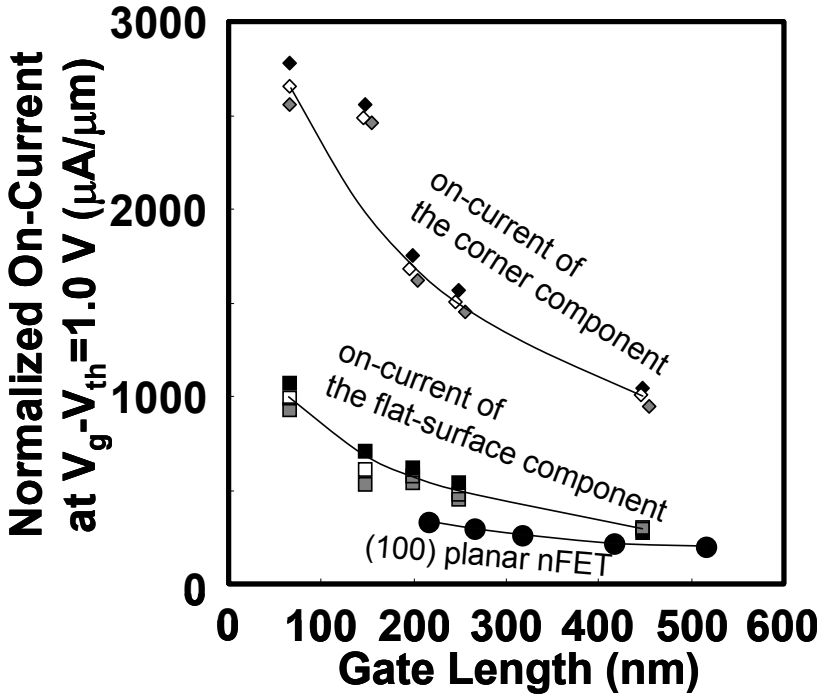


Figure 3.36 Normalized on-current of corner component and flat-surface component calculated in the previous section. Black square, gray square, and white square are the normalized on-current of flat-surface components calculated using SiNW FETs with the channel width w_{NW} of (i) 19 and 28

nm, (ii) 28 and 39 nm, and (iii) 19 and 39 nm. Black diamond, gray diamond, and white diamond are normalized on-current of corner component of SiNW nFETs with w_{NW} of 19, 28 and 39 nm.

3.9 Conclusions

In this chapter, dc characteristics, especially on-current and off-current of the SiNW FETs were investigated. Electrical characteristics of the SiNW FET with larger cross-sectional dimensions of 30 nm have little structural effects. As the cross-sectional dimensions decreased down to 10 nm, structural effects appeared as the increase of the normalized on-current.

As the channel width w_{NW} decreased, the difference of the normalized on-current between the SiNW FET increased. I speculate that the increase of the normalized on-current as the w_{NW} decrease is due to the structural advantage of the SiNW FET.

I speculated that the structural effect is due to the increased inversion charge density near the corners of the SiNW FET as shown in the chapter 2. Therefore, I separated the on-current to the corner component and the flat surface component. These results showed that the corner component of the on-current is about 60 % with w_{NW} of 19 nm, and the corner component was dominant.

These experimental results suggest that the corner play an important role for enhancement of the SiNW FET with rectangular cross-section.

References

[3.1] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho. A new method to determine MOSFET channel length. *IEEE Electron Device Lett.* **1** (1980) 170-173.

[3.2] International Technology Roadmap for Semiconductors 2009 edition. http://www.itrs.net/reports.html

[3.3] L. T. Su, M. J. Sherony, H. Hu, J. E. Chung, and D. A. Antoniadis. Optimization of series resistance in sub-0.2 μm SOI MOSFETs. *Int'l Electron Device Meet.* 1993. 723-726.

[3.2] Y. Liu, O. Gluschenkov, J. Li, A. Madan, A. Ozcan, B. Kim, T. Dyer, A. Chakravarti, K. Chan, C. Lavoie, I. Popova, T. Pinto, N. Rovedo, L. Zhijiong, R. Loesing, W. Henson, K. Rim. Strained Si Channel MOSFETs with Embedded Silicon Carbon Formed by Solid Phase Epitaxy. *Proc. Symp. VLSI Technology.* 2007. 44-45.

[3.3] S. Kamiyama, E. Kurosawa, S. Abe, M. Kitajima, T. Aminaka, T. Aoyama, K. Ikeda, and Y. Ohji. V_{th} fluctuation suppression and high performance of HfSiON/metal gate stacks by controlling capping-Y_2O_3 layers for 22nm bulk devices. *Int'l Electron Device Meet.* 2009. 431.

[3.4] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S.-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, and S. Natarajan. High performance 32nm logic technology featuring 2nd generation high-k + metal gate transistors. *Int'l Electron Device Meet.* 2009. 659.

[3.5] Y. Jiang, T. Y. Liow, N. Singh, L. H. Tan, G. Q. Lo, D. S. H. Chan, and D. L. Kwong. Performance breakthrough in 8 nm gate length Gate-All-Around nanowire transistors using metallic nanowire contacts. *Proc. Symp. VLSI Technology.* 2008. 34.

[3.6] H.-S. Wong, L.-H. Tan, L. Chan, G.-Q. Lo, G. Samudra,Y.-C. Yeo. Gate-all-around quantum-wire field-effect transistor with Dopant Segregation at Metal-Semiconductor-Metal heterostucture. *Proc. Symp. VLSI Technology.* 2009. 92.

[3.7] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank, J. W. Sleight. High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling. *Int'l Electron Device Meet.* 2009. 297.

[3.8] C. Dupre, A. Hubert, S. Becu, M. Jublot, V. Maffini-Alvaro, C. Vizioz, F. Aussenac, C. Arvet, S. Barnola, J. M. Hartmann, G. Garnier, F. Allain, J. P. Colonna, M. Rivoire, L. Baud, S. Pauliac, V. Loup, T. Chevolleau, P. Rivallin, B. Guillaumot, G. Ghibaudo, O. Faynot, T. Ernst, S. Deleonibus. Performance breakthrough in 8 nm gate length Gate-All-Around nanowire transistors using metallic nanowire contacts. *Int'l Electron Device Meet.* 2009.

[3.9] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D.-S. Shin, K.-H. Lee, H. S. Park, J. N. Han, C. J. Park, J.-B. Park, D.-W. Kim, D. Park, B.-I. Ryu. *Int'l Electron Device Meet.* 2005. 735.

Chapter 4

Evaluation of the effective carrier mobility of SiNW FET

4.1. Introduction

In **chapter 3**, on-current of the SiNW FETs with various cross-sectional shapes were evaluated, and optimization of cross-sectional shapes for high-performance SiNW FET was discussed. The drain current is proportional to inversion charge density and effective carrier mobility. However, it is difficult to separate contribution of effective carrier mobility and the contribution of inversion charge density from Dc characteristics. Therefore, investigation and separation to the inversion charge density and effective carrier mobility is effective for characterization of the dependence of the electrical characteristics on cross-sectional shapes of the SiNW FET.

In this chapter, inversion charge density (Q_{inv}) and effective carrier mobility (μ_{eff}) of the SiNW FETs were evaluated with the split-CV technique. For accurate evaluation of the gate capacitance of the SiNW FETs, mulch-channel SiNW FETs fabricated simultaneously on the same wafer as the single-channel SiNW FET. For accurate evaluation, advanced split-CV technique was adopted for elimination of the effects of parasitic series resistance and parasitic capacitance.

4.2. Split-CV method [4.1]

For characterization of inversion charge density and effective carrier mobility, Split-CV method was employed. Measurement setup for split C-V method is shown in **Fig. 4.1**. Measured C-V characteristics of silicon nanowire FET were not ideal because parasitic capacitance is superimposed on intrinsic capacitance of transistor as shown in **Fig. 4.1**. Advanced split-CV method was proposed. Capacitance of transistor is calculated using two C-V characteristics of transistors with different mask gate length. C-V characteristic of smaller L_{mask} is subtracted from larger L_{mask} and ΔC_{gc} is obtained. Difference of drain conductance of larger L_{mask} and smaller L_{mask} is also calculated as **Eq. 4.1**.

$$\Delta C_{gc} = \int_{-\infty}^{V_g} \left(C_{gc1} - C_{gc2} \right) dV \qquad (4.1)$$

The difference of drain conductance of the two devices can be calculated as shown in the equation (4.2).

$$\frac{1}{\Delta R} = \frac{1}{g_{d1}} - \frac{1}{g_{d2}} \qquad (4.2)$$

The effective carrier mobility (μ_{eff}) is calculated using the equation (4.3).

$$\mu_{eff} = \frac{Q_{inv}}{(\Delta L)^2 \Delta R} \qquad (4.3)$$

As the effective carrier mobility is plotted against the normalized inversion carrier density, the normalized inversion carrier density is calculated by division of the amount of inversion charge by the peripheral length of the SiNW channel. In this work, tri gate-like structure was adopted. Therefore, the peripheral length is the sum of top, left, and side surface of silicon nanowire channel. The Q_{inv} of planar SOI FET was calculated by sore division by actual channel width.

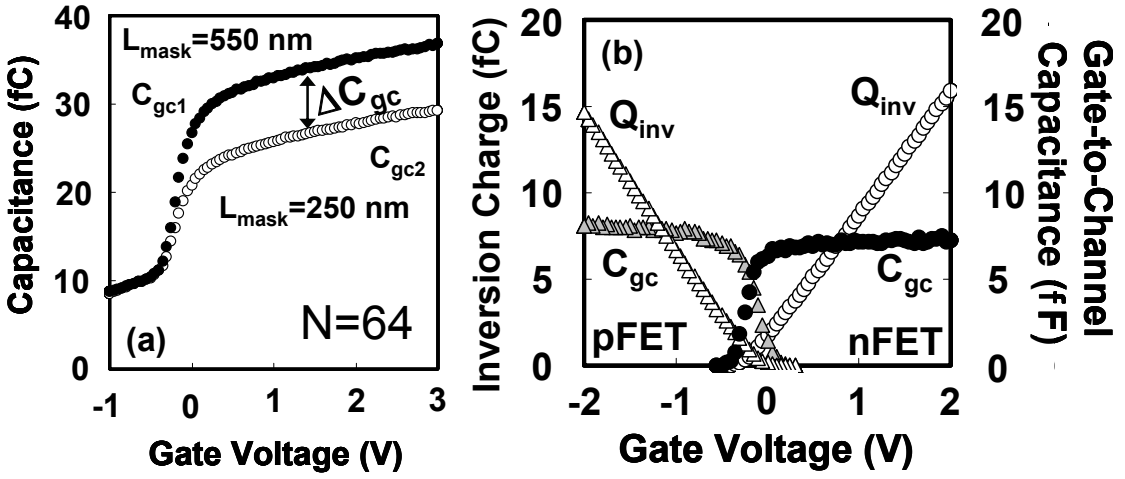


Figure 4.1 (a) Measured gate-to-channel capacitance of multi-channel silicon nanowire FET with different mask gate length. (b) Gate-to-channel capacitance and the amount of the inversion charge obtained using advanced split-CV method.

4.3. Evaluation of rectangular cross-section

4.3.1. Inversion charge density

In this section, I evaluate inversion charge density (Q_{inv}) of the SiNW FETs using advanced split-CV technique. First, I evaluated inversion charge density of the SiNW FETs with rectangular channel cross-sections. The amount of inversion charge is shown in **Fig. 4.2 (a)**. As the cross-sectional dimensions increased, the amount of inversion charge also increased. Both SiNW nFETs and pFETs had the same trend. Inversion charge densities normalized by peripheral length are shown in **Fig. 4.2 (b)**. As the cross-sectional dimensions decreased, the inversion charge density also increased.

Results of technology computer aided design (T-CAD) software in chapter 2 support the experimental results. As the high inversion charge density regions are at the corners of rectangular channel cross-section, higher inversion charge density was obtained with smaller channel cross-sectional dimensions.

The inversion charge density of SiNW FETs is higher than the inversion charge density of planar SOI FETs. In section 3, however, the on-current of SiNW nFETs is

much larger than the on-current of planar SOI nFETs. It is difficult to explain the increased normalized on-current of the SiNW FETs. Effective carrier mobility should be considered and discussed for explanation of the high normalized on-current of the SiNW FETs.

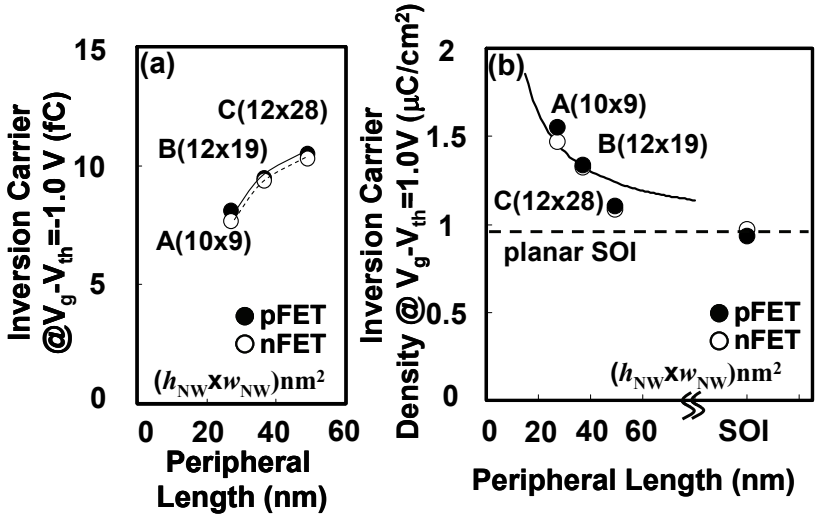


Figure 4.2 (a) The amount of inversion charge obtained using advanced split-CV technique. (b) Inversion charge density normalized by peripheral length of channel cross-section. The channel height h_{NW} is 10 or 12 nm. Dotted line indicates the inversion charge density of planar SOI nFET.

4.3.2. Effective carrier mobility of SiNW FETs with rectangular cross-sections

In this subsection, effective carrier mobility of the SiNW nFETs with rectangular cross-sections are evaluated and discussed. **Fig. 4.3** shows effective carrier mobility of the SiNW nFET with rectangular cross-sections using split-CV technique of the gate mask length of 550 and 250 nm. Higher high-field effective carrier mobility was obtained with SiNW nFETs compared with the planar SOI pFETs fabricated simultaneously on the same wafers.

Effective electron mobility and inversion charge density of the SiNW nFETs with rectangular cross-sectional shapes are summarized in **Tab. 4.1**. Effective electron

mobility is extracted at the inversion carrier density of 10^{13} cm^{-2}. Enhancement factors of inversion charge density, effective carrier mobility and normalize on-current are also summarized in the table. Inversion charge density of SiNW nFETs with tall rectangular cross-section (h_{NW} = 20 nm, w_{NW} = 12 nm) is smaller than the inversion charge density of other SiNW FETs with low rectangular cross-sections (h_{NW} = 10 or 12 nm). In chapter 2, thermal oxide thickness of (100)-planer is larger than the oxide thickness of (110)-plane. Thermal oxidation condition was 1000 ^{o}C for 1 hour in dry oxygen ambient. It was also reported that oxidation rate during thermal oxidation process depended on the crystal lattice plane [4.2]. I speculate that thick gate oxide thickness of (110)-oriented surface resulted in lower gate capacitance and lower inversion charge density.

Effective carrier mobility of SiNW pFETs and planar SOI pFETs were also evaluated as shown in **Fig. 4.5**. Contrary to the SiNW nFETs, the effective hole mobility of the SiNW pFETs with rectangular cross-sections were comparable with μ_{hole} of the planar SOI pFETs. Difference between μ_{hole} of different channel cross-sectional dimensions was little.

Enhancement factors of inversion charge density, effective carrier mobility and normalize on-current are summarized in **Tab. 4.2**.

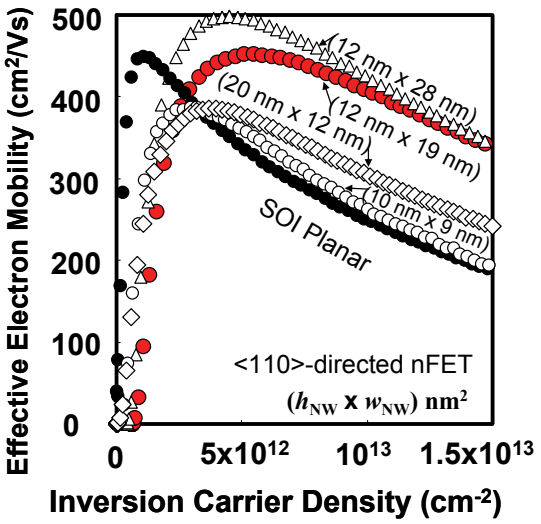


Figure 4.3 Effective electron mobility of the SiNW nFETs with rectangular channel cross-sections and planar SOI nFET fabricated simultaneously on the same wafers.

w_{NW} x h_{NW} (nm)	10 x 9	12 x 19	12 x 28	20 x 12	planar SOI
μ_{eff} (cm^2/Vs) at $N_s=10^{13}$ cm^{-2}	262	404	420	299	247
Noramlized factor (mobilty)	1.06	1.64	1.70	1.21	1
Q_{inv} ($\mu C/cm^2$) at V_g-V_{th}=1.0 V	1.47	1.32	1.09	0.92	0.97
Noramlized factor (inversion charge)	1.52	1.36	1.12	0.95	1
Total factor	1.61	2.23	1.91	1.15	1

Table 4.1 Effective electron mobility of SiNW nFETs with rectangular cross-sectional shapes at the inversion carrier density of 10^{13} cm^{-2} and inversion charge density at the overdrive voltage of 1.0 V. The values of the SiNW nFETs are compared with the values of planar SOI nFET. The factor compared with the planar SOI nFETs are also calculated. Total factor is the product of normalized factor (mobility) and normalized factor (inversion charge density).

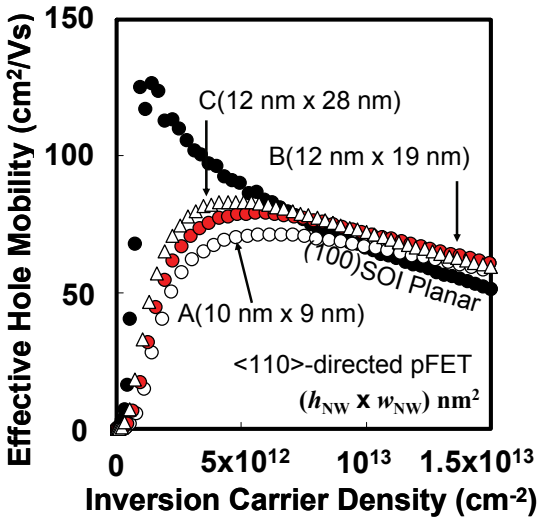


Figure 4.4 Effective hole mobility of SiNW pFETs with rectangular cross-sections and planar SOI pFETs.

w_{NW} x h_{NW} (nm)	10 x 9	12 x 19	12 x 28	20 x 12	planar SOI
μ_{eff} (cm^2/Vs) at $N_s=10^{13}$ cm^{-2}	67	71.8	72	48.1	66.5
Noramlized factor (mobilty)	1.01	1.08	1.08	0.72	1
Q_{inv} ($\mu C/cm^2$) at V_g-V_{th}=1.0 V	1.55	1.34	1.11	1.42	0.94
Noramlized factor (inversion charge)	1.65	1.43	1.18	1.51	1
Total factor	1.66	1.54	1.28	1.09	1

Table 4.2 Effective hole mobility and inversion charge density of the SiNW pFETs with rectangular cross-section and planar SOI pFETs. The effective hole mobility and inversion charge density are compared with the values of the planar SOI pFET, and normalized factors are calculated. Total factor is the product of the normalized factor of mobility and inversion charge density.

4.5. Evaluation of triangular and trapezoidal cross-sections

In the previous sections, effective carrier mobility of the SiNW FETs with rectangular cross-sections was evaluated and discussed. Corner angle of the rectangular channel cross-section is near 90°. <100>-directed SiNW FETs have triangular and trapezoidal cross-sections. Cross-sectional transmission electron microscope images of channel cross-sections are shown in **Fig. 4.5**.

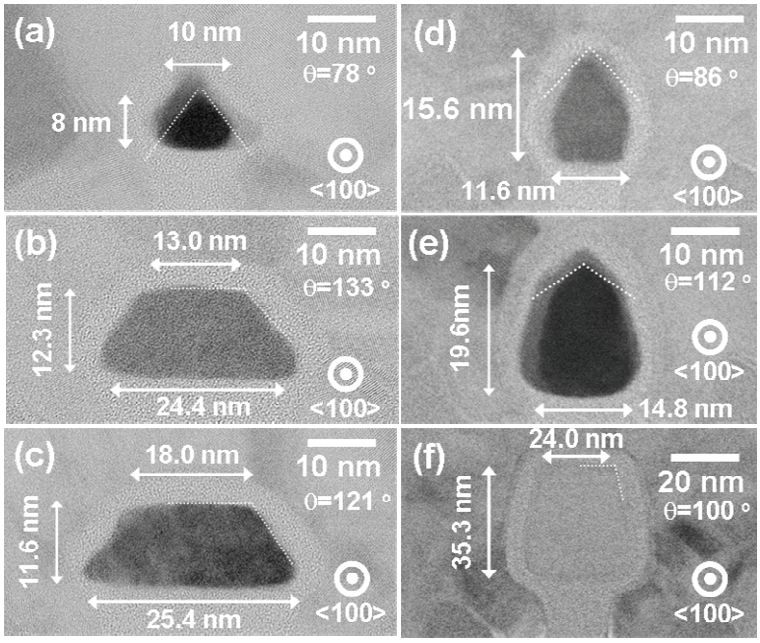


Figure 4.5 Cross-sectional transmission electron microscope images of the SiNW FETs. Angles of upper corners of triangle and trapezoidal cross-sections are also described in figures.

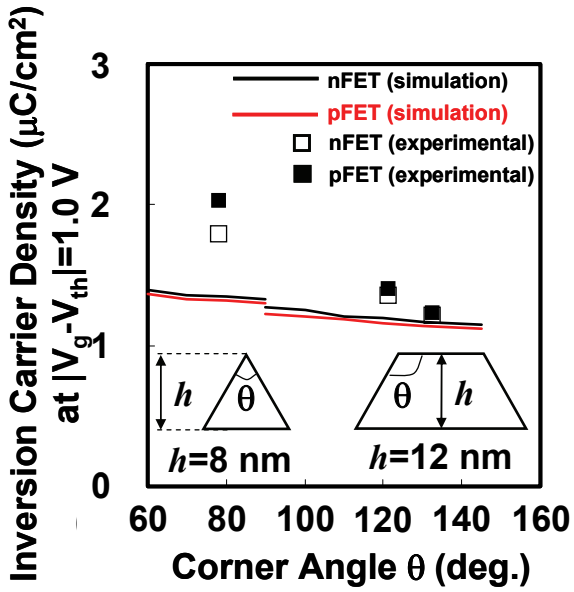


Figure 4.5 Normalized inversion charge density of SiNW FETs with triangle or trapezoidal cross-sectional shapes.

As θ decreased, Q_{inv} monotonically increased as shown in **Fig. 4.6**. We calculated the additional amount of inversion charge (Q_{add}) for the evaluation of a structural advantage of the SiNW FETs on the inversion charge density. We calculated the additional amount of inversion charge (Q_{add}) as shown in **Eq. 4.4**.

$$Q_{add} = \int_{-\infty}^{V_{ov}} c_{gc\_NW} dV - A \cdot \int_{-\infty}^{V_{ov'}} C_{gc\_SOI} dV \,, \tag{4.4}$$

where c_{gc_NW} is the gate-to-channel capacitance of the SiNW FET (not normalized). V_{ov} is the overdrive voltage of SiNW FET above 1.0 V from the threshold voltage. A is the channel area of the SiNW FET. C_{gc_SOI} is the normalized gate-to-channel capacitance of the planar SOI FET. $V_{ov'}$ is the overdrive voltage of the planar SOI FET above 1.0 V from the threshold voltage. The additional amounts of inversion charge Q_{add} are shown in **Fig. 4.7** A larger value of Q_{add} was obtained with a smaller value θ for both pFETs and nFETs.

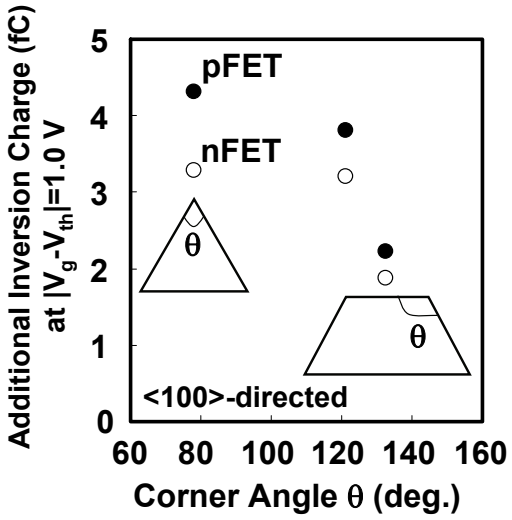


Figure 4.7 Additional inversion charge of SiNW FETs with triangle or trapezoidal cross-sections.

Fig. 4.9 shows effective carrier mobility of SiNW FETs with triangle and trapezoidal cross-sectional shapes and planar SOI FETs. It is not easy to analyze μ_{eff} of SiNW FETs with triangular and trapezoidal cross-sections because (*i*) cross-sectional area is different with each other and (*ii*) various surface orientations appear on the surface of SiNW FETs. As the effective carrier mobility depends on the surface orientation, extraction of μ_{eff} around corners is difficult. Further investigation is necessary.

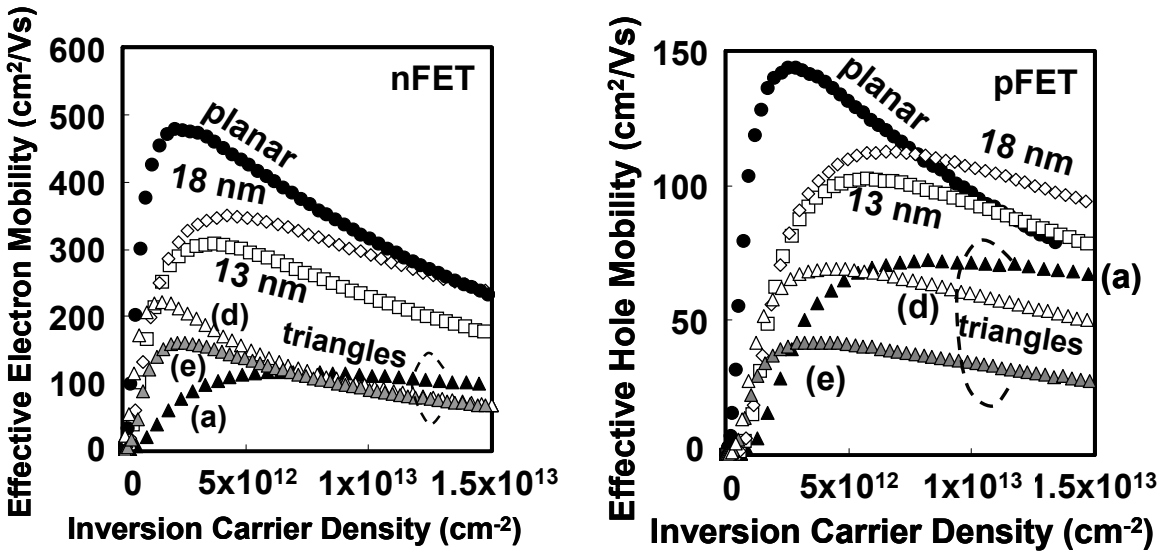


Figure 4.8 Effective carrier mobility of SiNW FETs with different cross-sectional shapes. μ_{eff} of the SiNW FET with triangle in the cross-section degraded compared with other trapezoidal and planar SOI FETs.

4.5. Conclusions

In this chapter, inversion charge density and effective carrier mobility of SiNW FETs were evaluated for establish guidelines for high performance SiNW FET. Summary is:

- Inversion charge density
  - As an angle of corner decrease, higher inversion charge density can be obtained.
  - Select channel surface orientation because of anisotropic oxidation rate during gate oxide formation process.

- Effective carrier mobility
  - For nFETs, rectangular cross-section with small channel height h_{NW} is favorable for high effective carrier mobility.
- Overall

Rectangular SiNW channel cross-section is recommended for high performance SiNW FET.

For achieve, high on-current of SiNW nFETs with rectangular cross-section, SiNW FET with the channel width w_{NW} of 19 nm and channel height h_{NW} of 12 nm as shown in **Fig. 4.10** because I found trade-off relationship between inversion charge density and effective carrier mobility below w_{NW} of 19 nm. This is a guide line for design of channel width w_{NW} of rectangular cross-section.

μ_{eff} of SiNW FETs with triangular and trapezoidal cross-sections were also evaluated. One can find a trend that as the cross-sectional area increased, μ_{eff} was also improved. It is not easy to analyze effects of cross-sectional shapes on μ_{eff} because (*i*) cross-sectional area affects μ_{eff} of SiNW FETs and (*ii*) various surface orientations appeared on the surface of SiNW channels with triangular and trapezoidal cross-sections. Further investigation and analysis is necessary.

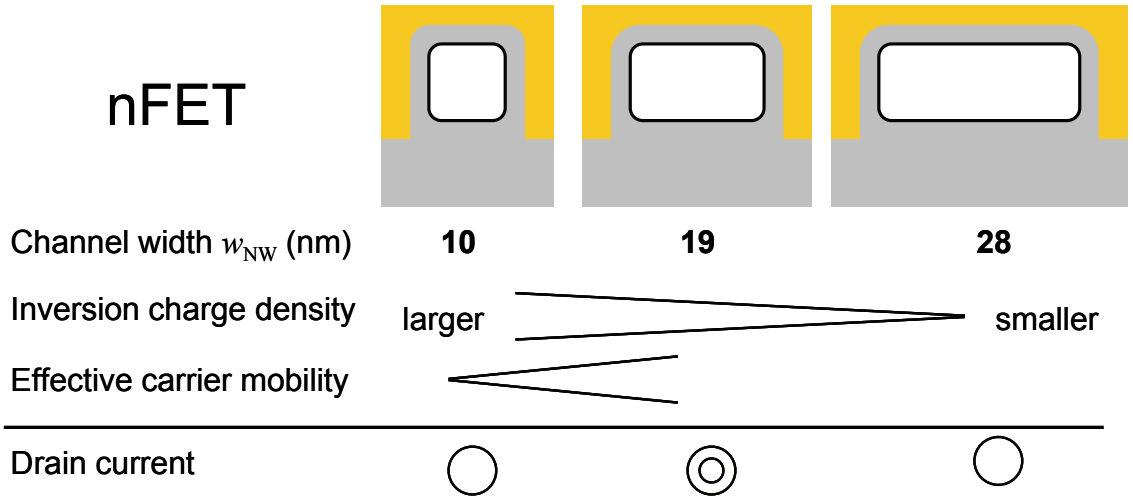


Figure 4.10 Optimization of cross-sectional shape for high normalized on-current of SiNW nFET with rectangular cross-sections.

References

[4.1] H. Irie, A. Toriumi. Advanced split-CV technique for accurate extraction of inversion layer mobility in short channel MOSFETs. Extended Abstracts of International Conference on Solid State Devices and Materials. 2005:864-865.

[4.2] E. A. Irene, H. Z. Massoud, and E. Tiemey. Silicon oxidation studies: Silicon orientation effects on thermal oxidation. J. Electronchem. Soc. 1986:1253-1256.

Chapter 5

Subthreshold characteristics of SiNW FET

5.1. Introduction

In previous sections, neither hump nor kink in the transfer characteristics of the SiNW FETs fabricated in this work was not observed. On the other hand, the on-current of the SiNW FETs was dominated by the corner component as the channel width w_{NW} decreased. Therefore we have to investigate the corner-effect of the SiNW FETs in this work.

In this chapter, the effect of cross-sectional shape on the electrical characteristics of the SiNW FET, especially corner-effect was investigated with theoretical approaches and technical computer aided design (TCAD) software. Finally I investigated the sub-threshold drain current by experiments and discussed about the corner effect.

5.2. Corner Effect

Three-dimensional multi-gate (MuG) MOSFET usually has corners across their channel cross-sections as shown in **Fig. 5.1**. In the literature, the corner effect is defined as the formation of independent channels with different threshold voltages next to the corners of the multi-gate silicon-on-insulator MOSFETs [5.1] because of the concentration of electric field near the corners of the channel of MuG FET. The parasitic channel has smaller threshold voltage for nFETs (larger threshold voltage for pFETs) compared with the main channel because of the concentration of the electric field. Therefore, the drain current with the lower threshold voltage of the parasitic channel is superimposed on the main drain current curve. As a result, the subthreshold slope moves to the left and degrades off-current. Therefore the corner-effect of multi-gate transistors should be controlled and eliminated.

It was shown that the corner effect strongly depends on the doping concentration in the channel [5.1]. The channel with low doping concentration exhibited the single maximum in the $d\ g_m/d\ V_g$ curve and reached 60 mV/dec. at the room temperature. The single maximum suggests that the single threshold voltage was obtained and that the corner effect is suppressed. On the other hand, the channel with high doping

concentration exhibits double maximum in the $d\,g_m/d\,V_g$ curve. Anomalous increase was also observed in the $d\,(V_g)/d\,(\log I_d)$ curve. These results suggest corner effect [5.3]. The corner effect also depended on the curvature of the corner, and as the radius of the corner increases the corner effects were suppressed [5.1].

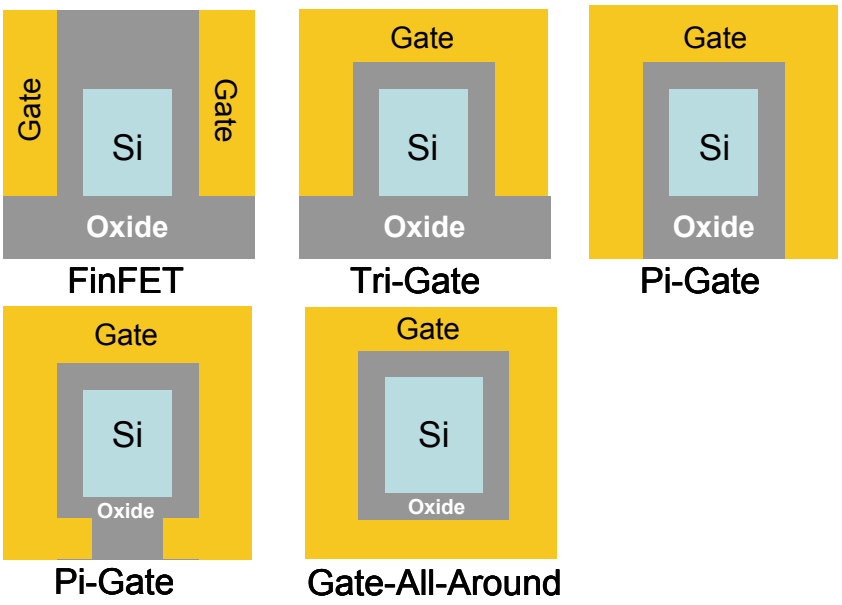


Figure 5.1 Various cross-sections of various multi-gate MOSFETs.

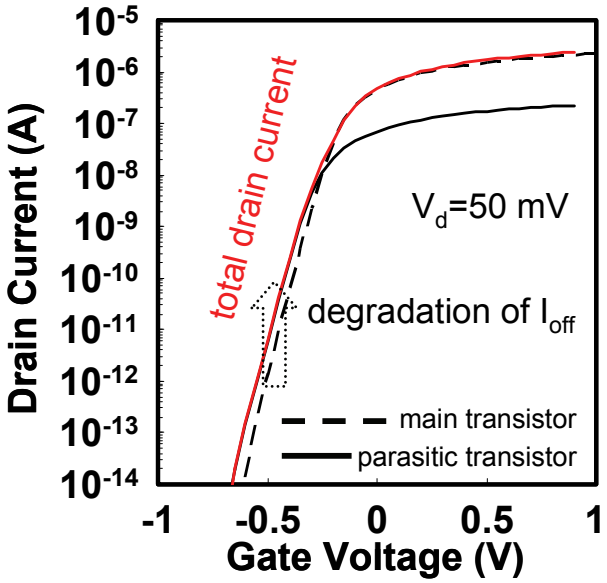


Figure 5.2 I_{off} degradation induced by the parasitic transistor of the multi-gate MOSFET.

5.3. Theoretical investigation on the corner-effects

5.5.1. Threshold Voltage of MOSFET

Threshold voltage of planar bulk MOSFET with long gate length is

$$V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{si} q N_a \psi_B}}{C_{ox}} \qquad (5.1)$$

$$\psi_B = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) \qquad (5.2)$$

where V_{fb} is the flat-band voltage, Ψ_B is the difference between Fermi level and intrinsic level, ε_{si} is the permittivity of silicon, N_a is the acceptor concentration, C_{ox} is gate oxide capacitance. The flat-band voltage is determined by the difference of work function of gate material and channel material; in this work, poly-Si and SiNW channel. Ψ_B is also determined by channel dopant concentration. We assume that dopant concentration around corners and flat-surface is equal. When we consider difference of threshold voltage of corner and flat-surface, the third term of RHS should be considered. Around corners, oxide capacitance C_{ox} is electrically smaller than C_{ox} along flat-surface because of concentration of electric field. **Fig. 5.4** shows difference of threshold voltage (ΔV_{th}) at corners and along flat-surface depicted in **Fig. 5.3**.

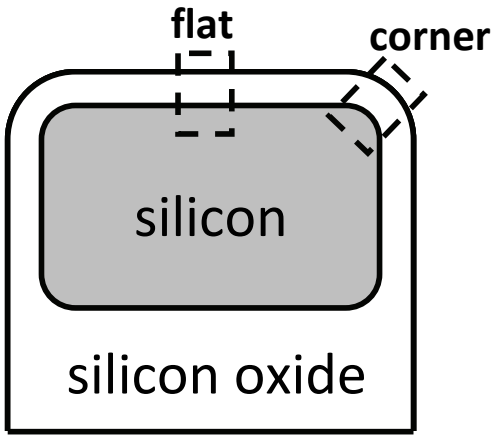


Figure 5.3 Schematic illustration for discussion of threshold voltage at corner and along flat-surface.

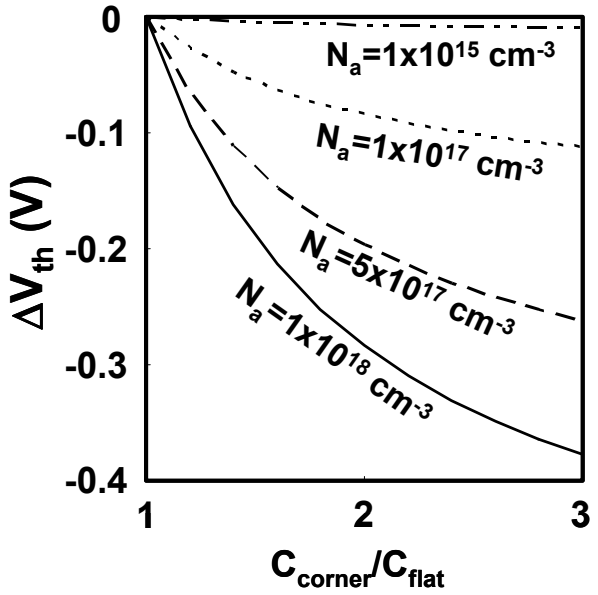


Figure 5.4 Difference of threshold voltage of MOSFET with different gate oxide capacitance.

5.5.2. Drain current in the subthreshold region

Theoretically, the transfer characteristics of the MOSFET can be written as follows [5.1].

$$I_{ds} = \mu_{eff} \frac{W}{L} \sqrt{\frac{\varepsilon_{si} q N_a}{4\psi_B}} \left(\frac{kT}{q}\right)^2 e^{q(V_{gs}-V_t)/mkT} \left(1 - e^{-qV_{ds}/kT}\right) \qquad (5.3)$$

, where μ_{eff} is the effective carrier mobility, W is the gate width, L is the gate length, ε_{Si} is the permittivity of silicon, q is the electrical element, N_a is dopant concentration, Ψ_B is the surface potential, k is the Boltzmann constant, T is the temperature, V_{gs} is the gate voltage, V_t is the threshold voltage, m is the body factor, V_{ds} is the drain voltage. Because we discuss about subthreshold region, we assume that the effective carrier mobility μ_{eff} is constant. Other parameters are also constants, and variables are $\exp((V_{gs}-V_t)/mkT)$. Now I add two different transfer characteristics in subthreshold region.

$$I = I_1 + I_2$$
$$= A_1 \exp\left(\frac{q\left(V_{gs} - V_t\right)}{m_1 kT}\right) + A_2 \exp\left(\frac{q\left(V_{gs} - V_t\right)}{m_2 kT}\right) \qquad (5.4)$$

Partial differentiation of I can be written as

$$\frac{\partial}{\partial V_g}\left(\frac{\partial(\log I)}{\partial V_g}\right)^{-1} = -C\left(\frac{1}{m_1} - \frac{1}{m_2}\right)^2 < 0 \qquad (5.5)$$

, where C is a positive constant.

This result suggests that the partial differentiation of log I monotonically decrease. Therefore the hump cannot be observed in the subthreshold region is the transfer characteristics with different m factor of different V_t.

5.4. Investigation of the corner-effect with TCAD simulation

5.4.1. Investigation of the transfer characteristics

As previously discussed, the corner effect has been investigated by many authors. In this section, I performed the simulation to investigate the effect of the corner effect on transfer characteristics and subthreshold slopes. Cross-section of SiNW channel used in this work is shown in **Fig. 5.5**.

We can observe the monotonically decrease of the subthreshold slopes in **Fig. 5.6**. This result is consistent with the results in the previous section. As the gate voltage increase, *SS* increased because V_g is reaching the threshold voltage. We can observe no kink or hump at the V_g above subthreshold region.

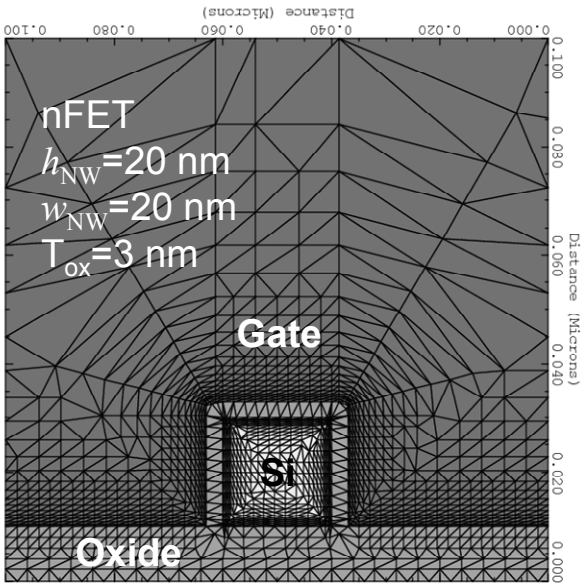


Figure 5.5 Channel cross-section for evaluation of the corner effect using TCAD software.

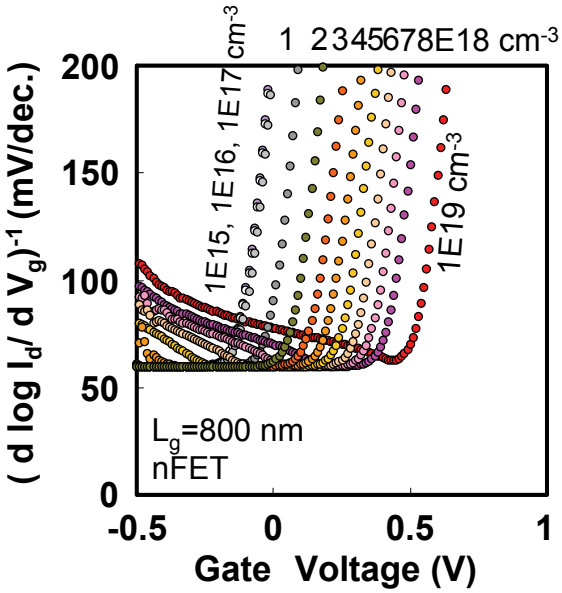


Figure 5.6 Subthreshold slopes with different channel doping concentration. As the doping concentration increases, the corner-effect appears.

5.4.2. Investigation of the inversion charge distribution and strong inversion conditions

In this subsection, inversion carrier density and strong inversion conditions around corners and along flat surface were investigated using TCAD software. **Fig. 5.7** shows the points that inversion carrier density was extracted. **Fig. 5.8** shows inversion carrier density distribution around corners and along flat surface as a function of channel concentration at the overdrive voltage of 1.0 V. As one can see inversion carrier density at corners and flat-surface changed as the channel doping concentration changed. **Fig. 5.9** shows difference of gate voltages that channel near corner and flat-surface reached strong inversion conditions (ΔV_g). As the doping concentration increased, ΔV_g also increased, which leads to the corner effect. Details are shown in **Fig. 5.10** and **Fig. 5.11**.

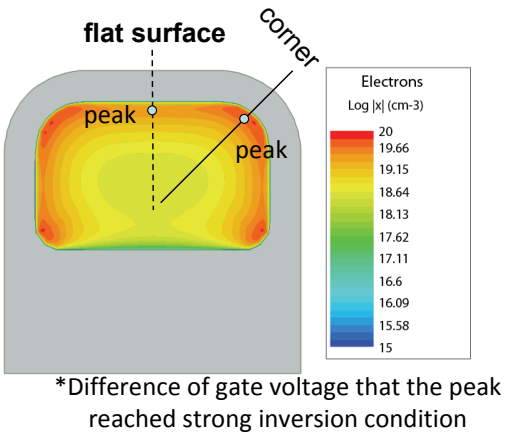


Figure 5.7 Schematic illustration of the point that inversion carrier density was extracted.

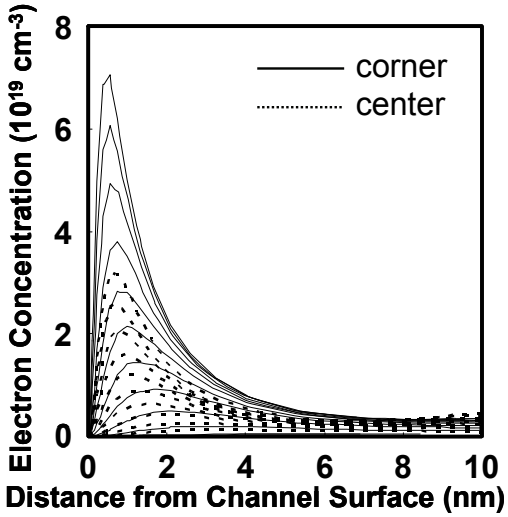


Figure 5.8 Inversion carrier distributions around corners and along flat-surface as a function of channel dopant concentrations.

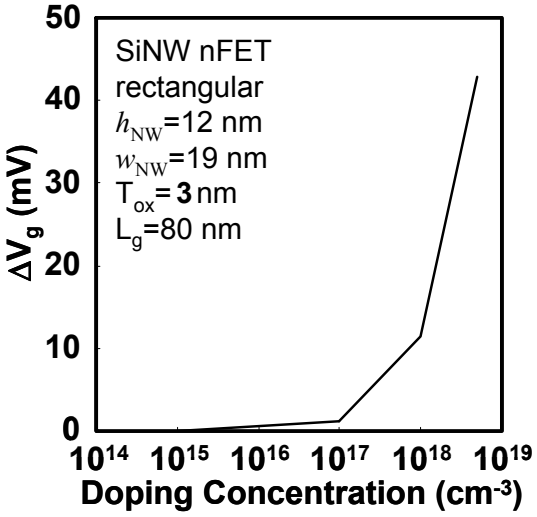


Figure 5.9 Difference of gate voltages that channel near corner and flat-surface reached strong inversion conditions.

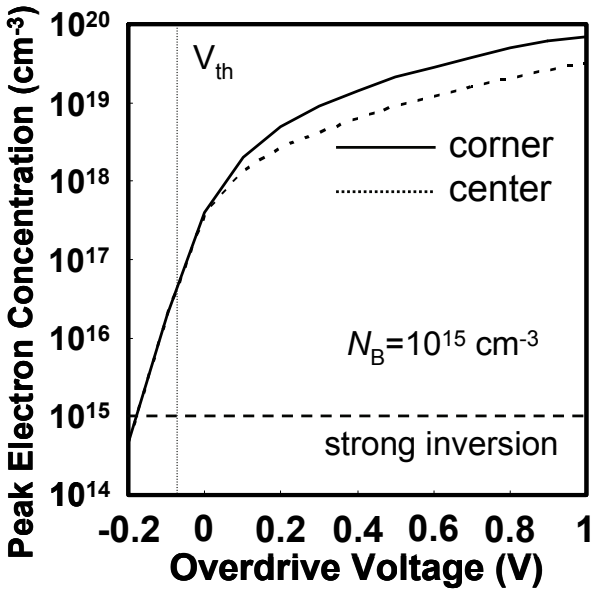


Figure 5.10 Peak inversion carrier concentrations around the corners and along flat-surface at N_b of 1×10^{15} cm^{-3}.

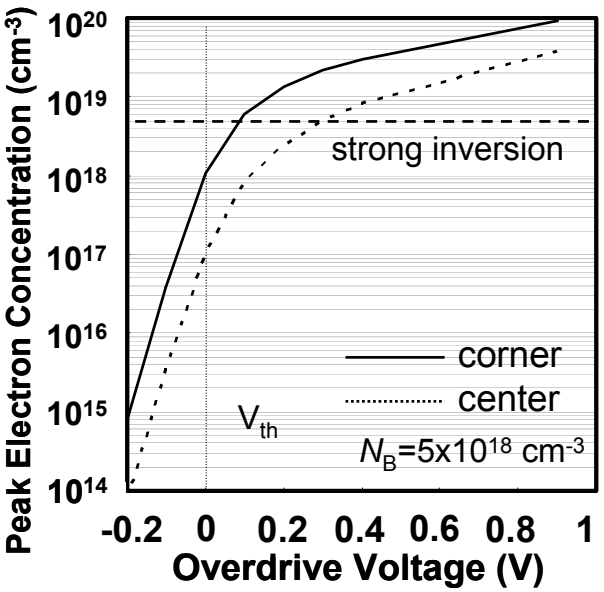


Figure5.11 Peak inversion carrier concentrations around the corners and along flat-surface at N_b of 5×10^{18} cm^{-3}.

5.5. Experimental investigation on the subthreshold characteristics

5.5.1. Is there corner effect?

The transfer characteristics of the SiNW FETs and planar SOI FETs were measured at different temperatures. Measurement step was 2 mV using middle integral time mode. **Figure 5.11** shows the transfer characteristics of the SiNW FETs and planar SOI FET. **Figure 5.12** shows subthreshold slopes. We can observe several humps at the partial differentiation of natural logarithm of the drain current of the SiNW FETs. According to the section 5.3, the corner effect can be observed as a monotonic decrease of the **Eq. 5.5**. Therefore the humps are not due to the corner effect.

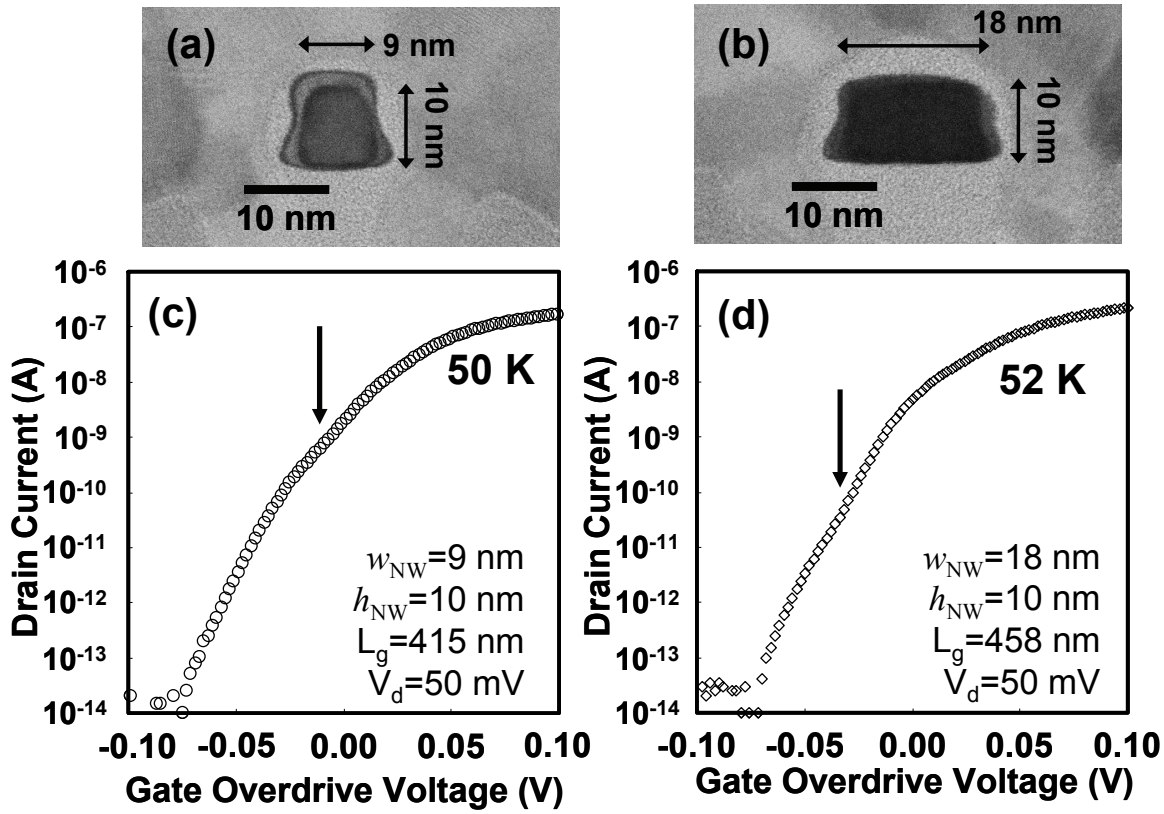


Figure 5.11 Transfer characteristics of SiNW nFETs with rectangular cross-sections.

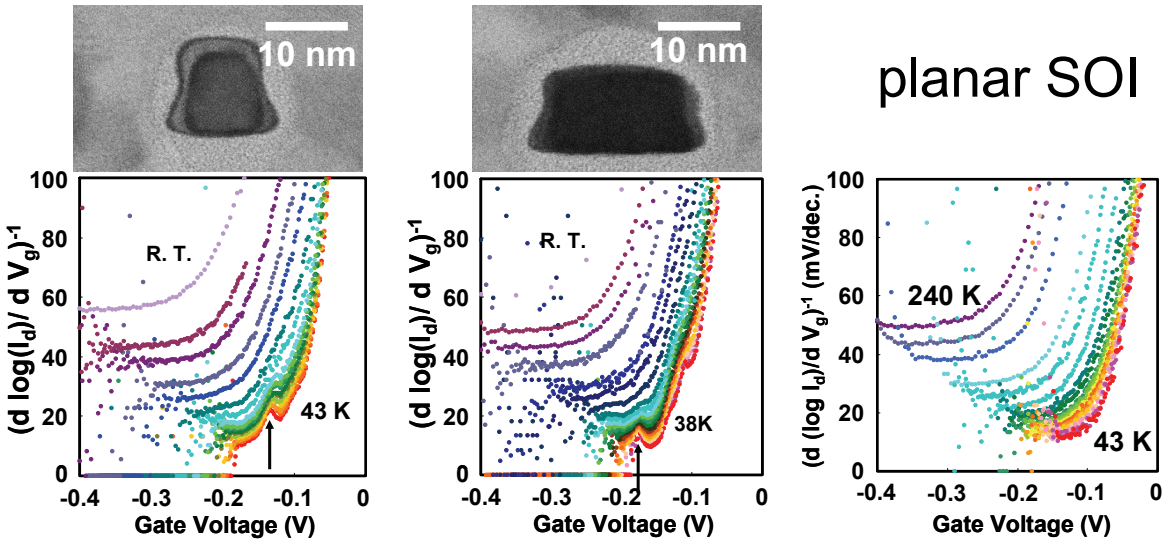


Figure 5.12 Subthreshold slopes of SiNW nFETs and planar SOI nFETs measured at temperatures from 43 to 290 K.

5.5.2. Explanation of the humps

As the subthreshold swing of the planar MOSFET is defined as

$$S.S. = \ln 10 \cdot \frac{kT}{q}\left(1 + \frac{C_{dm} + C_{it}}{C_{OX}}\right) \quad (5.6)$$

, where k is the Boltzmann constant, T is the temperature, C_{ox} is the gate oxide capacitance, C_{dm} is the depletion layer capacitance, C_{it} is the interfacial state capacitance. C_{it} is defined as

$$C_{it} = \frac{\partial Q_{it}}{\partial \psi_s} \quad (5.7)$$

, where Q_{it} is the interfacial state charge and Ψ_s is the surface potential. Therefore C_{it} depends on the surface potential and gate bias voltage. The experimental results suggest local distribution of the interfacial state density in the forbidden gap of silicon.

The minimum SS values at each temperature of SiNW nFETs with w_{NW} of 9 and 18 nm showed linear relationship on measurement temperatures from 86 to 290 K in **Eq. (5.6)** with a slope of 2.0×10^{-4} and 2.1×10^{-4} V/K, which corresponds to constant D_{it} of 2.9×10^{11} and 2.7×10^{11}cm^{-2}/eV, respectively. Moreover, at the measurement

temperatures below 74 K, kinks in transfer characteristics become predominant as shown in **Fig. 5.11**. Note that this feature was not observed for the planar-type SOI nFET (not shown). *SS* of SiNW nFET with w_{NW} of 9 nm and planar SOI nFET were shown in **Fig. 5.12**. Based on **Eq. (5.6)**, the kinks in the subthreshold slopes of the SiNW FET in **Fig. 5.12** can be attributed to the increase in C_{it} (φ_s), which indicate localized interfacial states in the forbidden bandgap of the SiNW channel. Therefore, a slight increase in the V_g may fill the local D_{it} with electrons (Q_{it}) to weaken the control of φ_s, which causes the kink in the subthreshold slope. The kink appeared at higher gate overdrive voltage (V_{ov}) as the measurement temperature increased. This is because larger increase of gate voltage is necessary to increase φ_s in strong inversion condition than in depletion and weak inversion conditions.

To extract the energy distribution of the interfacial states D_{it} (E), subthreshold slopes were calculated assuming an arbitrary D_{it} profile and compared with the obtained experimental data. A compact MOSFET model, HiSIM (Hiroshima-university STARC IGFET Model), was used for SS calculation. Interfacial state density distribution was expressed as a sum of the Gaussian functions in **Eq. (5.8)**.

$$D_{it}(E) = D_{it,peak} \exp\left(\frac{E - E_{it}}{2\sigma^2}\right) \qquad (5.8)$$

$$Q_{it}(\varphi_s) = q\int D_{it}(E)F(E,T,\varphi_s)dE, \qquad (5.9)$$

where E is the energy level in the silicon bandgap, F(E,T,φ_s) is the Fermi-Dirac distribution function, $D_{it,peak}$ is the maximum of the interfacial state density distribution, σ is the variance of the Gaussian function, E_{it} is the center of localized interfacial state distribution. C_{ox} was extracted by split-CV method applied to a multi-channel SiNW nFETs, so that 1.64 μF/cm^2 and 1.28 μF/cm^2 were extracted for 9×10 and 18×10 nm^2 SiNW nFETs, respectively. The extracted D_{it} (E) is shown in Fig. 3 (a). One can observe two distinct peaks in the profile; a component A with a peak interfacial state density of 1.3×10^{13} cm^{-2}/eV below 10 meV of E_c, and a component B with a peak interfacial state density of 5.4×10^{12} cm^{-2}/eV below 31 meV of E_c. The constant D_{it} obtained from the minimum *SS* measured at temperatures from 86 to 290 K are also shown in Fig. 3

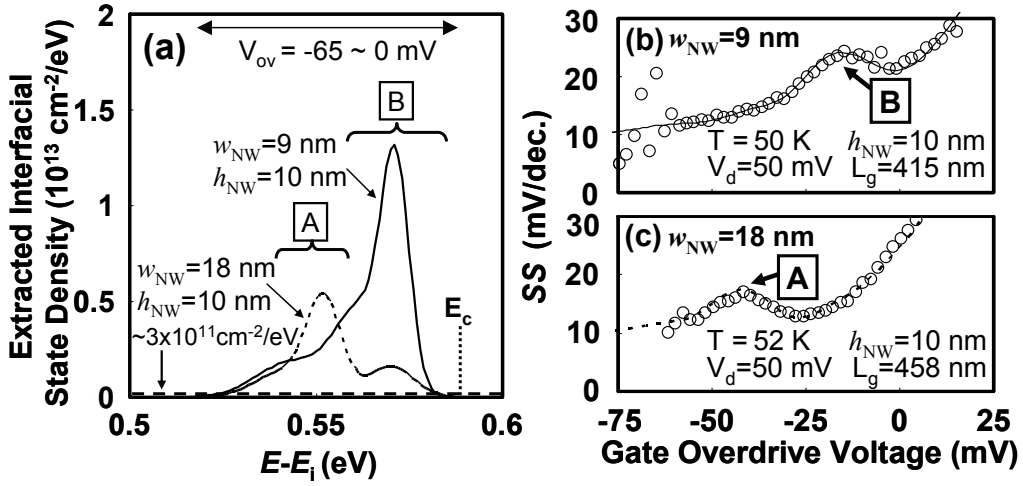


Figure 5.13 (a) Interfacial state density of the SiNW nFETs with wNW of 9 nm (solid line) and 18 nm (dotted line) as a function of the energy levels in the band gap of the SiNW channels. Dashed line indicates constant interfacial state density in all energy levels. Subthreshold slopes of the SiNW nFETs with wNW of (b) 9 nm and (c) 18 nm obtained by experiments (open circle) and calculations (solid and dotted lines).

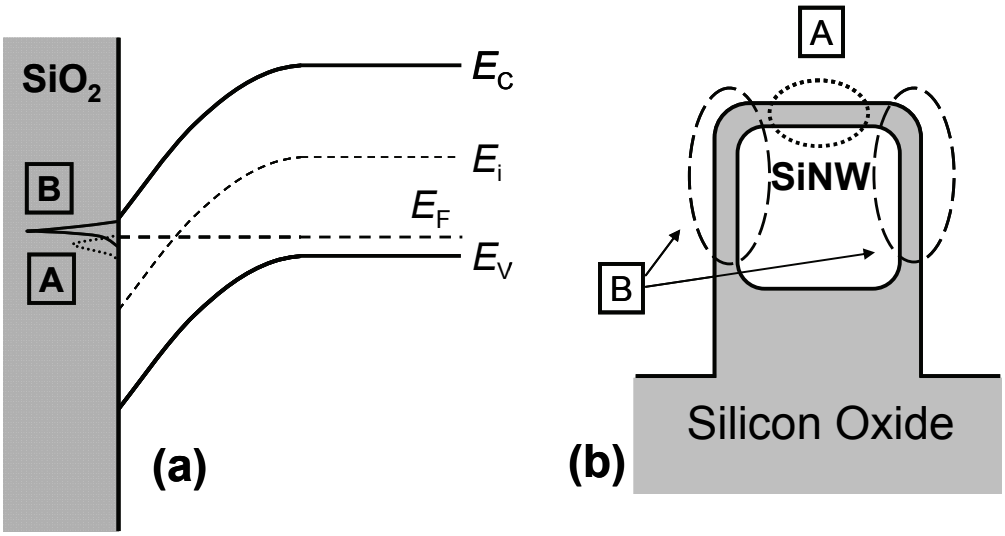


Figure 5.14 (a) A schematic band diagram for probing of the localized interfacial states with components A and B. (b) A schematic illustration for the relationship between the components of the additional interfacial states and the locations.

(a). These values are relatively small compared with the extracted D_{it}. The calculated *SS* explains well the measured SS as shown in **Fig. 5.13 (b) and (c)**. A schematic band diagram for probing of the additional *D*it (*E*) is shown in **Fig. 5.14 (a)**. While decreasing w_{NW} from 18 to 9 nm, the component *B* increased. On the other hand, the component *A* was larger with larger channel width. These results suggest that the component *B* is related to D_{it} along the side surfaces including the corners, and that the component *A* is related to D_{it} at the top surface as shown in **Fig 5.14 (b)**. Note that no kink was observed with planar SOI nFET as shown in **Fig. 5.12 (b)**, indicating the specific D_{it} distribution at the side surfaces or at the corners that have curved surface of the SiNW channel.

It has been reported using the electron spin resonance (ESR) that the trivalent silicon defect at silicon and silicon dioxide interface, which is called P_b center, is the origin of the interfacial states [5.6, 7]. Energy-resolved deep level transient spectroscopy (DLTS) is another evaluation method of interfacial states [5.8]. Two kinds of P_b center, P_{b0} and P_{b1} have been proposed, and the energy levels of Pb centers have been investigated by many authors. However, the peak energy levels of the interfacial state density distribution in **Fig. 5.13 (a)** are not consistent with the peak energy levels of P_{b0} and P_{b1} on (100) [5.18,10,11,12,13,15], (110) [5.12,15] , and (111) [5.8,9,12,14,15] -oriented silicon/silicon dioxide interfaces. These facts indicate that the interfacial states of the SiNW nFETs are physically different from those P_{b0} and P_{b1} on (100), (110), and (111)-oriented surfaces.

It has also been reported that stress was induced around the corners of the SiNW channel during gate thermal oxidation processes because of the volume expansion of silicon dioxide [5.16,17]. Ngai and White reported that the energy level of the interfacial defect changed as the distance between silicon atoms changed [5.18]. One possible explanation to the interfacial states near the conduction band edge of the SiNW channel is that energy levels of the interfacial states (P_b centers) split due to the distortion of the bond distances induced by the stress around corners during the thermal oxidation process.

Another possible reason might be the additional energy states due to the interstitial silicon atoms [5.19] in the channel, as interstitial silicon atoms can be injected from the oxidation front into silicon beam structure during the thermal oxidation process [5.20]. The model suggests that interstitial silicon atoms near the oxide/channel interface injected by sacrificial oxidation and following gate oxidation processes, which generated energy states near conduction band edge that evaluated in this work.

5.6. Conclusions

In this chapter, the corner effect of the SiNW FET was investigated. I demonstrated that low dopant concentration in SiNW channel suppresses the corner effect using theoretical formulas and technology computer aided design (T-CAD) software. The corner effect was defined as the formation of independent channel with different threshold voltage, which leads to degradation of off-characteristics. I also reconfirmed that the corner effect appears as the monotonic decrease in the partial differentiation of logarithm of drain current with gate voltage, not the hump. Experimental results showed no monotonic decrease in the partial differentiation of logarithm of drain current. Moreover, we observed a hump in transfer characteristics and subthreshold slopes. It can be speculated this is not the corner effect but localized interfacial state that is negligible in the room temperature.

In this chapter, I confirmed that at on-state inversion charge density is enhanced by corners and that at off-state there was no corner effect. This result guaranteed that degradation of off-characteristics was not induced. This result supports the design guideline in this work that corner enhances on-current of the SiNW FETs.

References

[5.1] F. J. G. Ruiz, A. Godoy, F. Gamiz, C. Sampedro, and L. Donetti. A comprehensive study of the corner effects in Pi-Gate MOSFETs including quantum effects. IEEE Trans. Electron Devices 54(12)2007, 3369-3377.

[5.2] W. Xiong, J. W. Park, and J. P. Colinge. Corner effect in multiple-gate SOI MOSFETs. IEEE International SOI conference. 2003. 111-113.

[5.3] J. P. Colinge, J. W. Park, and W. Xiong. Threshold voltage and subthreshold slope of multiple-gate SOI MOSFETs. IEEE Electron Device Lett. 24 (2003) 515.

[5.4] R. M. Swanson, and J. D. Meindl. Ion-implanted complementary MOS transistors in low-voltage circuits. *IEEE J. Solid-State Circuits*. **SC-2** (1972) 146.

[5.5] M. M.-Mattausch, H. J.-Mattausch, and T. Ezaki, The Physics and Modeling of MOSFETs: Surface-potential Model HiSIM, World Scientific Publishing, 2008.
11M. M.-Mattausch, U. Feldmann, A. Rahm, M. Bollu, and D. Savignac, IEEE Trans. Computer-Aided Design Integr. Circuits Syst. 15, 1 (1996).

[5.6] Y. Nishi, Jpn. J. Appl. Phys. 10, 52 (1971).

[5.7] P. J. Caplan, E. H. Poindexter, B. E. Deal, and R. R. Razouk, J. Appl. Phys. 50, 5847 (1979).

[5.8] D. Vuillaume, D. Goguenheim, and G. Vincent, Appl. Phys. Lett. 57, 1206 (1990).

[5.9] E. H. Poindexter, G. J. Gerardi, M.-E. Rueckel, and P. J. Caplan, J. Appl. Phys. 56, 2844 (1984).

[5.10] G. J. Gerardi, E. H. Poindexter, and P. J. Caplan, Appl. Phys. Lett. 49, 348 (1986).
17B. J. O'Sullivan, P. K. Hurley, C. Leveugle, and J. H. Das, J. Appl. Phys. 89, 3811 (2001).

[5.11] P. K. Hurley, B. J. O'Sullivan, F. N. Cubaynes, P. A. Stolk, F. P. Widdershoven and J. H. Das, J. Electrochem. Soc. 149, G194 (2002).

[5.12] J. P. Campbell and P. M. Lenahan, Appl. Phys. Lett. 80, 1945 (2002).

[5.13] P. K. Hurley, A. Stesmans, V. V. Afanas'ev, B. J. O'Sullivan and E. O'Callaghan, J. Appl. Phys. 93, 3971 (2003).

[5.14] N. H. Thoan, K. Keunen, V. V. Afanas'ev, and A. Stesmans, J. Appl. Phys. 109, 013710 (2011).

[5.15] L. Sekaric, O. Gunawan, A. Majumdar, X-H. Liu, D. Weinstein, J-W. Sleight, Appl. Phys. Lett. 95, 023113 (2009).

[5.16] A. Seike, T. Tange, I. Sano, Y. Sugiura, D. Kosemura, A. Ogura, and I. Ohdomari, Appl. Phys. Lett. 91, 062108 (2007).

[5.17] K. L. Ngai and C. T. White, J. Appl. Phys. 52, 320 (1981).

[5.18] G. M. Lopez and V. Fiorentini, Phys. Rev. B. 69, 155206 (2004).

[5.19] A. M. Pyzyna, D. R. Clarke, and N. C. MacDonald, IEEE Int'l Conf. Micro Electro Mechanical Systems 189 (2004).

Chapter 6

Effects of the gate oxide thickness of the SiNW FETs

6.1. Introduction

Oxide thickness is one of the scaling parameter. As the gate oxide thickness (t_{ox}) decreases, gate capacitance increases. Increased gate capacitance results in the increase of on-current as shown in **Eq. 6.1**.

$$I_{ds} = \mu_{eff} \frac{W}{L} C_{ox} \left(V_g - V_{th}\right) V_{ds} \qquad (6.1)$$

The gate oxide thickness t_{ox} also affects the off-characteristics of MOSFET. Subthreshold swing (S. S.) is described as

$$S.S = \ln 10 \cdot \frac{kT}{q} \left(1 + \frac{C_{dm} + C_{it}}{C_{ox}} \right) \qquad (6.2)$$

, where k is the Boltzmann constant, T is the temperature, q is the electrical element, C_{dm} is the depletion capacitance, C_{it} is the interfacial state capacitance, and C_{ox} is the gate oxide capacitance. Therefore, as the C_{ox} increases subthreshold swing *S.S.* also improves. In addition, drain induced barrier lowering (*DIBL*) will be also reduced because of the increase of the electrostatic controllability of the gate electrode on channel. Improved *S. S.* and DIBL result in the reduction of off-state leakage current of MOSFET.

However, the degradation of the effective carrier mobility (μ_{eff}) because of the reduction of t_{ox} has been reported [6.1]. A degradation mechanism is remote surface-roughness-scattering. Carrier in channel is affected by the surface roughness between gate oxide and poly-silicon interface. As the electric field is concentrated near corners at the high gate voltage of the SiNW FET with the rectangular cross-section, excessive surface roughness scattering might affects worse.

Gate leakage current is a main concern of gate oxide scaling. It is well known that as the gate oxide thickness decreases gate leakage current increases. Physics of gate leakage current of three-dimensional MOSFET is different from the mechanism of planar bulk silicon devices [6.4]. As the increased inversion charge density was obtained using rectangular cross-section, electric field concentrated at the corners. As the gate oxide thickness decrease, gate leakage current might increase.

Another concern is related to fabrication process of gate oxide dielectric. As the silicon nanowire FET has various surface orientations around the channel, conformal forming of gate oxide by rapid thermal oxidation cannot be expected. At the corners of the channel cross-section, the gate oxide thickness might be thinner than the oxide thickness at the flat surface because of the stress during formation of the gate oxide. The stress induced by the gate oxidation process has been pointed out by many authors [6.2] [6.3].

Therefore, it is not guaranteed that the equivalent oxide thickness (EOT) decreases in the same manner as EOT of planar bulk FET. One possibility is that the EOT around corners decrease slowly compared with EOT along the flat-surface.

Another issue related to the process technology is resistivity against over-etching process during gate patterning process. As mentioned in chapter 2, the SiNW FET requires large amount of the over-etching to eliminate stringers at the bottom of the gate electrode. There is a possibility that the thin gate oxide could not endure the over-etching process.

In this chapter, the SiNW FETs and planar SOI FETS with three different gate oxide thicknesses were fabricated on the same wafer. The electrical characteristics of the three wafers were characterized and evaluated. Finally I conclude the scalability of the SiNW FET with conventional processes.

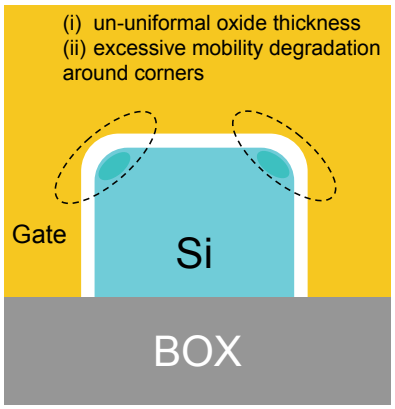


Figure 6.1 Concerns about the scaling of silicon dioxide dielectric film

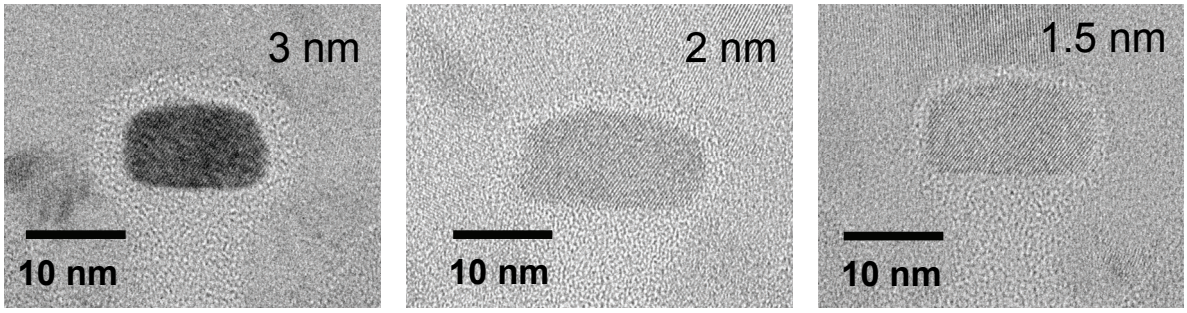
6.2. Device Fabrication

6.3.1. Gate oxide formation conditions

The SiNW pFETs and planar SOI pFETs were fabricated on the same wafers. After formation of the fin structures, the wafers were subjected to the sacrificial oxidation processes in dry oxygen ambient at 1000 ^{o}C. After removal of residual sacrificial oxide, the silicon dioxide firm was formed using rapid thermal oxidation process with 3, 2, and 1.5 nm. Process conditions were confirmed using monitor bulk silicon wafers. As the optical characteristic of SOI wafer is different from the characteristics of the bulk silicon wafer, the process temperature might different from the temperature of the monitor bulk silicon wafer.

6.3.2. Cross-sectional shapes of the SiNW FETs

Fig. 6.2 shows the cross-sectional shapes of the SiNW pFETs with different gate oxide thicknesses. Similar cross-sectional dimensions were obtained.



w_{NW}: 14 nm
h_{NW}: 9 nm

w_{NW}: 16 nm
h_{NW}: 10 nm

w_{NW}: 17 nm
h_{NW}: 10 nm

Figure 6.2 Cross-sectional shapes of the SiNW pFETs with different gate oxide thicknesses.

6.3. Long channel characteristics

First, inversion charge density of the SiNW pFETs and planar SOI pFETs with three different gate oxide conditions using split-CV measurement were evaluated. The experimental results are shown in **Fig. 6.3**. As the gate oxide thickness decreases, the inversion charge density increased. It is confirmed that the gate oxide thickness is decreases with proper process conditions for formation of gate oxide thickness.

Reduction of gate oxide thickness also affected the drain current. **Figure 6.4** shows the normalized on-current of the SiNW pFET with different gate oxide thicknesses. To ignore the effects of the parasitic series resistance, on-current of long channel devices were obtained.

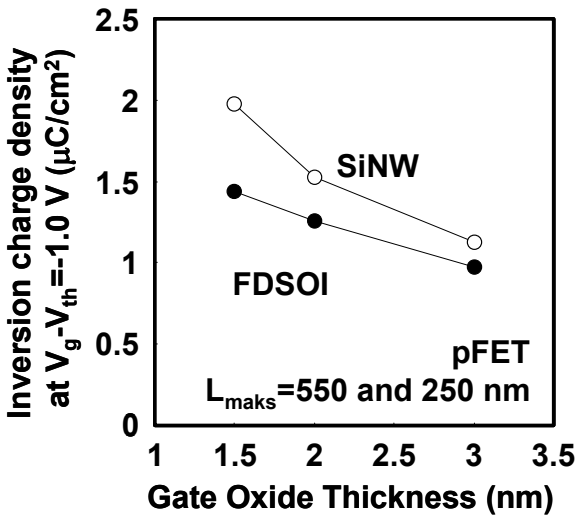


Figure 6.3 Inversion charge density at the overdrive voltage of 1.0 V as a function of the gate oxide thickness of the SiNW FET and planar SOI FET fabricated on the same wafer.

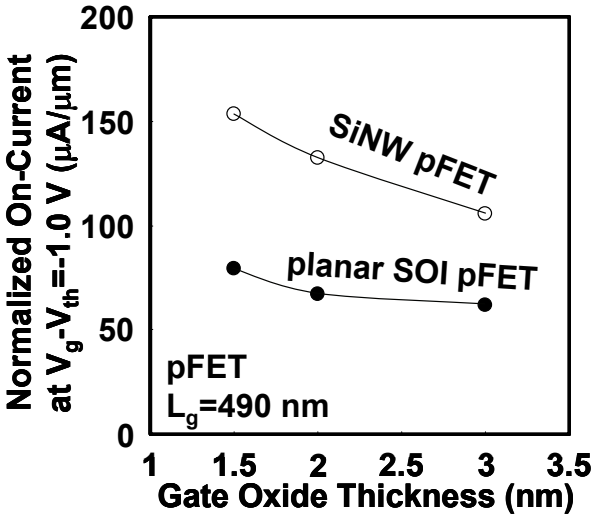


Figure 6.4 Normalized on-current at the overdrive voltage of 1 V of the SiNW pFETs and planar SOI pFETs fabricated on the same wafer as a function of the gate oxide thickness.

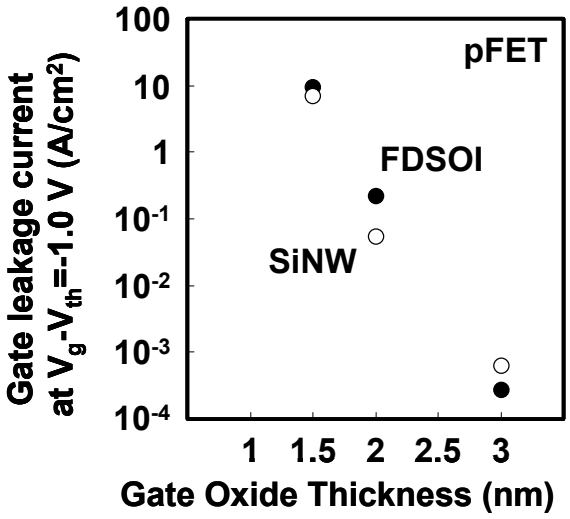


Figure 6.5 Gate leakage current of the SiNW pFETs and planar SOI pFETs fabricated on the same wafer.

6.3.1. Effective carrier mobility

Figure 6.6 shows effective carrier mobility of SiNW pFETs and plana SOI pFETs with different gate oxide thicknesses. Effective hole mobility of both SiNW pFETs and planar SOI pFETs degraded as the oxide thickness decreased. These results suggest that anomalous degradation of μ_{hole} of SiNW pFET did not occur.

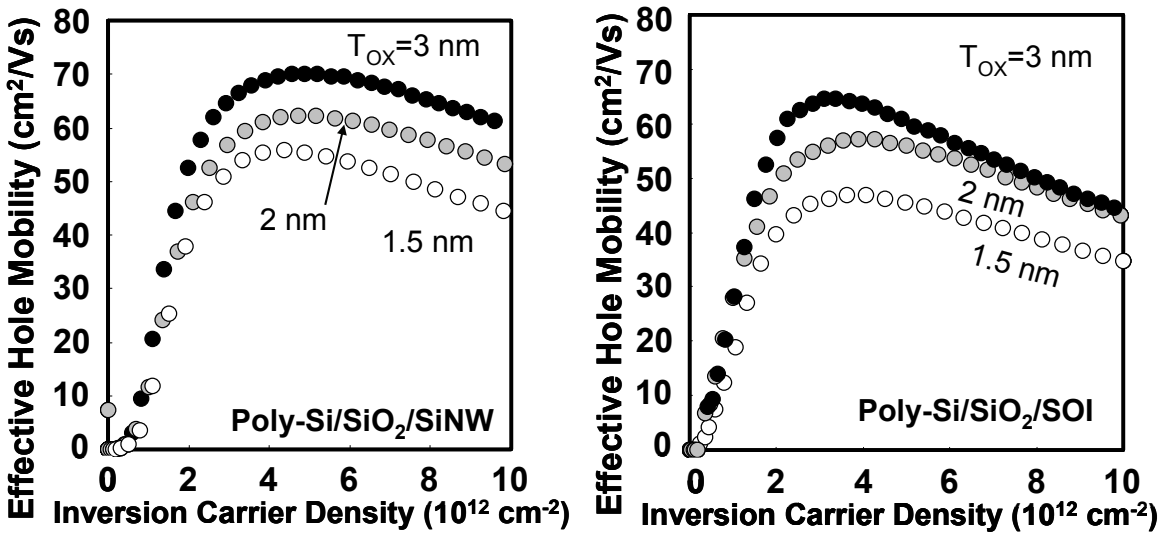


Figure 6.6 Effective hole mobility of SiNW pFETs and planar SOI pFETs fabricated on the same wafer as a function of gate oxide thicknesses.

6.4. Short channel characteristics

As the gate oxide thickness decreased, the gate capacitance increased, which resulted in the improvement of off-characteristics of MOSFETs. Subthreshold swings of the SINW FETs with the gate length of 65 nm are shown in **Fig. 6.7**. As the gate oxide thickness decrease, subthreshold characteristics improve. **Fig. 6.8** shows improvement of DIBL as the gate oxide thickness decreased.

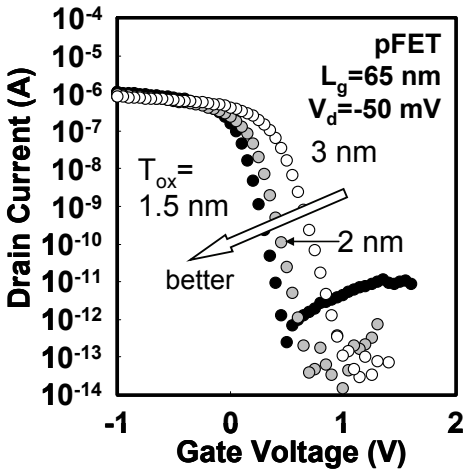


Figure 6.7 Typical transfer characteristics of SiNW pFET with gate length of 65 nm as a function of gate oxide thickness.

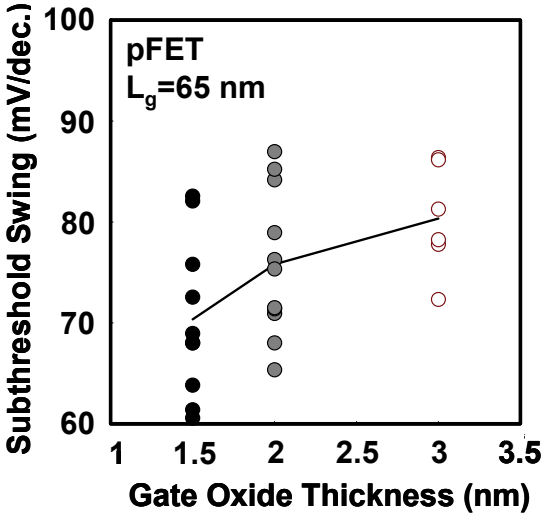


Figure 6.8 Subthreshold swings of the SiNW pFETs with the gate length of 65 nm as a function of the gate oxide thickness.

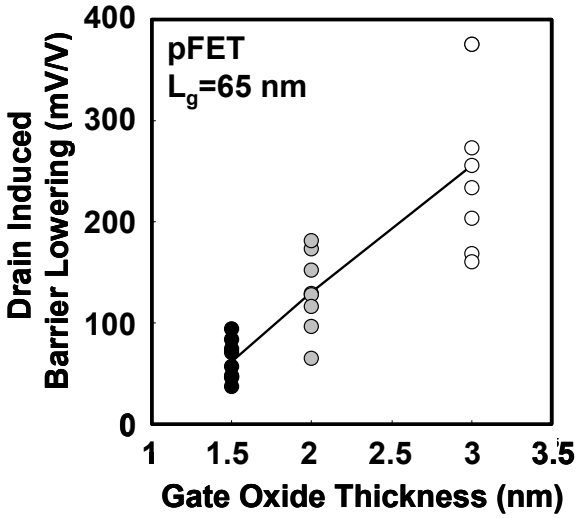


Figure 6.9 Drain induced barrier lowering (DIBL) of the SiNW pFETs with the gate length of 65 nm as a function of the gate oxide thickness.

Finally, I characterized I_{ON}/I_{OFF} characteristics, which is shown in **Fig. 6.10**. As the gate oxide thickness decrease, I_{OFF} decreases. On the other hand, I_{ON} is almost consistent with different gate oxide thickness, which is opposite to the results of long channel devices. One reason is the significant parasitic source/drain resistance. As the channel length decrease, intrinsic total resistance of MOSFET decreases. **Figure 6.11** shows I_{ON}/I_{OFF} ratio of the SiNW pFETs. As the gate oxide thickness decreases, I_{ON}/I_{OFF} characteristics improved.

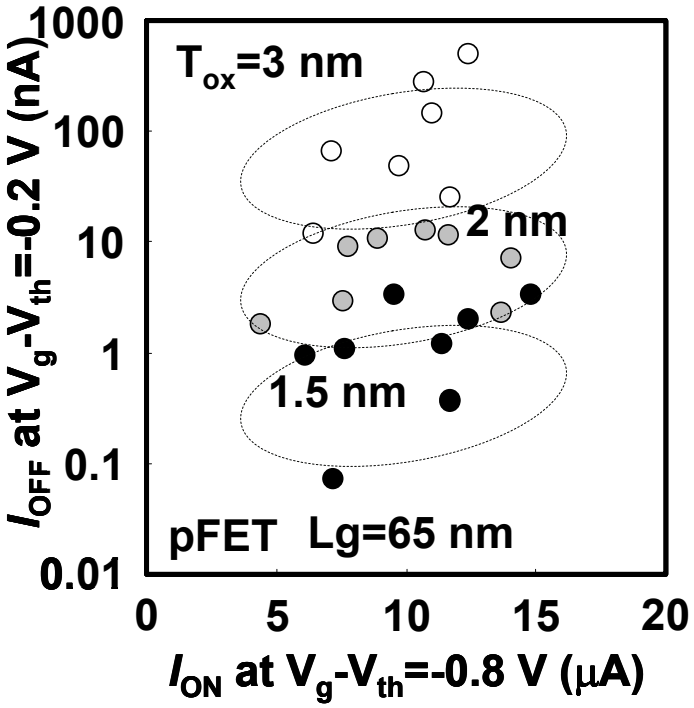


Figure 6.10 Plot of on-current at the overdrive voltage of 0.8 V and the off-current at the overdrive voltage of -0.2 V with the gate length of 65 nm as a function of the gate oxide thickness.

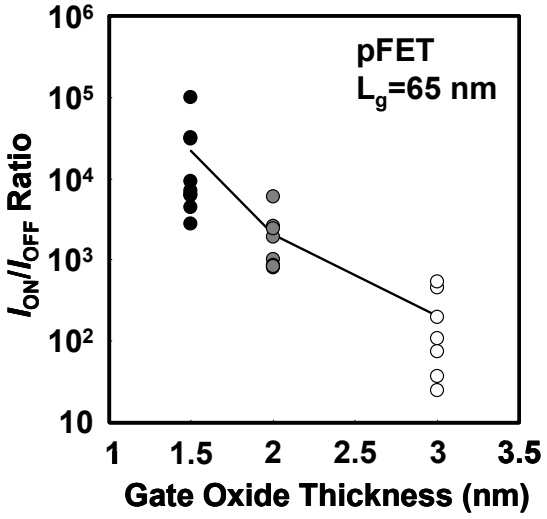


Figure 6.11 The I_{ON}/I_{OFF} ratios of the SiNW pFETs with the gate length of 65 nm as a function of the gate oxide thickness.

6.5. TCAD simulation of gate oxide scaling

Figure 6.10 (a) shows relationship between the equivalent oxide thickness (EOT) and physical gate oxide thickness of SiNW nFET with w_{NW} of 19 nm and h_{NW} of 12 nm. When T_{ox} is large and nearly 3 nm, as the cross-sectional dimension decreased, EOT decreased. As T_{OX} decreased, EOT of each device reached each other, and also reached to EOT of planar SOI nFET. These results suggest that structural merit of the reduction of EOT decreased as the physical oxide thickness decreased. **Figure 6.10 (b)** shows oxide capacitance of SiNW nFETs. In small T_{OX} region, gain of gate capacitance increased as the T_{OX} decreased. As EOT decreases, more gain of gate capacitance is required for decrease of EOT. Therefore, EOT of SiNW nFETs tend to shrink to one point.

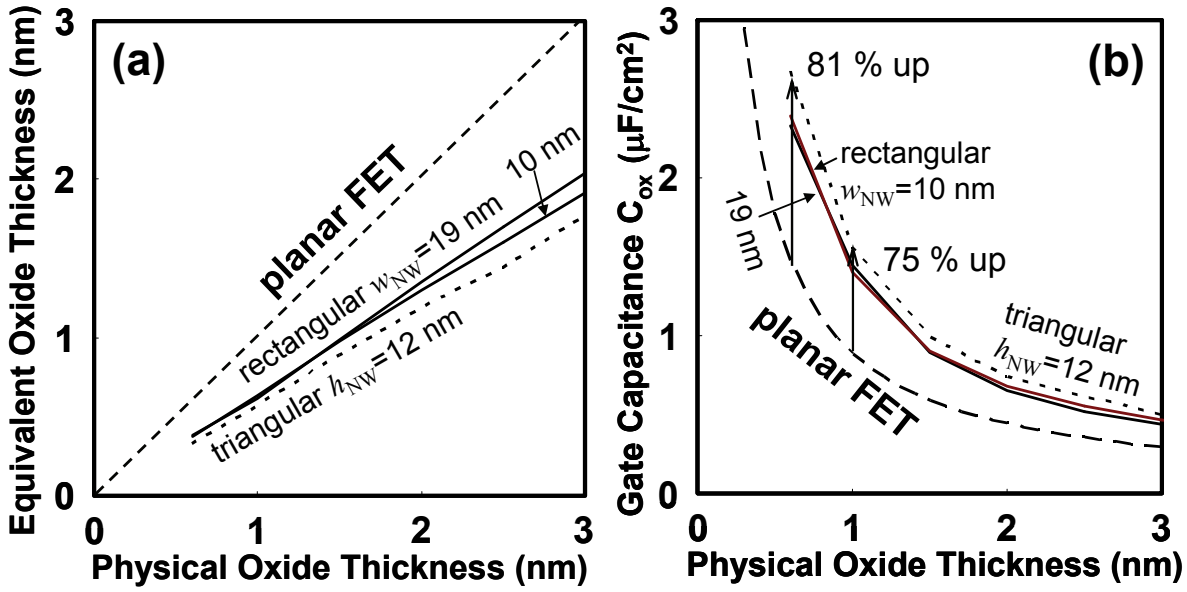


Figure 6.10 (a) Equivalent oxide thickness of SiNW nFET with h_{NW} of 12 nm and w_{NW} of 19 nm as a function of gate physical oxide thickness. (b) Gate capacitance of SiNW FET as a function of gate physical oxide thickness.

6.6. Conclusion

In this chapter, effects of the gate oxide thickness of the SiNW pFETs were examined. The SiNW pFETs with the gate oxide thickness down to 1.5 nm were successfully fabricated none the less of the large amount of over-etching step. One reason might be the semi gate-around structure, which enables decreases of the over-etching step time.

Gate leakage current of the SiNW pFETs is comparable with that of the planar SOI pFETs fabricated at the same time. This result suggests that the corner does not enhance the gate leakage current of the SiNW FET.

Effective hole mobility of the SiNW pFET is comparable with the mobility of the SOI planar pFETs and significant degradation of the SiNW pFET was not observed.

Inversion charge density of the SiNW FET is comparable with that of the planar SOI pFETs. This result suggests that the gate oxide thickness is scalable using rapid thermal oxidation process.

As the planar FETs, the I_{ON}/I_{OFF} characteristics of the SiNW pFETs also improved by the reduction of the gate oxide thickness. This result suggests that the I_{ON}/I_{OFF} characteristics in chapter3 can be improved by reduction of the gate oxide thicknesses.

References

[6.1] S. Saito, K. Torii, Y. Shimamoto, S. Tsujikawa, H. Hamamura, O. Tonomura, T. Mine, D. Hisamoto, T. Onai, J. Yugami, M. Hiratani, and S. Kimura. Effects of remote-surface-roughness scattering on carrier mobility in field-effect-transistors with ultrathin gate dielectric. *Appl. Phys. Lett.* **84** (2004) 1395.

[6.2] L. Sekaric, O. Gunawan, A. Majumdar, X. H. Liu, D. Weinstein, and J. W. Sleight. Size-dependent modulation of carrier mobility in top-down fabricated silicon nanowires. *Appl. Phys. Lett.* **95** (2009) 023113.

[6.3] A. Seike, T. Tange, Y. Sugiura, D. Kosemura, A. Ogura, and I. Ohdomari. Transconductance enhancement of nanowire field-effect transistors by built-up stress during thermal oxidation. *Appl. Phys. Lett.* **91** (2007) 062108.

[6.4] L. Chang, K. J. Yang, T-C. Yeo, I. Polishchuk, T.-J. King, and C. Hu. Direct-tunneling gate leakage current in double-gate and ultrathin body MOSFETs. *IEEE Trans. Electron Device.* **49** (2002) 2288.

Chapter 7

The SiNW FET with four-terminal geometry

7.1. Introduction

The device operation of meta-oxide-silicon field-effect transistors (MOSFET) is critically determined by the electrical potential profile in channel [7.1]. Nehari *et al*. showed that, in theory, the profile of conduction band edge of the silicon nanowire (SiNW) FETs is different from profile of planar MOSFETs [7.2]. Horiguchi *et al*. calculated the potential variation induced by the stress generated during the pattern-dependent oxidation (PADOX) process of silicon [7.3]. PADOX is an important process because it is usually involved in the fabrication of a silicon nanowire channel. Therefore, the characterization of the channel potential is important for the investigation of the device operation of the SiNW FET. Using a purely electric atomic force microscope, Nakamula et al. observed the channel potential profile of pentacene thin-film transistors [7.4]. Kelvin probe force microscope [7.5] and scanning capacitance microscope (SCM) are also used for the characterization of the channel potential profile [7.6, 7]. SCMs were also used for the observation of *pn* junctions. The observations for *pn* junctions with SCM have also been performed [7.8] [7.9]. Microscopes are an effective technology, which allows the direct observation of electrical potentials with high resolution. However, microscopes can be used only for devices with an exposed channel, such as back gate devices or cross-sections of a MOSFET on a wafer. Therefore, to investigate front gate devices, we need alternative methods because the channel surface is covered by the gate oxide and a gate electrode. We implemented a four-terminal geometry, which was originally employed for the measurement of the conductance of a quantum wire [7.10] [7.11]. In this work, we experimentally demonstrate the implementation of the four-terminal geometry for the electrical characterization of the quasi-Fermi potential profile in the channel of the SiNW FET.

7.2. Device structure and fabrication

We fabricated the SiNW FET with the four-terminal geometry on a silicon-on-insulator (SOI) wafer with the SOI layer and buried-oxide (BOX) thickness of 61 and 145 nm, respectively. The double-dagger like structure with embedded source, drain, and voltage-measurement terminals V_1 and V_2 were formed in ArF lithography and dry-etching processes as shown in **Fig. 7.1**. The device was subjected to thermal oxidation in dry oxygen ambient for 1 hour at 1000 ^{o}C. After removing the sacrificial oxide with the wet etching process, we obtained a gate oxide of 5 nm using thermal oxidation. We deposited a poly-Si gate electrode of 75 nm was deposited using the chemical-vapor deposition method. After the gate electrode patterning and spacer formation, we implanted arsenic ions into source, drain, V_1, and V_2. After a rapid thermal annealing, the self-align nickel silicidation process reduced the parasitic resistance of source and drain (R_{SD}). The device structure after the self-align nickel silicidation process is shown in **Fig. 7.2** and **Fig. 7.3**. The details of the device fabrication process are described in elsewhere [7.12].

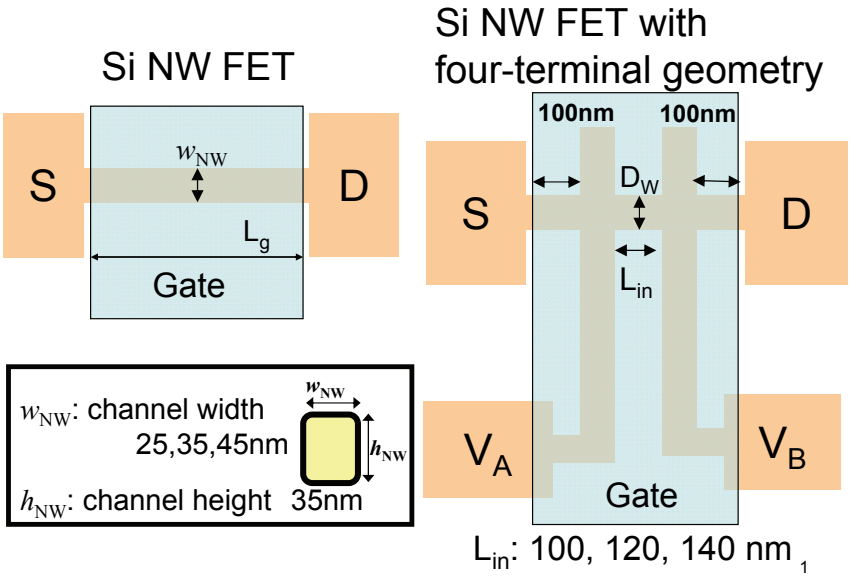


Figure 7.1 Device structure of the silicon nanowire FET with the four-terminal geometry.

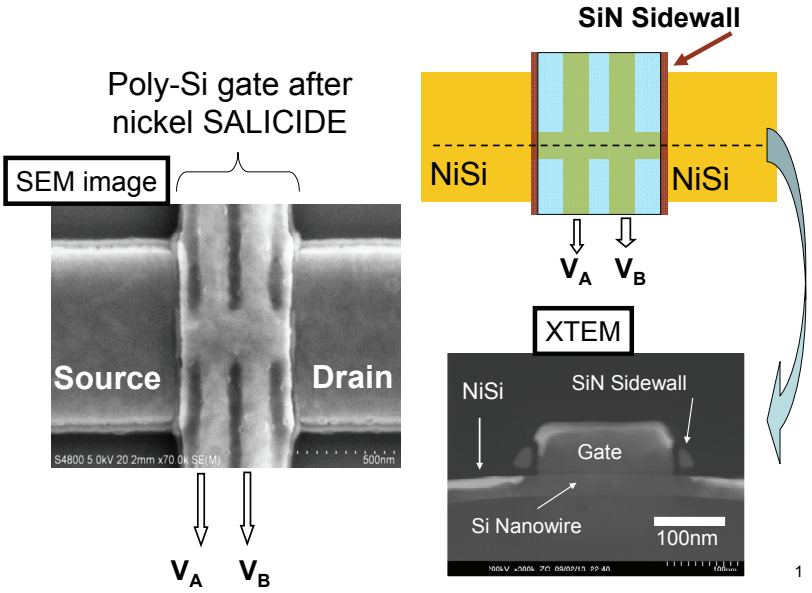


Figure 7.2 Secondary electron microscope image and transmission electron microscope images of the SiNW FET with four-terminal geometry.

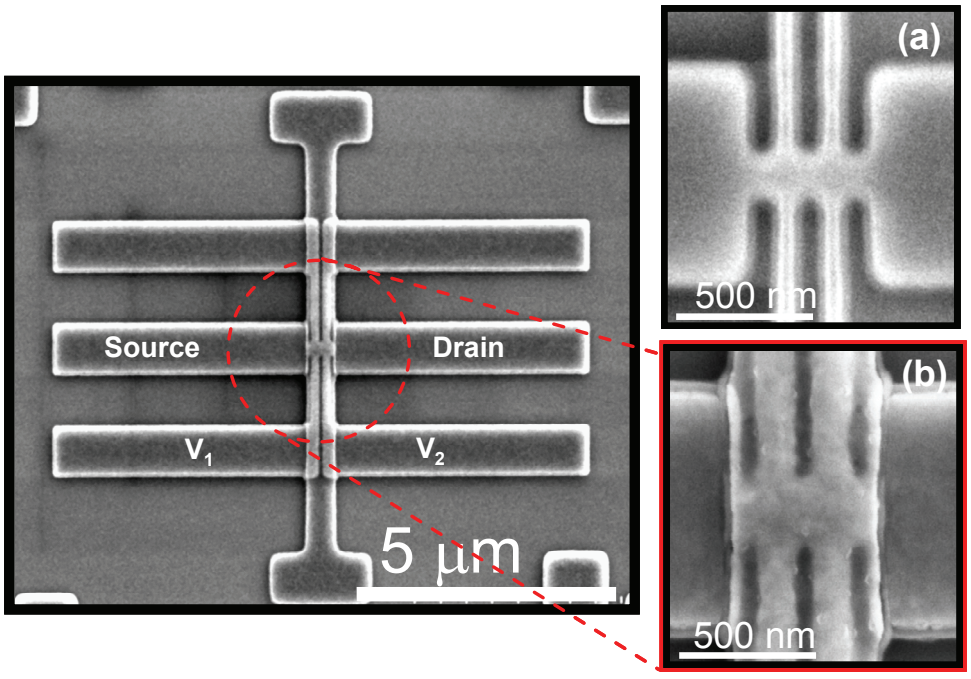


Figure 7.3 Review secondary electron microscope images of the SiNW FET with four-terminal geometry before and after gate formation process.

7.3. Electrical characteristics

Using gate, source, and drain electrodes, we measured the electric characteristics of the SiNW FET with four-terminal geometry. We obtained the transfer and output characteristics that are typical for MOSFET as shown in **Fig. 7.4**. We obtained the subthreshold swing of 98 mV/dec. a threshold voltage of -0.33 V. We confirmed the usual operation of the SiNW FET with four-terminal geometry as an MOSFET.

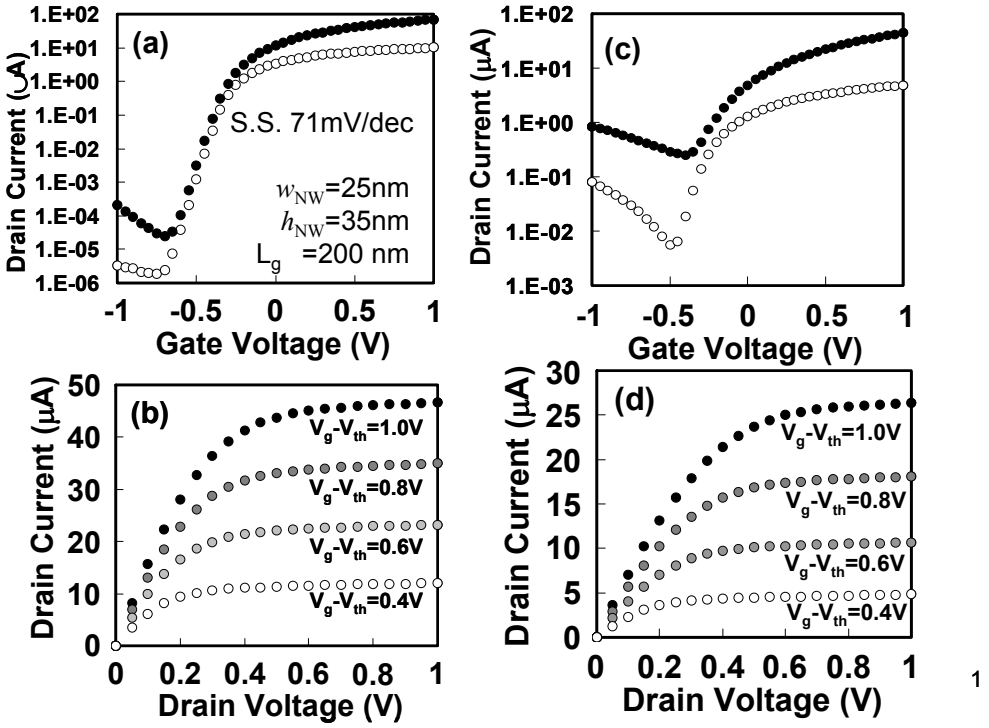


Figure 7.4 Transfer and output characteristics of (a) (b) the conventional SiNW FET and (c) (d) the SiNW FET with four-terminal geometry.

7.4. Calculation of quasi-Fermi potential profile

Next, we measured all terminal voltages (gate, source, drain, V_1, and V_2). We extracted the source/drain parasitic resistance R_{SD} of the SiNW FET with four-terminal geometry using Chern's channel-resistance method with different gate lengths, which resulted in 1.5 kΩ [7.13]. For the measurement of the terminal voltages V_1 and V_2, we

used the voltage measurement mode of the Agilent 4156C semiconductor parameter analyzer. We propose a device analysis model as shown in **Fig. 7.5 (a)**. We also calculated the intrinsic terminal voltage drops (ΔV_{c1}, ΔV_{c2}, and ΔV_{c3}). During this calculation, the voltage drops caused by the external R_{SD} were eliminated. ΔV_{c1} was the voltage drop near the source edge, ΔV_{c2} was the voltage drop near the channel center, and ΔV_{c3} was near the drain edge of the SiNW FET with four-terminal geometry (cf. **Figs. 7.5 (b)** to **(d))**. As the gate voltage V_g increased, ΔV_{c1} and ΔV_2 also increased. On the other hand, ΔV_{c3} decreases with the increase of V_g. We speculate that this result reflects the conditions of inversion layer near the drain edge. An increase of V_g results in the formation of the inversion layer near the drain edge. Therefore, the channel resistance in the region of ΔV_{c3} was reduced and ΔV_{c3} decreased. The reduction of ΔV_{c3} resulted in an increase of ΔV_{c1} and ΔV_{c2}. Finally, we summed up ΔV_{c1}, ΔV_{c2}, and ΔV_{c3} to obtain the quasi-Fermi potential at the drain. As the same manner, we obtained the quasi-Fermi potential at V_2 by adding ΔV_1 and ΔV_2. The quasi-Fermi potential at V_1 was equal to ΔV_{c1}. The results were the quasi-Fermi level at each terminal of the SiNW FET with four-terminal geometry. The quasi-Fermi potential obtained by our experiments is shown in **Fig. 7.6**. When V_g-V_{th} = 0.4 V, the potential drop near the drain edge was severe because the channel near the drain edge was depleted. Therefore, the applied voltage between drain and source electrodes were entirely implemented on the drain edge. On the other hand, when V_g-V_{th} = 1.4 V, all channel regions were inverted, and we observed a potential profile consistent with that of MOSFET in the strong inversion condition. It has been shown that the quasi-Fermi potential profile in the channel of the conventional planar bulk MOSFET is a quadratic function in the linear region,[14] which is consistent with the result that the potential profile is a quadratic function as shown in **Fig. 7.6 (b)**. This result suggests that the device operation of the SiNW FET with four-terminal geometry is consistent with that of the conventional planar bulk MOSFET. A possible reason is the wide SiNW channel.

Finally, the quasi-Fermi potential profile of the SiNW FET as a function of the gate voltage is shown in **Fig. 7.7**. At low drain bias voltage, the potential seems to be described by the charge-sheet model of MOSFET. At high drain bias voltage, we can

see the relaxation of pinch-off in the channel as the gate voltage increases.

When the SiNW channel near the drain edge is depleted, the terminal V_2 is also depleted, which results in a large resistance between the terminal V_2 and the channel cross-point. Therefore, we investigated whether the channel potential measured using theV_1 and V_2 terminal was accurately extracted instead of the substantial voltage drop in the branches between the channel cross-point and V_1 and V_2. Considering the channel potential profile as shown in **Fig. 7.6**, we speculate that such a voltage drop has little effect. We assume that the input impedance of the measurement apparatus is substantially higher than the resistance of the branches from the cross-point to the voltage measurement terminals V_1 and V_2. The input current from the channel cross-point to the measurement apparatus is also small so that no voltage drop occurs in the branches.

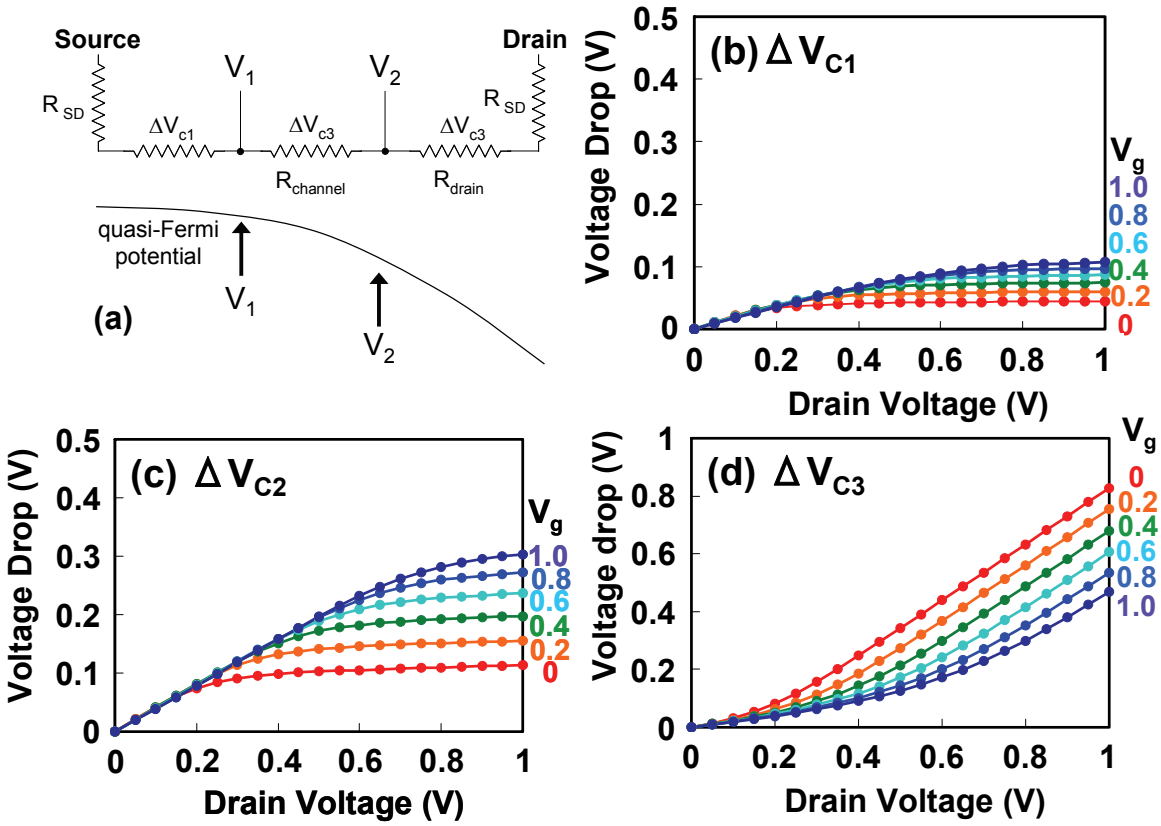


Figure 7.5 (a) Analytical model for construction of quasi-Fermi potential profile in the silicon nanowire channel. Calculated voltage differences of (b) ΔV_{c1}, (c) ΔV_{c2} and (d) ΔV_{c3} as a function of gate voltage and drain

voltage are also shown.

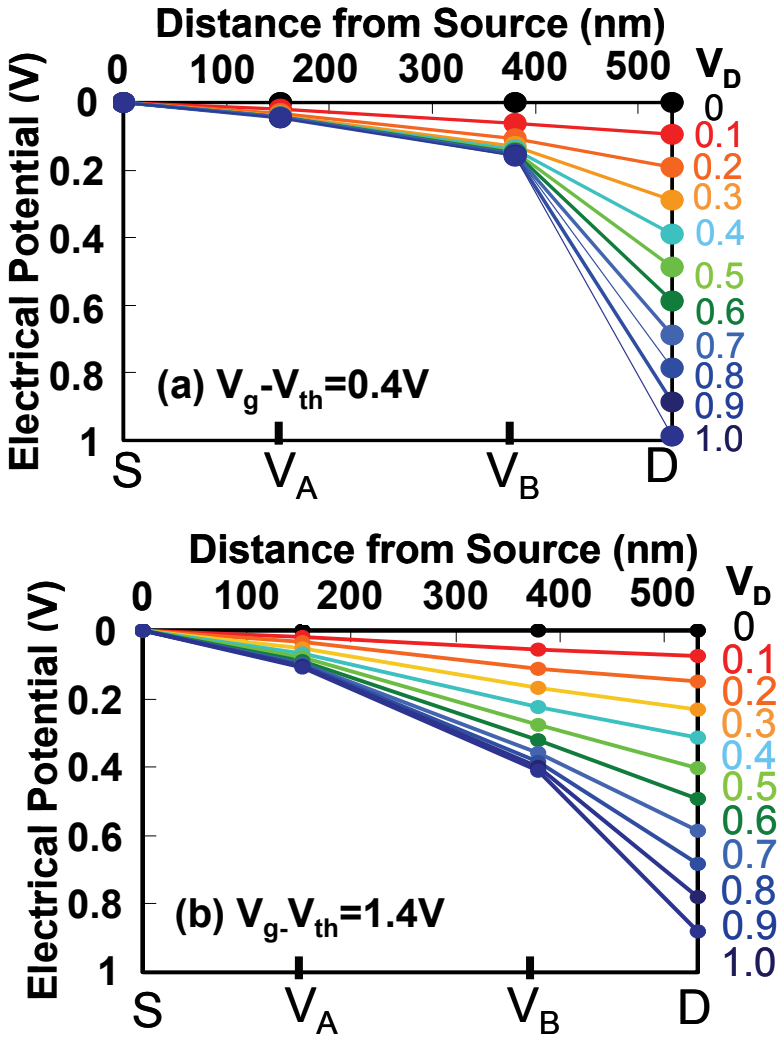


Figure 7.6 (a) Calculated quasi-Fermi potential profile at the gate overdrive voltage of 0.40 V and (b) 1.4 V as a function of the drain bias voltages. Dashed lines are quadratic function fitted to the experimental data of the quasi-Fermi potential profile.

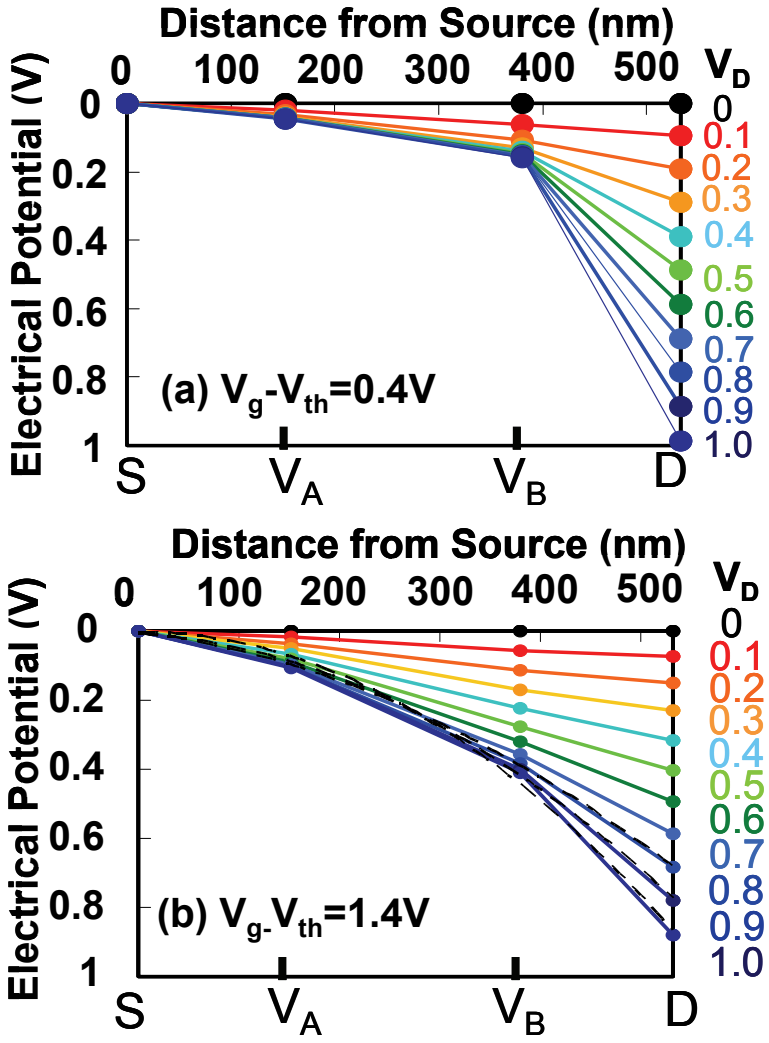


Figure 7.7 Quasi-Fermi potential profiles at (a) the drain voltage of 50 mV and (b) 1.0 V as a function of the gate voltage from -0.4 V to 1.0 V.

7.5. Conclusion

In summary, we implemented the four-terminal geometry for the evaluation of the quasi-Fermi potential profile in the channel in the SiNW FET. We believe that this structure is a promising shape for the evaluation of the quasi-Fermi potential distribution in the SiNW channel. Narrowing of channel cross-point is scope for future work. We will focus on a more accurate characterization and evaluation of narrower channels.

References

[7.1] M. S. Lundstrom, and Z. Ren: IEEE Trans. Electron Devices 49 (2002) 133.

[7.2] K. Nehari, N. Cavassilas, and F. Michelini: Appl. Phys. Lett. 90 (2007) 132112.

[7.3] S. Horiguchi, M. Nagase, K. Shiraishi, H. Kageshima, Y. Takahashi, and K. Murase: Jpn. J. Appl. Phys. 40 (2001) L29.

[7.4] M. Nakamura, N. Goto, N. Ohashi, M. Sakai and K. Kudo: Appl. Phys. Lett. 86 (2005) 122112.

[7.5] K. P. Puntambekar, P. V. Pesavento, and C. D. Frisbie: Appl. Phys. Lett. 83 (2003) 5539.

[7.6] C. Y. Nakakura, D. L. Hetherington, M. R. Shaneyfelt, and P. J. Shea: Appl. Phys. Lett. 75 (1999) 2319.

[7.7] R. N. Kleiman, M. L. O'Malley, F. H. Baumann, J. P. Garno, and G. L. Timp: J. Vac. Sci. Technol. B. 18 (2000) 2034.

[7.8] M. L. O'Malley, G. L. Timp, S. V. Moccio, J. P. Garno, and R. N. Kleiman: Appl. Phys. Lett. 74 (1999) 272.

[7.9] G. H. Buh, H. J. Chung, C. K. Kim J. H. Yi, I. T. Yoon, and Y. Kuk: Appl. Phys. Lett. 77 (2000) 106.

[7.10] R. Picciotto, H. L. Storner, L. N. Pfeiffer, K. W. Baldwin, and K. W. West: Nature. 411 (2001) 51.

[7.11] B. E. Kane, G. R. Facer, A. S. Dzurak, N. E. Lumpkin, and R. G. Clark: Appl.

Phys. Lett. 72 (1998) 3506.

[7.12] S. Sato, K. Kamimura, H. Arai, P. Ahmet, K. Ohmori, K. Yamada, and H. Iwai: Solid-State Electron. 54 (2010) 925.

[7.13] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho: IEEE Electron Device Lett. 1 (1980) 170.

[7.14] Y. Taur and T. H. Ning: Fundamentals of modern VLSI devices (Cambridge University Press, 2002) 1st ed., p. 123.

[7.15] M. D. Levenson: Jpn. J. Appl. Phys. 33 (1994) 6765.

[7.16] N. Singh, K. D. Buddharaju, S. K. Manhas, A. Agarwal, S. C. Rustagi, G. Q. Lo, N. Balasubramanian, and D. L. Kwong: IEEE Trans. Elecron Devices. 55 (2008) 3107.

Chapter 8

Conclusions

8.1. Conclusions

8.2 Perspective for future work

8.1. Conclusion of this study

In this study, the silicon nanowire (SiNW) field-effect transistors (FETs) with semi gate-around structure were successfully fabricated with conventional bulk CMOS fabrication facilities. It was shown that the SiNW FET using semi gate-around structure with high-performance can be fabricated without special process facilities, for example hydrogen annealing facility and silicon epitaxial growth facilities. The semi gate-around structure proposed in this work contributed to the successful fabrication of the SiNW FET with conventional fabrication facilities. This fact is meaningful because it suggests that research, development and fabrication of the SiNW FET can be done easily by semiconductor device fabricators or research institutes using conventional fabrication facilities.

Hydrogen annealing process or high temperature sacrificial oxidation process is necessary for fabrication of the SiNW FET with cylindrical channel cross-sections as shown in **chapter 1**. Therefore, it is easier to fabricate the SiNW FET with rectangular, triangular, and trapezoidal cross-sectional shapes as shown in **chapter 2. In chapter 3**, it was demonstrated that corners of rectangular SiNW cross-section enhanced the normalized on-current of SiNW nFETs. In **chapter 4**, device design guideline for high performance SiNW FET was proposed using effective carrier mobility and inversion charge density by split-CV technique. I believe that these guide lines are valuable because various applications can be considered for SiNW FET.

- Reduction of intrinsic delay time

  Intrinsic delay time τ is defined as

$$\tau = \frac{CV}{I} \qquad (8.1)$$

where C is the gate capacitance, V is power supply voltage, and I is saturation drain current. I is proportional to C and the effective carrier mobility. For reduction of the delay time τ, enhancement of effective carrier mobility is necessary. Therefore, SiNW nFET with rectangular cross-section is useful.

- High gate capacitance

SiNW FET with triangular cross-section has high gate capacitance although effective carrier mobility was degraded in **chapter 4**. The high gate capacitance of the SiNW FET with triangular cross-section is due to high electric field near corners. For nonvolatile memory cells, high gate capacitance is favorable. Therefore, the SiNW FET with triangular cross-section is a candidate for memory cell. High electric field near corners can be applied to writing step using gate tunneling injection.

8.2. Perspective for future work

For further investigation of SiNW FET, device fabrication process flow and mask pattern should be reconsidered.

- SiNW FET with more various channel width w_{NW} should be fabricated on the same wafer. In this work, five different channel widths can be fabricated. More detailed design is recommended.
- Fabricate separately channel mask pattern and embedded source/drain pattern so that smaller channel length can be fabricated without optical approximation effects.
- Optimization of ion-implantation conditions to source/drain electrode.
- The number of parallel channel width should be larger than 64.

Control of threshold voltage of SiNW FET is a remaining problem in this work. A candidate is use of metal gate that has proper work function. However, detailed control by metal material is difficult. Therefore, dopant introduction into SiNW channel seems to be the best solution as before. Direct implantation into SiNW channel with the diameter less than 15 nm seems to be difficult. Penetration from gate electrode or diffusion from source/drain electrode is candidates.

In this work, SiNW channel was left up by explosion of BOX layer under the SiNW channel because of sacrificial oxidation process. The lift up should induce stress to device. One way to analyze the stress is to fabricate SiNW FET with the same SOI layer thickness and different BOX layer thickness.

Parasitic source/drain resistance of <110>-directed SiNW pFET and <100>-directed

SiNW pFET was substantially different. This result suggests that diffusion of boron in the SiNW channel depends on channel orientation. For detailed analysis, SiNW FETs with various tilt angles from 0^o to 45^o are desired.

Published papers and presentations

Journal papers

[1] S. Sato, H. Kamimura, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Yamada, and H. Iwai. Electrical characterization of Si nanowire field-effect transistors with semi gate-around structure suitable for integration. Solid-State Electron. 2010;54(9):925-928.

[2] S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, and H. Iwai. Structural advantages of rectangular-like channel cross-section on electrical characteristics of silicon nanowire field-effect transistors. Microelectronics Reliability doi:10.1016/j.microrel.2010.12.007

[3] S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, and H. Iwai. Effects of corner angle of trapezoidal and triangular channel cross-sections on electrical performance of silicon nanowire field-effect transistors with semi gate-around structure. (Submitted to Solid-State Electronics)

[4] S. Sato, K. Ohmori, K. Kakushima, P. Ahmet, , K. Natori, K. Yamada, and H. Iwai. Experimental characterization of quasi-Fermi potential profile in the channel of a silicon nanowire field-effect transistor with four-terminal geometry.
Applied Physics Express 4 (2011) 044201.

[5] S. Sato, W. Li, K. Kakushima, K. Ohmori, K. Natori, K. Yamada, and H. Iwai.

Extraction of additional interfacial states of silicon nanowire field-effect transistors

(Submitted to Applied Physics Letters)

International conferences (Reviewed)

[1] S. Sato, H. Kamimura, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Yamada and H. Iwai. High-performance Si nanowire FET with a semi gate-around structure

suitable for integration. 39th European Solid-State Device Research Conference, Athens, Greece.

[2] S. Sato, Y. Lee, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada and H. Iwai. Gate semi-around Si nanowire FET fabricated by conventional CMOS process with very high drivability. 40th European Solid-State Electronic Device Research Conference, Ceville, Spain.

International Conferences (not reviewed)

[1] S. Sato, H. Arai, K. Kakushima, P. Ahmet and H. Iwai. Evaluation of Channel Potential Profile of Si Nanowire Field Effect Transistor, G-COE PICE International Symposium on Silicon Nano Devices, Oct. 2009.

[2] S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada and H. Iwai. Structural effects of channel cross-section on a gate capacitance of silicon nanowire field-effect transistors. China Semiconductor Technology International Conference 2011.

Domestic conferences

[1] S. Sato, H. Kamimura, H. Arai, K. Ohmori, K. Kakushima, P. Ahmet, T. Kazuo, T. Hattori, N. Sugii, K. Yamada and H. Iwai. Investigation of Shapes of Cylindrical Si Nanowire with Optimization of Si Fin Aspect Ratio prior to Sacrifice Oxidation. The 69th Fall meeting, 2p-CH-7, Tyubu university, 2008.

[2] S. Sato, H. Kamimura, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Tsutsui, N. Sugii, T. Hattori, K. Yamada and H. Iwai. An analysis of voltage drop within channel region with 4-point measurement TEG. The 56th Spring meeting, 1a-V-5, Tsukuba University, 2009.

[3] S. Sato, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, H. Iwai and K. Yamada. Electrical characteristics of Si nanowire FETs with various cross-sectional sizes. The 57th Spring meeting. 18p-B-11, Tokai University, 2010.

[4] **(*invited*)** S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, H. Iwai and Y. Keisaku. An analysis of effective carrier mobility of silicon nanowire FET. The 101st Research Conference, Silicon Technology Division, Japan Society of Applied Physics.

[5] S. Sato, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, H. Iwai and K. Yamada. Fabrication process and electrical characterization of Si nanowire FET. The 15th Workshop on Gate Stack Technology and Physics, the Japan Society of Applied Physics.

[6] S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, and H. Iwai. Effects of corners of channel cross-section on electrical performance of silicon nanowire field-effect transistors. The 16th Workshop on Gate Stack Technology and Physics, the Japan Society of Applied Physics.

[7] S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, and H. Iwai. Electrical characteristics of silicon nanowire field-effect transistors as a function of gate oxide thickenss. The 58th spring meeting. 25a-KC-5, Kanagawa Institute of Technology, 2011.

[8] L. Wei, S. Sato, K. Nakajima, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, and H. Iwai. Evaluation of interfacial state density from silicon nanowire field-effect transistors with subthreshold slope measured at various measurment temperatures. The 58th spring meeting. 25a-KC-6, Kanagawa Institute of Technology, 2011.

Other papers and presentations

[1] S. Sato, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai. Thermal-stability improvement of LaON thin film formed using nitrogen radicals. Microelectronic Engineering. 2007;84(9-10):1893-1897.

[2] S. Sato, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai.Thermal-stability improvement of LaON thin film formed using nitrogen radicals. Insulating Films on Semiconductor, 2007, Athens, Greece.

[3] S. Sato, K. Tachi, J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai. Effects of nitrogen incorporation into La_2O_3 using nitrogen radicals. Technical Conference on silicon device and materials, the Institute of Electronics, Information and Communication Engineers, June, 2007.

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