Doctorial Thesis

A Study on High-k / Metal Gate Stack MOSFETs with Rare Earth Oxides

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Abstract

Si-based large-scale-integrated circuits (LSIs) have progressed dramatically in the last 40 years. This progress has been attained on the basis of the downsizing of MOSFET. However, it is difficult to enhance the MOSFET performance by only shrinking its device size since 90nm technology. Especially, SiO_2 gate oxides have already reached at a few atom lengths, resulting in increase of power consumption by excess gate leakage current due to quantum mechanical tunneling effect. To solve this power crisis, high dielectric material (high-k) for gate insulator is necessary to obtain a high gate capacitance with low gate leakage. Moreover, by aggressive scaling of MOSFETs, poly-Si depletion effect can not be ignored to improve the MOSFET performance. Thus, metal gate must be also introduced with high-k gate dielectrics. Although a great deal of research has been conducting, many problems are still remained on high-k/metal gate stacks. The studies described in this thesis were investigated to realize high performance Si MOSFETs with high-k/metal gate stacks. Prospective problems were analyzed and introduced new concepts, as described in the following.

HfO_2 and its related material have been widely investigating for gate dielectrics. However, a thin SiO_2 layer is typically formed as interfacial layer to improve the electrical characteristics of MOSFETs. The scaling in equivalent oxide thickness

(EOT) is limited by the presence of SiO_2 interfacial layer. Direct contact of high-k/Si structure is indispensable for further EOT scaling. Rare earth oxides, such as La_2O_3, can achieve the direct contact of high-k/Si structure owing to La-silicate formation at La_2O_3/Si interface. One of the serious issues in high-k/metal gate stacks is degradation of effective mobility. It can be easily expected that effective mobility is reduced with high-k directly in contact of Si. Approach and strategy for improving effective mobility are described in this thesis.

Stacked HfO_2/La_2O_3/Si structure was utilized for improving effective mobility with small EOT. It was experimentally revealed that increase of EOT can be suppressed by stacked structure compared with each single layer. Moreover, amorphous form can be obtained by stacked HfO_2/La_2O_3/Si structure. It was reported that effective mobility with amorphous HfO_2 is higher compared with crystallized HfO_2. The effect of stacked HfO_2/La_2O_3/Si structure on the effective mobility was studied.

Device process approach was also investigated to improve effective mobility. It was found that the interface properties and effective mobility were remarkably improved by high temperature annealing. This study includes the analysis of the effective mobility for electron and hole by low temperature measurement.

One of the essential issues for high-k/metal gate stacks is oxygen vacancies in high-k dielectrics associated with its ionic nature. The oxygen vacancies strongly affect on the electrical characteristics of MOSFETs such as Fermi-level pinning, degraded carrier mobility and reliability. How to compensate oxygen vacancies in high-k dielectrics was studied with La-silicate dielectrics. Oxygen incorporation process was developed to compensate the oxygen deficiency. It was found that

supplied oxygen in La-silicate is preserved even after reducing process. As a results, effective hole mobility can be recovered by oxygen incorporation without EOT degradation in a controlled manner. In contrast, supplied oxygen in HfO_2 was released by forming gas annealing. The optimum devices process was proposed from the viewpoint of mobility improvement and little EOT penalty.

In order to obtain small EOT with low interface state density, selection of metal gate materials and its structure was investigated. In this study, Metal Inserted Poly-Si (MIPS) stack structure was utilized to prevent the excess oxygen incorporation during high temperature annealing process. EOT of 0.69nm was attained with close to the ideal C-V characteristics. Oxygen incorporation was also demonstrated after Si removal. The V_{FB} shift by 490mV to positive direction was attained with EOT increase below 1Å.

Impact of MIPS structure on effective electron mobility was examined. Electron mobility of 155 cm^2/Vsec at 1MV/cm was achieved with 0.71nm in EOT. This result is comparable to electron mobility with HfO_2 reported by IBM group. Gate leakage current was also extremely suppressed. High electron mobility and low gate leakage current may be due to amorphous structure of La-silicate observed by TEM images. Device process technology for high electron mobility with direct contact of high-k/Si structure was proposed and developed.

Contents

Chapter 1 Introduction

1.1 Background

Si-based large-scale-integrated circuits (LSIs) have developed rapidly in the last forty years. The Complementary Metal Oxide Semiconductor (CMOS) Field Effect Transistor (FET) is the most important electronic device. The recent dramatic advances in information technology (mobile PC, cell- phone, Internet, etc.) owe to high speed, small, and low power consumption. Electronics and information technology based on Si-LSIs has been improved quality of life more freely and comfortably. Si-LSIs are greatly contributed to the development of civilization and indispensable in modern society. The MOSFET forms the basis of LSIs. Figure 1.1 shows the schematic illustration of the MOSFET [1.1]. MOSFET has one capacitance and two PN diodes. MOSFET is basically constructed by Si-based materials. Silicon dioxide (SiO_2) is utilized as gate

insulator. Poly-Si is used as gate electrode. Therefore, MOSFET consists of simple structures and materials. MOSFET are working as fundamental switches to perform logic operation in LSIs. MOSFET is dominant logic device in solid state electronic devices.

The progress of LSIs has been accomplished with the downsizing of transistors. It is called as "Scaling". The scaling rule of MOSFET was published by R. Dennard [1.2]. Figure 1.2 shows the principle of scaling rule. According to this rule, the device dimension and supply voltage of MOSFET should be reduced by the same factor α. The doping concentration should be increased by the same factor α. As a result, the electric field in MOSFET remains constant despite the technology node. Moreover, the circuit speeds up by the same factor α. Power dissipation per circuit is reduced by α^2. It notes that the device feature size decreases each year and the number of transistors on a LSI doubled every two years. This empirical law is called as "Moore's Law". The International Technology Roadmap for Semiconductor (ITRS) [1.3] defines how the device parameters are scaled for the next technology node.

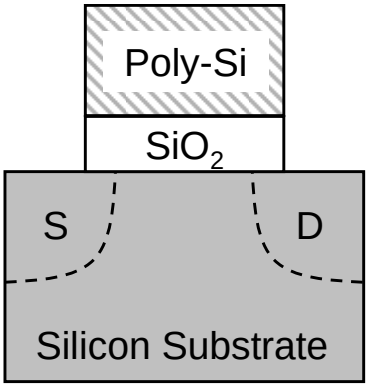


Figure 1.1 *Schematic illustration of MOSFET.*

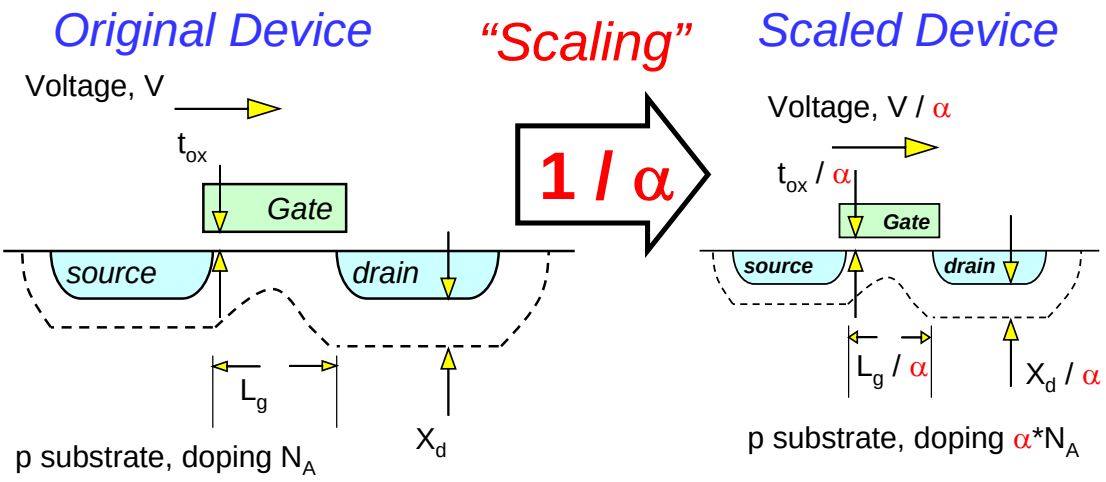


Figure 1.2 *Principle of scaling rule.*

Figure 1.3 shows the scaling trend of MOSFET [1.4]. Feature size of MOSFET becomes smaller, smaller and smaller. MOSFET count per CPU increased higher, higher and higher. Moreover, cost per MOSFET decreased by half every two years in accordance with the Moore's Law. Although CMOS is not fastest devices in solid state devices [1.5], CMOS is easy for integration because of planar device. Thus, CMOS has the highest integration level. Billions of CMOS transistors are integrated on a single chip.

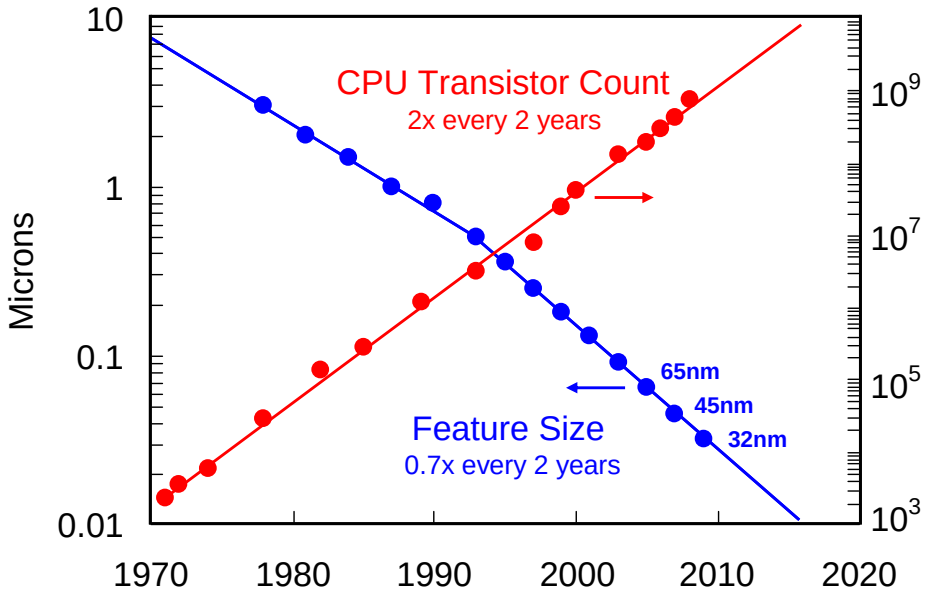


Figure 1.3 *Scaling trend of MOSFET.*

The performance of MOSFET is measured in terms of drain current or On current. The drain current in MOSFET at saturation region, I_{dsat}, can be written as [1.1]

$$I_{dsat} = \frac{W}{2L}\mu_{eff}\frac{A\varepsilon_{ox}\varepsilon_o}{T_{ox}}\left(V_g - V_{th}\right)^2 \qquad \text{.....} \quad (1.1)$$

where W is the gate width, L is the gate length, μ_{eff} is the effective mobility, ε_{ox} is the oxide permittivity, ε_o is the vacuum permittivity, V_g is the gate voltage, V_{th} is the threshold voltage. From the Eq. (1.1), scaling the oxide thickness and the gate length has been resulted in higher drain current. Thus, the scaling of transistors is important both for high-speed operation and for high integration of LSIs. High performance and low cost can be achieved by scaling simultaneously.

However, MOSFET performance has not been improved by only shrinking its feature size because of various tradeoff problems since 90nm node technology. Figure 1.4

shows the CMOS scaling trend [1.6]. Recently, it is difficult to enhance the MOSFET performance by device feature scaling. New materials and new structures in MOSFET have been introduced to improve the performance. It is called as “Equivalent Scaling”. Device structure and fabrication process has been more complicated.

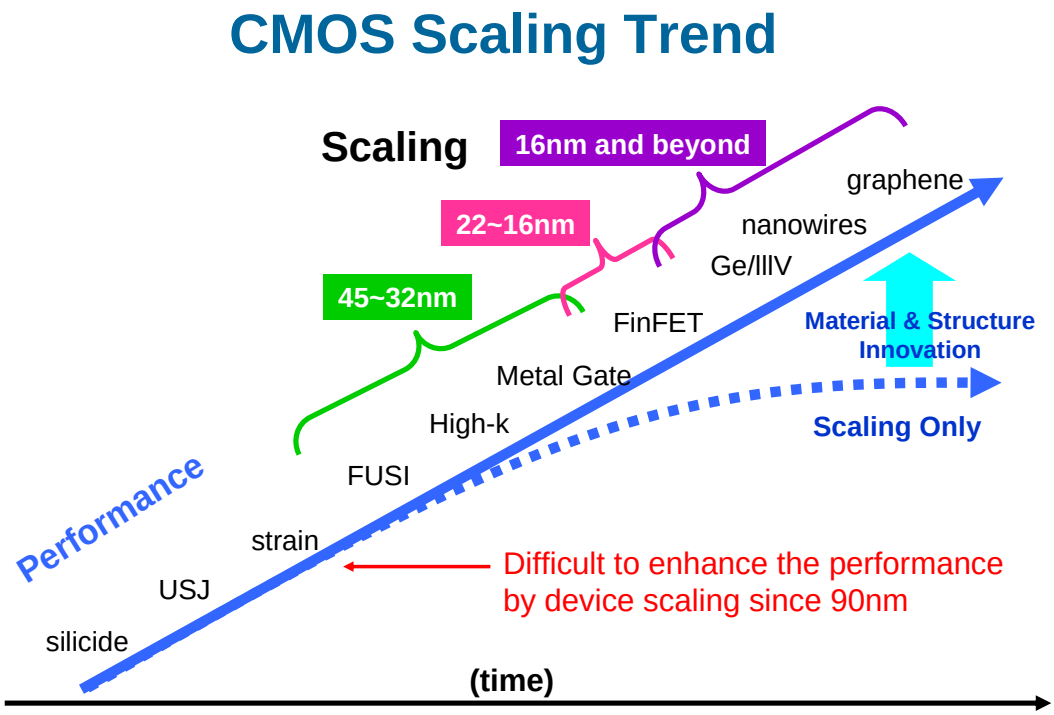


Figure 1.4 *CMOS scaling trend.*

According to Moore’s Law, the transistor has been shrunk to get higher performance and reduce the costs. Most concern issue is gate oxides. The gate oxide, which separates the gate electrode from the substrate, is the most important part of MOSFETs. As previously mentioned, Silicon dioxide (SiO_2) has been used as ideal gate dielectrics for forty years because SiO_2 is compatible with silicon substrate, namely low interface state density, good thermal stability, etc. Silicon dioxide (SiO_2) is usually formed by thermal

oxidation of silicon substrate. SiO_2 has successfully scaled so far. As a result, SiO_2 physical thickness becomes thinner until 1.2nm. It means a thickness of a few atomic layers. Figure 1.5 shows the TEM images of SiO_2 gate oxides [1.7]. Since the thickness of SiO_2 is under 1.5nm, gate leakage current due to direct tunneling of electron through the SiO_2 becomes too high, exceeding $1A/cm^2$ at 1V [1.8]. As a result, power consumption increases unacceptable level. Figure 1.6 shows the Power Density as a function of gate length [1.9]. The passive power is comparable to the active power. The power consumption due to gate leakage current is remarkably increased. LSIs confront the power crisis. Something must be considered to solve this power crisis of LSIs. In principle, SiO_2 can no longer be utilized as gate insulator due to excess gate leakage current.

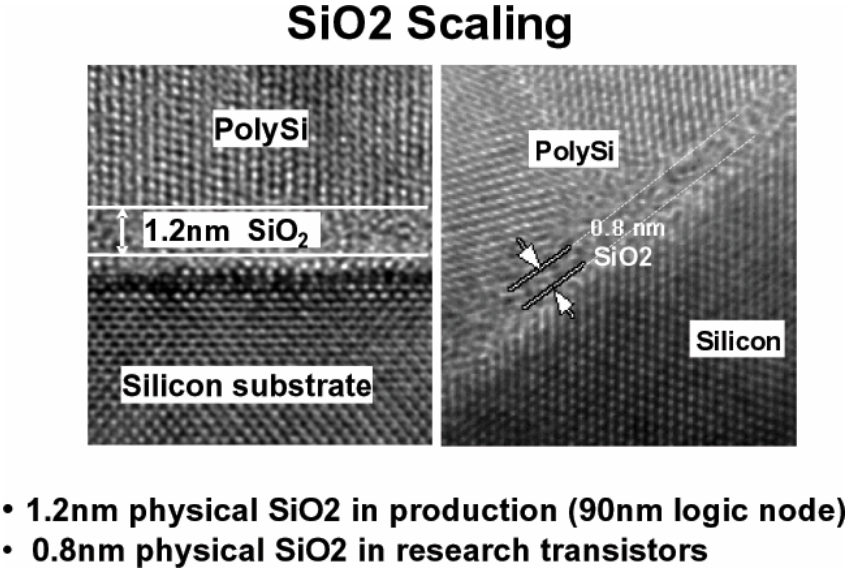


Figure 1.5 *TEM images of SiO_2 gate oxides.*

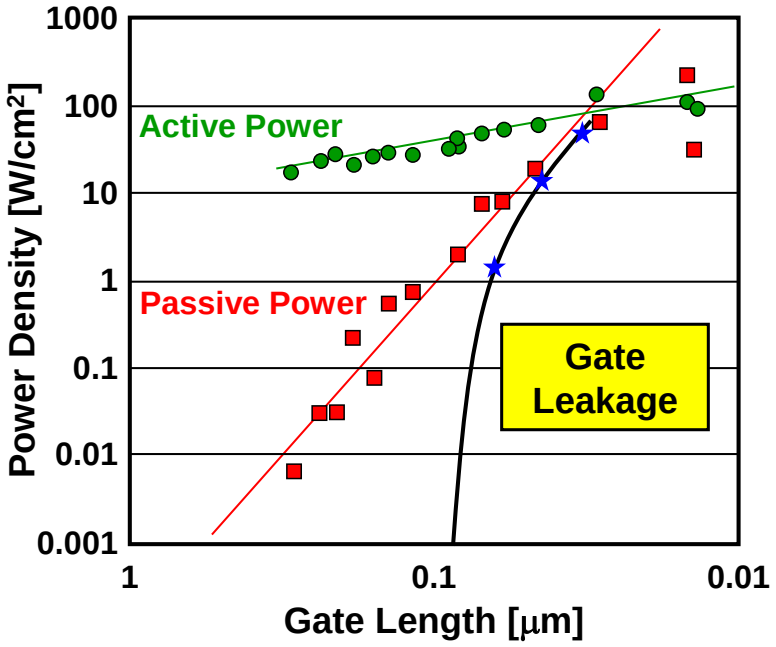


Figure 1.6 *Power Density as a function of gate length.*

It is often said that the reason for success of MOSFET is not the silicon crystalline material but silicon dioxides (SiO_2). It is also said that interface properties of SiO_2/Si is excellent. However, high dielectric constant material (high-k) must be introduced as gate dielectrics to suppress the excess leakage current. By using high-k materials as gate dielectrics, large gate capacitance can be obtained with low gate leakage current at the same time. The guideline for selecting an alternative gate dielectrics materials are high dielectric constant, large band gap and high band offset to silicon, thermodynamic stability, interface quality, process compatibility, and reliability. Relationship between physical thickness of SiO_2 and high-k gate oxide obtained by same gate capacitance value (C) is written as

$$C = \frac{\varepsilon_o \varepsilon_{SiO_2}}{T_{SiO_2}} = \frac{\varepsilon_o \varepsilon_{High-k}}{T_{High-k}} \qquad \text{.....} \quad (1.2)$$

where ε_o is the vacuum permittivity, ε_{SiO2} is the dielectric constant of SiO_2 (=3.9), $\varepsilon_{High\text{-}k}$ is the dielectric constant of high-k materials, $T_{High\text{-}k}$ is the physical thickness of high-k gate oxide. EOT (Equivalent-Oxide-Thickness) is expressed as,

$$T_{EOT} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{High-k}} T_{High-k} \qquad \text{.....} \quad (1.3)$$

where $T_{High\text{-}k}$ is the physical thickness of high-k gate oxide.

Therefore, gate leakage currents are reduced by using the high-k materials as a gate dielectric while maintaining a small equivalent oxide thickness (EOT). Figure 1.7 shows the schematic illustration for replacement of Poly-Si/SiO_2 with high-k/metal gate. To improve the MOSFET performance, metal gate is also required by the replacement of Poly-Si gate.

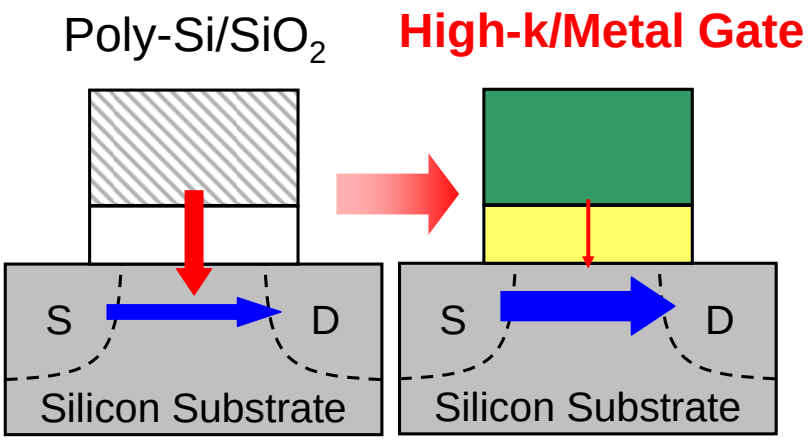


Figure 1.7 *Replacement of Poly-Si/SiO_2 with high-k/metal gate.*

As previously mentioned, the real magic in silicon technology is not silicon material but SiO_2 gate oxides. Poly-Si is also revolutionary technology in terms of fabrication

process. However, Poly-Si is not the metal but the semiconductor. Effect of depletion in Poly-Si on MOSFET performance can not be ignored with device downsizing. Poly-Si depletion layer corresponds to about 0.3nm in EOT. Figure 1.8 shows the comparison of total gate capacitance in gate stacks.

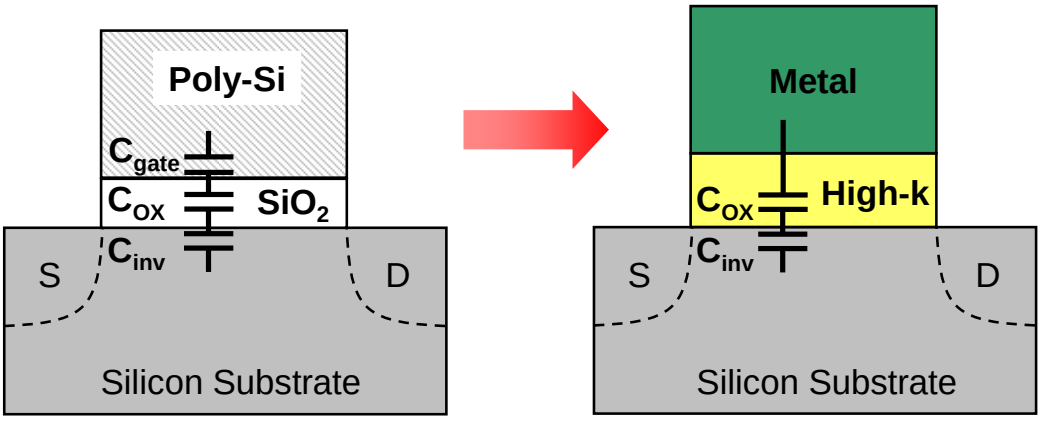


Figure 1.8 *Comparison of total gate capacitance in gate stacks.*

Total gate capacitance, C_{total} can be written as,

$$\frac{1}{C_{total}} = \frac{1}{C_{gate}} + \frac{1}{C_{ox}} + \frac{1}{C_{inv}} \qquad \text{.....} \quad (1.4)$$

where C_{gate} is the capacitance of gate depletion layer, C_{ox} is the capacitance of gate oxides and C_{inv} is the capacitance of inversion layer. In an inversion layer of a MOSFET, carriers are confined in a potential well very close to the silicon surface [1.1]. The well is formed by the oxide barrier and the silicon conduction band if the carrier is electron. Because of confinement of motion in the direction normal to the surface, inversion layer electrons have a peak distribution 10-20 Å away from the surface. It corresponds to the the capacitance of the inversion layer, C_{inv}.

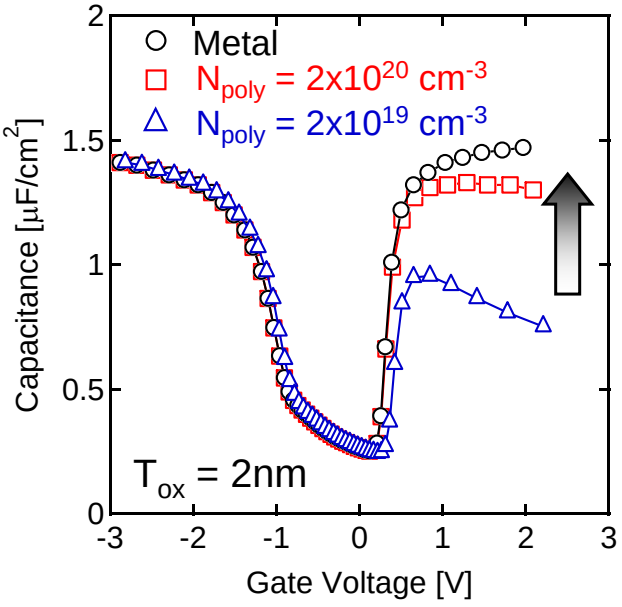


Figure 1.9 *Effect of Poly-Si depletion on C-V characteristics.*

It is well known that capacitance with series connection reduce the total capacitance. Figure 1.9 shows the calculation results for effect of Poly-Si depletion on C-V characteristics. Since the inversion layer capacitance is intrinsic component in total gate capacitance, it can not be eliminated. On the other hand, total gate capacitance can be increased by utilizing metal gate substitute for Poly-Si gate. Thus, metal gate is necessary to eliminate Poly-Si depletion.

For selection of high-k material, relationship between dielectric constant and band offset must be considered. Excess high dielectric constant is undesirable because there is the tradeoff relationship between dielectric constant and band offset. Figure 1.10 shows the relationship between dielectric constant and band offset for candidate high-k gate dielectrics [1.10].

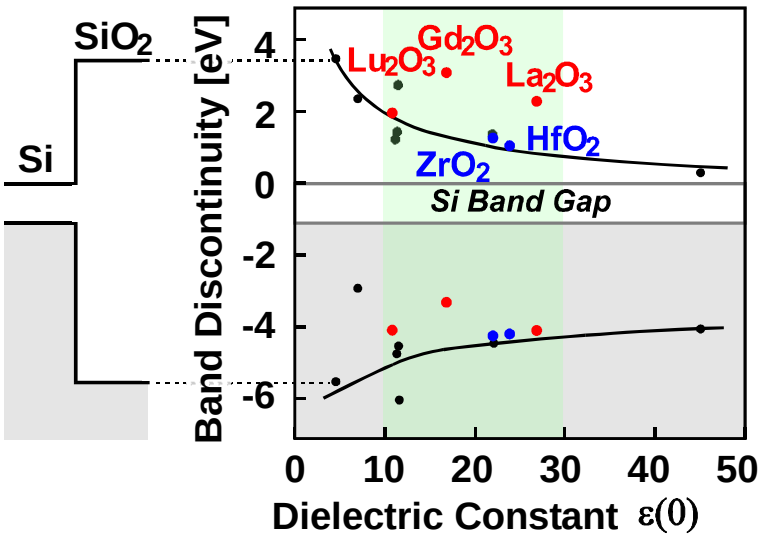


Figure 1.10 *Dielectric constant versus band offset for candidate high-k gate dielectrics.*

Hf-based oxides have been widely investigated for gate insulator application because of its high dielectric constant and large band offset. Selection of metal material is extremely important. Figure 1.11 shows the work functions of various metal materials for metal gate. In the case of Poly-Si gate, Fermi level corresponds to the work function. Fermi level of Poly-Si can be modulated by ion implantation technique. This is great advantage for threshold voltage adjustment. On the other hand, work function of metal is basically intrinsic material properties. Thus, appropriate metal materials must be selected for n- and p-MOSFET. Moreover, integration of metal in MOSFET process is one of the serious issues. Poly-Si has excellent thermal stability and process compatibility. By considering not only the work function but also process integration, window for metal selection becomes narrower. TiN metal have been widely utilized as metal gate because of its high thermal stability [1.11]. Thus, high-k/metal gate has been

converged on the Hf-based oxides and TiN metal gate, respectively. However, there are still many issues remained to be solved in high-k/metal gate system.

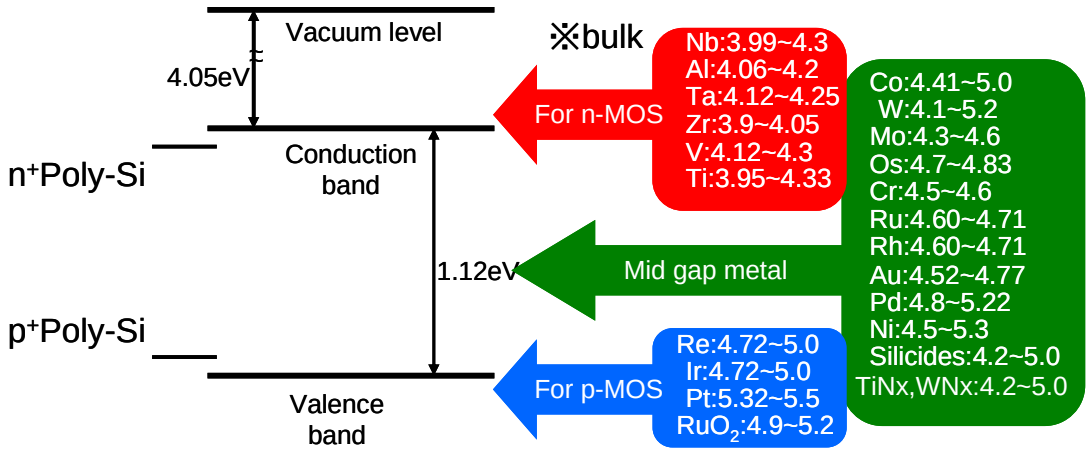


Figure 1.11 *Work functions of various metal materials.*

Next, the importance of EOT scaling with high-k/metal gate stacks is described. As previously mentioned, excess gate leakage current due to direct tunneling can be suppressed by high-k dielectrics with maintaining large gate capacitance. EOT scaling with high-k/metal gate is also effective to suppress the Drain Induced Barrier Lowering (DIBL) and Short-Channel Effect (SCE). Figure 1.12 shows the relationship between DIBL and gate length [1.12]. DIBL can be lowered with high-k/metal gate compared with Poly-Si/SiON. This is not surprising experimental results.

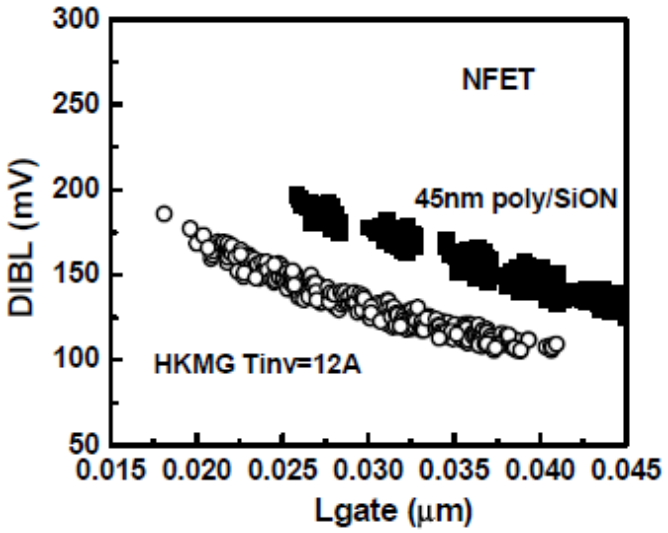


Figure 1.12 *Relationship between DIBL and gate length.*

DIBL and SCE can be expressed as [1.13],

$$DIBL = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{X_j^2}{L_{el}^2}\right)\frac{T_{ox}T_{dep}}{L_{el}^2}V_{ds} \qquad \text{.....} \quad (1.5)$$

$$SCE = 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{X_j^2}{L_{el}^2}\right)\frac{T_{ox}T_{dep}}{L_{el}^2}\Phi_d \qquad \text{.....} \quad (1.6)$$

where ε_{Si} is the permittivity of silicon, ε_{ox} is the permittivity of oxide, X_j is the junction depth, L_{el} is the gate length, T_{ox} is the oxide thickness, T_{dep} is the depletion layer thickness, V_{ds} is the source-drain voltage and Φ_d is the supplied voltage. DIBL and SCE are proportional to the oxide thickness. Hence, DIBL and SCE can be suppressed by EOT scaling with high-k/metal gate.

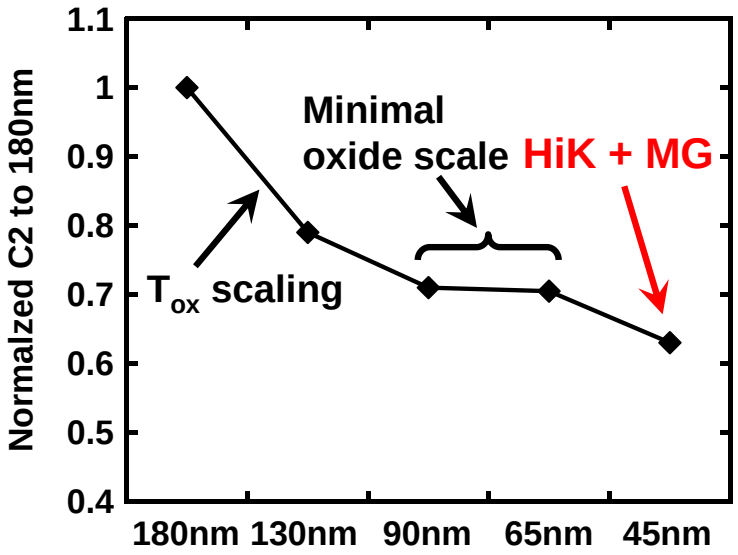


Figure 1.13 *Suppression of random threshold voltage variation by oxide scaling.*

EOT scaling with high-k/metal gate is also effective to suppress the random threshold voltage variation. Figure 1.13 shows the suppression of random threshold voltage variation by oxide scaling [1.14]. Random threshold voltage variation can be expressed as [1.14],

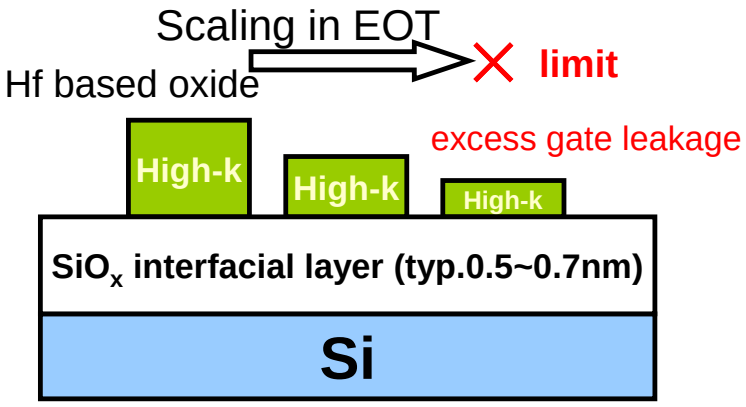
$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3 \varepsilon_{Si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{L_{eff} \cdot W_{eff}}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{L_{eff} \cdot W_{eff}}} \right) \quad \text{.....} \quad (1.7)$$

where q is the elemental charge, ε_{Si} is the permittivity of silicon, ϕ_B is the bulk Fermi energy, T_{ox} is the oxide thickness, ε_{ox} is the permittivity of oxide, N is the channel doping concentration, L_{eff} is the effective gate length, W_{eff} is the effective gate width and c_2 is mismatch coefficient. Lowering mismatch coefficient represents the small threshold voltage variation. From the Eq. (1.7), scaling the EOT directly leads to suppression of random threshold voltage variation. Short-Channel Effect and threshold

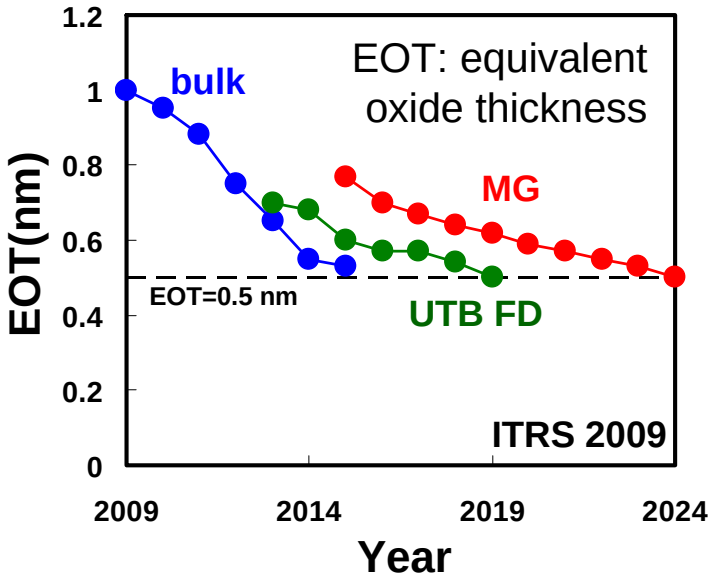
voltage variation has been becoming severe problems in state-of-the-art MOSFETs [1.13]. Therefore, EOT scaling with high-k/metal gate is crucially important to suppress not only gate leakage current but also severe short-channel effect and random threshold voltage variation.

1.2 Problems to be Solved in High-k/Metal Gate System

As previously explained, high-k/metal gate stack is necessary for reduction of gate leakage current, short-channel effect and random threshold voltage variation. However, serious problems are still remained to be solved. In the case of Hf-based oxides, SiO_2 interfacial layer was formed prior to formation of Hf-based oxides to recover the electrical characteristics [1.11]. Mobility reduction and poor reliability is still serious problems in high-k/metal gate stacks [1.15, 1.16]. Figure 1.14 (a) shows the schematic illustration of scaling limit in EOT. Figure 1.14 (b) shows the EOT requirement as a function of year [1.3]. EOT less than 0.8nm can not be achieved with SiO_2 interfacial layer. Therefore, direct contact of high-k/Si structure must be realized for further EOT scaling.



(a)



(b)

Figure 1.14 (a) *Limit of EOT scaling and* ***(b)*** *EOT requirement of ITRS 2009.*

First of all, selection of high-k materials for direct contact of high-k/Si structure is extremely important. In previous study [1.17], it has been reported that a direct contact structure can achieved using rare earth such as La_2O_3 for gate dielectrics owing to the

material nature to form La-silicate at the interface. nMOSFET operation has been demonstrated with scaled EOT [1.18]. Figure 1.15 TEM images of La_2O_3 gate dielectrics. Dielectric constant of La-silicate is two or three times larger than that of SiO_2. Thus, direct contact structure can be easily achieved with La_2O_3 as gate dielectrics.

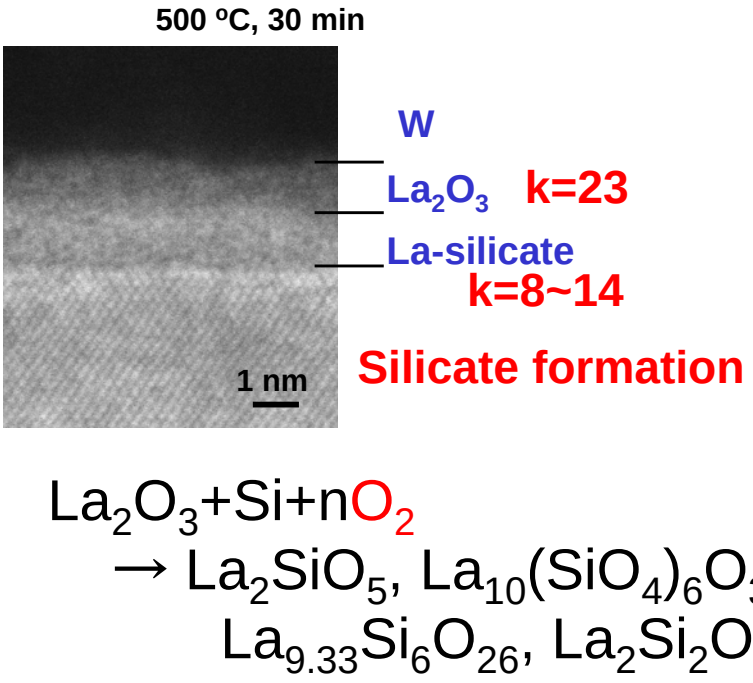
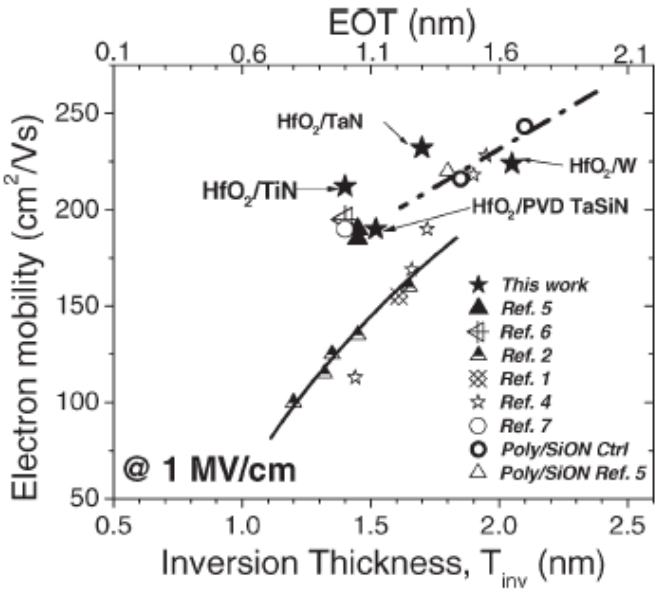


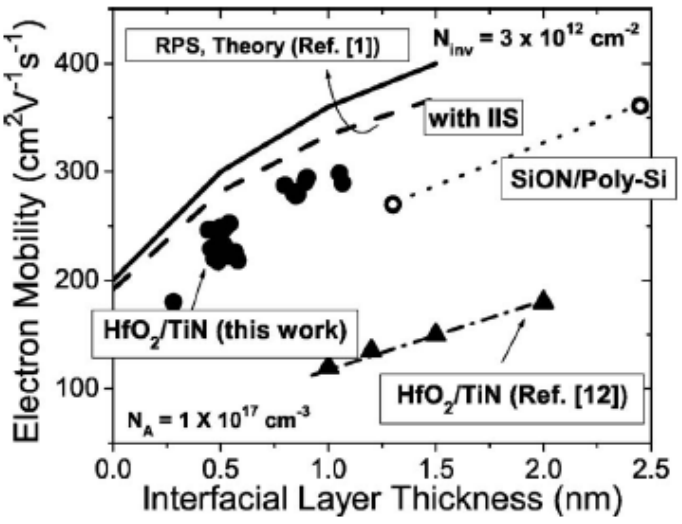
Figure 1.15 *TEM images of La_2O_3 gate dielectrics.*

Reduced mobility in MOSFETs is one of the severe problems for high-k/metal gate stacks. It was reported that several scattering sources have been responsible for mobility reduction [1.19]. As previously mentioned, SiO_2 interfacial layer is inserted between high-k and Si substrate to improve the effective mobility owing to excellent interface properties at SiO_2/Si interface. Moreover, several scattering sources are physically

distant from inversion channel layer. Many experimental reports have revealed that effective mobility is absolutely degraded with decreasing EOT. Figure 1.16 shows the effective mobility as a function of inversion thickness (or interfacial layer thickness) [1.20, 1.21]. Although several models to explain the mobility degradation have been proposed, cause of reduced mobility is still unclear. Moreover, there are few reports how to improve the effective mobility in spite of its importance. It is easy expected that effective mobility will be severely degraded with direct contact of high-k/Si structures. The solutions to improving effective mobility should be developed.



(a)



(b)

Figure 1.16 *Electron mobility as a function of* ***(a)*** *inversion thickness and* ***(b)*** *interfacial layer thickness.*

1.3 Purpose of This Study

The studies discussed in this thesis were conducted for the purposes of investigating the above problems related to the EOT scaling. The solutions to effective mobility improvement are studied and thereby contributing to the realization of scaled MOSFET with direct contact of high-k/Si structure.

The purpose of this thesis is to study the device and process technology for improving the effective mobility in direct contact of high-k/Si structure with La_2O_3 gate dielectrics. Figure 1.17 shows the possible sources for reduced mobility in high-k gate stacks based on previous reports [1.19]. Coulomb and roughness scattering can be

avoided by material and process technology. Moreover, the method induce to increment of EOT should be avoided. The concern issues for improving mobility are follows.

Improving interface properties at high-k/Si interface is critical issue. How to control the interface properties is one of the important factors. Fixed charges in high-k dielectrics is also important. It induces not only mobility degradation but also threshold voltage instability. Improving effective mobility corresponds to improve the quality of gate stacks. There are few reports on improving mobility except for mobility boosting technology such as strain [1.22] or hybrid orientation [1.23]. Improving the effective mobility is challenge to be addressed.

Figure 1.18 shows the contents of this thesis. This thesis is consisted of 8 parts.

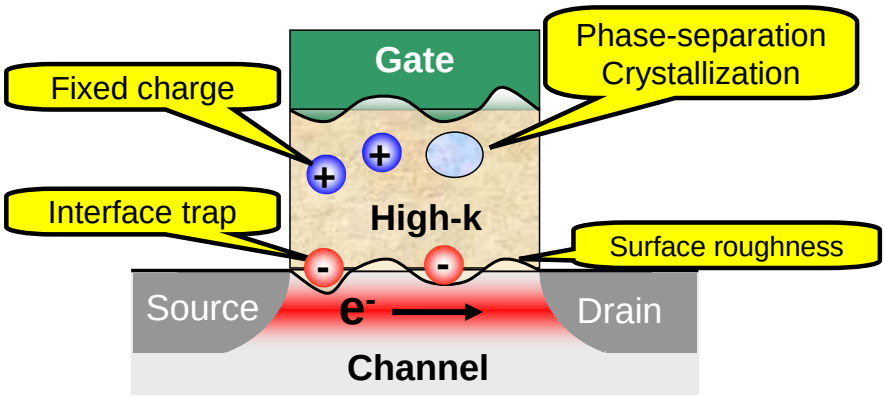


Figure 1.17 *Possible sources for reduced mobility in high-k gate stacks.*

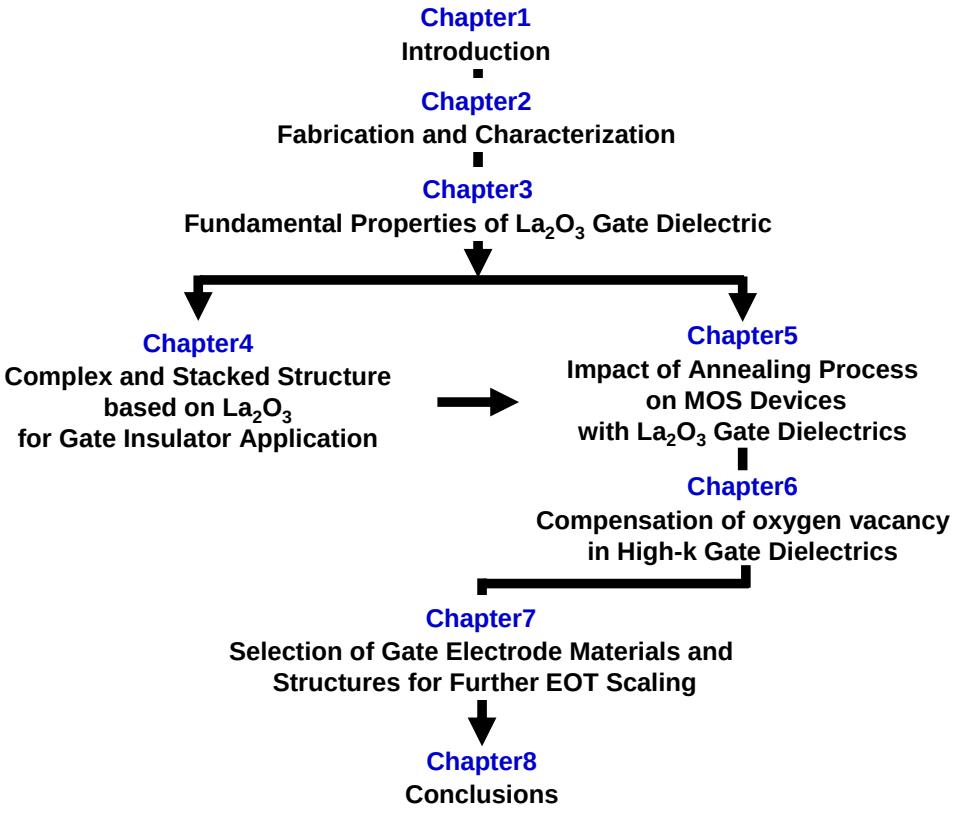


Figure 1.18 *Contents of this thesis.*

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Chapter 2 Fabrication and Characterization

2.1 Fabrication Procedure

Figure 2.1 shows the basic device fabrication flow of MOS devices with high-k gate dielectrics in this study. The high-k gate dielectrics MOS capacitors were fabricated on n-type (100)-oriented Si substrate. The substrate impurity concentration of MOS capacitors is $3x10^{15}$ cm^{-3}. To determine the capacitor area, 400nm thermal oxide was formed and patterned by photolithography. After the substrates were cleaned with H_2SO_4/H_2O_2 mixture at 100^oC for 5min to remove resist-related organic contamination, diluted HF treatment was performed. The high-k thin films were deposited on the substrate using e-beam evaporation at 300^oC in ultra-high vacuum chamber 10^{-7} Pa as shown in Figure 2.2. Tungsten (W) gate electrodes were formed by RF sputtering without breaking the ultra-high vacuum to avoid absorption of moisture from the air.

The gate electrode was patterned by lithography and formed by RIE. Source and Drain pre-formed Si (100) substrates were also utilized to fabricate MOSFETs. The substrate impurity concentration of MOSFETs is $3x10^{16}$ cm^{-3}. Post-Metallization annealing (PMA) was performed. An Al films were evaporated on the source/drain region and back side of the substrate of the substrate as a contact for electrical measurement. Equivalent oxide thickness (EOT) and flatband voltage (V_{FB}) were extracted by NCSU CVC program [2.2].

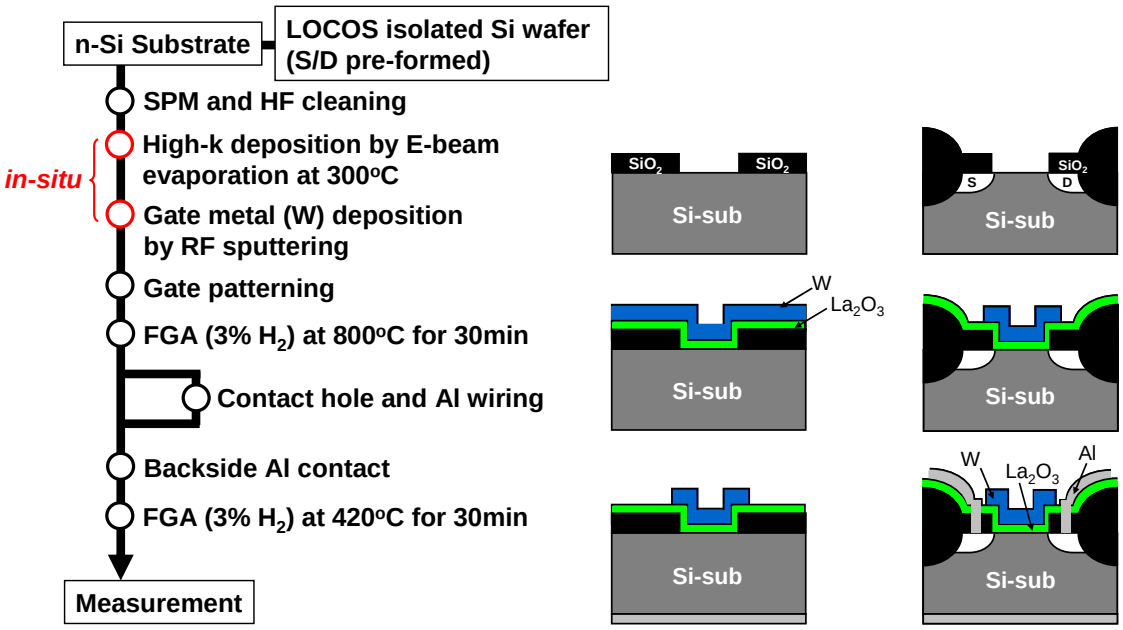

Fig. 2.1 *Fabrication procedure for MOS devices.*

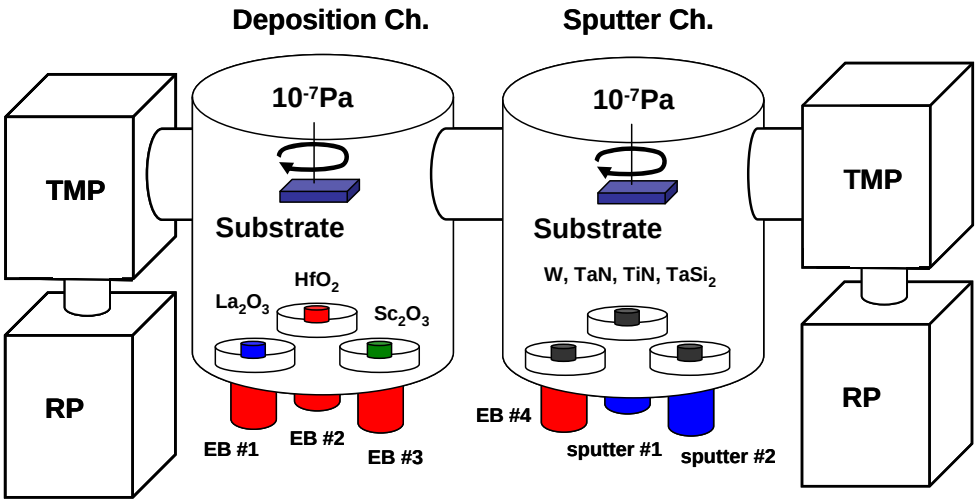

Fig. 2.2 *Schematic illustration of e-beam evaporation and RF sputtering system.*

2.2 Characterization of MOSFETs

As the MOSFET is the fundamental switching devices in the LSI circuits, the threshold voltage V_{th} is an important parameter of the MOSFET. The threshold voltage can be determined by plotting I_{ds} versus V_g at low drain voltage, typically 50-100mV, as shown in Figure 2.3. The extrapolated intercept of the linear portion of the I_{ds} versus V_g curve with the V_g –axis gives the V_g value. It needs to regard the point of slope because the threshold voltage varies the point of I_{ds} - V_g slope. It is commonly used the point of slope on the I_{ds} - V_g curve by a maximum in the transconductance, fit a straight line to the I_{ds} - V_g curve at that point and extrapolate to I_{ds} = 0, as shown in Figure 2.3. In this study, the threshold voltage is extracted by linear extrapolation method [2.1].

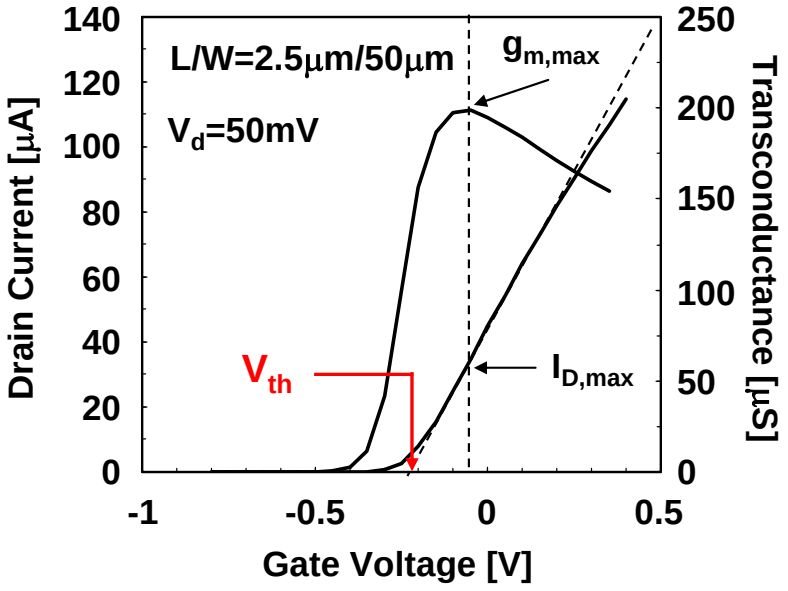

Fig. 2.3 *Threshold voltage determination by the linear extrapolation technique.*

As shown in Figure 2.3, the drain current rapidly approach to zero below the threshold voltage on a linear scale. On a logarithmic scale, however, the drain current remains nonnegligible level even below the V_{th}. This is because the inversion charge abruptly does not to drop zero. The slope is usually expressed as the subthreshold slope *S.S.* in Figure 2.4. This value is that gate voltage necessary to change the drain current by one decade, and given by

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \quad \text{.....} \quad (2.1)$$

where k is a Boltzmann's constant, T is temperature, q is a electronic charge, C_{dm} is a depletion-layer capacitance. If the interface trap density is high, the subthreshold slope may be graded. Because the capacitance attributed to the interface trap is in parallel

with the depletion-layer capacitance [2.1].

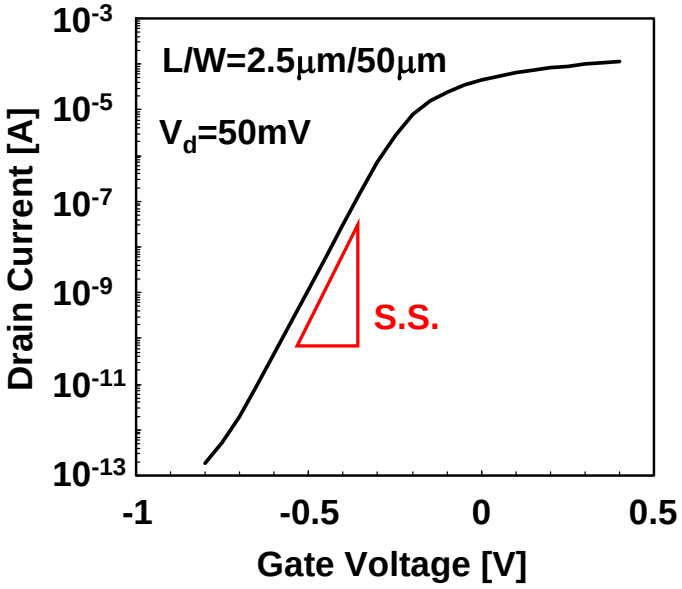

Fig. 2.4 *Typical MOSFET I_d-V_g characteristics on logarithmic scale.*

The effective inversion layer mobility in MOSFET is a very important parameter for device analysis, design and characteristics. Since the effective inversion mobility shows sensitivity to device properties or interface properties, it can be also used to probe the properties of high-k gate dielectrics.

The effective mobility, μ_{eff}, is defined in terms of the measurement of drain current, I_d, of the MOSFET at low drain voltage, V_d, in the linear region as [2.3]

$$\mu_{eff} = \frac{L}{W} \cdot \frac{I_d}{V_d} \cdot \frac{1}{Q_{inv}} = \frac{L}{W} \cdot g_d \cdot \frac{1}{Q_{inv}} \qquad \text{.....} \quad (2.2)$$

where $g_d = I_d/V_d$ is the channel conductance, Q_{inv} is the inversion layer charge. The channel conductance is calculated from differential I_d-V_g measurements at 20mV and

40mV as shown in Figure 2.5 to compensate the degradation of the channel conductance due to leakage current. Thus, the effective mobility is given by

$$\mu_{eff} = \frac{L}{W} \cdot \frac{\left(I_{d\,40mV} - I_{d\,20mV}\right)}{20mV} \cdot \frac{1}{Q_{inv}} \qquad \text{.....} \quad (2.3)$$

In this study, the effective mobility is calculated by Eq. (2.3).

For accurate extraction of effective mobility, accurate value of Q_{inv} must be used in Eq. (2.3). A Split C-V measurement is one of the extraction techniques for inversion layer charge accurately. Figure 2.6 represents the Split C-V measurement arrangement [2.1]. The inversion layer charge is obtained from the voltage integral of a gate-channel capacitance as shown in Figure 2.7. The inversion layer charge Q_{inv} can be written as

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc}\left(V_g\right) dV_g \qquad \text{.....} \quad (2.4)$$

where C_{gc} is the gate-to-channel capacitance. Similarly, the depletion layer charge Q_b is also obtained due to integrate the gate-body capacitance, C_{gb}, from flatband voltage toward the inversion as shown in Figure 2.8.

$$Q_b = \int_{V_{FB}}^{V_g} C_{gb}\left(V_g\right) dV_g \qquad \text{.....} \quad (2.5)$$

The effective electric field E_{eff} can be expressed as [2.4]

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(\eta Q_{inv} + Q_b\right) \qquad \text{.....} \quad (2.6)$$

where η are 1/2 for electrons and 1/3 for holes.

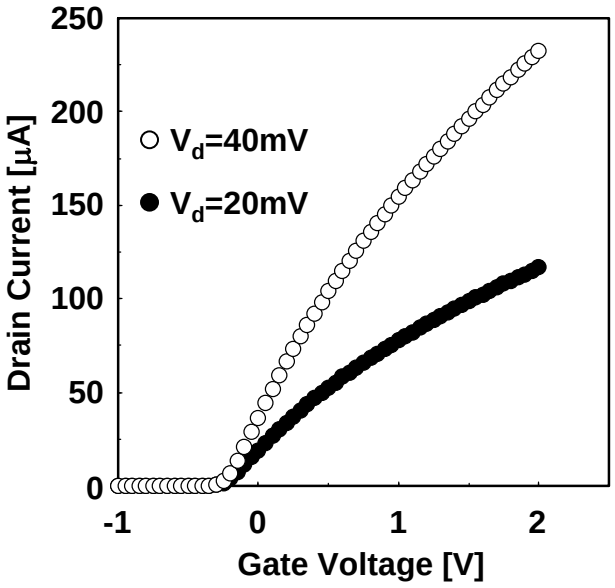

Fig. 2.5 *I_d-V_g measurements at 20mV and 40mV.*

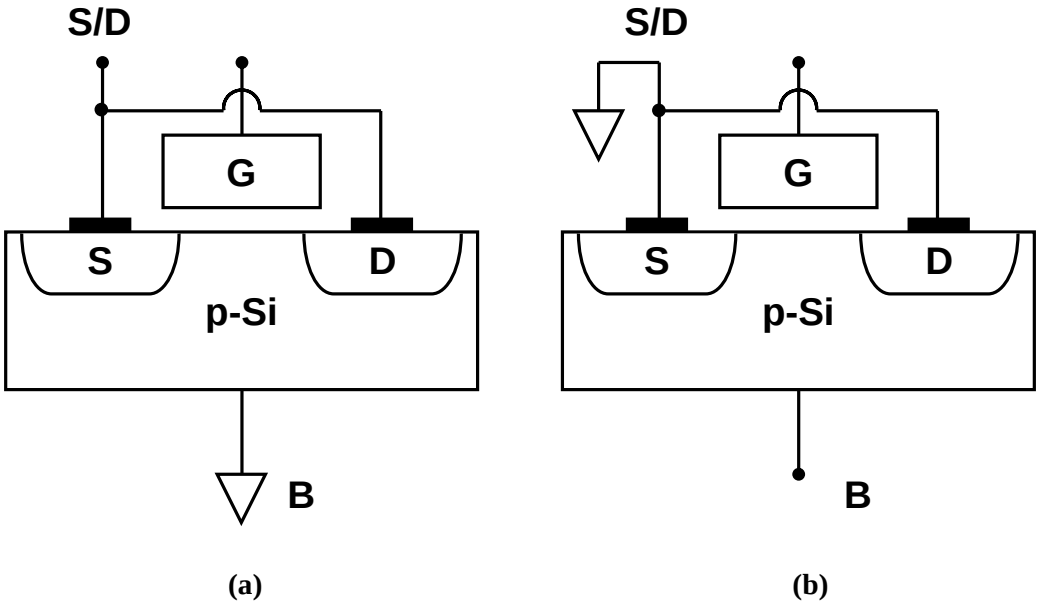

Fig. 2.6 *Configuration for **(a)** gate-to-channel and **(b)** gate-to-body capacitance measurements.*

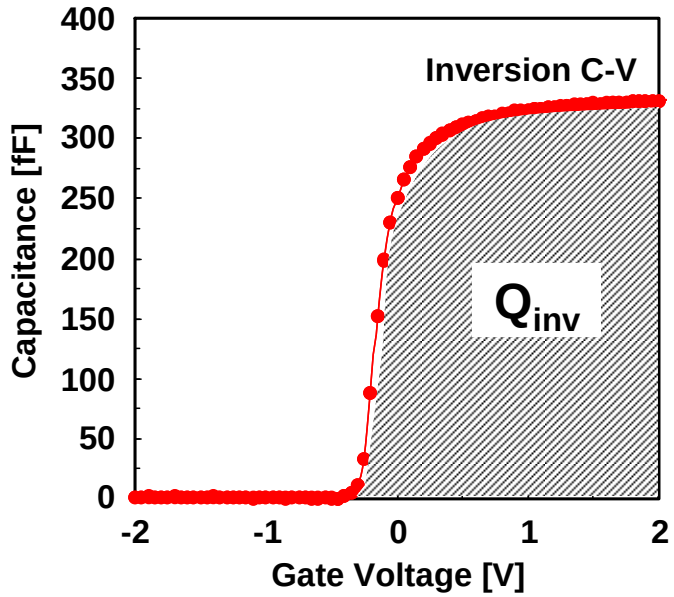

Fig. 2.7 *Gate-to-channel capacitance of nMOSFET.*

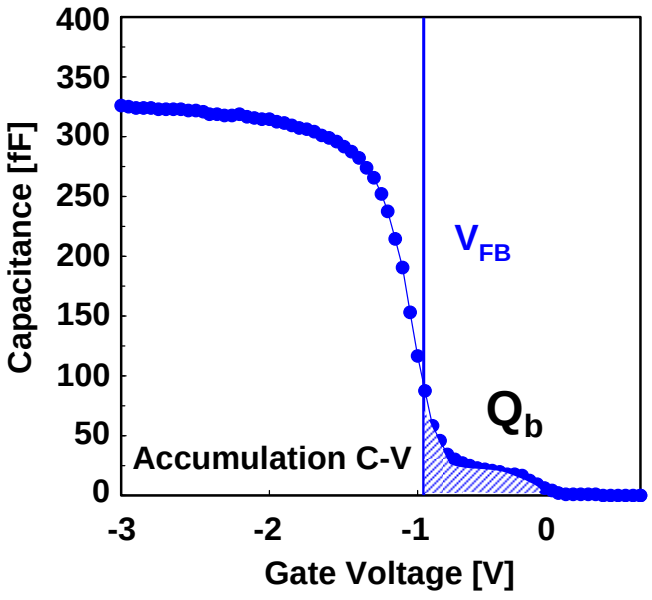

Fig. 2.8 *Gate-to-body capacitance of nMOSFET.*

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Chapter 3 Fundamental Properties of La_2O_3 Gate Dielectric

3.1 Introduction

Understanding basic material properties of La_2O_3 and its impact on electrical characteristics are most important issue. Hf-based oxides have been widely studying for gate insulator application [3.1]. On the other hand, there are few reports on the fundamental electrical properties of La_2O_3 as a gate dielectric compared with the Hf-based oxides. As the material properties strongly affect on the device characteristics, material and electrical characterization should be conducted. Moreover, the selection of gate electrode materials is also significantly important for MOS devices. The main object of this chapter is to reveal the difference of material properties between HfO_2 and La_2O_3 by experimentally. The appropriate gate electrode material is also investigated. After the evaluation of basic properties of La_2O_3 and selection of gate metal materials,

electrical characteristics of MOS devices with La_2O_3 are examined.

3.2 Investigation of Fundamental Aspects of La_2O_3 as Gate Dielectrics

Figure 3.1 shows the fabrication process of MOS capacitors. The MOS capacitors with both La_2O_3 and HfO_2 were prepared to compare with the characteristics. The La_2O_3 and HfO_2 were deposited by e-beam evaporation in an ultra-high vacuum chamber, followed by *in-situ* metal deposition by RF sputtering. Tungsten (W) metal was utilized as gate electrode. The reason why the W was used will be described later. The samples were post-metallization annealed in forming gas ambient (N_2 : H_2 = 97% : 3%) at 500 ^oC for 30min. Finally, Al was deposited on the back side of Si substrate as a contact.

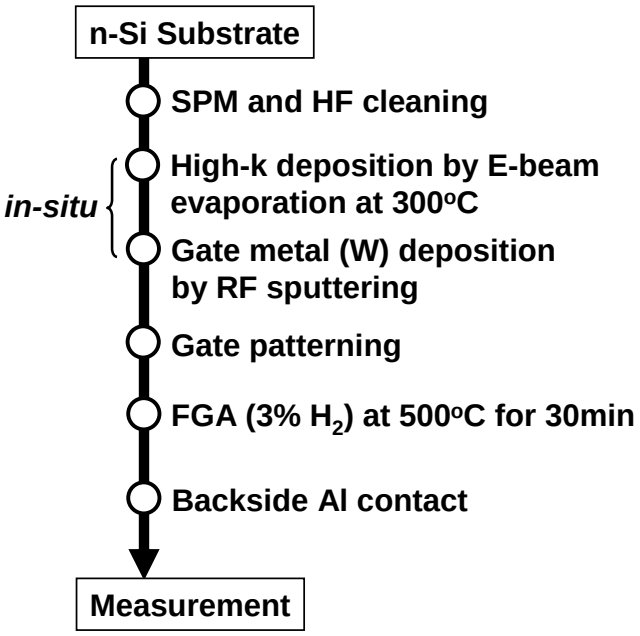


Figure 3.1 *Sample fabrication process for MOS devices.*

As previously mentioned in chapter 1, direct contact of high-k/Si structure can be easily achieved owing to the material nature of the La_2O_3 to form the La-silicate at La_2O_3/Si interface after thermal annealing. Figure 3.2 (a) and (b) show the TEM and XPS analysis with La_2O_3 MOS capacitors. The formation of La-silicate can be observed. Meanwhile, SiO_x interfacial layer was formed after thermal annealing process in the case of HfO_2. Figure 3.3 (a) and (b) show the TEM and XPS results of HfO_2 MOS capacitors. These are the experimental evidences that La_2O_3 is necessary for achieving the direct contact of high-k/Si structure. This is the great advantage. Complex fabrication process for the direct contact can be avoided by using the La_2O_3 as gate dielectrics. Recent theoretical study also explained the material nature to form the La-silicate in La_2O_3 and SiO_2 in HfO_2 [3.2].

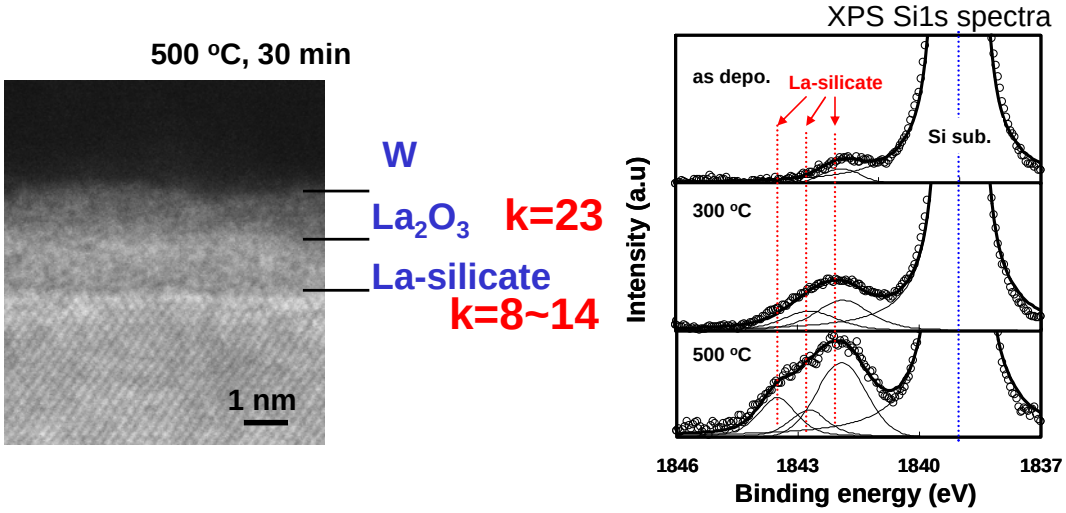
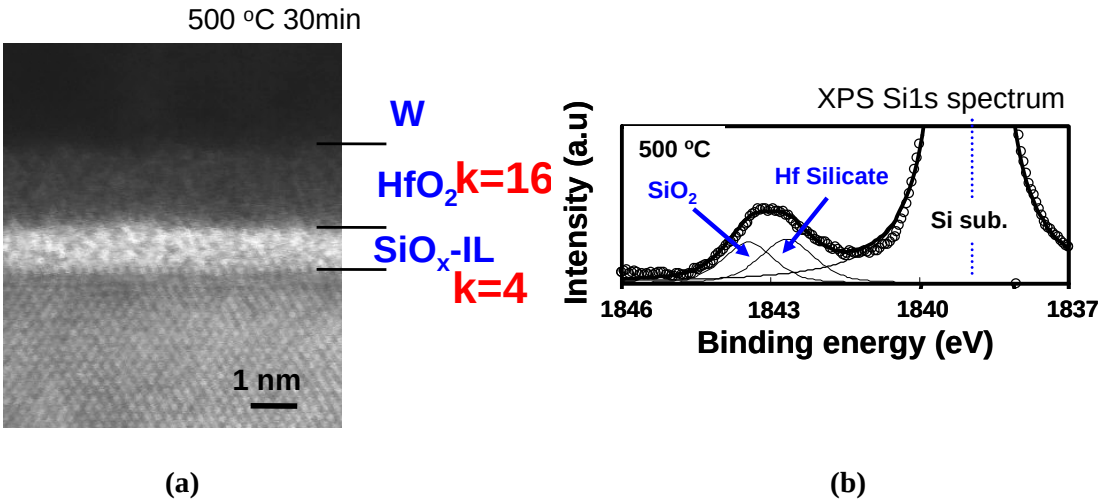


Figure 3.2 (a) *TEM image and* ***(b)*** *XPS analysis of MOS capacitors with La_2O_3 gate dielectrics.*



(a) **(b)**

Figure 3.3 (a) *TEM image and* ***(b)*** *XPS analysis of MOS capacitors with HfO_2 gate dielectrics.*

3.3 Selection for Gate Metal and Electrical Characteristics of MOS Devices

The Poly-Si has been employed as the gate electrode in conventional MOSFET [3.3]. The Poly-Si gate is one of the most important and excellent technology in terms of not only device physics but also process integration. The Fermi level of Poly-Si can be modulated by ion implantation technique. Thus, threshold voltage (V_{th}) of MOSFET can be widely adjusted to obtain the desired V_{th} value. Poly-Si can be also utilized as a mask for self-align process [3.3]. Moreover, Poly-Si gate has excellent thermal and chemical stability in device fabrication process. It is well known that the reason for the success of MOSFET is due to the SiO_2 as the gate oxides and excellent SiO_2/Si interface. The Poly-Si gate is also revolutionary technology as same as SiO_2 gate oxides. However, one of the main problems is depletion in Poly-Si layer. By aggressive EOT scaling,

Poly-Si depletion can not be ignored any more as mentioned in chapter 1. Therefore, the metal gate is necessary for elimination of Poly-Si depletion and improving the drain current of MOSFET.

First priority for selection of metal as the gate electrode is its work function [3.4]. In MOS devices, the concept of "effective work function (EWF)" is introduced because the work function of metal on oxides is different compared to vacuum work function due to the interaction at metal/oxide interface [3.5]. Thus, the work function typically represents not the vacuum work function but the effective work function in Metal-Oxide-Semiconductor (MOS) system. In the case of Poly-Si, the Fermi level corresponds to the work function of the metal. Bandedge work function is desirable for low V_{th} MOSFETs. The metal properties roughly correlate with its electronegativity [3.6]. Figure 3.4 shows the general trends of metal properties.

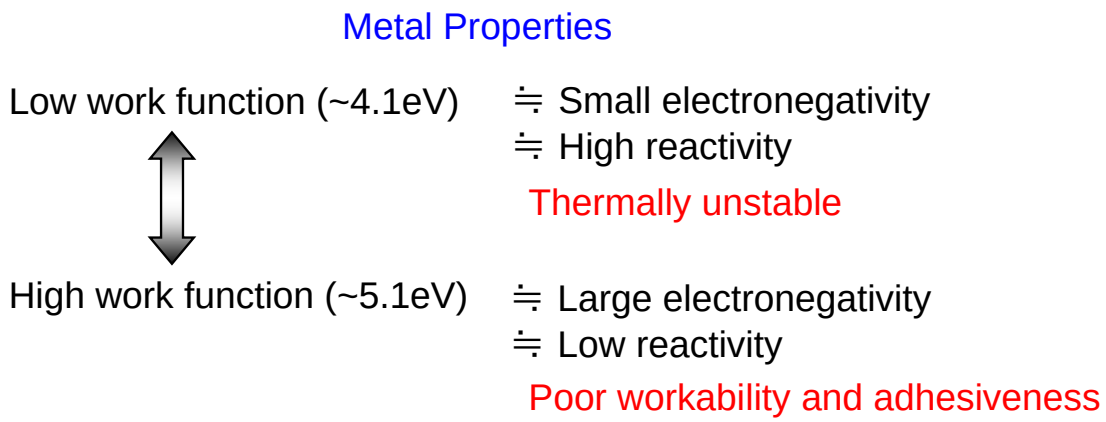


Figure 3.4 *General trends of metal properties.*

The metal with small electronegativity shows low work function, high reactivity, namely, thermally unstable. On the other hand, the metal with large electronegativity

has high work function, low reactivity, namely, poor material workability and adhesiveness. These characteristics must be also considered for device fabrication process. It has reported that low work function metals, such as Al or Ta, were easily reacted with Hf-based oxide, resulting in the excess gate leakage [3.6]. The metals like high work function is electrically unstable after recovery annealing in forming gas ambient [3.7]. According to the recent study, TiN is widely utilized as the gate electrode because of its high thermal stability and standard Fab material [3.8].

In this study, tungsten (W) is used as gate electrode in terms of metal with a high melting point and etching process. The W metal can be easily patterned by reactive ion etching (RIE) with SF_6 chemistry to form gate electrode. As the La_2O_3 and W were deposited by *in-situ* process shown in Figure 3.1, supply of oxygen to the La_2O_3 is necessary. It was reported that the sputtered W contains large amount of oxygen [3.9]. The W layer can play a role to supply the oxygen from W metal to La_2O_3 dielectrics. These are the reason that the W metal is utilized for gate electrode.

Next, the electrical characteristics of MOS capacitors with W/La_2O_3 gate stacks were investigated. Figure 3.5 shows the C-V characteristics of W/La_2O_3/Si capacitor. The ideal C-V curve is also shown in Figure 3.5. The ideal C-V curve is calculated by only considering the difference between the work function of W metal and the Fermi level of n-Si substrate. Large negative flatband voltage (V_{FB}) shift can be observed compared with the ideal C-V curves. The work function of W was extracted from thermally-grown W/SiO_2 MOS capacitor. It is considered that the work function of W metal on La_2O_3 may be varied compared with that on SiO_2. Or, the La_2O_3/Si bottom interface may induce the V_{FB} shift of MOS capacitor. Hetero interface strongly affect on the electrical characteristics of MOS devices.

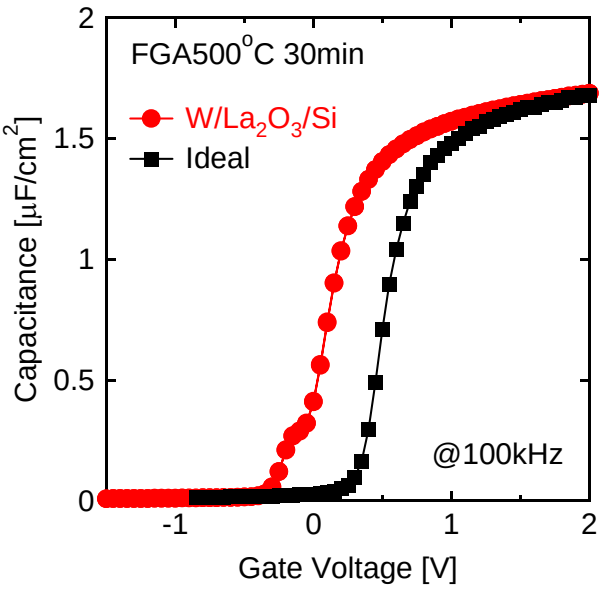


Figure 3.5 *C-V characteristics of W/La_2O_3/Si capacitor. The ideal C-V curve is calculated by only considering the difference between the work function of W metal and the Fermi level of n-Si substrate.*

To further investigate for the origin of the large negative V_{FB} shift, the MOS capacitor with single and by-layer structure was prepared shown in Figure 3.6. The influence of top and bottom interface on the V_{FB} shift was examined by this experiment. If the bottom interface determines the V_{FB} value, the C-V curve of by-layer structure coincides with La_2O_3 MOS capacitor. Whereas, if the V_{FB} value is determined by the top interface, the C-V curve of by-layer structure coincides with HfO_2 MOS capacitor. C-V curves of each MOS capacitors are different if both of top and bottom interface affect on the V_{FB} shift. Figure 3.7 shows the experimental results of MOS capacitors. The C-V curve of by-layer structure is almost identical to the La_2O_3 MOS capacitor. It can be concluded that the V_{FB} is determined by the high-k materials in contact with Si substrate and its interface. In the case of La_2O_3 gate dielectrics, the V_{FB} shift toward

negative direction. It means the lowering effective work function of metal on La_2O_3. This is quite different and interesting experimental results compared with SiO_2 gate oxides.

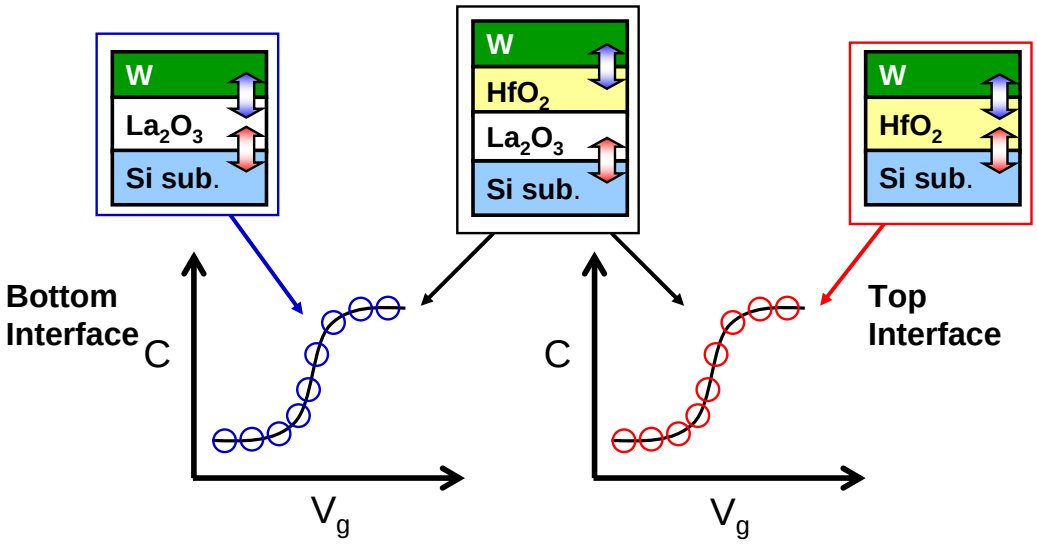


Figure 3.6 *Schematic illustration for the influence of the top and bottom interface on* V_{FB}.

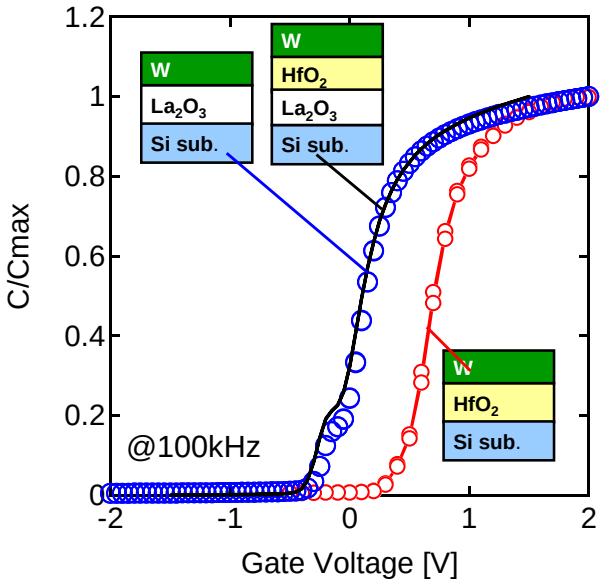
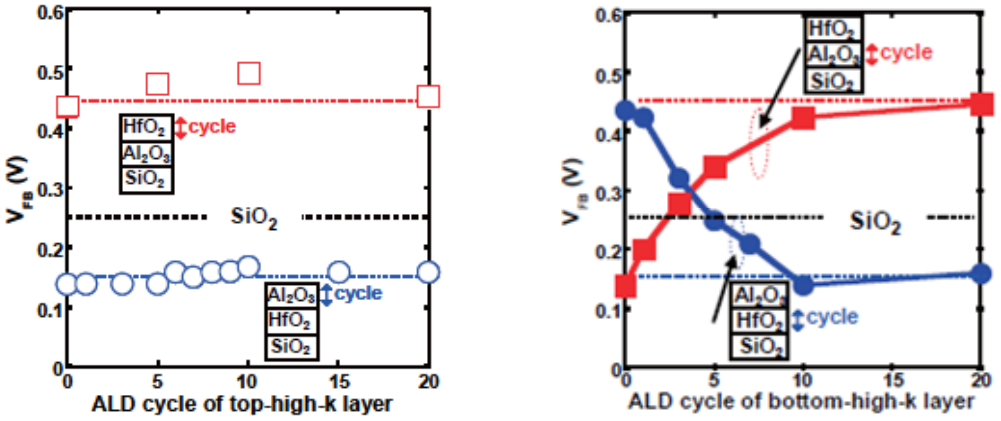


Figure 3.7 *Experimental results of MOS capacitors with single and by-layer structure.*

MIRAI groups systematically investigate the V_{FB} shift due to high-k gate materials on SiO_2 interfacial layer [3.10]. Figure 3.8 (a) and (b) show the impact on the V_{FB} shift with varying the top and bottom high-k thickness by atomic layer deposition (ALD) process. No V_{FB} shift can be observed by varying the top high-k layer thickness while V_{FB} shift are observed with increasing the bottom high-k layer thickness. Therefore, it can be conclude that the V_{FB} shift strongly depend on both SiO_2 and Si bottom interface.



(a) **(b)**

Figure 3.8 *Correlation between V_{FB} and ALD cycle of* ***(a)*** *top high-k layer and* ***(b)*** *bottom high-k layer.*

It was recently reported that the potential offset at La-silicate/Si was observed by XPS measurement and fairly nice agreement with electrical measurement [3.11]. To investigate the amount of lowering in effective work function of W metal on La_2O_3, thermally-grown SiO_2 nMOSFET with Al gate was fabricated. Figure 3.9 compared the I_d-V_g characteristics of W/La_2O_3 and Al/SiO_2 gate stack nMOSFETs. The V_{th} is

extracted from the point of slope on the I_{ds} - V_g curve by a maximum in the transconductance, fit a straight line to the I_{ds} - V_g curve at that point and extrapolate to I_{ds} = 0, as mentioned in chapter 2.

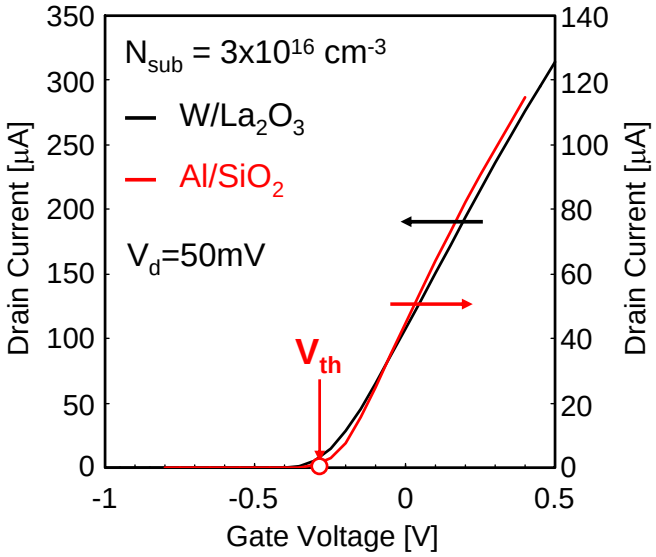
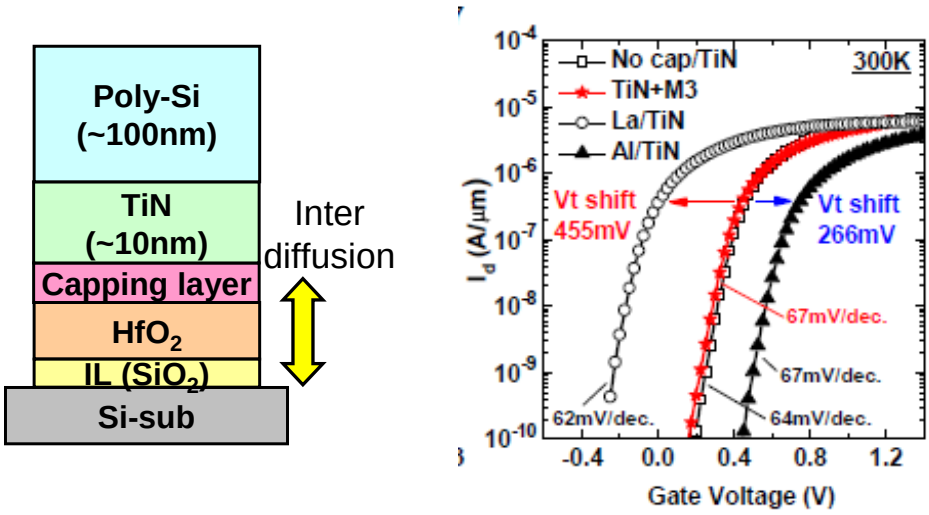


Figure 3.9 *Comparison of the I_d-V_g characteristics of W/La_2O_3 and Al/SiO_2 gate stack nMOSFETs .*

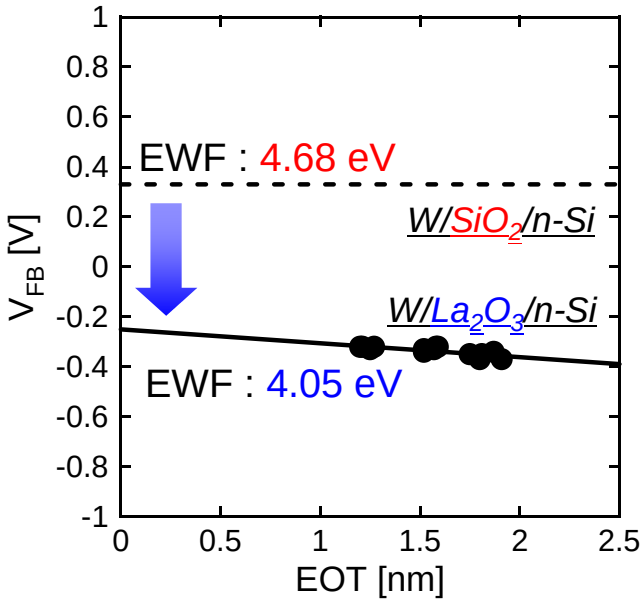
The V_{th} of W/La_2O_3 nMOSFET almost coincides with that of Al/SiO_2 nMOSFET. The effective work function of Al is near the conduction bandedge (~4.1eV) whereas the W is midgap metal (~4.5eV) [3.4]. Hence, the effective work function of W on La_2O_3 is lowered by about 500mV corresponding to the half value of Si bandgap. This result indicates that low V_{th} nMOSFET can be achieved with W/La_2O_3 stacks. Recently, bandedge nMOSFET can be successfully demonstrated with HfO_2 gate dielectrics by combination of La capping technique shown in Figure 3.10 [3.8].



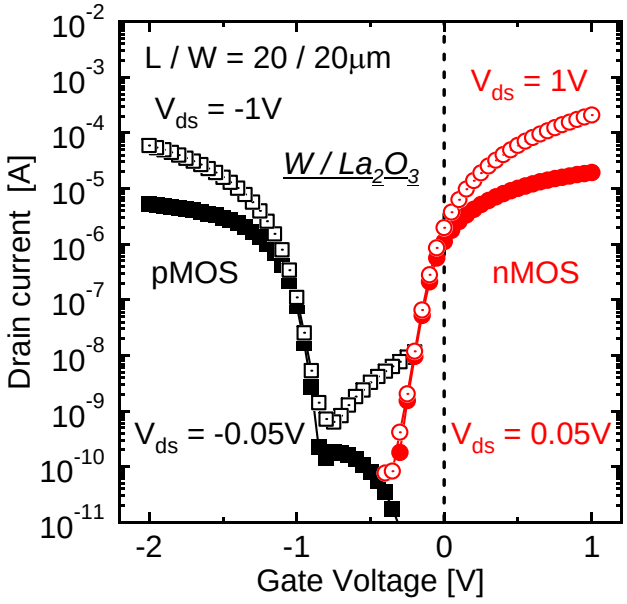
(a) **(b)**

Figure 3.10 *Capping technique for V_{th} control.* ***(a)****Gate stack structure and* ***(b)*** *I_d-V_g characteristics.*

The V_{th} shift by 455mV toward negative direction can be observed with La capping and fairly nice agreement with V_{th} shift shown in Figure 3.9. According to their recent study, La atoms diffuse through the HfO_2 layer and form the La-silicate due to reaction with SiO_2 interfacial layer [3.12]. This result implies that the La-silicate/Si interface also cause the negative V_{FB} shift. Figure 3.11 (a) and (b) summarize the V_{FB} and V_{th} behavior. The effective work function is lowered compared with W/SiO_2 MOS capacitor and the low V_{th} nMOSFET is successfully achieved with W/La_2O_3 stacks. On the other hand, the V_{th} of pMOSFET becomes so high to negative direction. It can be concluded that the negative V_{FB} shift, resulting in lowering effective work function is inherent material properties of La_2O_3 as gate dielectrics.



(a)



(b)

Figure 3.11 (a) *EOT-V_{FB} plots of W/La_2O_3/Si MOS capacitors. The effective work function is extracted from the intercept of y-axis.* ***(b)*** *I_d-V_g characteristics of W/La_2O_3/Si n&pMOSFETs.*

3.4 Conclusions

Fundamental material properties of La_2O_3 as gate dielectrics have been investigated experimentally. It was revealed that La_2O_3 is necessary to realize the direct contact of high-k/Si structure due to La-silicate formation. The W metal was utilized as gate electrode in terms of its high melting point and easily etched by RIE. Moreover, sputtered W is supply to La_2O_3 during thermal annealing process. The electrical characteristics of MOS capacitor and MOSFET were evaluated with W/La_2O_3 gate stacks. The large negative V_{FB} shift and lowering effective work function of metal is inherent material properties of La_2O_3 even the direct contact with Si substrate.

3.5 References

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Chapter 4 Complex and Stacked Structure based on La_2O_3 for Gate Insulator Application

4.1 Introduction

In previously mentioned in chapter 3, La_2O_3 is necessary to achieve direct contact of high-k/Si structure. It has reported that there are many oxygen vacancies in high-k gate dielectrics compared with SiO_2. It is considered that carriers may be trapped these oxygen vacancies [4.1]. Trapped charge scatters in inversion carriers, resulting in reduced inversion mobility. Therefore, high-k material which has great affinity with oxygen must be selected. According to negative enthalpy of oxide formation, the Sc_2O_3 has great affinity with oxygen shown in Table 4.1 [4.2]. On the other hand, HfO_2 or Hf-based oxides are most candidate high-k material [4.1]. It has reported that incorporation of La_2O_3 into HfO_2 can increase the crystallization temperature [4.3]. In

addition, the oxygen vacancy which is predominant defect can suppress by incorporation of La_2O_3 into HfO_2 [4.4]. It indicates that combination of La_2O_3 and HfO_2 could improve the inversion mobility.

The purpose of this chapter is to study a material-based approach based on La_2O_3 for improving effective mobility. Impact of various high-k gate stack engineering based on La_2O_3 on effective mobility is experimentally investigated. Firstly, the electrical characteristics with La-Sc oxides complex are examined. Subsequently, electrical characteristics of HfO_2 and La_2O_3 stacked MOSFET replacement with SiO_2-based interfacial layer are examined.

Table 4.1 *Negative enthalpy of oxide formation*

negative enthalpy of oxide formation

-ΔH formation in kJ per mol O	Metal
<0	Au
0 - 50	Ag, Pt
50 - 100	Pd
100 - 150	Rh
150 - 200	Ru, Cu
200 - 250	Re, Co, Ni, Pb
250 - 300	Fe, Mo, Sn, W, Ge
300 - 350	Rb, Cs, Zn
350 - 400	K, Cr, Nb, Mn
400 – 450	Na, V
450 – 500	Si
500 - 550	Ti, U, Ba, Zr
550 - 600	Al, Sr, Hf, Ce, La
600 - 650	Sm, Mg, Th, Ca, Sc, Y

Reduction of SiO_2

4.2 Experimental Procedure

The concern of complex high-k oxides or ternary high-k dielectrics is how to control the composition ration of the films. As shown in chapter 2, the oxide sintered compact is used for the source of e-beam evaporation. The periodically stacked LaO/ScO layers were deposited on the Si substrate using shutter during the evaporation shown in Figure 4.1 (a). Figure 4.1 (b) represents a schematic view of the complex film structure composed of LaO and ScO. The composition ratio of LaO to ScO can be controlled due to changing the physical thickness [4.5]. Two kinds of films with different composition ratio of LaO to ScO were prepared. The Post Metallization Annealing (PMA) was performed after gate electrode formation.

Stacked structure is so easy to fabricate compared with complex oxide. The La_2O_3 was deposited by e-beam evaporation, followed by HfO_2 deposition. The W metal was deposited by RF sputtering without breaking in an ultra-high vacuum. After the deposition of high-k and metal, same device fabrication process was performed.

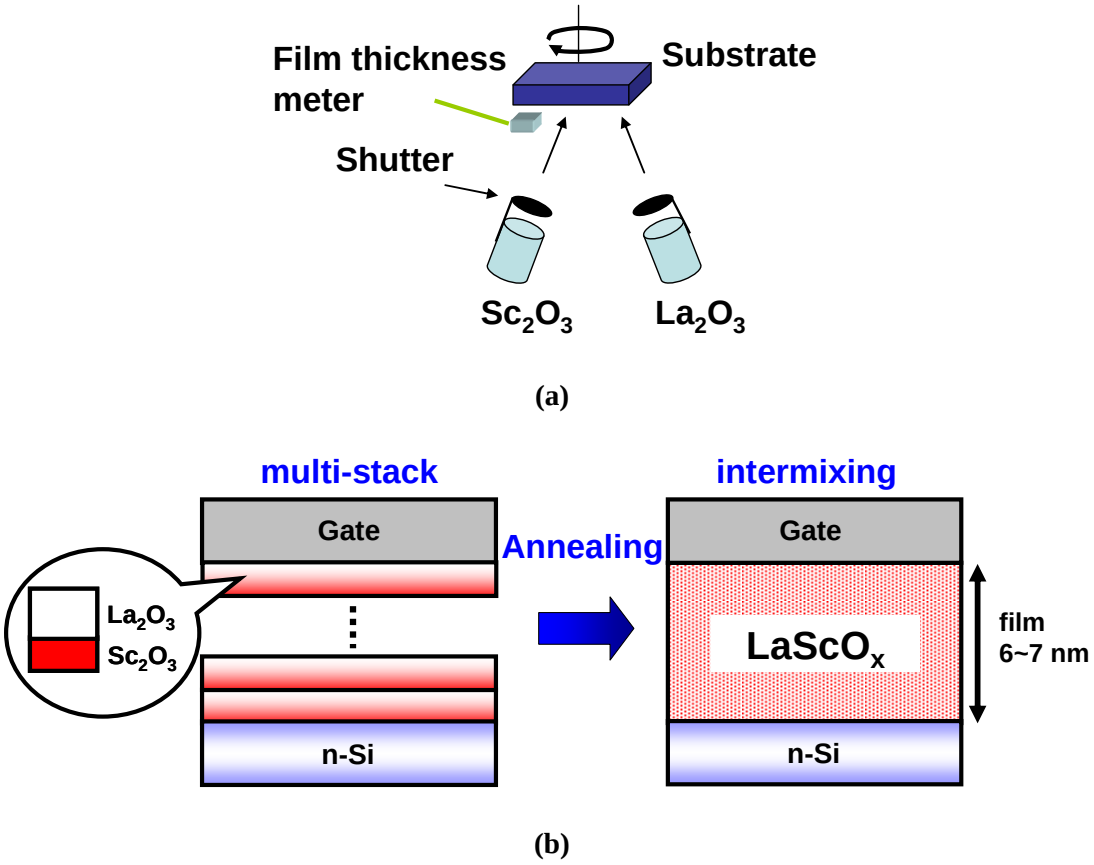


Fig. 4.1 *Sample fabrication method* ***(a)*** *deposition system and* ***(b)*** *schematic view of high-k.*

4.3 Experimental Results of Complex Oxides

Firstly, the C-V characteristics of La-Sc oxides complex gate MOS capacitors were investigated. Prepared samples are Sc/(La+Sc) = 33% and 67%. Figure 4.2 shows the C-V characteristics of the La-Sc oxides complex gate MOS capacitors with (a) Sc/(La+Sc) = 33% and (b) Sc/(La+Sc) = 67% as a function of annealing temperature. Several C-V curves show the C-V hysteresis. The direction of all the C-V hysteresis was in the clockwise. Using the n-type Si substrate, these results suggest the carriers are

injected from the substrate into the gate oxide. Large bumps, which indicate the large interfacial state density [4.6], were observed in the case of Sc/(La+Sc) = 33% sample. On the other hand, the C-V curves indicating the lower interfacial state density as well as small C-V hysteresis were obtained for the Sc/(La+Sc) = 67% case. Considering the large bump reported for the La_2O_3/Si capacitors [4.7], the incorporation of Sc into La_2O_3 can play a role to suppress the interfacial state density. Flatband voltage (V_{FB}) of the as PMA300°C capacitors are summarized in Figure 4.3. La incorporation to Sc_2O_3 can reduce the charge trapping. However, the PMA at higher temperature leads to lower capacitance value as shown in Figure 4.2. Higher LaO concentration leads to negative flatband voltage shift, which is in good agreement with reported flatband voltage shift reported in [4.8], and it would be suitable for band edge threshold voltage (V_{th}) control.

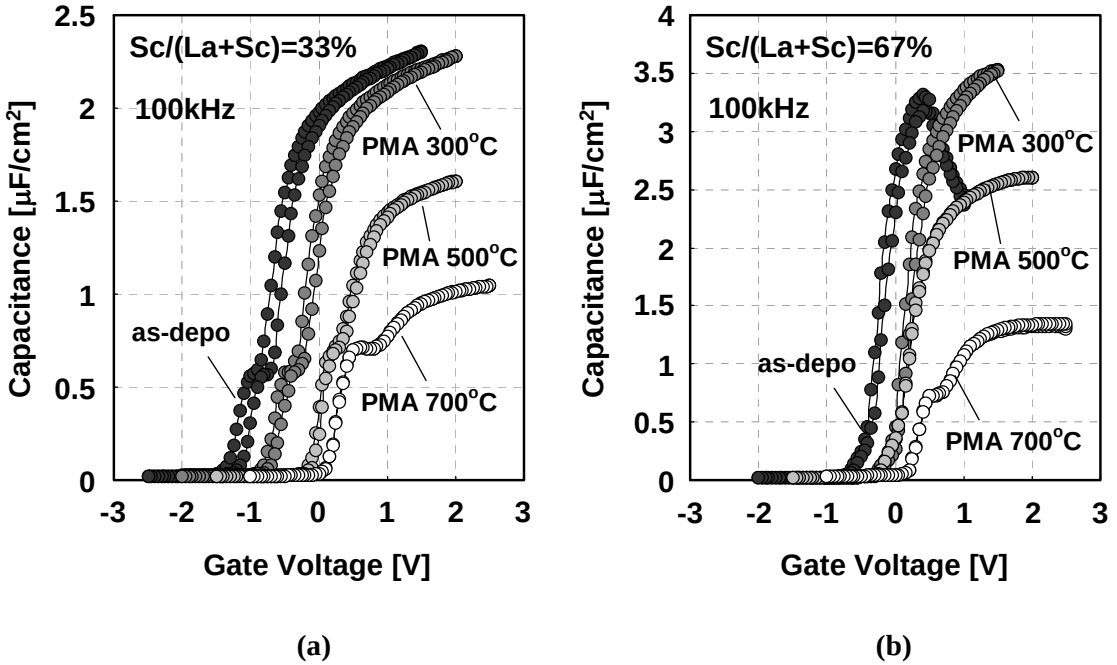


Fig. 4.2 *C-V characteristics as a function of annealing temperature.* ***(a)*** *Sc/(La+Sc)=33% capacitors and* ***(b)*** *Sc/(La+Sc)=67% capacitors.*

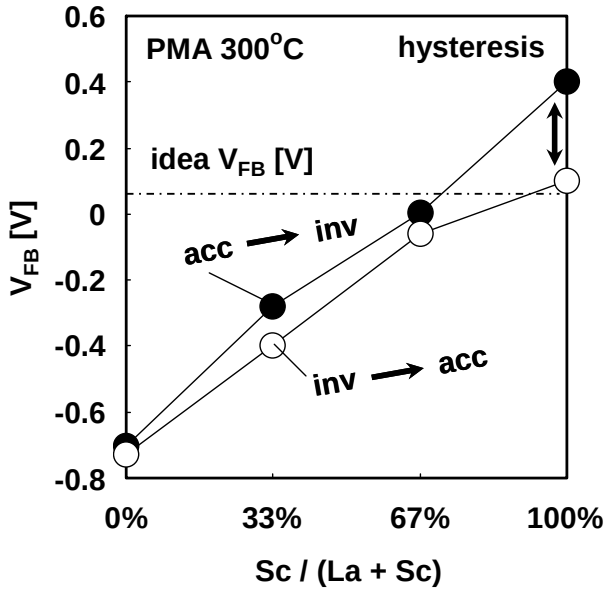


Fig. 4.3 *V_{FB} Shift as a function of Sc concentration. Hysteresis was observed in C-V curves.*

However, excessively negative V_{FB} is not desirable for pMOSFETs as the V_{th} would be high. On the other hand, the Sc_2O_3 film induces positive V_{FB} shift even taking into account. It was reported that positive V_{FB} shift was confirmed by Sc incorporation into Hf-based oxides compared with LaO incorporation [4.9]. Therefore, large negative V_{FB} shift induced by La_2O_3 can be controlled by incorporation of the ScO. Considering the ideal V_{FB} of 0.06V obtained on the W/SiO_2/Si, Sc/(La+Sc) = 67% concentration seems to be optimum to cancel the effect of La.

Figure 4.4 represents the V_{FB} with different composition ratio as a function of annealing temperature. The results of Sc_2O_3/Si and La_2O_3/Si capacitors are used as reference. It can be confirmed that the V_{FB} values are shifted between the Sc_2O_3/Si and La_2O_3/Si single-layer capacitors. In addition, the amount of V_{FB} shift increases with concentration of LaO.

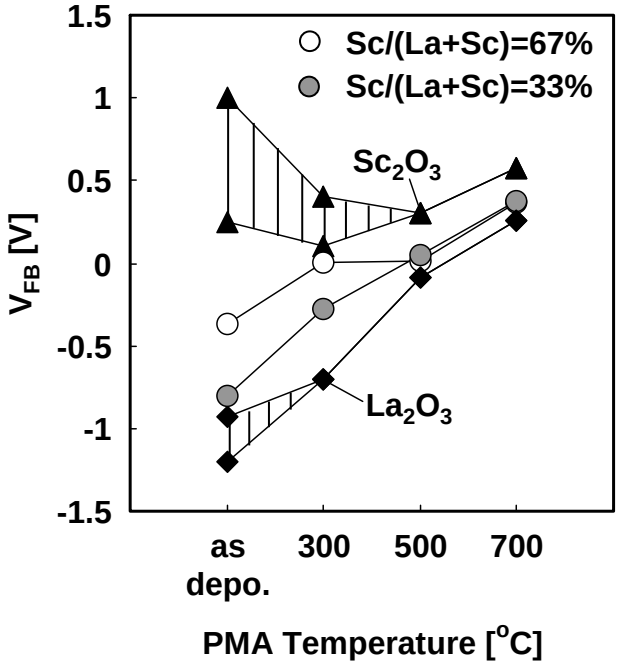


Fig. 4.4 *V_{FB} Shift as a function of annealing temperature.*

Figure 4.5 shows the EOT change along PMA temperature. The behavior of EOT change of Sc/(La+Sc) = 33% sample is similar to that of Sc/(La+Sc) = 67% sample. On the other hand, complex films are suppressed the EOT increasing with higher annealing temperature even low Sc concentration compared to La_2O_3/Si single-layer capacitors. It is considered that incorporation of Sc into La suppressed the interfacial layer formation as described chapter 3. Thus, it is conceivable that incorporation of Sc into La is one of effective methods to control the EOT increase.

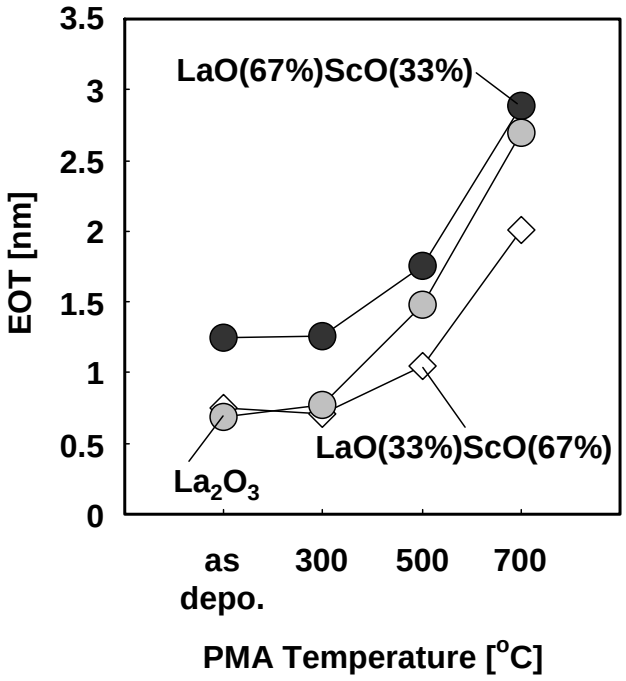


Fig. 4.5 *EOT change as a function of annealing temperature.*

Next, nMOSFETs with complex oxides was examined. The interface state density is estimated using charge pumping method. Figure 4.6 shows the charge pumping current. The interface state density is calculated from peak of charge pumping current. Small interface state density was confirmed with low Sc concentration in Figure 4.6. These results are more higher compared with that of HfSiON gate MOSFET [4.10]. It is considered that inversion carriers may be scattered by interface state density and degrade effective mobility. It is found that interface state density becomes lower with increasing amount of LaO.

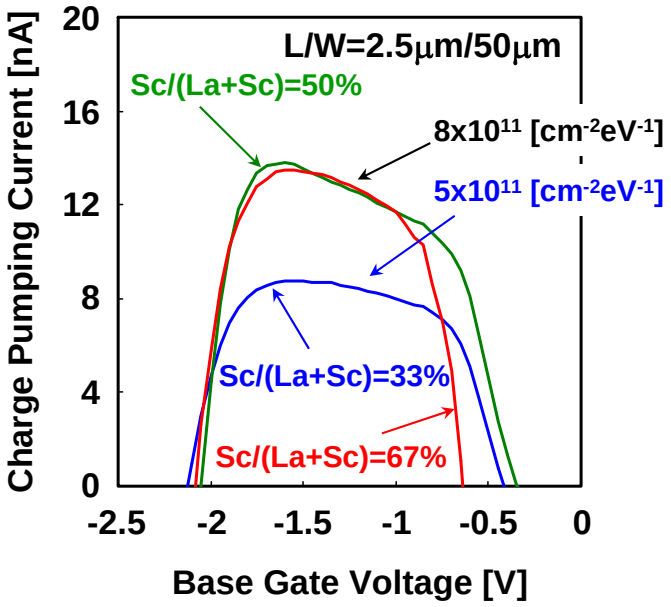


Fig. 4.6 *Charge pumping current and interface state density.*

By charge pumping measurement, small interface state density was confirmed with low Sc concentration. The effective mobility of La-Sc oxides complex MOSFET with various film compositions are experimentally evaluated. Mobility is measured by Split C-V method at 1MHz. The parasitic capacitances are subtracted by measuring different gate length (L_g) samples [4.11]. Figure 4.7 shows the gate-channel capacitance (C_{gc}) measured by Split C-V technique. As using the tungsten (W) metal gate, decreasing gate capacitance due to depletion of poly-Si gate do not occur. Therefore, the EOT can be extracted using NCSU CVC program. The EOT values of Sc/(La+Sc) = 50% and 67% samples are almost identical, EOT = 1.4nm. On the other hand, capacitance value of Sc/(La+Sc) = 33% samples are drastically decreased compared to Sc/(La+Sc) = 50% and 67% samples. The difference of EOT is about 1nm. This result indicates decreasing dielectric constant. It has reported that dielectric constant of Hf-silicate is lower

compared with HfO_2 [4.12]. Thus, decreasing capacitance value indicates changing La_2O_3 to La-silicate according to react with Si substrate, resulting in formation of low dielectric constant layer. Figure 4.8 represents the effective mobility of La-Sc oxides complex MOSFETs. Sc/(La+Sc) = 33% sample shows most high mobility in three samples. This result is agreement with interface state density by charge pumping measurement.

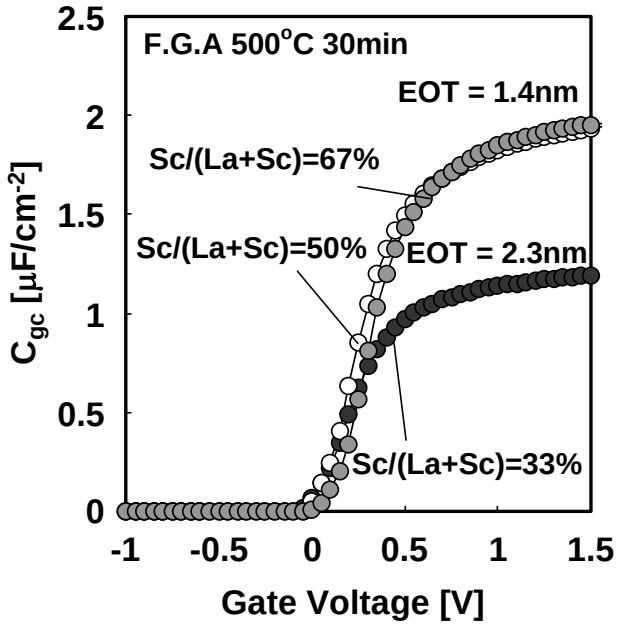


Fig. 4.7 *Gate-channel capacitances measured by Split C-V method.*

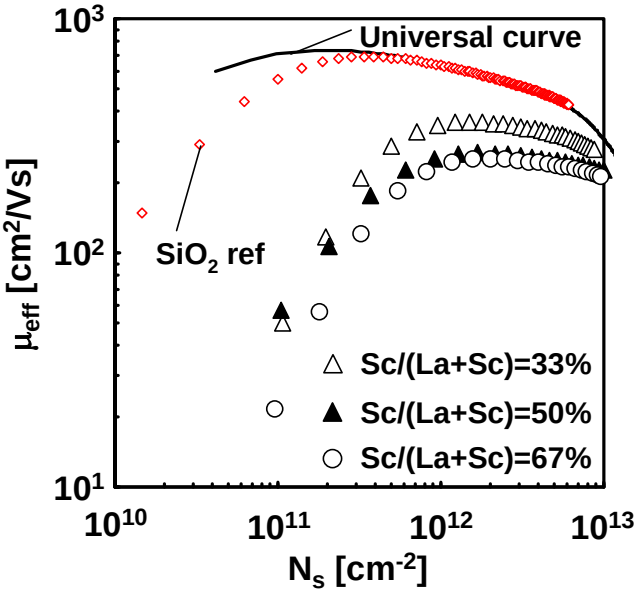


Fig. 4.8 *Effective mobility of La-Sc oxides complex gate MOSFETs.*

It has reported that drain current of HfSiON gate MOSFET is degraded with different Hf/Hf+Si ratio. The higher Hf concentration is more degraded than low Hf concentration [4.13]. In addition, a lot of charge trap sites are existence in the HfSiON with higher Hf concentration. It is considered that degradation of mobility for low La concentration is same as HfSiON gate MOSFET. According to changing La_2O_3 to La-silicate, a lot of trap sites may be suppressed and increasing mobility. On the other hand, charge trap sites remain in gate oxides for low La concentration samples and leading mobility reduction.

4.4 Experimental Results of Stacked structure

As previously explained in chapter 3, the impact of W/La_2O_3 gate stacks on the V_{FB} or V_{th} was investigated experimentally. The V_{th} is one of the most important factors for the MOSFETs because the MOSFET basically operate as switches in VLSI and the V_{th} determine the On/Off states of MOSFETs. On the other hand, the effective mobility is also important parameter because circuit speed strongly depends on the effective mobility. The aim of this section is to investigate how to improve the effective mobility of MOSFET with direct contact in high-k/Si structure. Material-based approach was conducted to improve the effective mobility and maintain the small EOT. As previously mentioned, MOS capacitor with by-layer structure using La_2O_3 and HfO_2 were prepared to understand the V_{FB} shift behavior. Some benefits of by-layer structure were found by experimentally. The one is to suppress the increase of EOT. Figure 4.9 shows the comparison of increment in EOT with various gate stack structures. Although formation of the interfacial layer with low dielectric constant is inevitable for both of La_2O_3 and HfO_2, EOT increase can be slightly suppressed using by-layer structure. This is because the excess silicate reaction with Si substrate and Si diffusion from substrate to La_2O_3 was inhibited at HfO_2/La_2O_3 interface owing to less reactivity of HfO_2 with Si [4.14]. The other is crystallization suppression. Figure 4.10 shows the GIXD measurements. The peak indicating the crystallization can be observed in both La_2O_3 and HfO_2 single layer. However, crystallization of high-k layer is successfully inhibited in the case of by-layer structure.

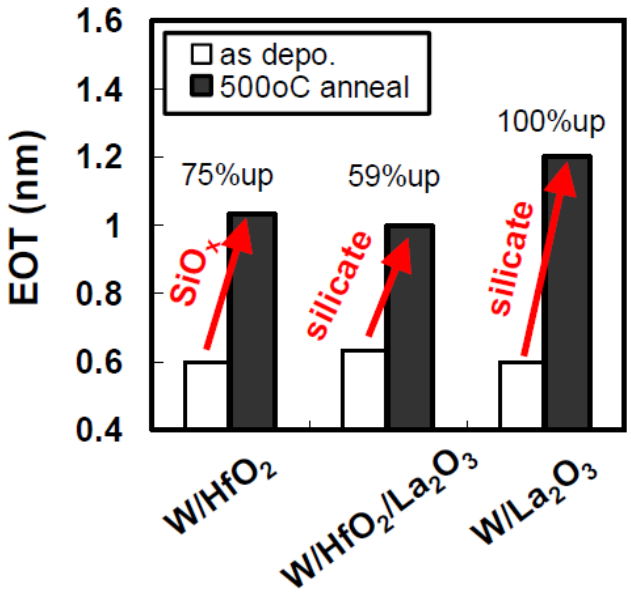


Figure 4.9 *Comparison of EOT increment with various gate stack structures.*

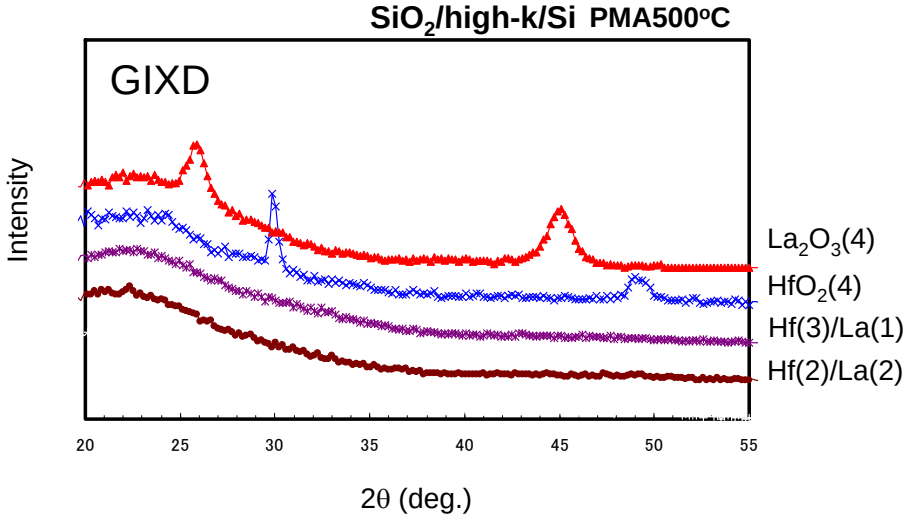
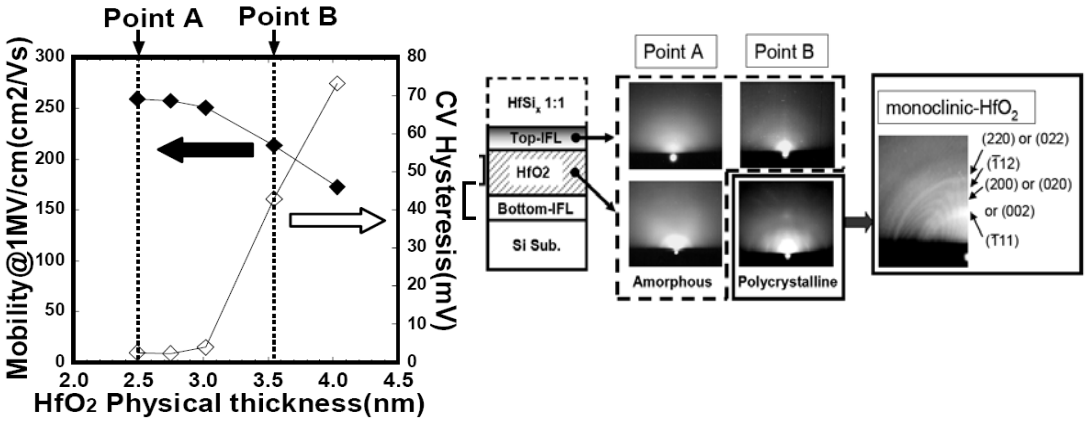


Figure 4.10 *GIXD measurements with various gate stack structures.*

It has been reported that the reduced effective mobility strongly correlate with crystallization of high-k film. The HfO_2 transients from polycrystalline form to

amorphous with decreasing its physical thickness shown in Figure 4.11 [4.15]. The defects at grain boundaries scatter the carriers in inversion layer [4.16]. The effective mobility was improved by amorphous structure. Thus, amorphous form is suitable for improving the effective mobility. The effect of crystallization suppression with by-layer was examined by nMOSFET fabrication and characterization.



(a) **(b)**

Figure 4.11 (a) *Electron mobility and C-V hysteresis as a function of HfO_2 physical thickness.* ***(b)*** *RHEED patterns of point A and B.*

Sample fabrication process is as same as MOS capacitors explained in chapter 3. Source and drain pre-formed p-Si substrate were utilized to fabricate the nMOSFETs. The substrate doping concentration is 3 x 10^{16} cm^{-2}. Al was deposited on the source/drain region and back side of the substrate as an electrical contact. Split C-V method was employed to measure the effective electron mobility of nMOSFET. Figure 4.12 shows comparison of the effective electron mobility with single and by-layer structure. EOT is about 1.3nm. Contrary to expectations, the effective electron mobility

of by-layer structure is lower compared with that of La_2O_3 single layer. As the La_2O_3 is in contact with Si substrate, the interface properties at high-k/Si interface is almost identical. One of the possible origins for reduced effective mobility due to the by-layer structure is HfO_2/La_2O_3 interface. As there are several hetero interfaces in gate insulator, the by-layer structure with HfO_2 and La_2O_3 is overly complex structure. It is concluded that the single La_2O_3 layer is suitable for improving the effective mobility. Simple device structure is desirable for not only the mobility improvement but also the device fabrication process.

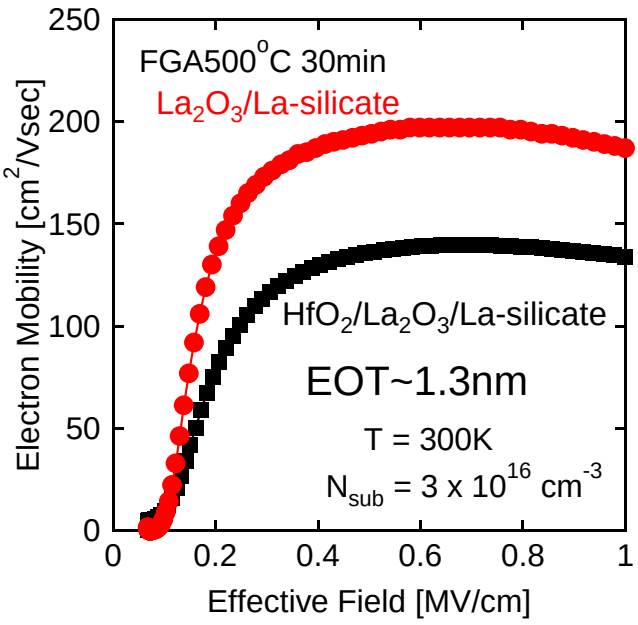


Figure 4.12 *Comparison of electron mobility with single and by-layer structure.*

4.5 A Serendipitous Discovery for Different Approach

An interesting phenomenon was found out through the MOSFET characterization. Figure 4.13 shows the picture of sample. As the MOS capacitors are also prepared, the EOT and V_{FB} can be measured during the MOSFET fabrication process. In this experiment, nMOSFET was fabricated thereby Si substrate is p-type. The p-MOS capacitor was measured during the nMOSFET fabrication to examine the EOT and V_{FB}.

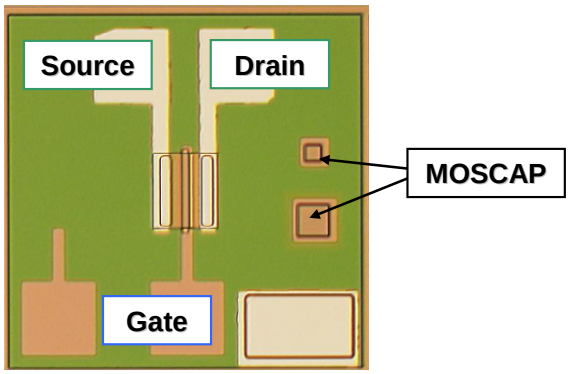
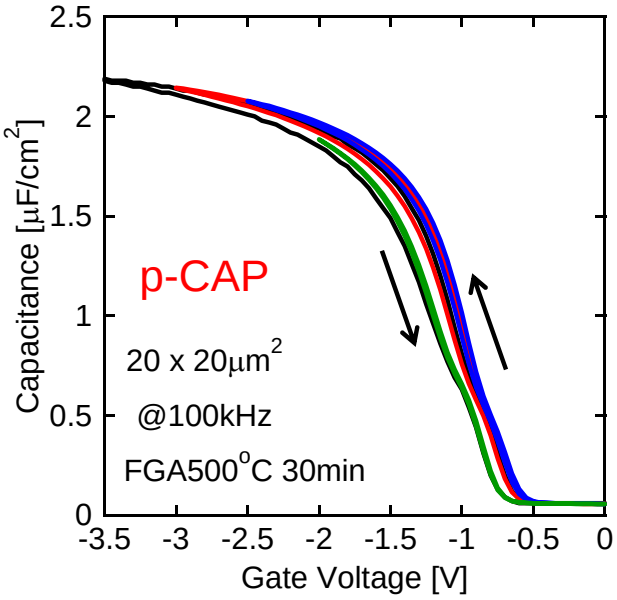


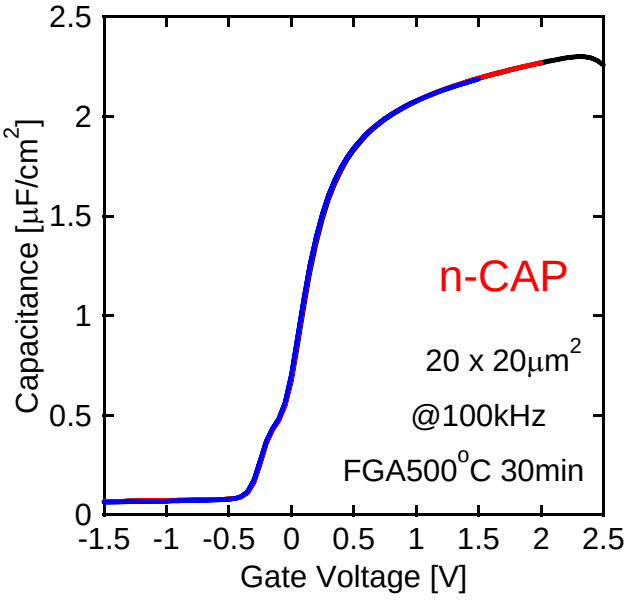
Figure 4.13 *Picture of MOSFET substrate.*

Figure 4.14 shows the comparison for the C-V characteristics of n- and p-MOS capacitors with La_2O_3 gate dielectrics. The hysteresis of C-V curve can be only observed in p-MOS capacitor. Moreover, the hysteresis becomes wider by increasing gate voltage shown in Figure 4.14 (a). On the other hand, no hysteresis was confirmed with increasing the gate voltage as shown in Figure 4.14 (b). It is well known that the hysteresis is typically associated with traps in oxides. However, it can not be explained

by the traps in oxides the reason why the hysteresis is only observed in p-MOS capacitor because both of samples were fabricated at the same time.



(a)



(b)

Figure 4.14 *C-V characteristics of* ***(a)*** *p-MOS capacitor and* ***(b)*** *n-MOS capacitor.*

To investigate whether the hysteresis in p-MOS capacitor is associated with the type of Si substrate or not, split C-V measurement was conducted for nMOSFETs. Figure 4.15 shows the measurement results of nMOSFET. The hysteresis can be confirmed in gate-body capacitance (C_{gb}) whereas no hysteresis was observed in gate-channel capacitance (C_{gc}). This result coincides with MOS capacitor as shown in Figure 4.14. Therefore, it can be considered that the excess interface state density (D_{it}) or trap states exist near the valence bandedge. Figure 4.15 shows the schematic showing the effect of asymmetric high D_{it} on capacitor. Asymmetric high D_{it} has also reported the high mobility channel substrate [4.17]. According to the previous report [4.17], when the D_{it} exceeds the C_{ox}/q, the hysteresis of C-V curve may be appeared.

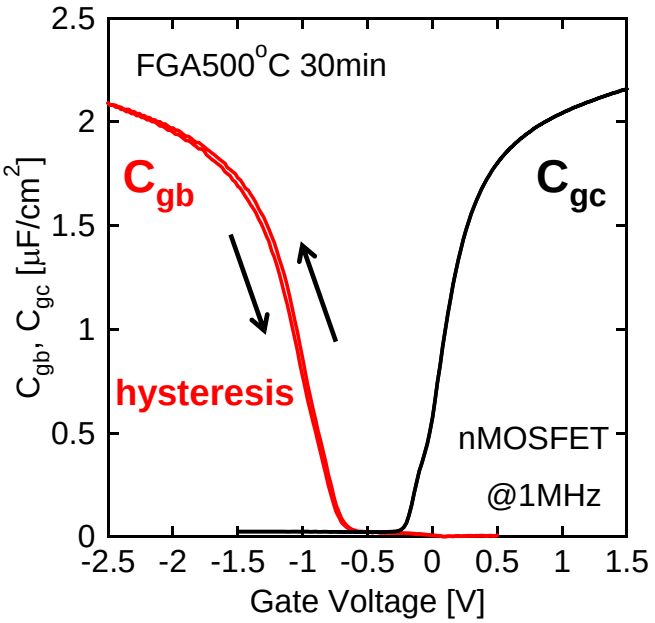


Figure 4.15 *Split C-V characteristics of nMOSFET.*

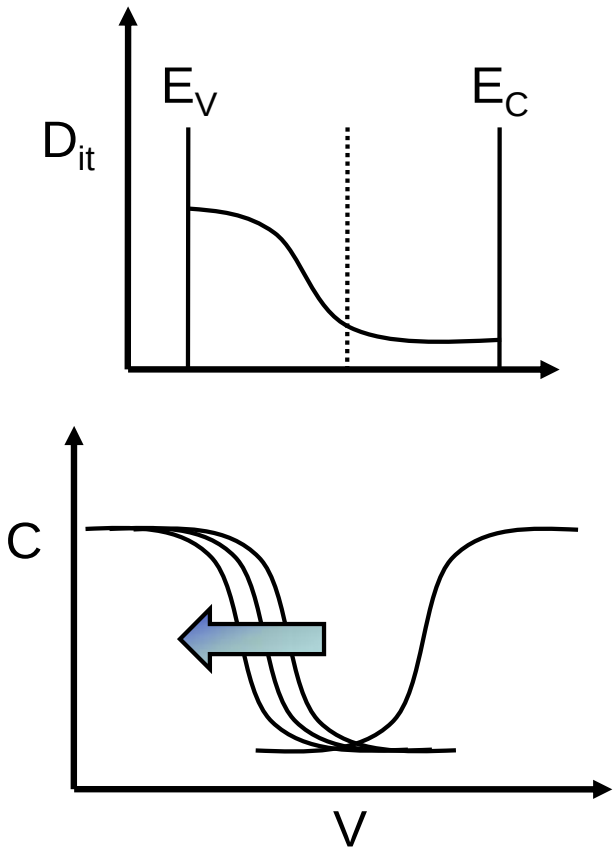


Figure 4.16 *Schematic showing the effect of asymmetric high D_{it} on capacitor.*

To evaluate the D_{it} at La-silicate/Si interface, conductance method was carried out for estimation of the D_{it} as a function of energy. Figure 4.17 shows the interface state density as a function of energy by conductance method. No significant difference of D_{it} can be confirmed in measurement energy region. However, as conductance measurement was employed at room temperature, the interface state near the valence and conduction bandedge can not be detected. Figure 4.18 shows the calculated energy ranges for visible interface state density by conductance method [4.18]. Low temperature measurement should be conducted to examine the bandedge interface state density.

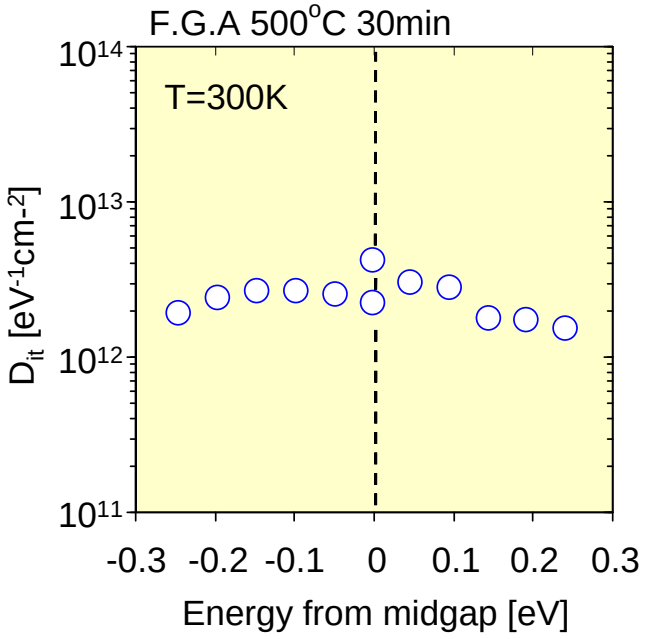


Figure 4.17 *D_{it} as a function of energy measured by conductance method.*

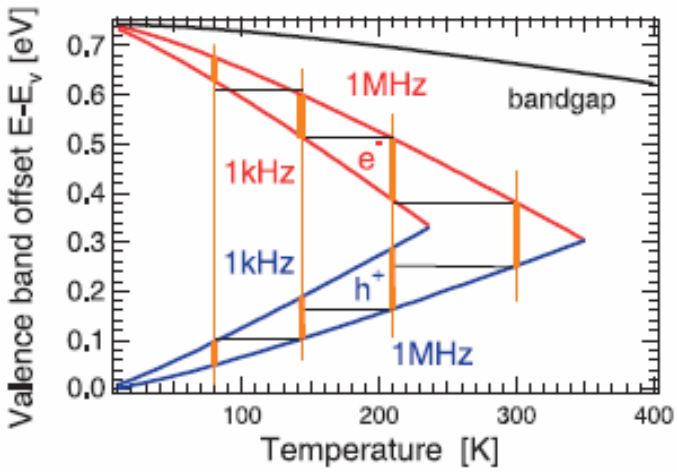
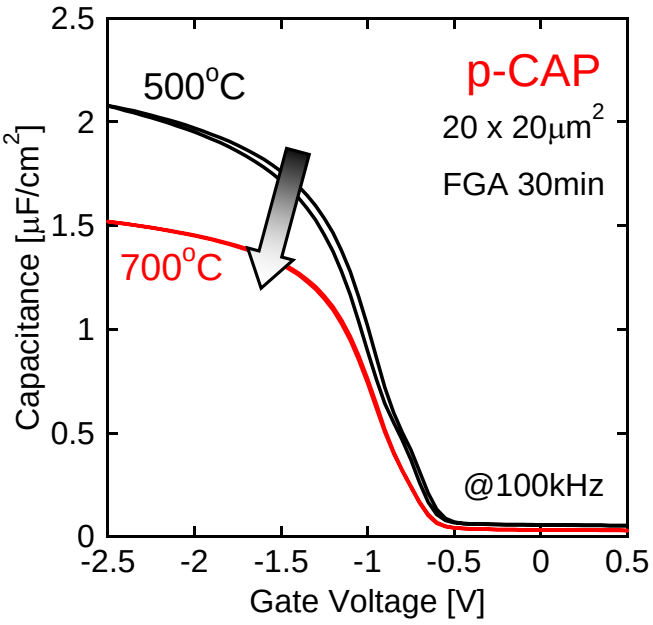


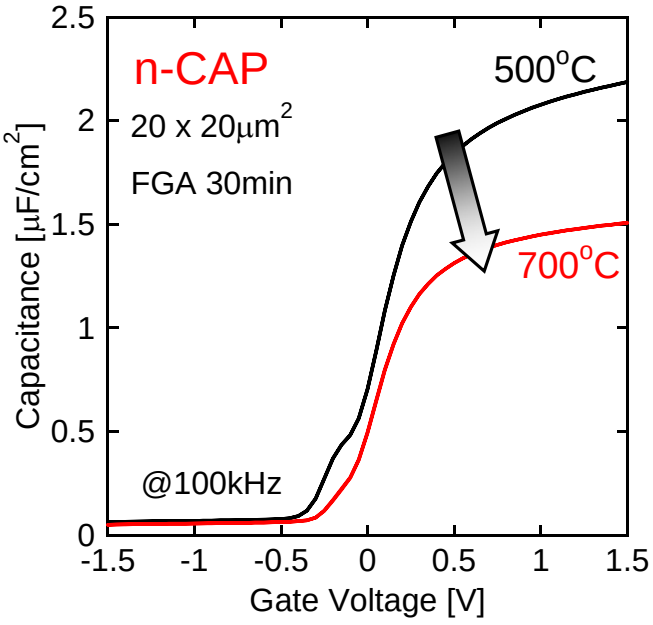
Figure 4.18 *Calculated energy ranges for visible interface state by conductance method.*

Though the interface states or trap states at near the bandedge can not be evaluated,

these charges lead to the mobility degradation because of the sources for coulomb scattering. Since the cause of asymmetric C-V characteristic is still unclear, it indicates that damage during fabrication process may be remained in gate stacks. Thus, high temperature annealing at 700 ^{o}C in forming gas ambient for 30min was performed to eliminate the hysteresis. Figure 4.19 shows the C-V characteristics of n-and p-MOS capacitors as a function of annealing temperature. Although the EOT increase with increasing the annealing temperature, the hysteresis of p-MOS capacitor also becomes smaller. Moreover, hump in C-V curve ascribed to the interface state density also decreased with increasing annealing temperature. It indicates that the interface properties at La-silicate/Si interface will be improved by high temperature annealing.



(a)



(b)

Figure 4.19 *Effect of annealing temperature on the C-V characteristics of* ***(a)*** *p-MOS capacitor and* ***(b)*** *n-MOS capacitor.*

4.6 Conclusions

Material-based approach was adopted to improve the effective mobility. In the complex oxides, higher La concentration MOSFET presents small interface state density, resulting in high mobility in prepared samples. Although the V_{FB} can be modulated by Sc incorporation, improvement mobility by elemental addition is little effect. EOT increment and crystallization can be suppressed by the stack structure with La_2O_3 and HfO_2. However, the effective mobility is lower compared with La_2O_3 single layer. Plausible origin of reduced mobility with by-layer may be the influence at HfO_2/La_2O_3. It is difficult to satisfy small interface state, small EOT and mobility improvement simultaneously by material-based approach. The simple device structure may be suitable for improving mobility.

An asymmetric C-V characteristic measured by split C-V method was accidentally found through the nMOSFET fabrication and characterization. The high temperature annealing will have potential to improve the interface properties and effective mobility. The approach for improving the effective mobility will be changed from material-based to device/process-based approach.

4.7 References

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Chapter 5 Impact of Annealing Process on MOS Devices with La_2O_3 Gate Dielectrics

5.1 Introduction

In chapter 4, material-based approach for improving the effective mobility has been described. As previously explained, the effective mobility is improved by the suppression of polycrystalline form with decreasing the HfO_2 physical thickness. Recently, grain boundaries driven gate leakage was reported with Hf-based oxides [5.1]. Therefore, high-k gate dielectric with amorphous structure is desirable for gate insulator application as well as SiO_2 gate dielectric. The amorphous form can be obtained by stack structure with La_2O_3 and HfO_2 as shown in chapter 4. Moreover, the EOT increment can be also suppressed with by-layer structure compared with each single layer structure under the same annealing conditions. However, the effective mobility

with stack structure is lower than that of La_2O_3 single layer.

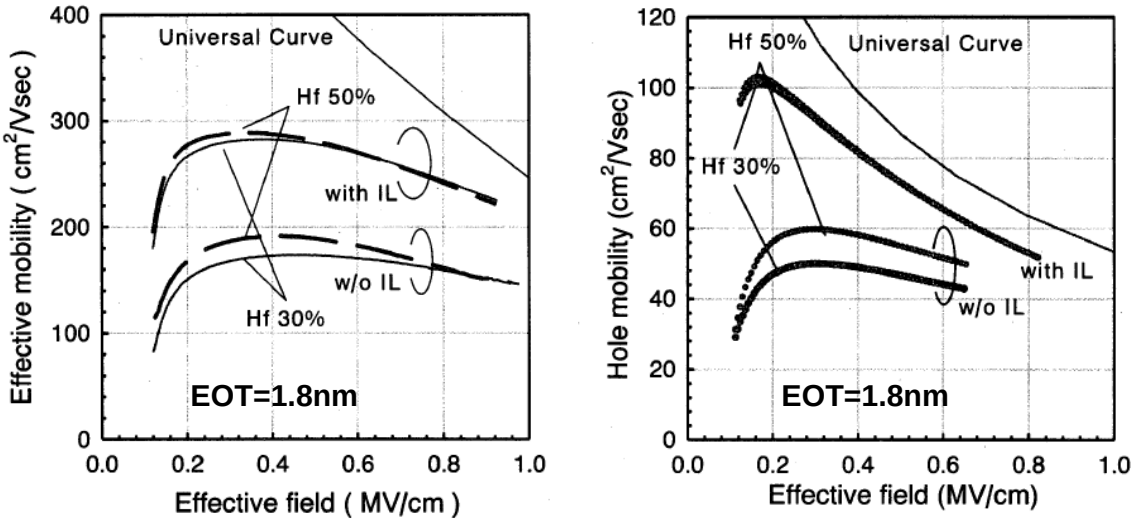
Through the nMOSFET characteristics, it was accidentally found that the high temperature annealing will be promising new idea for improving the interface properties, resulting in recover of the effective mobility. Since the inversion channel layer is formed at Si surface, the carriers are strongly affected by the oxides/Si interface. On the basis of this way of thinking, the approach for improving the effective mobility was converted from material-based to device/process-based method.

Purpose of this chapter is firstly to establish the process technology for improving the direct contact of high-k/Si interface. Especially the high temperature annealing process will be focused. Moreover, the effect of annealing process on electrical characteristics is examined. It can be easily expected that high temperature annealing leads to the EOT increase. However, the method how to suppress the EOT increase with low interface state density is not discussed in this chapter. After the establishment of process for improving the interface properties, characterization of the effective mobility with direct contact high-k/Si MOSFETs is conducted to understand the difference compared with SiO_2 or other high-k gate dielectrics.

5.2 Reports of Research and Experimental Procedure

The reduced effective mobility is one of the serious issue remained to be solved. It has been reported that the effective mobility can be recovered by formation and increasing of interfacial layer thickness because of its excellent interface properties at

SiO_2/Si interface. Moreover, the scattering sources are physically distance from the inversion channel [5.2]. Figure 5.1 shows the impact of interfacial layer and Hf concentration on the effective mobility [5.3]. Both electron and hole mobility can be recovered with interfacial layer compared to Hf concentration. As mentioned in chapter 1, the effective mobility reduced by decreasing the thickness of the interfacial layer. It is concluded that the formation of interfacial layer is quite important and effective to obtain the high effective mobility at an increase in EOT. The mobility reduction with direct contact high-k/Si structure can be easily expected.



(a) **(b)**

Figure 5.1 *Impact of interfacial layer and Hf concentration on* ***(a)*** *electron mobility and* ***(b)*** *hole mobility.*

The other reason focusing the high temperature annealing is described. Figure 5.2 (a) shows the intel's 45nm high-k/metal gate process [5.4]. It is called high-k fast/metal last.

Figure 4.2 (b) shows the IBM's high-k/metal gate process [5.5]. The high temperature process, such as source/drain activation, is implemented after gate stack formation. As shown in Figure 5.2 (a), removal process of Poly-Si gate is employed. It can be considered that a certain level of thermal annealing is necessary for high-k gate dielectrics to improve the electrical characteristics. This is the other reason to focus the high temperature annealing process. Hence, optimized annealing condition including temperature, time and atmospheric should be conducted to improve the interface properties of the high-k/Si interface.

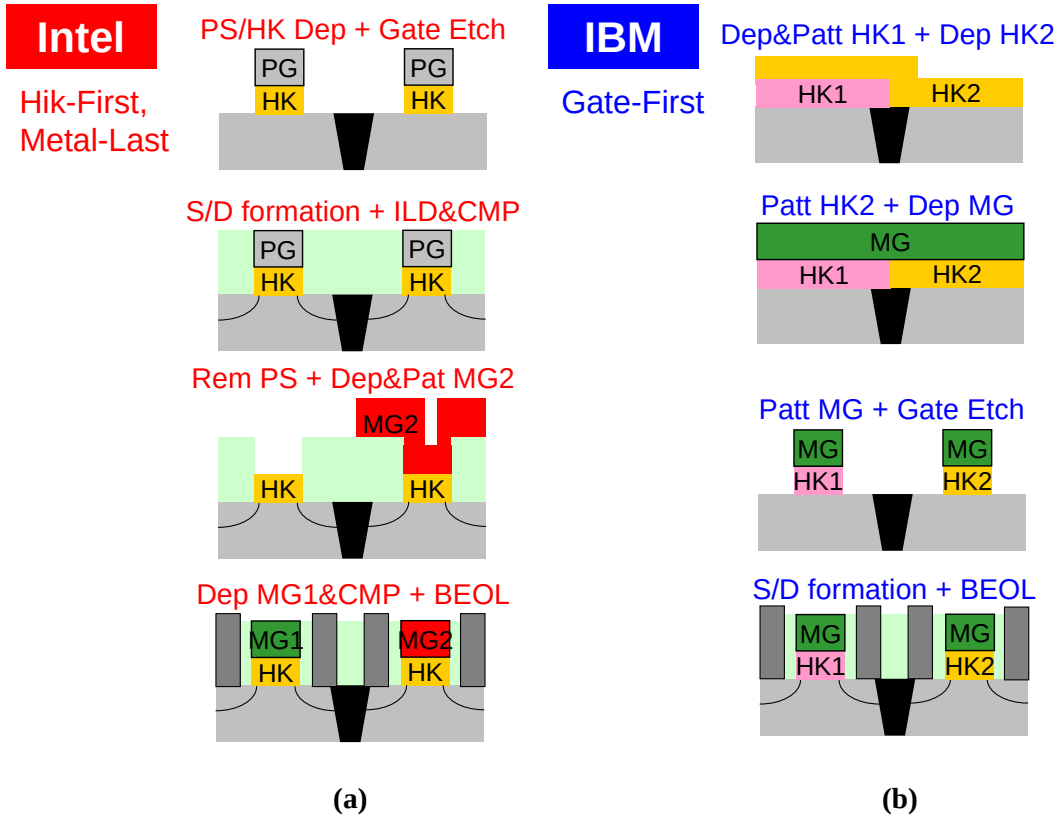
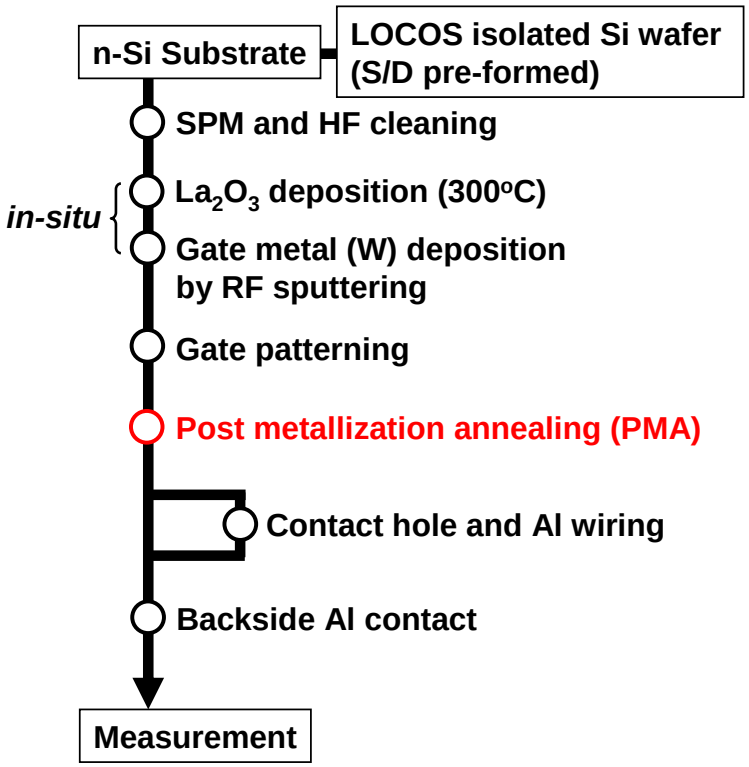


Figure 5.2 *Report of high-k/metal gate process.* ***(a)*** *high-k-fast/metal-last and* ***(b)*** *gate first.*

Figure 5.3 shows the sample fabrication process for MOS capacitors and MOSFETs. The La_2O_3 was deposited by e-beam evaporation in an ultra-high vacuum chamber, followed by *in-situ* metal deposition by RF sputtering. The thickness of W metal was 50nm. The post-metallization annealing was performed with various temperatures, times and atmospheric to establish the optimum condition for improving the interface properties. Source and drain pre-formed Si substrate were utilized to fabricate the MOSFETs. The substrate doping concentration is 3 x 10^{16} cm^{-2}. Al was deposited on the source/drain region and back side of the substrate as an electrical contact. Split C-V method was employed to measure the effective mobility of MOSFET. The charge pumping measurement was carried out to evaluate the interface state density.



(a)

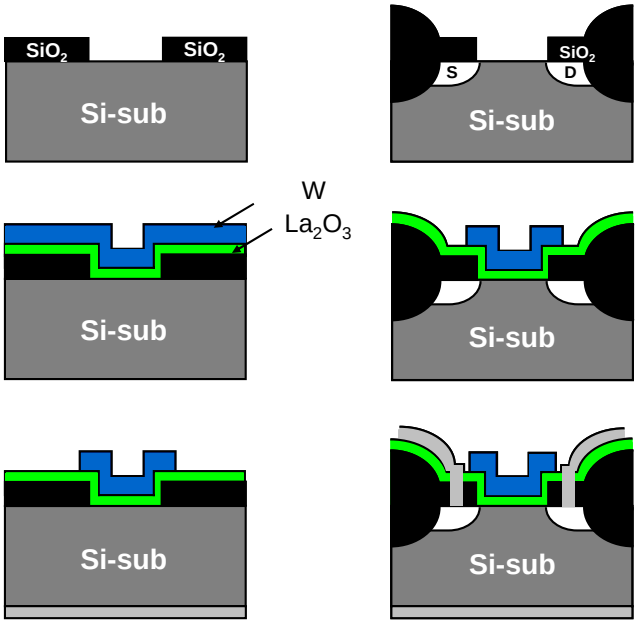


Figure 5.3 (a) *Sample fabrication process. Schematic illustration of* ***(b)*** *MOS capacitor and* ***(c)*** *MOSFET.*

5.3 Optimization of Post-Metallization Annealing

Figure 5.4 shows the relationship between EOT and annealing temperature. The annealing ambient is forming gas (H_2 : N_2 = 3% : 97%). The annealing time is 30min. As expected, EOT dramatically increase with increasing the annealing temperature. This is because the excess silicate reaction with Si substrate by increasing the annealing temperature. Moreover, increment of physical thickness with low dielectric constant layer is also considered.

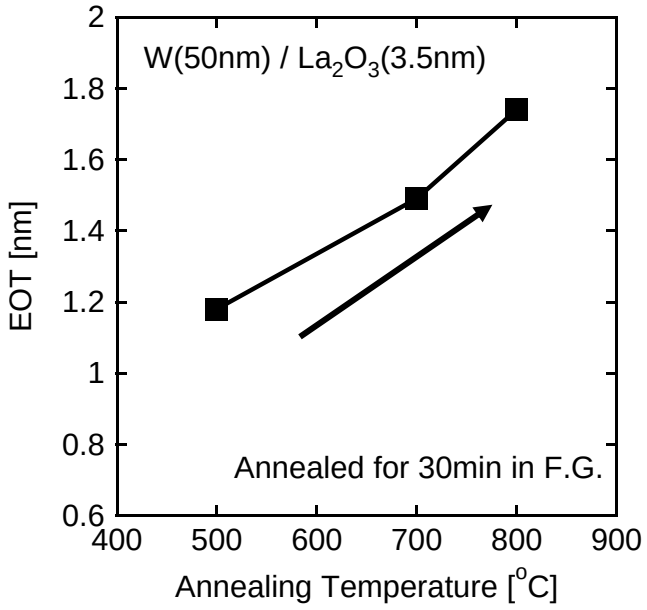


Figure 5.4 *Relationship between EOT and annealing temperature.*

To investigate whether the EOT increase is due to the silicate reaction with Si substrate or not, XPS analysis was carried out. Figure 5.5 shows the Si *1s* spectra as a function of annealing temperature. The Si *1s* spectra were analyzed through the W metal layer with about 5nm in thickness to avoid moisture absorption of La_2O_3 dielectrics. The photoelectrons at higher binding energy against un-oxidized Si substrate peak indicate the formation of La-silicate layer shown in Figure 5.5. The peak intensity of the La-silicate layer increase with increasing the annealing temperature. This is the experimental evidence for increment of the EOT due to silicate reaction with Si substrate.

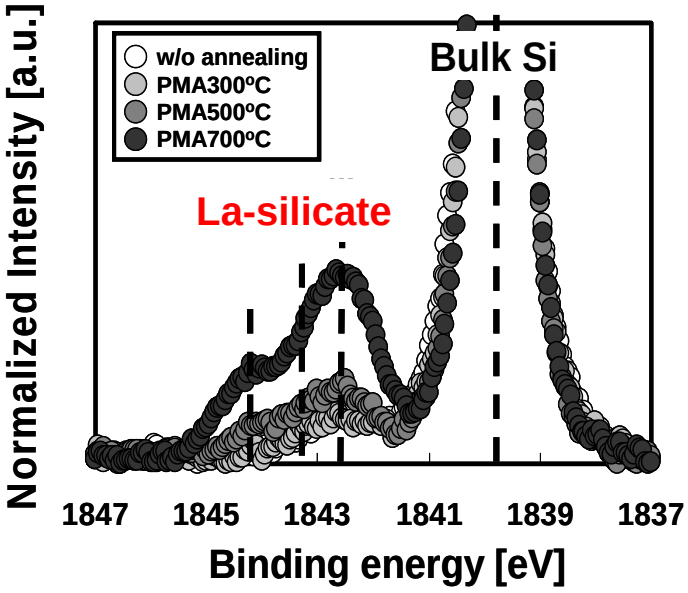


Figure 5.5 *Si 1s spectra as a function of annealing temperature.*

The SiO_x interfacial layer is formed with HfO_2 gate dielectrics after annealing process as shown in chapter 3. The formation mechanisms of the SiO_x interfacial layer underlying the HfO_2 is quite different compared with thermally-grown SiO_2 [5.6]. The SiO_x interfacial layer underlying the HfO_2 is inferior to thermally-grown SiO_2 in quality. That is why the interfacial layer is formed prior to the HfO_2 deposition. On the other hand, the C-V characteristics with La_2O_3 dielectrics after high temperature annealing were improved as shown in chapter 3. The impact of high temperature annealing on interface properties were closely examined. Figure 5.6 shows the impact of the annealing temperature on the C-V characteristics. The hump of C-V curve indicates the large interface state density [5.7]. A large frequency dispersion of the hump can be confirmed from the C-V curves of FGA at 500 ^{o}C. Because the carriers can not respond to the AC signal with increasing the frequency of C-V measurement, the hump in C-V

curve associated with interface state density becomes progressively smaller. The large frequency dispersion of the hump in C-V curve indicates the large interface state density. The frequency dispersion of the hump in C-V curve is dramatically reduced by increasing the annealing temperature. The C-V curves of FGA at 800 ^{o}C are almost identical with various frequencies. It implies the small interface state density, resulting in the improving effective mobility. However, the frequency dispersion of hump in C-V curve is qualitative evaluation. A Quantitative estimation of the interface state density should be conducted. The detailed results will be described later.

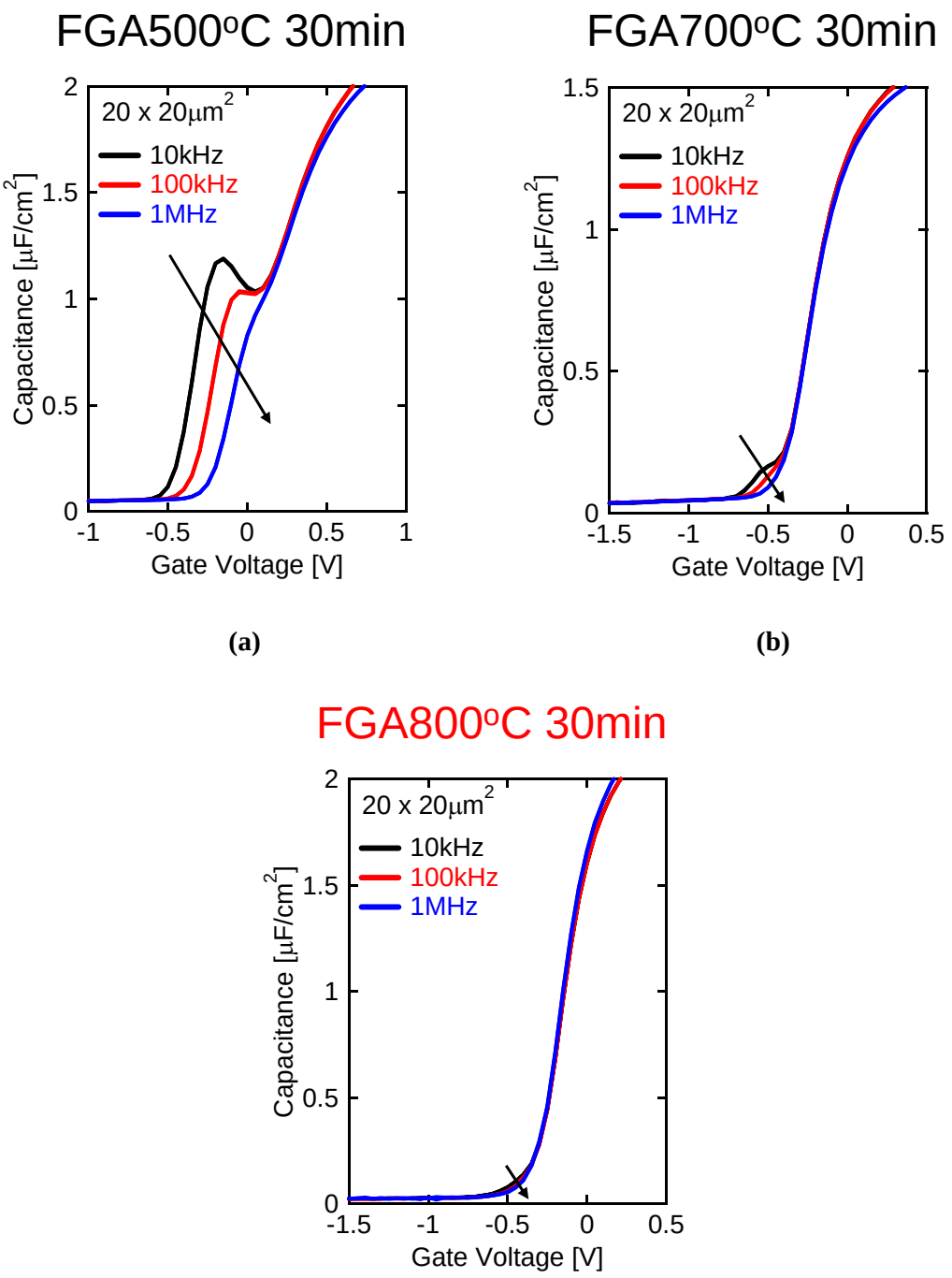


Figure 5.6 *Impact of annealing temperature on C-V characteristics.* ***(a)*** *FGA500 °C,* ***(b)*** *FGA700 °C and* ***(c)*** *FGA800 °C*

Figure 5.7 shows the fitting result by using NCSU CVC [5.8]. The annealing condition is at 800 ^{o}C for 30min in forming gas ambient. The experimental C-V curve completely coincides with ideal C-V curve. It was found that La-silicate with high temperature annealing shows the excellent interface properties.

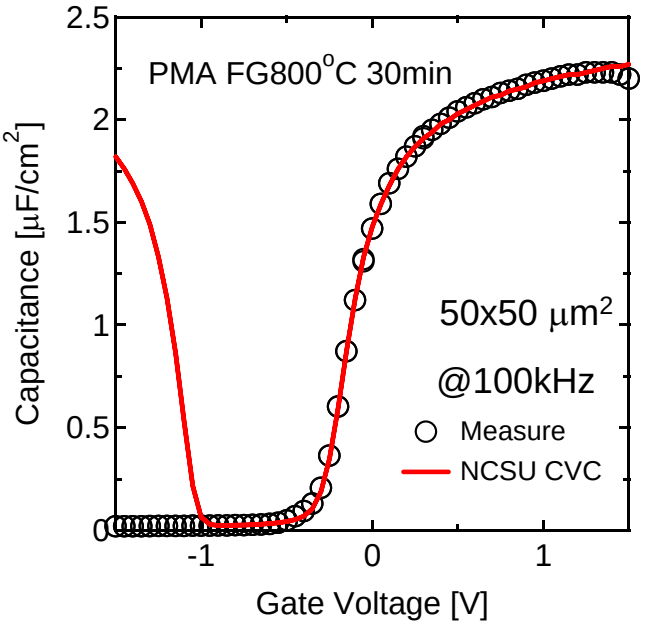


Figure 5.7 *Comparison between experimental and calculated C-V characteristics.*

Next, the effect of atmospheric during the annealing process was investigated. In conventional MOSFET process, high temperature annealing, such as source/drain activation, is typically performed in nitrogen ambient. Figure 5.8 shows the effect of atmospheric during the annealing process on C-V characteristics with various annealing conditions. The capacitance value significantly reduced with nitrogen ambient. The EOT is more than twice thicker with nitrogen ambient compared with that of forming gas ambient. The SiO_x interfacial layer will be formed after high temperature annealing

in nitrogen atmospheric by considering the significant EOT increment. It was found that the high temperature annealing should be conducted in reduction ambient to obtain close to the ideal C-V characteristic and suppression of EOT increment.

Subsequently, optimum annealing time was examined. The source/drain activation is typically performed from 2 to 5 second. The dependence of the annealing time on the C-V characteristics was conducted to optimize the annealing condition. The annealing temperature and ambient is 800 ^{o}C and forming gas, respectively. Figure 5.9 shows the C-V characteristics as a function of annealing time. The annealing time below 5min is insufficient for improving the interface properties. The C-V characteristic with 30min in annealing time is most close to the ideal C-V characteristics.

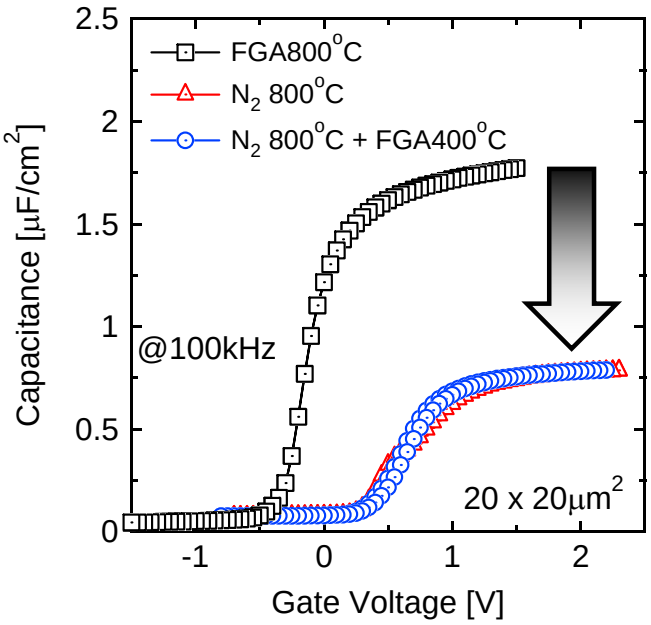


Figure 5.8 *Effect of atmospheric during annealing process on C-V characteristics.*

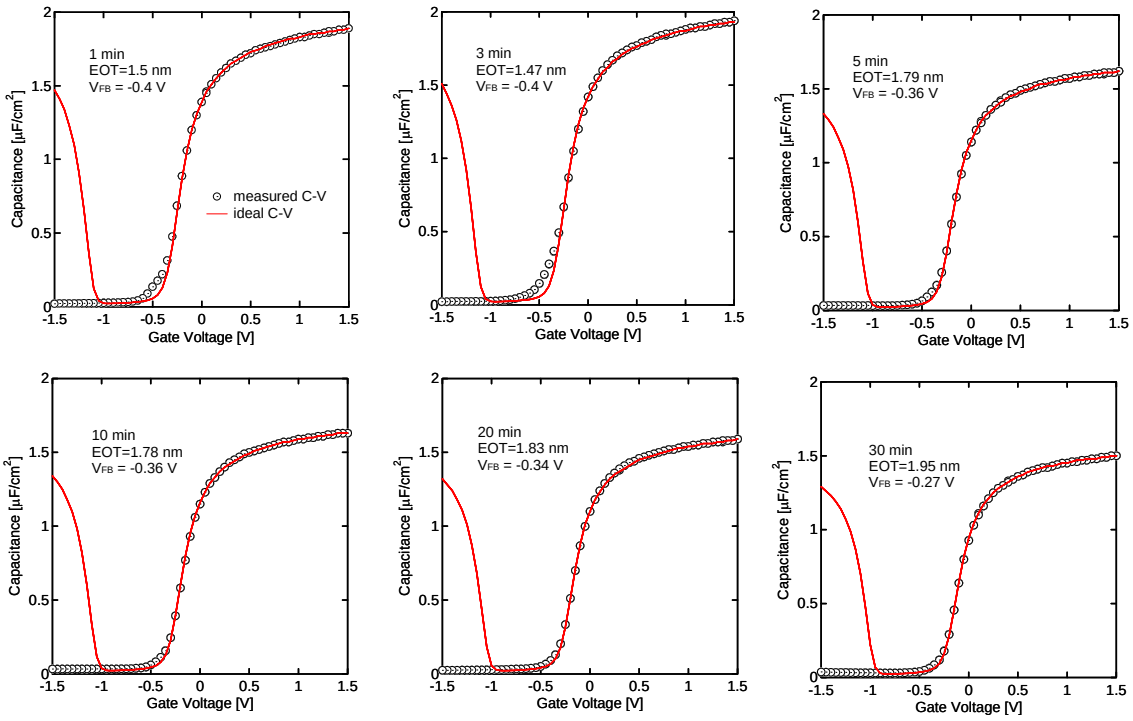


Figure 5.9 *C-V characteristics as a function of annealing time.*

Figure 5.10 shows the EOT and V_{FB} as s function of annealing time estimated by fitting with NCSU CVC. Although the EOT value is abruptly varied at annealing time from 3min to 5min, the EOT starts to saturate annealing time above 5min.

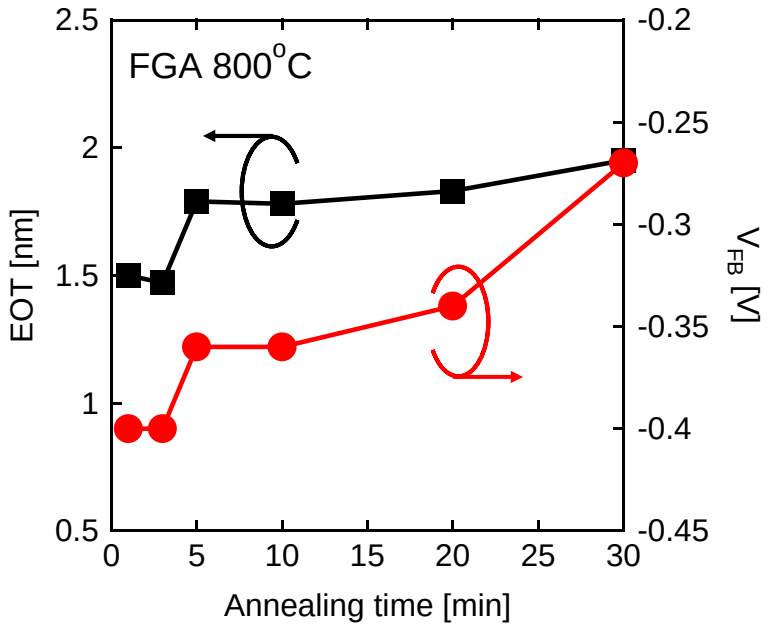


Figure 5.10 *EOT and V_{FB} as s function of annealing time.*

Finally, the impact of annealing condition on nMOSFET characteristics was investigated. The post-metallization annealing was performed with various temperatures at 30min in forming gas ambient. As previously mentioned, the interface state density should be quantitatively examined. The charge pumping method was carried out to evaluate the interface state density. Figure 5.11 shows charge pumping current as a function of pulse frequency. Small charge pumping current corresponds to the small interface state density. The small charge pumping current is clearly observed by increasing the annealing temperature. These results completely coincide with results of the frequency dispersion of hump in C-V curve as shown in Figure 5.6. An average interface state density can be estimated from the slope. The interface state density by 1.6 x 10^{11} $cm^{-2}eV^{-1}$ was confirmed using charge pumping method. Though this result is still larger compared with SiO_2/Si interface, the C-V characteristics close to the ideal C-V

curve can be obtained by FGA800 ^{o}C 30min. Figure 5.12 shows the effective electron mobility as a function of annealing temperature. The EOT is conformed by adjusting the physical thickness during La_2O_3 deposition because the effective mobility is degraded with decreasing the EOT. The effective electron mobility is recovered by increasing the annealing temperature. This is due to the improving interface properties by high temperature annealing. It was found that the interface properties can be dramatically improved by high temperature annealing. As a result, the effective mobility is also recovered.

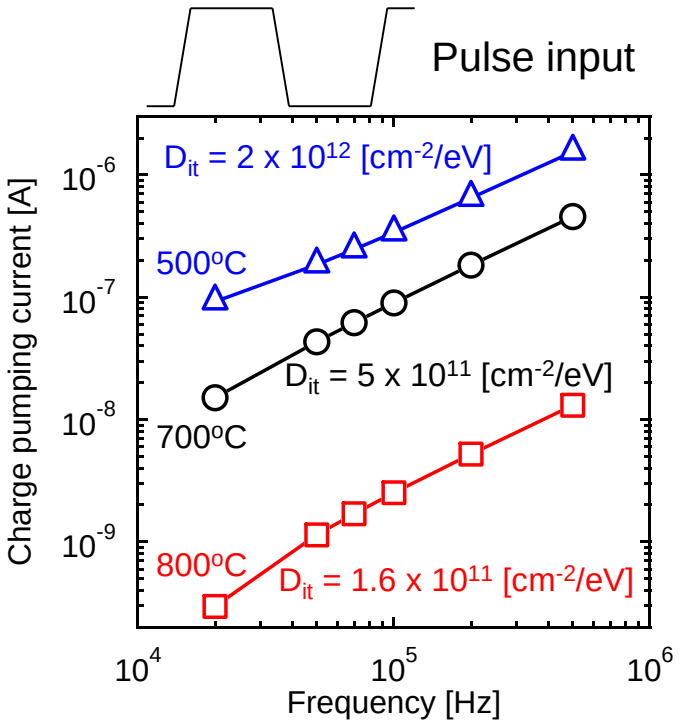


Figure 5.11 *Charge pumping current as a function of pulse frequency.*

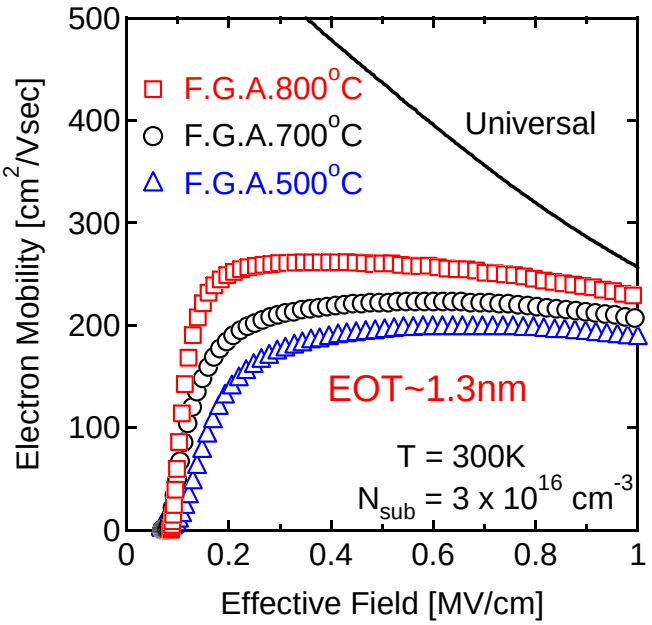


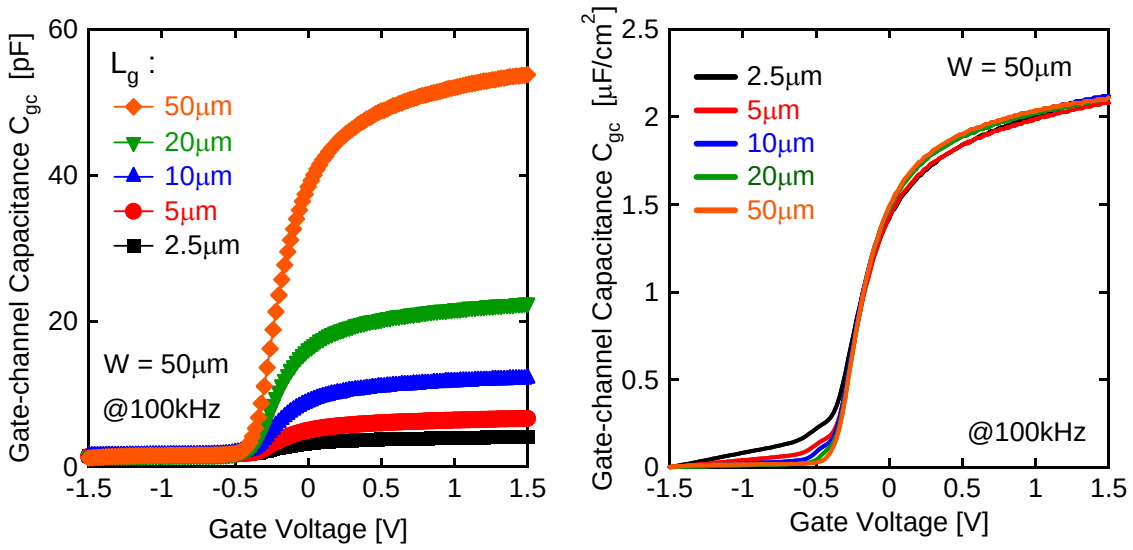
Figure 5.12 *Effective electron mobility as a function of annealing temperature.*

The origin for improving interface properties by high temperature annealing is considered. As previously explained in chapter 4, La_2O_3 gate dielectrics is crystallized after FGA at 500 ^oC for 30min. The peak of La-silicate layer in XPS results is also increased by increasing the annealing temperature as shown in Figure 5.5. It can be speculated that the suppression of crystallization by La-silicate formation may be key factor to improve the interface properties. More precise investigation is necessary. It can be concluded that the optimized post-metallization annealing is 800 ^oC for 30min in forming gas ambient.

5.4 *Evaluation of Effective Mobility with La-silicate dielectrics*

As previously mentioned, the C-V characteristics fairly close to the ideal C-V characteristics can be attained by thermal annealing at 800 ^{o}C for 30min in forming gas ambient. Next, the effective electron and hole mobility were estimated more precisely by split C-V method. The aim of this experiment is to examine the effective mobility of MOSFETs with La-silicate and to develop a plan to recover the effective mobility.

Here, gate length and frequency of split C-V must be determined for accurate mobility extraction. Figure 5.13 (a) shows the gate-channel capacitance as a function of gate length. Figure 5.13 (b) shows the gate-channel capacitance per gate area.



(a) **(b)**

Figure 5.13 *Gate-channel capacitance of* ***(a)*** *measurement data and* ***(b)*** *capacitance per gate area.*

The measurement frequency is 100kHz. Capacitance around threshold voltage gradually increased with decreasing gate length as shown in Figure 5.13 (b). Figure 4.14 shows the gate-channel capacitance per gate area magnified around threshold voltage. Increment of capacitance can be clearly observed with decreasing gate length. This is due to the parasitic capacitance [5.9]. The inversion carrier density can be obtained by integrated the gate-channel capacitance with respect to the gate voltage. The parasitic capacitance leads to the overestimation of inversion carrier density, resulting in underestimate of effective mobility. By using large gate length, it can be avoided.

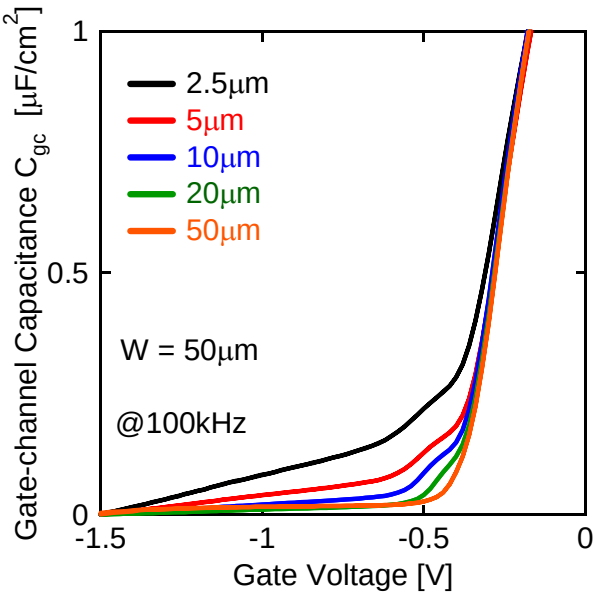


Figure 5.14 *Gate-channel capacitance per gate area.*

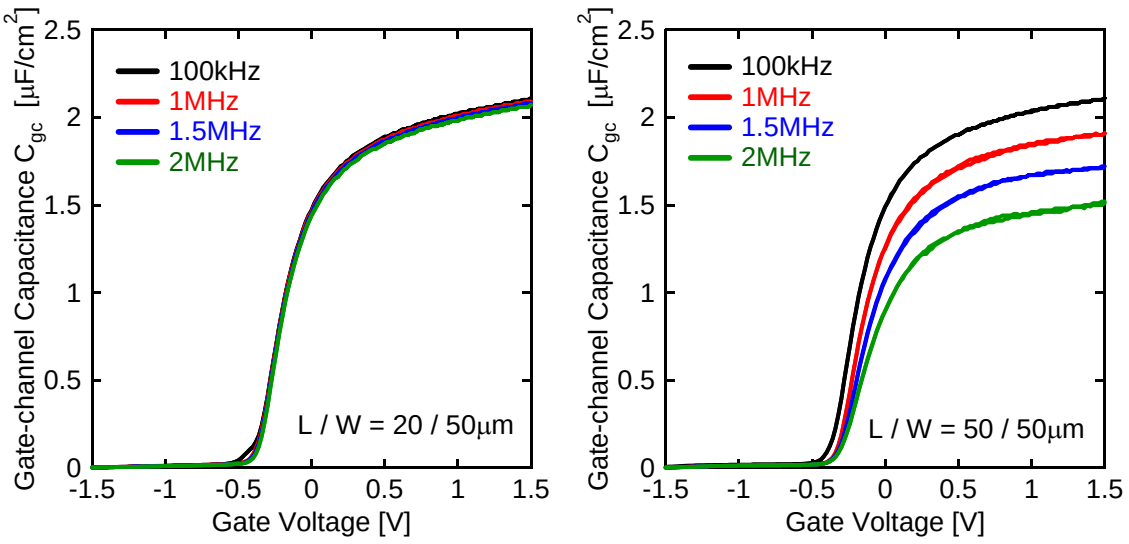


Figure 5.15 *Gate-channel capacitance as a function of frequency. Gate length is* ***(a)*** *20μm and* ***(b)*** *50μm, respectively.*

On the other hand, other problem is appeared by using large gate length. Figure 5.15 shows the gate-channel capacitance as a function of frequency. Capacitance degradation can be confirmed with increasing gate length shown in Figure 5.15 (b). This is the intrinsic phenomena in MOSFETs [5.10]. It can be avoided by utilizing low frequency. However, problem is still remained for using low frequency.

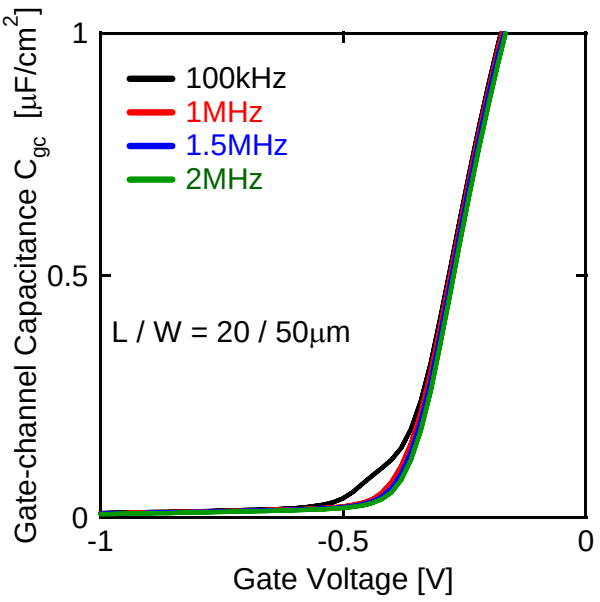


Figure 5.16 *Gate-channel capacitance per gate area as function of frequency.*

Figure 5.16 shows the gate-channel capacitance per gate area as a function of frequency magnified around threshold voltage. Hump in C-V curve due to interface state density can be eliminated by using high frequency. A hump can be confirmed in Figure 5.16 because post- metallization annealing was performed at 700 ^{o}C to observe the frequency dispersion of hump in C-V curve. Thus, it can be concluded that appropriate gate length and frequency are 10 μm or 20 μm and 100kHz or 1MHz, respectively. Next, effective mobility was examined based on these experimental results.

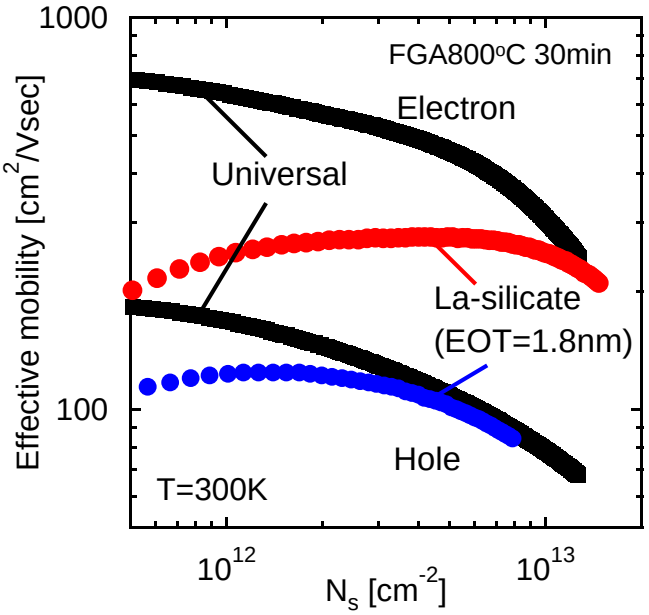


Figure 5.17 *Effective electron and hole mobility with La-silicate gate dielectrics.*

Figure 5.17 shows experimental results of the effective electron and hole mobility with La-silicate gate dielectrics. The universal mobility curves are also shown in Figure 5.17 [5.11]. The effective electron mobility at low inversion carrier density (N_s) region is especially degraded. It indicates the coulomb scattering is dominant scattering event associated with interface state density or fixed charges in high-k gate dielectrics [5.11]. The effective hole mobility is not greatly degraded compared with the electron mobility at low N_s region as shown in Figure 5.17. This is because the universal mobility of hole is already smaller than that of electron. Hence, the effect of coulomb scattering would be weaker for hole [5.2].

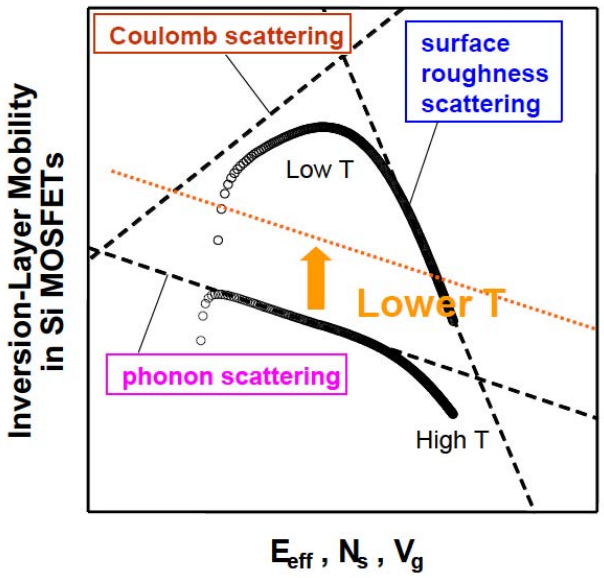
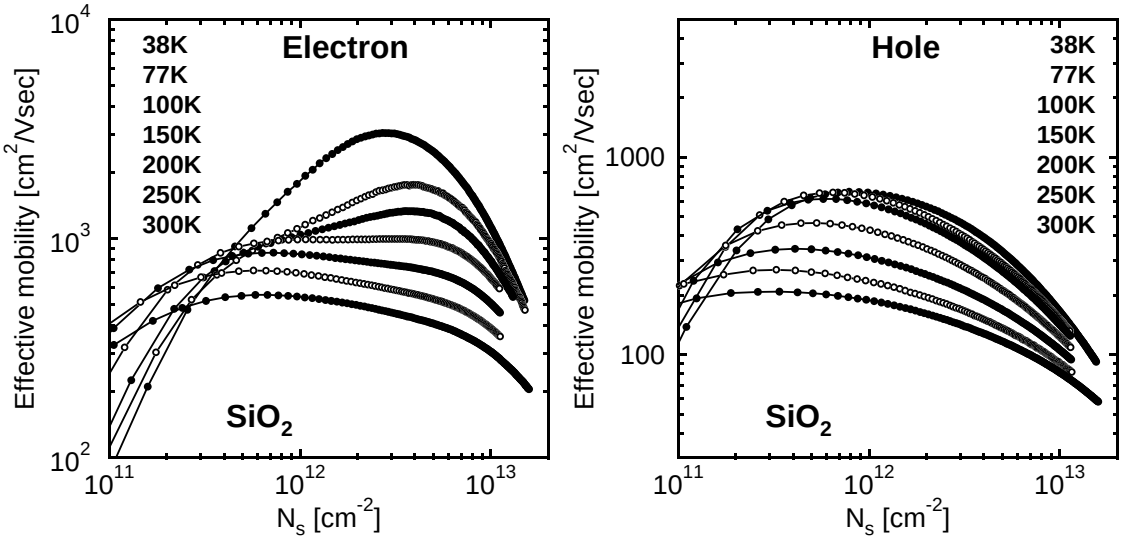


Figure 5.18 *Temperature dependence of the effective mobility in Si MOSFETs [5.11].*

Figure 5.18 shows the temperature dependence of the effective mobility in Si MOSFETs [5.11]. Scattering event in Si MOSFETs can be mainly classified into three mechanisms. As the phonon scattering is lattice oscillation, it is inevitable because of intrinsic phenomena. On the other hand, coulomb and surface roughness scattering can be avoided by improving process technology. By lowering temperature, the effect of phonon scattering can be eliminated. Coulomb and roughness scattering are more clearly observed. Thermally-grown SiO_2 n&pMOSFETs were also fabricated as a reference. The substrate doping concentration is 3 x 10^{16} cm^{-2} as well as that of La-silicate dielectrics to conform the impact of ionized impurity scattering. Figure 5.19 shows the effective mobility in MOSFETs with SiO_2 gate dielectrics as a function of measurement temperature. The effective mobility at N_s = 1 x 10^{11} cm^{-2} increase with increasing the measurement temperature while the effective mobility at N_s up to 1 x 10^{12}

cm^{-2} increase by lowering measurement temperature. At low N_s region, this is the specific trend for Coulomb scattering limited mobility due to interface state density or fixed charges [5.12]. Coulomb scattering limited mobility increase with increasing temperature due to increasing kinetic energy of inversion carrier. Moreover, Coulomb scattering limited mobility also increase with increasing the inversion carrier density due to screening effect [5.11]. On the other hand, the effect of phonon scattering can be eliminated by towering measurement temperature.



(a) **(b)**

Figure 5.19 *Effective mobility in MOSFETs for* ***(a)*** *electron and* ***(b)*** *hole with SiO_2 gate dielectrics as a function of temperature.*

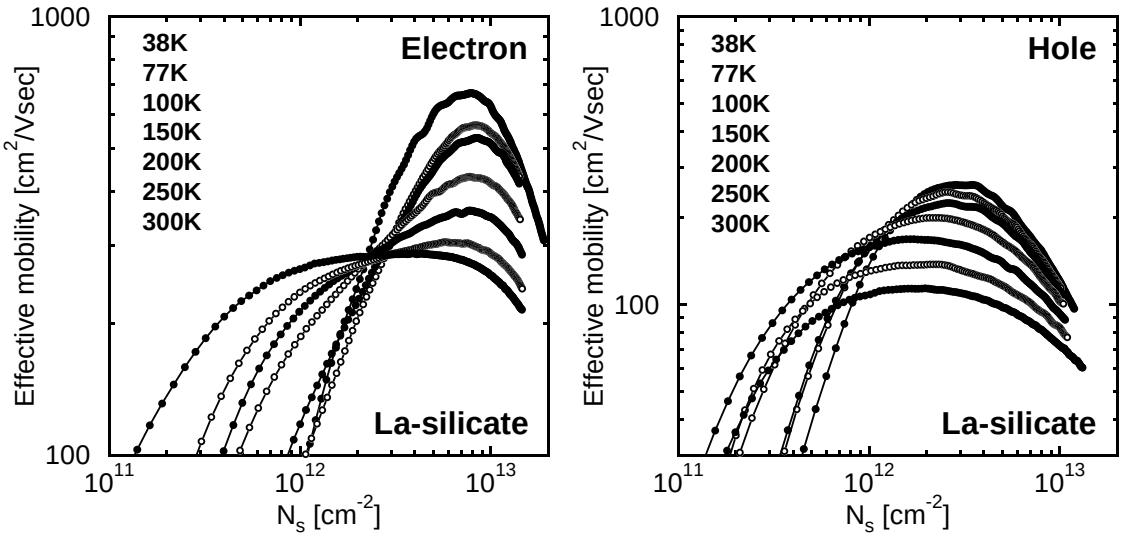


Figure 5.20 *Effective mobility in MOSFETs for* ***(a)*** *electron and* ***(b)*** *hole with La-silicate gate dielectrics as a function of temperature.*

Figure 5.20 shows the effective mobility in MOSFETs with La-silicate gate dielectrics as a function of measurement temperature. Same tendency can be also observed with La-silicate gate dielectrics. However, the effective mobility with La-silicate was not surpasses the mobility with SiO_2 for both electron and hole in all temperature region. To further understand the impact of device process proposed in previous section on the effective mobility, the comparison of the effective mobility at temperature of 38K is shown in Figure 5.21. As shown in Figure 5.18, the coulomb scattering associated with interface state density or fixed charges is dominant scattering event at low N_s region. These results indicate that the large amount of coulomb centers is still existed in high-k gate dielectrics. One of the interesting features is found in Figure 5.21. The weaker N_s dependence of the slope for La-silicate MOSFET can be observed in Figure 5.21 (a). As the temperature is 38K, indicating the phonon scattering is eliminated, the roughness

scattering is dominant at high N_s region. The slope of the SiO_2 MOSFET is inversely proportional to the square of the inversion carrier density. This slope completely coincides with universal mobility curve [5.11]. The effective field (E_{eff}) can be calculated from the sum of inversion and depletion charge density [5.11]. The depletion charge corresponds to the substrate doping concentration. Thus, the depletion charge density is constant. The effective field depends on the inversion carrier density. Figure 5.21 (a) implies that the split C-V measurement was successfully conducted. On the other hand, for hole mobility, the slope for La-silicate MOSFET is almost identical compared with SiO_2 MOSFET. It indicates the same N_s dependence of roughness scattering for hole.

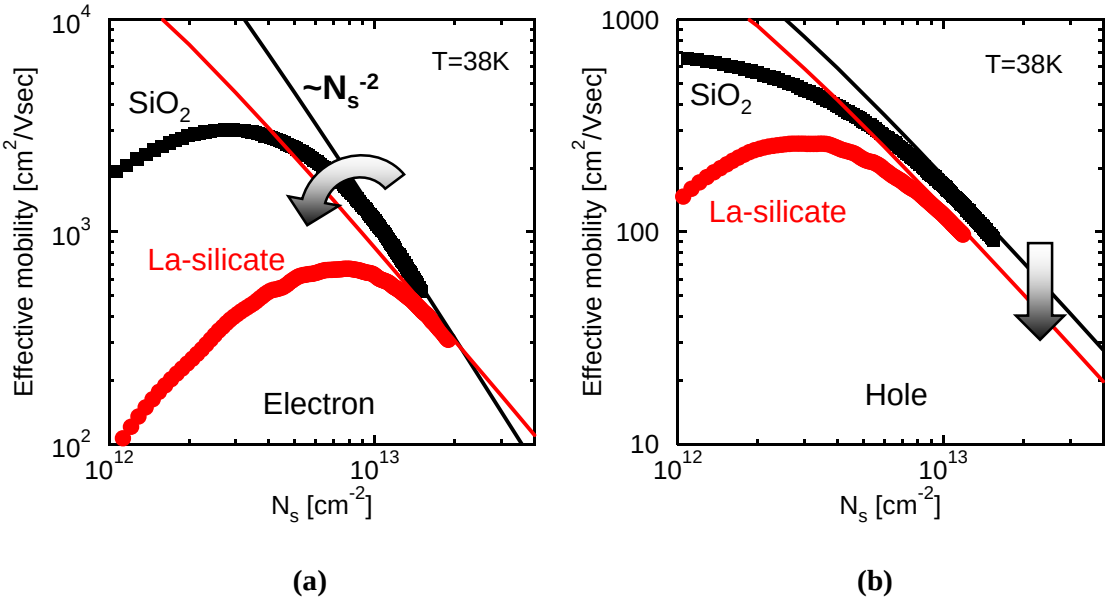
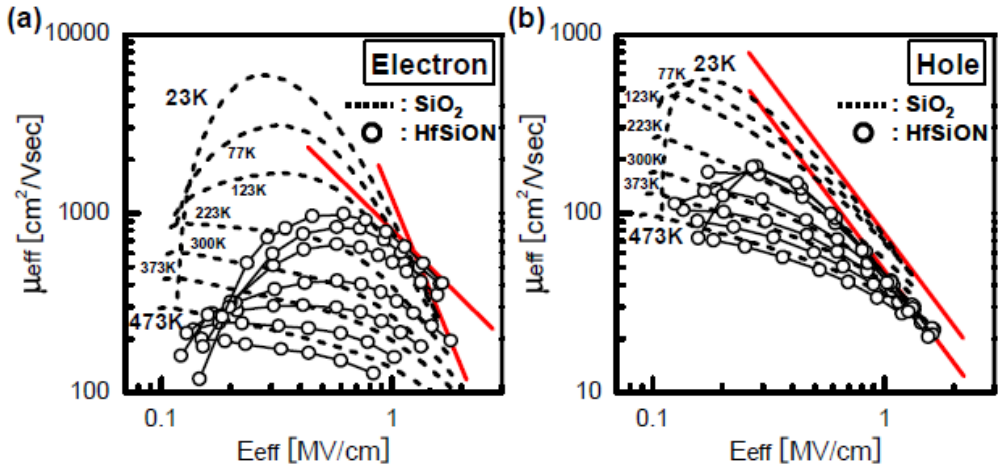


Figure 5.21 *Comparison of effective mobility in MOSFETs for* ***(a)*** *electron and* ***(b)*** *hole at temperature of 38K.*

It was reported that the weaker E_{eff} dependence was also observed in HfSiON gate dielectrics shown in Figure 5.22 [5.13]. This is quite similar to present experimental results as shown in Figure 5.21. It can be speculated that the weaker N_s or E_{eff} dependence of electron mobility is high-k inherent phenomenon.

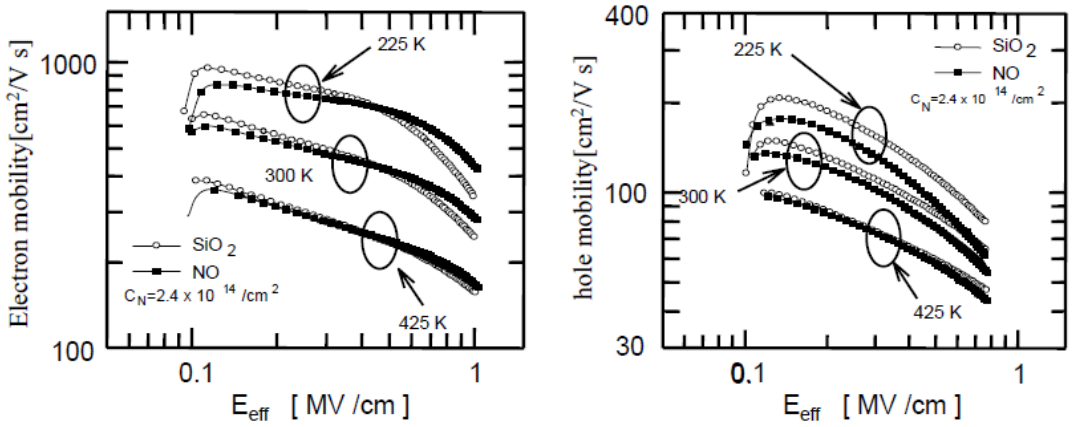


(a) **(b)**

Figure 5.22 *Temperature dependence of mobility in HfSiON dielectrics for* ***(a)*** *electron and* ***(b)*** *hole.*

Figure 5.23 shows the temperature dependence of effective mobility in oxynitride gate dielectrics. According to these reports, the surface roughness is smaller in the oxynitride film than that of SiO_2, resulting in the cause of better electron mobility [5.14]. The effective mobility dependence on correlation length distribution using their model was analyzed. It was estimated that the correlation length distribution of the oxynitride case is Gaussian and that of SiO_2 is exponential. According to these reports, the Gaussian distribution of roughness correlation significantly degrades the mobility of holes compared to the case of the exponential distribution. This is the cause of the degraded

hole mobility. Therefore, strange mobility behavior appears in the high N_s region shown in Figure 5.21 may be explained by analogy to oxynitride gate MOSFETs. However, there are very few experimental results to verify the hypothesis. More systematic study is necessary.



(a) **(b)**

Figure 5.23 *Temperature dependence of mobility in oxynitride for* ***(a)*** *electron and* ***(b)*** *hole.*

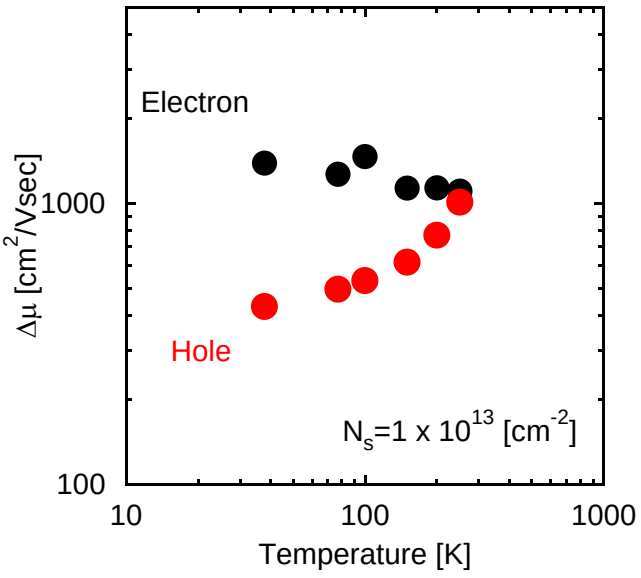


Figure 5.24 *Temperature dependence of* $\Delta\mu$.

The mobility component inherent in La-silicate, $\Delta\mu$, was extracted by using Matthiessen's rule as, $1/\Delta\mu = 1/\mu_{La\text{-}silicate} - 1/\mu_{SiO2}$, where $\mu_{La\text{-}silicate}$ and μ_{SiO2} are mobility of La-silicate and SiO_2 gate dielectrics for MOSFET, respectively. Figure 5.24 shows the temperature dependence of $\Delta\mu$ at $N_s = 1 \times 10^{13}$ cm^{-2}. The $\Delta\mu$ for electron slightly increase with decreasing temperature. It indicates the elimination of remote phonon scattering due to high-k dielectrics [5.13]. In the case of hole, $\Delta\mu$ decrease with decreasing temperature. This implies that the roughness scattering is dominant for hole mobility.

Finally, EOT dependence of effective mobility was examined. As previously mentioned in chapter 1, the effective mobility is decreased with decreasing the EOT. Figure 5.25 shows the EOT dependence of effective mobility. The annealed at 800 ^oC for 30min in forming gas ambient was performed. The reduced effective mobility can be observed for both electron and hole with decreasing the EOT. These results are same as other research of reports. The effective mobility is degraded even in direct contact of high-k/Si structure by decreasing the EOT. Model for decreasing effective mobility by thinner EOT has been reported [5.12]. Their model proposed the impact of metal/high-k interface. However, more precise investigation is need to better understanding the lowering effective mobility by decreasing the EOT.

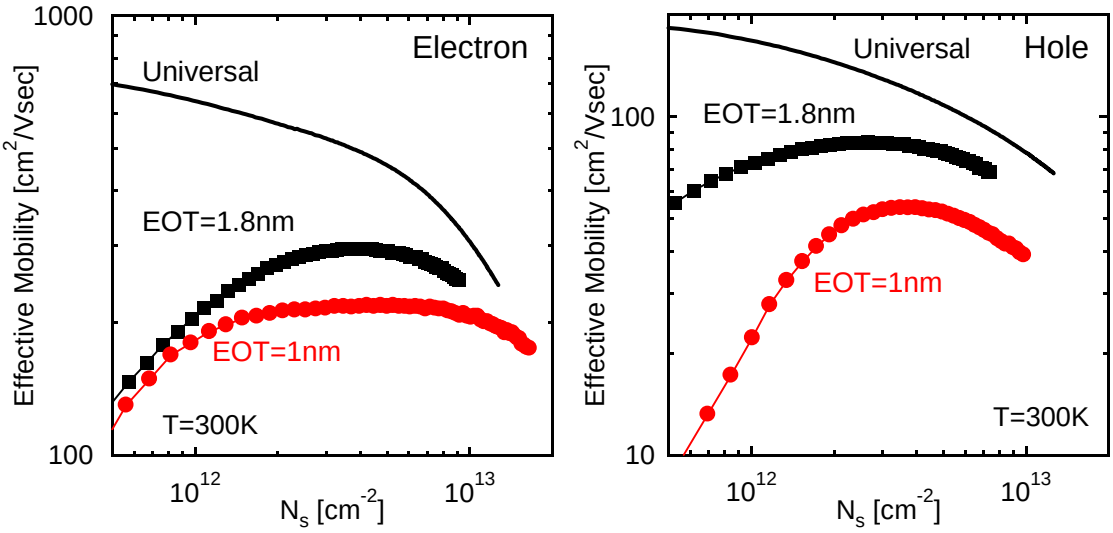


Figure 5.25 *EOT dependence of mobility in La-silicate for* ***(a)*** *electron and* ***(b)*** *hole.*

5.5 Conclusions

The effect of high temperature annealing on electrical characteristics of MOS capacitors and MOSFETs are described in this chapter. The details of the findings are as follows.

It is found that the C-V characteristics close to the ideal C-V curve can be obtained by annealed at 800 ^{o}C for 30min in forming gas ambient. It is revealed that the La-silicate formed by high temperature annealing shows the excellent interface properties. The effective electron mobility can be recovered by high temperature annealing in same EOT value due to its nice interface properties. However, it is also found that large amount of coulomb scattering sources is still existed by low

temperature mobility measurement.

The weaker N_s dependence of electron mobility for La-silicate MOSFET was observed. The strange mobility behavior appears in the high N_s region may be explained by analogy to oxynitride gate dielectrics. However, more systematic study is necessary, such as TEM observation at high-k/Si interface to evaluate the correlation length distribution. The effective mobility is also degraded with direct contact of high-k/Si structure by decreasing the EOT.

Problems remained to be solved are follows. The interface state density with 10^{10} $cm^{-2}eV^{-2}$ order of magnitude would be realized. Fluctuation of composition ratio between La and Si in La-silicate should be investigated. Film condition affects on the dielectric constant, resulting in fluctuation of EOT. It becomes sever problem in highly scaled MOSFETs. Understanding of effective mobility for high-k gate dielectrics is still lacking in spite of its importance.

5.6 References

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Chapter 6 Compensation of Oxygen Vacancy in High-k Gate Dielectrics

6.1 Introduction

As previously mentioned in chapter 5, the high temperature annealing process to obtain the C-V characteristics close to the ideal C-V curve was developed by La_2O_3 in directly contact with Si substrate. The formation of La-silicate by high temperature annealing suggests the improving interface properties. Fairly nice interface state density (D_{it} = 1.6 x 10^{11} $cm^{-2}eV^{-1}$) was attained measured by charge pumping method. On the other hand, the effective mobility is still terrible, especially at low N_s region by low temperature measurement as explained in chapter 5. It indicates that the coulomb scattering canters attributed to the interface state density or fixed charges are existed in gate stacks. Figure 6.1 shows the comparison of effective electron mobility between

SiO_2 and La-silicate for nMOSFETs. The electron mobility with SiO_2 was referred to the previous report [6.1]. According to their report, the interface state density was intentionally generated by Fowler-Nordheim stress. The impact on the interface state density on the electron mobility was experimentally examined. The referred interface state density is the difference value between before and after Fowler-Nordheim stress. However, it is well known that the interface state density at SiO_2/Si interface is less $10^{10}cm^{-2}eV^{-1}$ order by standard fabrication process [6.2]. Thus, it is possible to assume the intentionally increased value (ΔD_{it} = 2 x 10^{11} $cm^{-2}eV^{-1}$) as equal to D_{it} = 2 x 10^{11} $cm^{-2}eV^{-1}$ because the initial interface state density is one or two order of magnitude lower than that of after Fowler-Nordheim stress. To equally compare the impact of interface state density on electron mobility, the La-silicate for nMOSFET with equal amount of interface state density was prepared. The optimized fabrication process was conducted as previously mentioned in chapter 5.

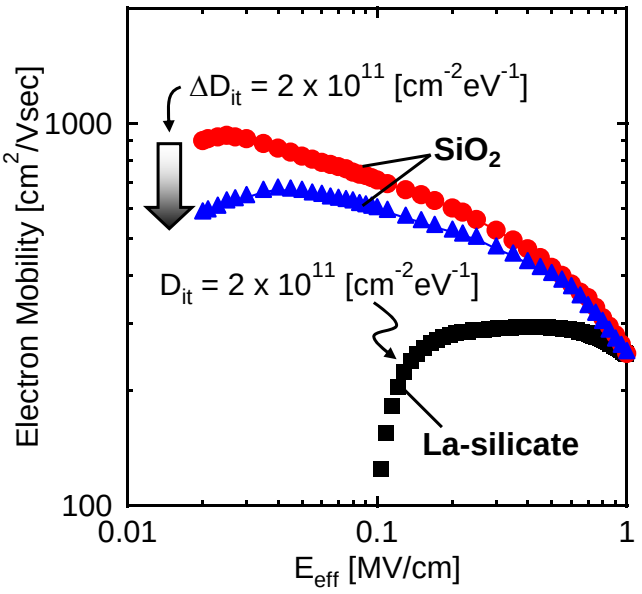


Figure 6.1 *Impact of the interface state density on the mobility with SiO_2 and La-silicate.*

The substrate doping concentration is relatively low level (~10^{16} cm^{-3}) in both devices. The effective electron mobility with La-silicate is degraded at low E_{eff} region even the interface state density is almost identical. It implies that large amount of fixed charges in high-k layer strongly affect on the electron mobility. The method how to eliminate fixed charges in high-k gate dielectrics must be considered for improving effective mobility.

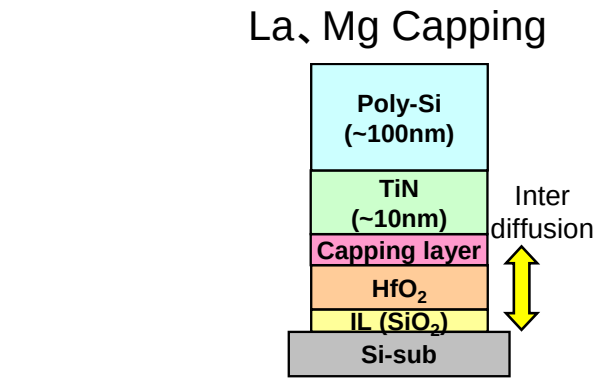
Oxygen vacancy leads to essential influence on MOSFET characteristic have been becoming a common understanding. One of the prominent features in high-k/metal gate system is Fermi level pinning associated with oxygen vacancy [6.3]. As compared to the SiO_2, high-k materials have lot of oxygen vacancies because of its material nature. SiO_2 dielectric is constructed by strong covalent bond while high-k materials have ionic binding properties. How to control of oxygen vacancies by material and process

technology is essential issue for high-k/metal gate system. It appears certain that the effective mobility degradation with high-k gate dielectrics is induced by oxygen defects in high-k layer.

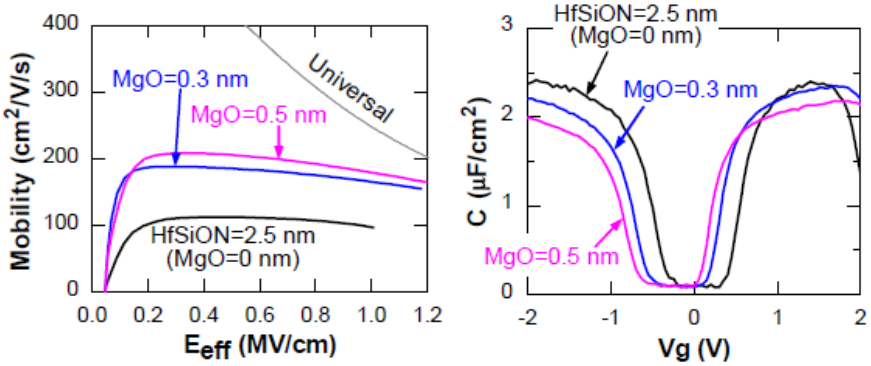
Purpose of this chapter is to study the device/process for compensation of oxygen vacancies to recover the effective mobility. The interface properties can be improved by high temperature annealing as previously mentioned in chapter 5. Therefore, most concerned issue in this study is to ensure the compatibility with improved interface properties. The method lead to the degradation of interface properties should be avoided. Moreover, the EOT increment would be also suppressed. The goal of this chapter is to establish the method for compensation of oxygen defects to improve the effective mobility with maintaining the small interface state density and small EOT increment.

6.2 Reports of Research and Experimental Procedure

Recent theoretical study reveals that oxygen defects in HfO_2 gate dielectrics can be suppressed by elemental addition such as Mg [6.4]. Figure 6.2 shows the effect of Mg incorporation into Hf-based oxides on electrical characteristics. According to this report, Mg element was introduced by capping layer deposited on Hf-based oxides. The capping technique is mainly adopted to modulate the threshold voltage as shown in Figure 6.2 (a) [6.6]. The effective mobility improved by incorporation of Mg while EOT penalty can be also observed.



(a)

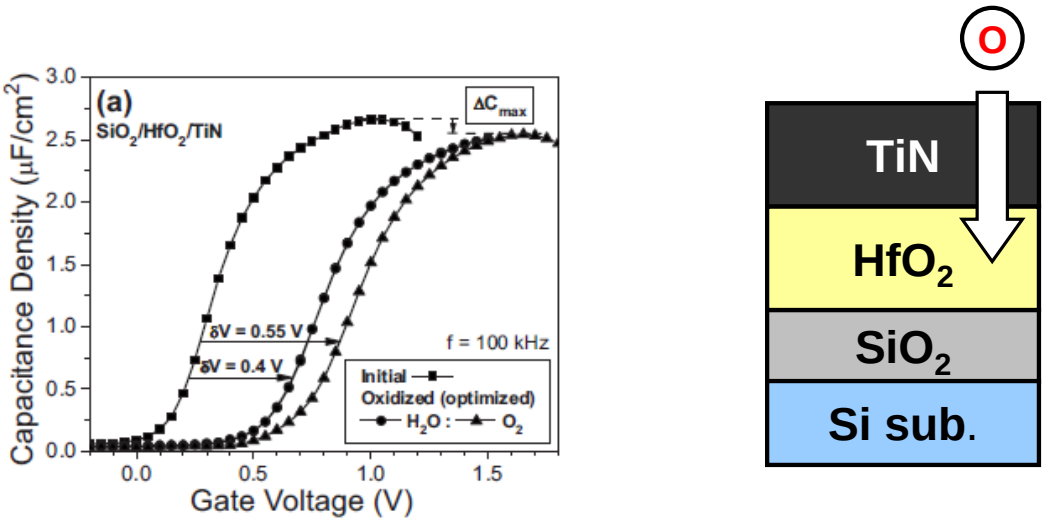


(b) **(c)**

Figure 6.2 *Impact of the Mg addition into Hf-based oxides.* ***(a)*** *device structure,* ***(b)*** *electron mobility and* ***(c)*** *C-V characteristics.*

By simply considering, additional oxygen introduction would be most simple and effective method. Figure 6.3 shows the effect of oxygen incorporation through the metal layer into HfO_2 gate dielectrics after source/drain activation annealing [6.7]. As oxygen vacancies in high-k dielectrics are charged positively [6.3], the flatbad voltage shits the positive direction by oxygen incorporation. This result demonstrates that compensation of the defects in the high-k layer without any cost in the EOT can be attained by process

optimization. This experimental result also indicates the possibility of mobility improvement not only by addition of elements into high-k but also by process such as annealing after gate electrode formation. However, there are few reports for the effect of oxygen incorporation into high-k dielectrics on effective mobility. It is of great interest to compensate oxygen defects in high-k layer for improving mobility by combining the high temperature annealing as demonstrated in chapter 5.



(a) **(b)**

Figure 6.3 *Impact of the oxygen incorporation into HfO_2.* ***(a)*** *C-V characteristics,* ***(b)*** *schematic illustration for oxygen incorporation into HfO_2.*

Device fabrication process is almost same as chapter 5. Process flow is summarized in Figure 6.4. La_2O_3 was deposited on HF-last n-Si wafer for MOS capacitors by e-beam evaporation in an ultra-high vacuum chamber, followed by *in-situ* W (tungsten) metal deposition by RF sputtering. The metal was patterned by reactive ion etching (RIE) with SF_6 chemistry to form gate electrodes. The substrate impurity concentration of

MOS capacitors is $3x10^{15}$ cm^{-3}. The samples were post-metallization annealed in forming gas ambient (H_2:N_2=3%:97%) at 800 ^oC for 30min. Source and Drain pre-formed n-Si (100) substrates were also utilized to fabricate MOSFETs. Al was deposited on the source/drain region and back side of the substrate as a contact. Oxygen ambient annealing (O_2:N_2=5%:95%) was applied to supply additional oxygen into gate stacks. In this study, oxygen ambient annealing is described as "Oxy". Finally, recovery annealing (FGA) was performed. EOT and V_{FB} were estimated by NCSU CVC program. Split-CV method was employed to measure an effective mobility of MOSFETs.

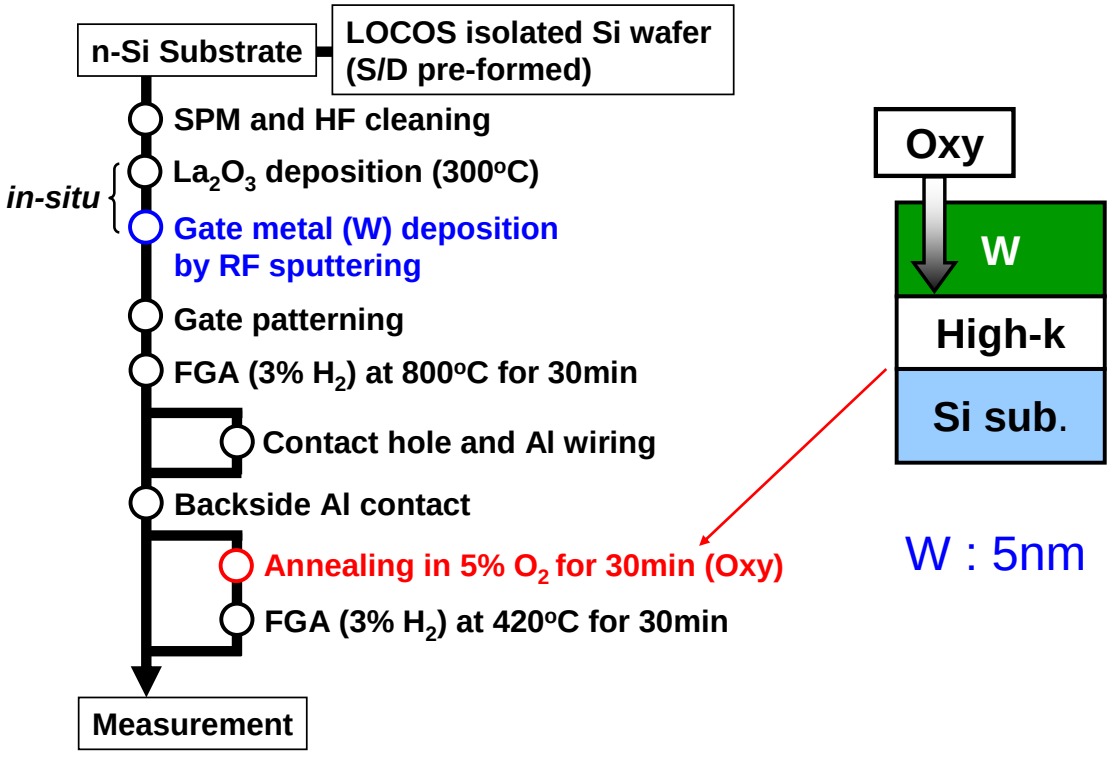


Figure 6.4 *Sample fabrication flow.*

It is considered that key factor for additional oxygen incorporation is metal layer thickness because additional oxygen is supplied through the metal layer. Therefore, W metal is basically arranged at 5nm in thickness. Here, the question is thickness dependence of effective wok function. As previously mentioned, oxygen vacancies is charged positively. Thus, faltband voltage (or threshold voltage) shift toward positive direction is experimental evidence for defect compensation in high-k layer. If the effective work functions of W metal depend on its physical thickness, accurate estimation can not be conducted from shift of faltband voltage (or threshold voltage). Firstly, relationship between the effective work functions of W and its physical thickness was investigated by using thermally-grown SiO_2 pMOSFETs. Utilizing SiO_2 gate dielectrics provide a correct assessment.

Figure 6.5 shows the I_d-V_g characteristics with SiO_2 for pMOSFETs as a function of W metal thickness. The threshold voltage is completely identical with various W thicknesses. It can be concluded that the influence of W thickness on faltband voltage (or threshold voltage) is negligibly small down to W of 5nm in thickness.

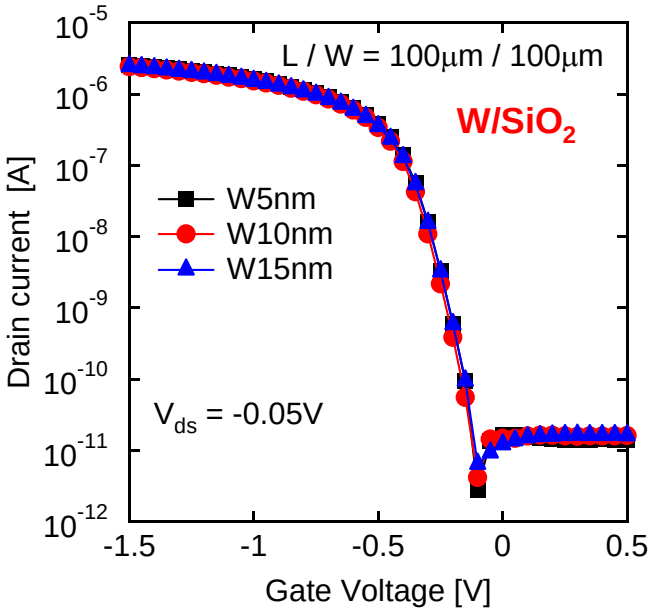


Figure 6.5 *I_d-V_g characteristics with SiO_2 for pMOSFETs as a function of W metal thickness.*

6.3 Experimental Results of MOS Capacitors

The effect of the oxygen ambient annealing on flatband voltage (V_{FB}) shift was examined. Figure 6.6 shows the C-V characteristics of W/La-silicate MOS capacitors. The C-V curves shifted to the positive direction while increasing the annealing temperature. It was reported that oxygen doped W with Ar/O_2 mixture deposition has showed a tuning of the V_{FB} by 400mV toward the Si valence band edge [6.8]. Compared to the report with Ar/O_2 mixture deposition, this experimental result suggests that the oxygen atoms can be successfully introduced into the gate stacks during the oxidant atmospheric annealing. The penalty on the EOT was less than 1Å, therefore, it can be obtained used for positive V_{FB} shift in high-k/metal gate stacks. The C-V curves of

MOS capacitors turn up in inversion region as shown in Figure 6.6. It implies de-passivation of dangling bonds or newly created minority carrier generation center after oxygen annealing [6.9].

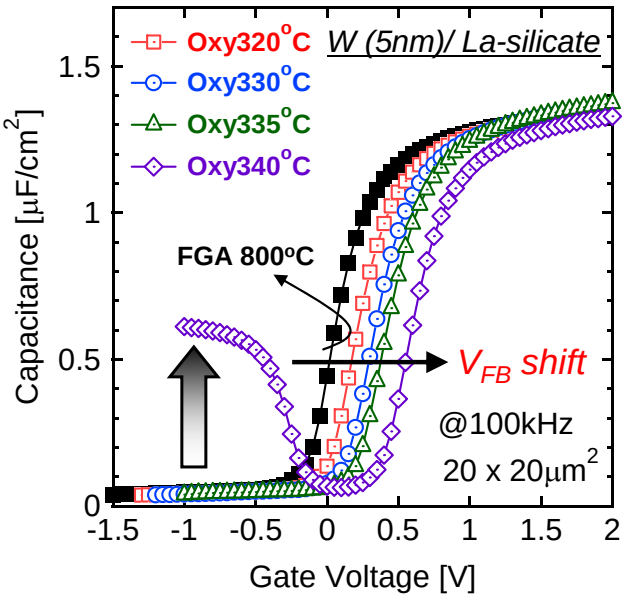


Figure 6.6 *C-V characteristics with La-silicate as a function of oxygen ambient annealing.*

To further understand the influence of the oxygen annealing, the relationship between the V_{FB} shift and EOT increase as s function of oxygen annealing temperature is plotted in Figure 6.7. Although V_{FB} shift monotonically increases at a temperature below 350 ^{o}C, the V_{FB} shift starts to saturate above 360 ^{o}C shown in the dashed line. The EOT increment can be successfully suppressed at a temperature below 340 ^{o}C while EOT penalty exceed 1Å at temperature above 350 ^{o}C. It can be speculated that excess oxygen supply induce formation of low-k interfacial layer such as SiO_x. It is found that large V_{FB} shift and little EOT penalty can be attained by oxygen annealing at temperature of

340 °C for 30min at the same time. Figure 6.8 shows the positive V_{FB} shifts as a function of oxygen annealing time. The oxygen annealing temperature is fixed at 340 °C. The positive V_{FB} shifts monotonically increased with increasing the oxygen annealing time. EOT penalty more than 1Å was not observed at a time blow 30min while the EOT was significantly increased after 1 hour at 340 °C in oxygen ambient. It can be concluded that the annealing at 340 °C for 30min in oxygen ambient is suitable for large V_{FB} shift and little EOT increment.

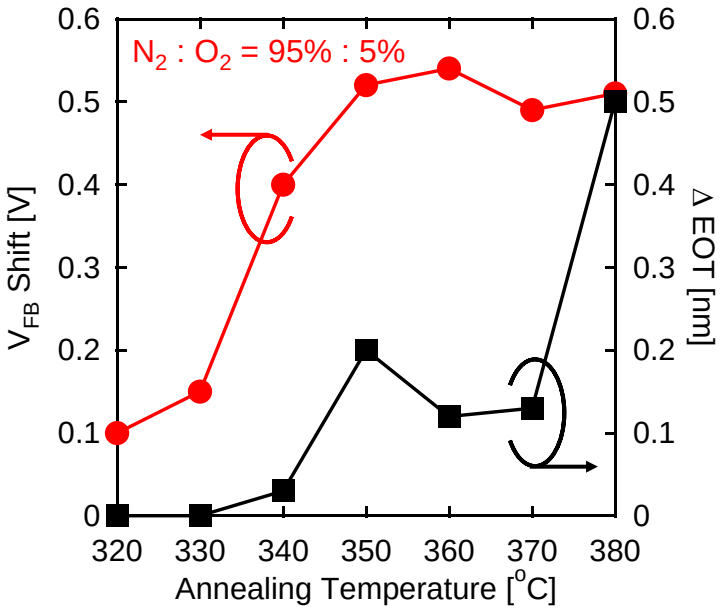


Figure 6.7 *Relationship between the V_{FB} shift and EOT increase as s function of oxygen annealing temperature.*

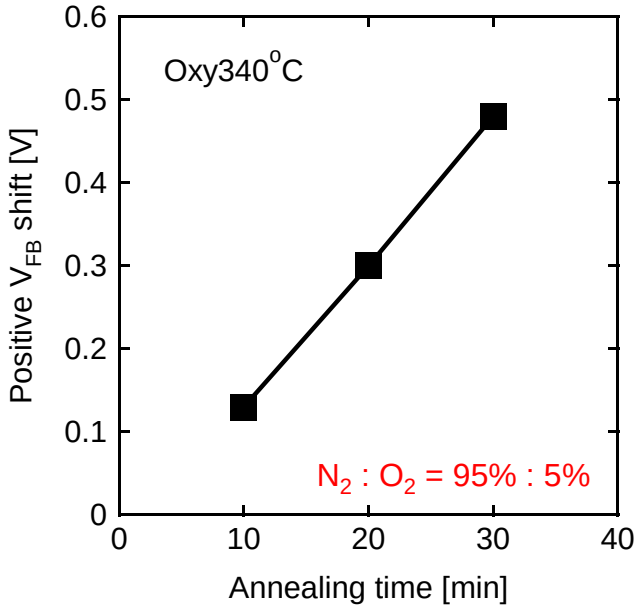


Figure 6.8 *Positive V_{FB} shifts as a function of oxygen annealing time.*

As previously mentioned, the C-V curves of MOS capacitors turn up in inversion region as shown in Figure 6.6. It indicates de-passivation of dangling bonds or newly created minority carrier generation center after oxygen annealing. It is well know that interface property strongly affects the inversion carrier mobility of MOSFET. Forming gas annealing (FGA) is effective to terminate the dangling bonds at SiO_2/Si interface [6.2]. Thus, annealing in forming gas ambient at 420 °C for 30min was performed after oxygen ambient annealing. Figure 6.9 shows the effect of subsequent FGA on C-V characteristics of MOS capacitors with different EOT. The subsequent FGA showed improvement in the C-V characteristics at inversion region while maintaining the V_{FB} at positive value even with the annealing in reduction ambient as shown in Figure 6.9. It indicates that the supplied oxygen atom to compensate the defects in the high-k layer is preserved even after reduction ambient annealing. Moreover, the effect of subsequent

FGA on C-V characteristics can be confirmed irrespective of EOT. It implies that the combination of oxygen annealing with FGA is effective in small EOT region.

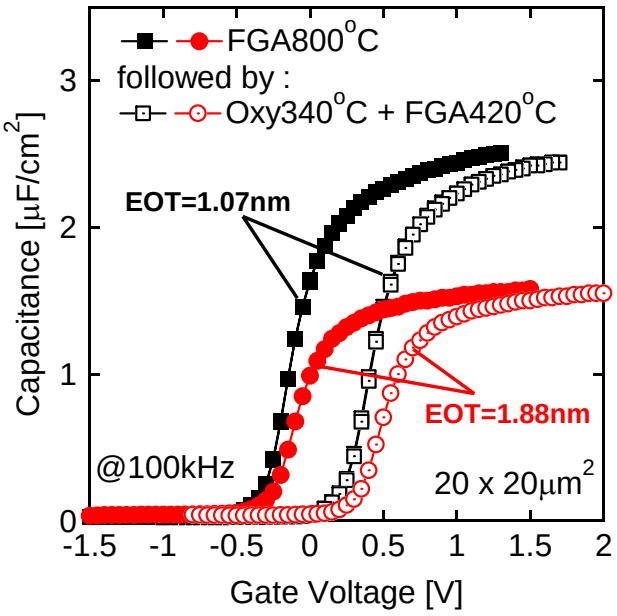


Figure 6.9 *Effect of subsequent FGA on C-V characteristics of MOS capacitors with different EOT.*

The V_{FB} behavior of metals with high work functions was reported to be unstable as shown in Figure 6.10 due to oxygen deficiency in high-k layer [6.9]. The negative V_{FB} shift occurs after FGA at temperature below 400 ^{o}C. Present works are completely different. It suggests that MOSFET characteristics may be improved by recovery annealing with positive V_{th} shift.

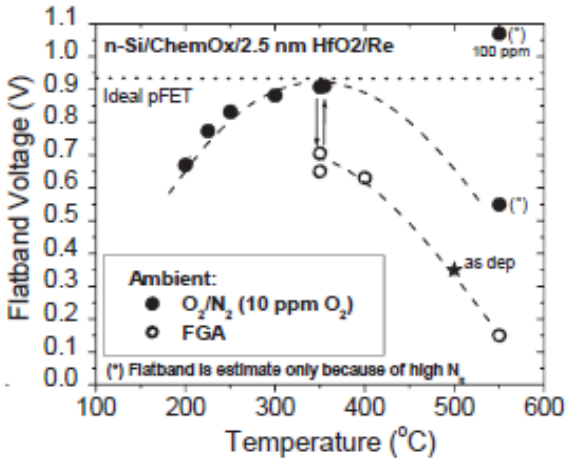


Figure 6.10 *Unstable V_{FB} behavior with high work function metal between oxidation and reduction ambient annealing.*

The effect of oxygen incorporation was previously examined through the electrical characterization with MOS capacitors. Next, TEM observation was carried out to evaluate the influence of oxygen annealing on gate stacks. The samples for TEM observation were utilized the MOS capacitors with EOT = 1.07nm as shown in Figure 6.9. Figure 6.11 shows the TEM images of MOS capacitors with different annealing conditions. The physical thickness of gate dielectrics is almost identical. These results support the little EOT degradation from C-V characteristics after oxygen ambient annealing as shown in Figure 6.9. On the other hand, increment of W metal thickness can be confirmed after oxygen and forming gas annealing as depicted in Figure 6.11 (b). An oxidation of the W metal can be considered. It was reported that oxidized W also has electrical conductivity [6.10]. As shown in Figure 6.9, the C-V characteristics were uneventfully measured. No frequency dispersion is also confirmed.

XPS analysis was subsequently employed to understand the influence of oxygen annealing on gate stacks. The XPS measurements were carried out through the W gate

electrodes with 5nm in thickness as same as MOS capacitors for electrical measurement. Since the W gate is electrically connected to the Si substrate, the Fermi Level of metal and Si substrate coincides. As previously mention, the oxidized W 3*d* peak was observed. Figure 6.12 (a) shows the Si 1*s* spectra of the MOS capacitors with various annealing conditions. The Si 1*s* spectra shift toward lower binding energy while maintain at lower binding energy after oxygen and recover annealing. The Si 1s shift to lower binding energy indicates that the Fermi Level move toward the Si valence band. These results agree with the electrical characteristics of MOS capacitors as shown in Figure 6.9. A structural change in high-k layer caused by the oxygen annealing process was also evaluated because La_2O_3 has material nature to reactively form the La-silicate by thermal annealing. The photoelectrons at higher binding energy against un-oxidized Si substrate peak indicate the formation of a silicate layer shown in Figure 6.12 (a). The structural change in high-k layer can be determined by comparison of the peak intensity ratio. It can be obtained from dividing peak intensity of La 3*d* shown in Figure 6.12 (b) by that of silicate layer. Figure 6.13 shows the peak intensity ratio with various annealing conditions. No significant differences can be observed. This result suggests that there was no structure change or no additional reaction due to oxygen annealing in high-k layer. Oxygen defects in high-k dielectrics are successfully compensated by oxygen incorporation without the any additional silicate reaction.

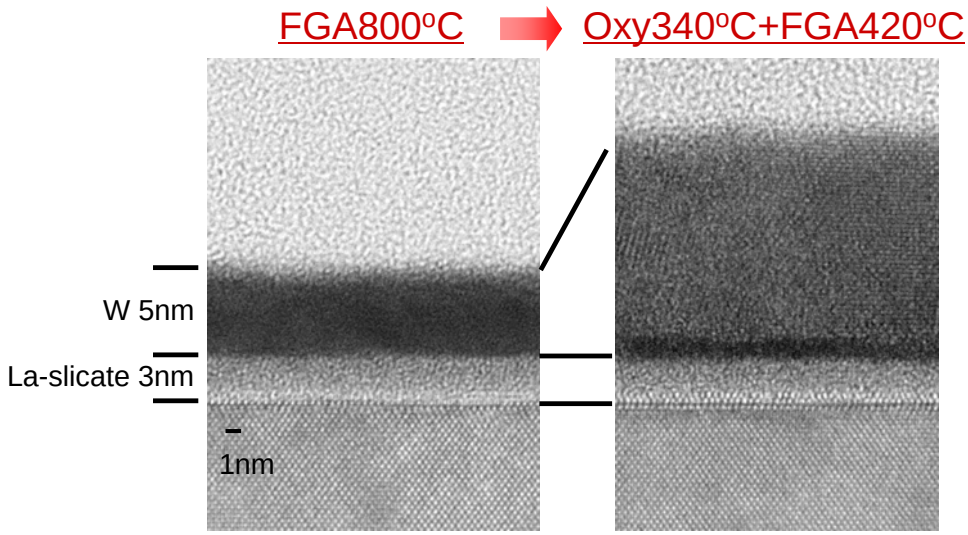


Figure 6.11 *TEM images of MOS capacitors* ***(a)*** *before and* ***(b)*** *after oxygen and recover annealing.*

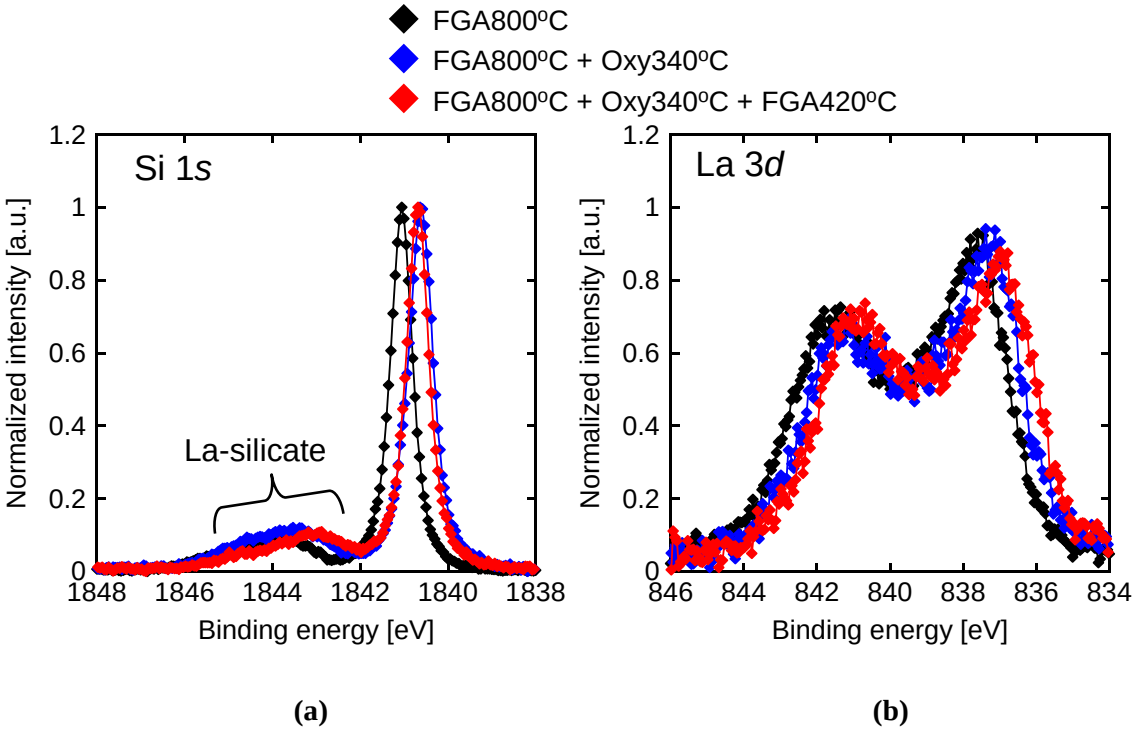


Figure 6.12 (a) *Si 1s spectra and* ***(b)*** *La 3d spectra of the MOS capacitors with various annealing conditions.*

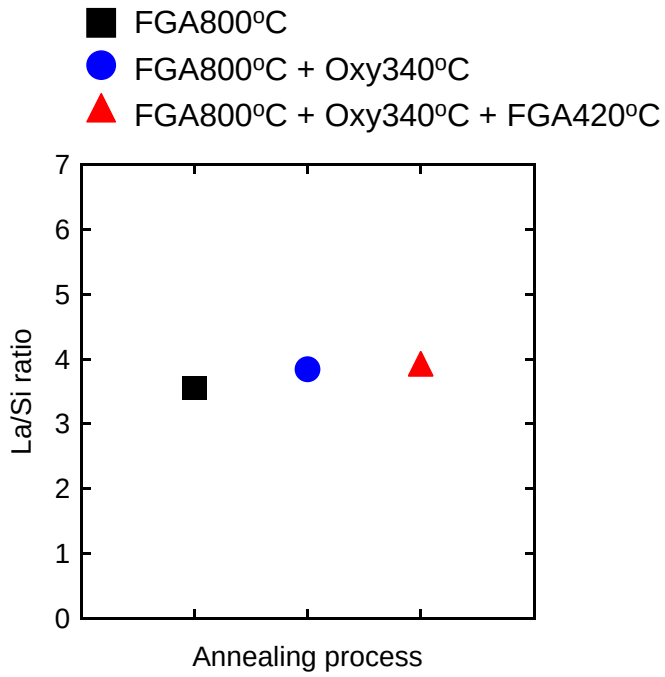


Figure 6.13 *Peak intensity ratio with various annealing conditions.*

As previously mentioned, the thickness of W metal is key factor for oxygen incorporation. The effect of metal gate thickness on the electrical V_{FB} shift was conducted. Figure 6.14 shows the V_{FB} shifts as a function of the thickness of W gate electrode after oxidation annealing with followed by FGA. A Positive V_{FB} shift can be observed with thinner W thickness.

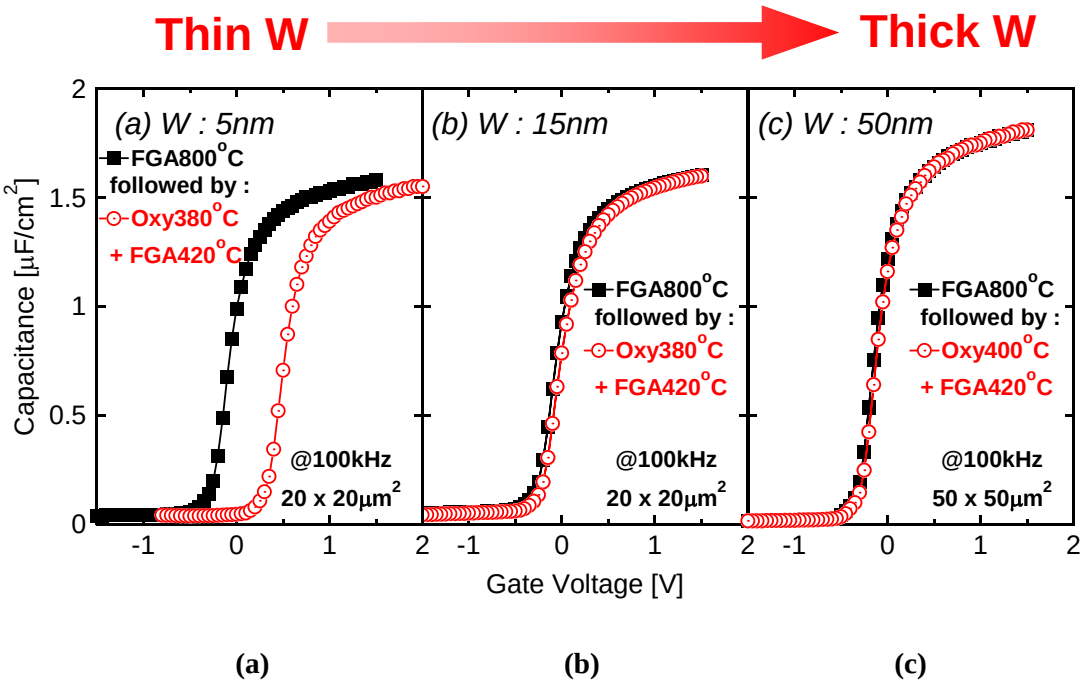


Figure 6.14 *W thicknesses dependence of C-V characteristics. W thickness is* ***(a)*** *5nm,* ***(b)*** *15nm, and* ***(c)*** *50nm, respectively.*

Figure 6.15 shows the relationship between the W thickness and positive V_{FB} shifts. The oxygen ambient annealing was performed at 340 °C for 30min, followed by FGA at 4200 °C for 30min. Positive V_{FB} shift abruptly varies with the thickness of W gate electrode. It is found that the W thickness should be less than 10nm as shown with dashed line in Figure 6.15 to supply additional oxygen into high-k layer through the metal gate. This is well agreement with previous report of $TiN/HfO_2/SiO_2$ gate stacks [6.7]. According to previous report, oxygen is supplied diffuse through the metal gate layer. The present experimental results are well fitted to the calculation with the exponentially-decaying function as shown in Figure 6.15. Therefore, it can be speculated that the oxygen atoms supplied during oxidant ambient to compensate the oxygen deficiency in the high-k diffuse through the W layer and incorporated into the

high-k dielectrics as shown in Figure 6.16.

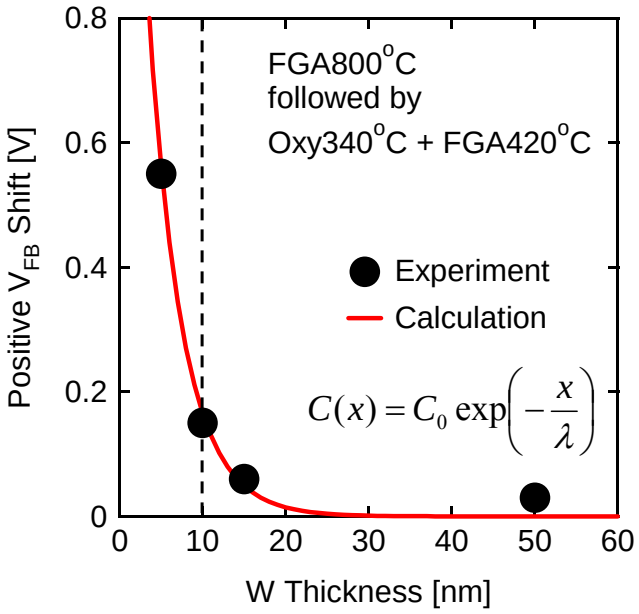


Figure 6.15 *Relationship between the W thickness and positive V_{FB} shifts.*

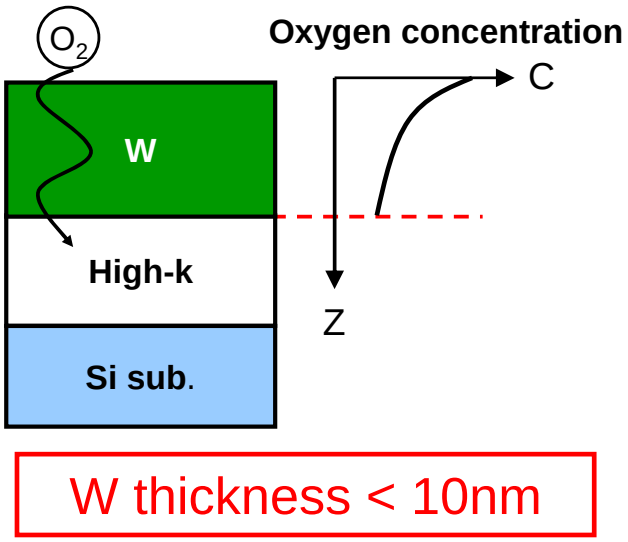
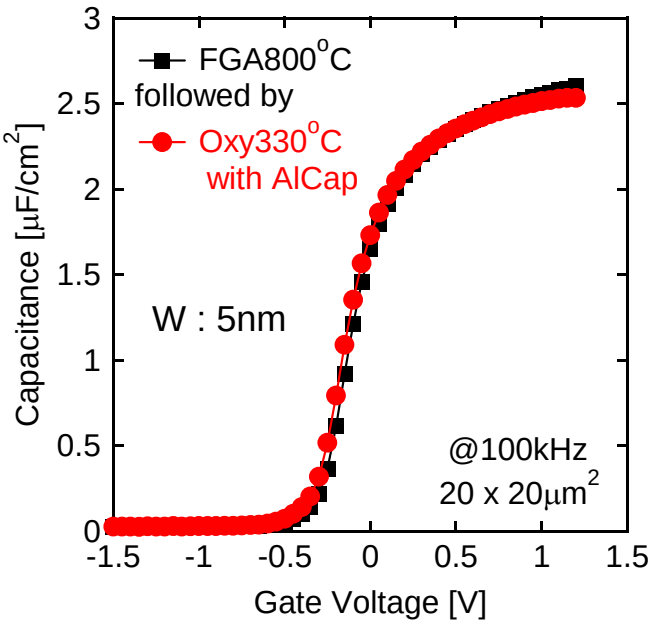
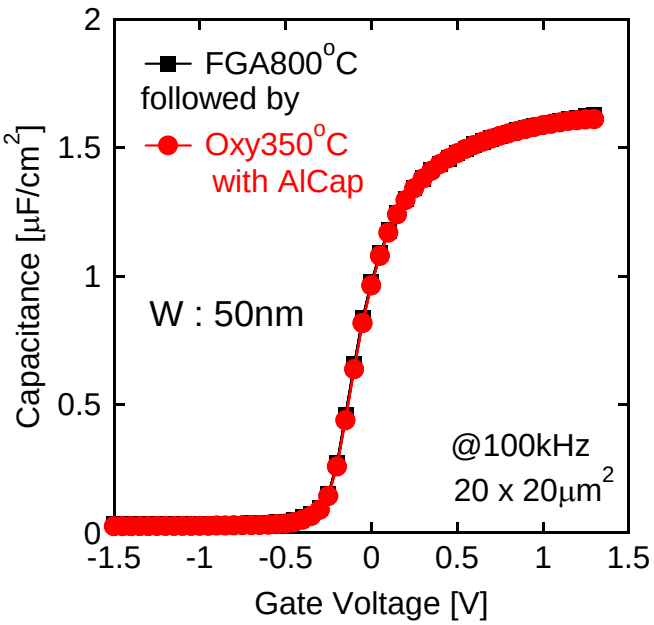


Figure 6.16 *Schematic illustration of diffused oxygen through the metal layer.*

The effect of oxygen annealing on the positive V_{FB} shift was also investigated by other method. It was reported that sputtered W contain large amount of oxygen [6.11]. Excess oxygen in W induces the EOT increment after annealing process. It can be controlled by altering the deposition method from sputtering to chemical-vapor deposition (CVD) [6.12]. In present work, the W metal is deposited by RF sputtering. The additional oxygen into high-k layer is supplied from oxygen atmospheric or not is still unclear. Therefore, source of additionally supplied oxygen was experimentally investigated. To examine whether the additional oxygen is provided from atmospheric or not, most simple method is to deposit Al film. Because an Al_2O_3 is formed at Al surface, oxygen atoms can not pass through the Al_2O_3 layer. The Al_2O_3 layer can play a role to barrier layer. The Al film of 50nm in thickness was deposited on W metal by thermal evaporation after post-metallization annealing at 800 ^oC because a melting temperature of Al is around 600 ^oC. As the thicker W metal is supposed to be the reservoir for large amount of oxygen, MOS capacitors of W metal with 5nm in thickness was also prepared. Oxygen ambient annealing was performed with Al capping layer. Figure 6.17 shows the effect of Al capping by oxygen annealing on V_{FB} shift with different W thickness. The C-V curves in both W thicknesses are almost identical. This is the experimental evidence. No EOT increase and V_{FB} shift can be confirmed from this experiment. Therefore, incorporated oxygen was supplied from oxygen atmospheric during annealing process. It is concluded that the oxygen ambient annealing must be conducted for supplying additional oxygen into gate stacks.



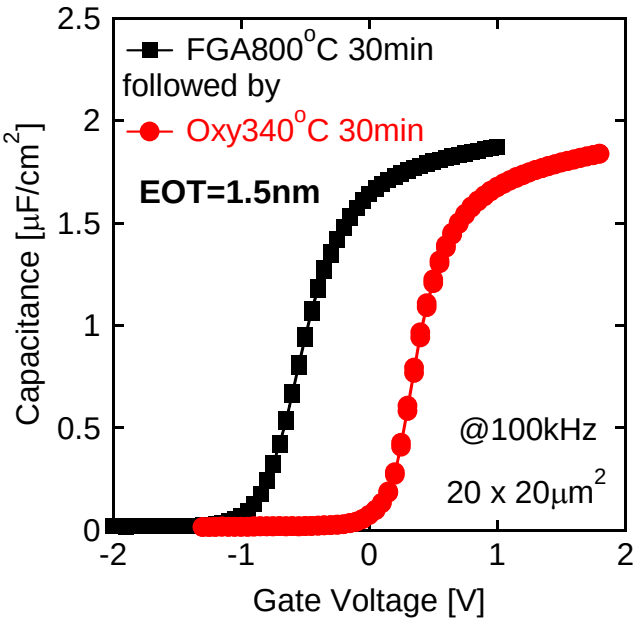
(a)



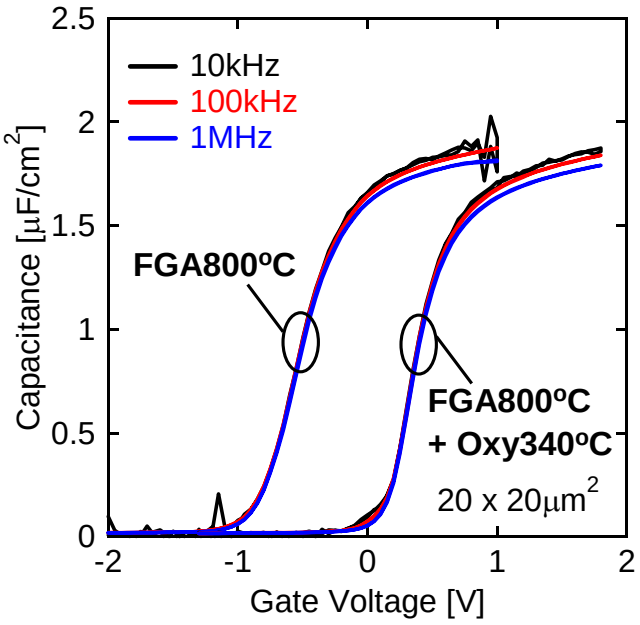
(b)

Figure 6.17 *Effect of Al capping by oxygen annealing on V_{FB} shift. W thickness is* ***(a)*** *5nm and* ***(b)*** *50nm.*

The effectiveness of oxygen ambient annealing was also demonstrated in Figure 6.18. Large negative V_{FB} shift is observed before oxygen ambient annealing in Figure 6.18 (a). Stretch out of C-V curves can be also confirmed. It is considered that degradation of electrical characteristics may be due to initial oxygen defects in high-k layer. Although it is not known exactly why the initial oxygen defects were increased, C-V characteristic was recovered by oxygen annealing. Moreover, the V_{FB} after oxygen annealing is almost same value as previously explained. The frequency dispersion around the flatband voltage is appeared after oxygen annealing as shown in Figure 6.18 (b). It indicates the degradation of interface properties. As previously demonstrated, interface properties can be improved by subsequent recover annealing in forming gas ambient.



(a)



(b)

Figure 6.18 *Demonstration for effectiveness of oxygen annealing.* ***(a)*** *Comparison of C-V curves at 100kHz and* ***(b)*** *frequency dispersion, respectively.*

6.4 Experimental Results of MOSFETs

In previous section, the device structure and annealing process was optimized for oxygen incorporation without EOT penalty. The aim of this chapter is to establish the method for improving the effective mobility. Therefore, in this section, the impact of oxygen incorporation on the effective mobility is investigated through the MOSFET characterization. Firstly, MOSFETs with various W thicknesses were fabricated as shown in Figure 6.19 to investigate whether the same results as MOS capacitors can be obtained or not. Because the fabrication process of MOSFETs is more complex than that

of MOS capacitors. Here, serious problem was occurred. Figure 6.20 (a) shows the I_d-V_g characteristics of pMOSFETs as a function of W thickness. Although the oxygen annealing was not performed, the threshold voltage (V_{th}) shifts toward positive direction with decreasing the W thickness. Figure 6.20 (b) shows the gate-channel capacitances measured by split C-V method. EOT increase and positive shift of C-V curves were confirmed with decreasing W thickness. Previous report revealed that the V_{FB} of MOS capacitor with La_2O_3 on SiO_2 is shifted to positive direction compared with that on Si substrate [6.13]. By considering the increment of EOT and positive shift of C-V curves, formation of SiO_x interfacial layer can be speculated. This is completely different result. V_{FB} of 5nm in W thickness coincides with that of 50nm as shown in Figure 6.17. EOT increase and positive shift of C-V curves with decreasing W thickness could be due to MOSFET fabrication process.

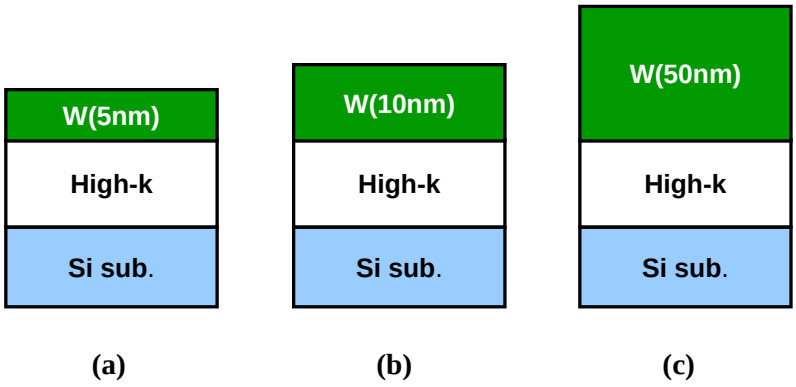
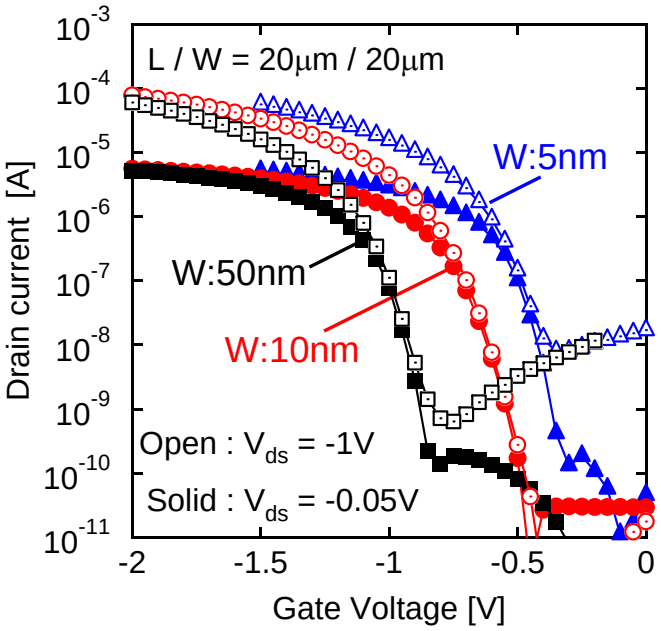
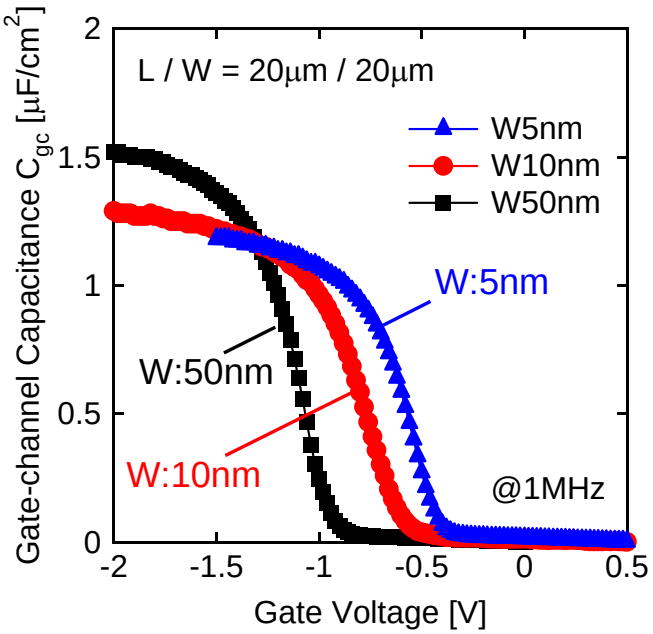


Figure 6.19 *Gate stack structures with various W thicknesses. W thickness is* ***(a)*** *5nm,* ***(b)*** *10nm, and* ***(c)*** *50nm, respectively.*



(a)



(b)

Figure 6.20 (a) *I_d-V_g characteristics and* ***(b)*** *gate-channel capacitance of pMOSFETs as a function of W thickness. Oxygen ambient annealing was not performed.*

The matter for serious problem of MOSFET fabrication is considered by compared with MOS capacitor fabrication. In this work, source/drain pre-formed Si wafer was utilized to fabricate MOSFET. Thus, the difference of sample fabrication process between MOSFET and MOS capacitor is source/drain (S/D) contact formation. To form the source/drain contact by Al wiring, high-k and SiO_2 on source/drain region must be removed. Wet etching such as HCl for high-k removal was not employed because over-etching to underlying gate region was confirmed. Thus, in present experiment, high-k layer was removed by reactive ion etching (RIE) with argon (Ar), followed by SiO_2 etching with BHF. The source/drain contact hole was patterned by lithography with resist film. An Oxygen ashing for 8min to eliminate unwanted resist film was performed twice in total. Most plausible origin of EOT increase and positive shift in C-V curves with decreasing W thickness may be oxidation of W metal. Excess oxygen in W would be diffused into high-k dielectrics during FGA 800 ^{o}C. Oxygen may be easily diffused with decreasing the W thickness. Therefore, blocking layer to prevent oxygen penetration must be formed on W metal layer. As previously demonstrated in Figure 6.17, Al film is effective to suppress the oxygen penetration into metal layer. Moreover, Al film can be easily removed by wet etching process using TMAH. Oxygen incorporation can be conducted after Al film removal. These are the main reason for utilizing Al as a barrier layer. Figure 6.21 shows the MOSFET fabrication process including Al deposition and removal process. A 50nm in Al thickness was deposited on W metal gate. It was also confirmed that Al was selectively removed until underlying W metal layer. Figure 6.22 shows the effect of Al capping layer on I_d-V_g characteristics of pMOSFETs with La-silicate dielectrics as a function of W thickness. By Al capping layer, I_d-V_g characteristics (or threshold voltage) with different W thickness are almost

identical. This is the experimental evidence that excess oxidation of W during oxygen ashing cause the increment of EOT after post-metallization annealing. Unanticipated oxygen incorporation can be avoided with Al capping layer. These experimental results strongly suggest that severe oxygen control must be implemented during not only high-k deposition but also electrode fabrication process. Moreover, these results also provide useful information concerning suppression of EOT increase. Henceforth, Al capping deposition for avoiding excess oxidation was adopted. After high-k etching by RIE with Ar, Al layer was removed by TMAH. Subsequently, post-metallization annealing was performed.

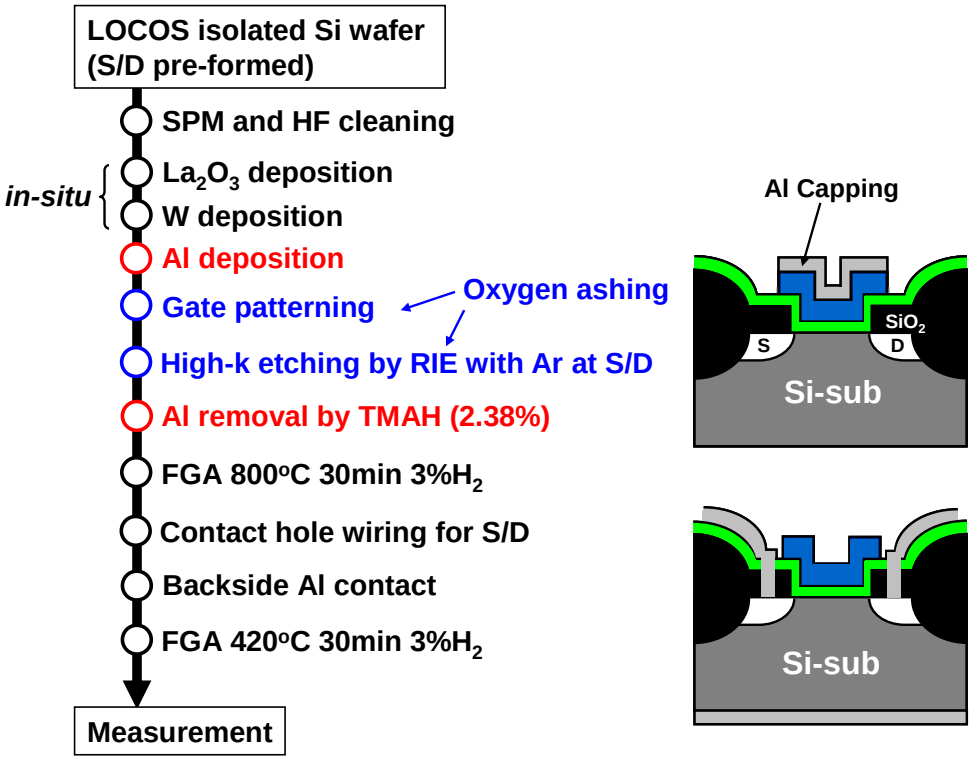


Figure 6.21 *MOSFET fabrication process including Al deposition and removal process.*

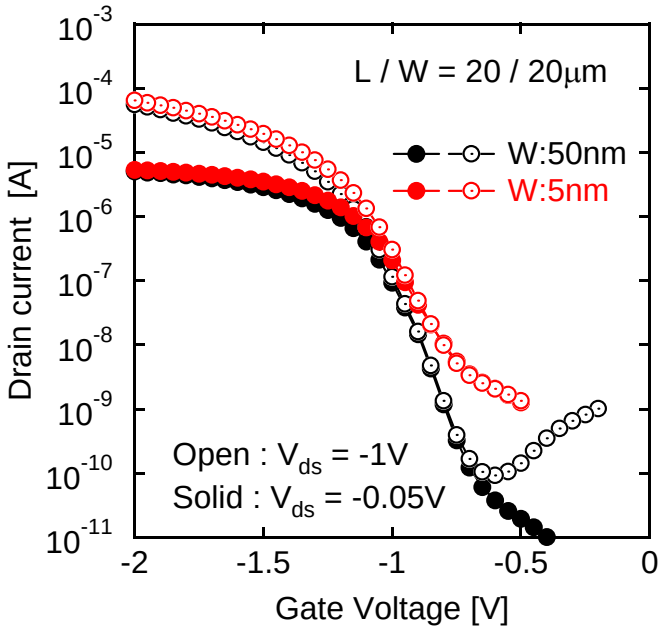
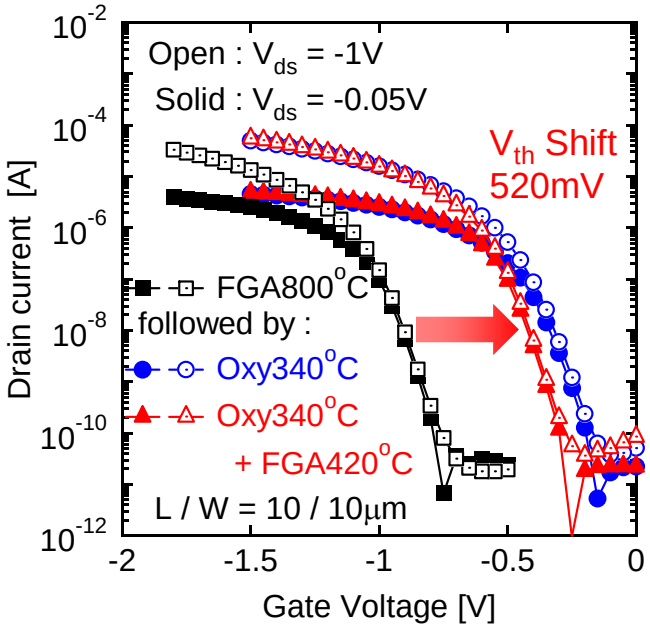


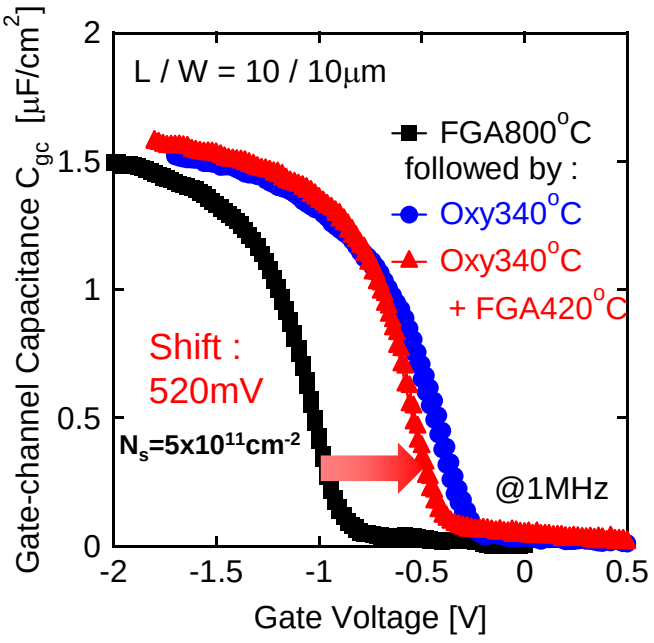
Figure 6.22 *Effect of Al capping layer on I_d-V_g characteristics of pMOSFETs with La-silicate dielectrics as a function of W thickness.*

The effect of oxygen ambient annealing on effective hole mobility was conducted with pMOSFETs. Figure 6.23 (a) shows the effect of oxygen ambient annealing on I_d-V_g characteristics. Oxygen annealing was performed at 340 ^oC for 30min. A V_{th} lowered by 520mV is in good agreement with the shift in the MOS capacitors. The sub-threshold slop (SS) showed a slightly degradation after oxygen annealing compared with FGA 800 ^oC. Degradation of The sub-threshold slop indicates the increase of interface state density. However, FGA process recovered the sub-threshold slop. In Figure 6.23 (b), the gate-to-channel capacitance (C_{gc}-V_g) curves confirm little difference in the EOT. EOT is 1.8nm extracted by NCSU CVC. The equal amount of V_{th} shift at N_s of $5x10^{11}$ cm^{-2} in Figure 6.23 (b) can be also attained. These I-V and C-V characteristics completely coincide with experimental results of MOS capacitors as explained in previous section. Figure 6.24 shows the impact of oxygen ambient annealing on the effective hole

mobility. The reduced mobility can be clearly observed after oxygen annealing at low surface carrier region. It indicates that the Coulomb scattering associated with newly created the interface state density by oxygen annealing is increased. However, with the combination of FGA, the effective hole mobility showed a dramatically improvement with peak mobility of 100 cm^2/Vs. This is the experimental evidence that the positive V_{th} shift is induced by suppression of fixed charges associated with defects in high-k dielectrics. It is found that the effective mobility can be recovered by oxygen annealing due to compensation of defects in high-k layer.



(a)



(b)

Figure 6.23 *Effect of oxygen annealing on* ***(a)*** *I_d-V_g characteristics and* ***(b)*** *gate-channel capacitance of pMOSFETs.*

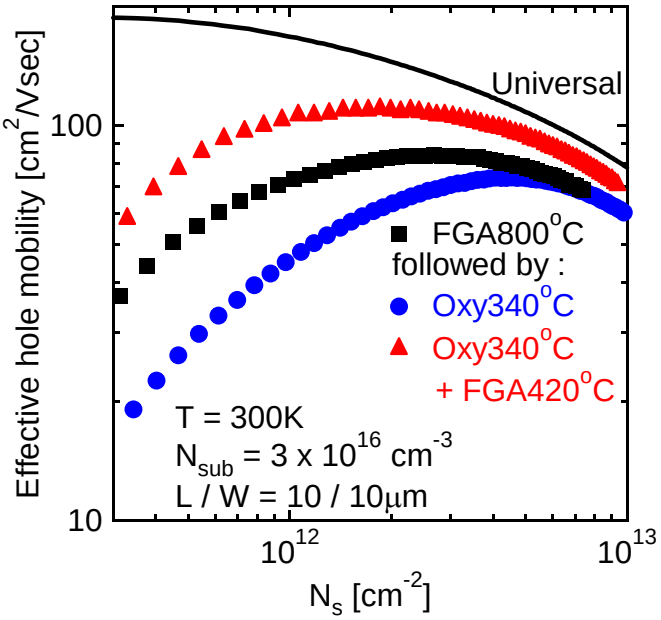
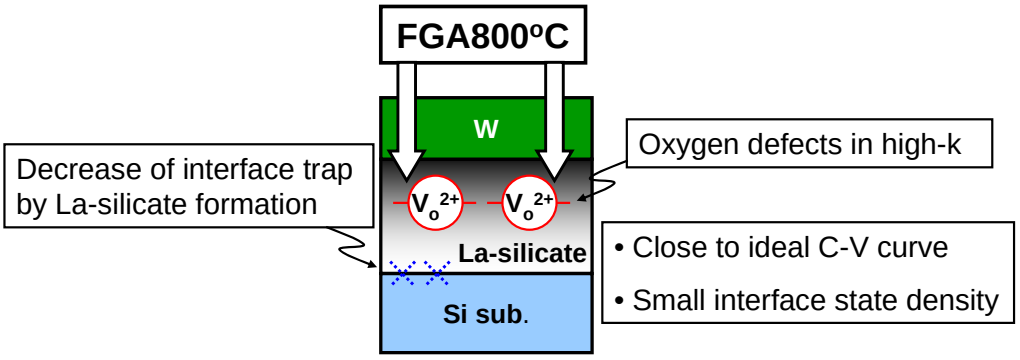


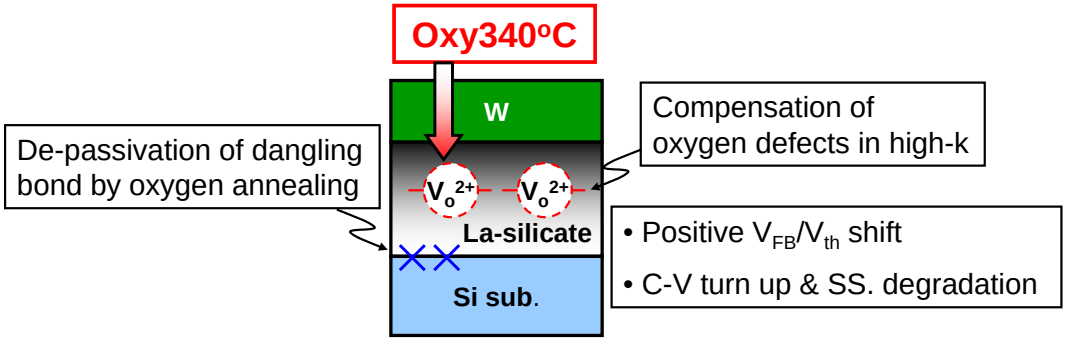
Figure 6.24 *Impact of oxygen ambient annealing on effective hole mobility.*

The positive V_{th} shift by 520mV was observed between before and after oxygen ambient annealing. The V_{th} shift of 520mV corresponds to half of Si bandgap energy. It indicates that huge quantities of oxygen defects in high-k layer are still existed. Continual effort is necessary for improving effective mobility.

Here, respective annealing processes for improving effective mobility would be organized. As previously mentioned in chapter 4, post-metallization annealing at 800oC for 30min in forming gas can improve the interface state density. As a result, the effective mobility is also improved. On the other hand, huge quantities of oxygen defects are remaining. Figure 6.25 (a) shows the effect of post-metallization annealing at 800oC for 30min in forming gas. The formation of La-silicate has been already confirmed by XPS measurement as explained in chapter 4. Figure 6.25 (b) shows a role of oxygen ambient annealing. Oxygen defects in high-k layer can be successfully compensated by oxygen incorporation through the thin W metal gate. Compensation of defects corresponds to the positive V_{FB} or V_{th} shift because oxygen vacancy is positively charged as previously mentioned. However, degradation of C-V curve and sub-threshold slop was observed after oxygen annealing. It indicates the degradation of interface properties. The possible origin is de-passivation of dangling bond by oxygen annealing. Figure 6.25 (c) shows a function of subsequent forming gas annealing (FGA). The C-V curve and sub-threshold slop was recovered by performing FGA. Moreover, effective hole mobility was also dramatically improved with maintaining the positive V_{th} shift. This is the experimental evidence that the positive V_{th} shift is due to compensation of oxygen defects in high-k by additional oxygen incorporation. Only oxygen annealing is insufficient for improving MOSFET characteristics. It can be concluded that the effective mobility is recovered by combining oxygen annealing with subsequent FGA.



(a)



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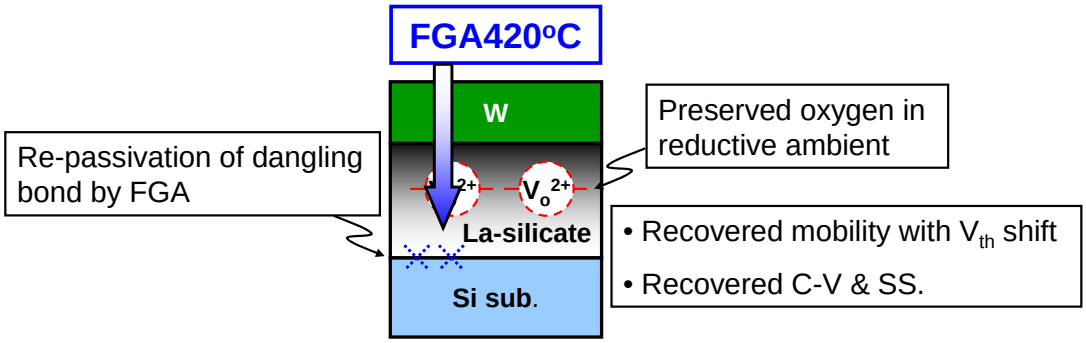
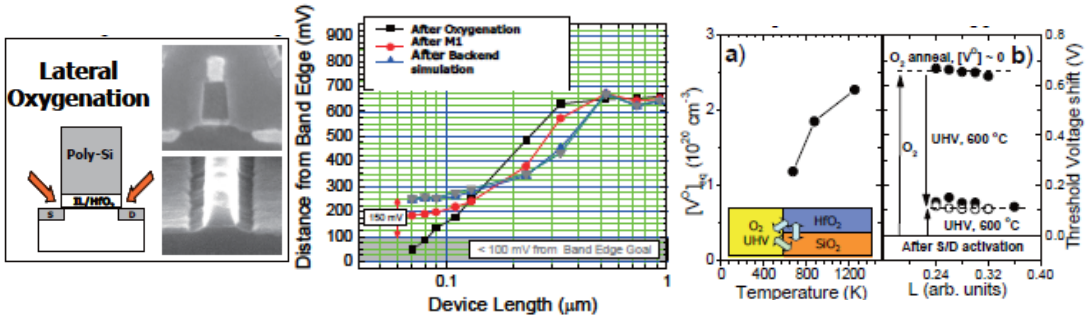


(c)

Figure 6.25 *Respective annealing processes for improving effective mobility.* ***(a)*** *FGA800 °C,* ***(b)*** *Oxy340 °C, and* ***(c)*** *FGA420 °C.*

It is found that additional supplied oxygen into La-silicate dielectrics is preserved even in reduction ambient. This is very interesting experimental results. As previously mentioned, oxygen vacancy of high-k materials is inherent feature based on its ionic bond. However, in this experiment with La-silicate dielectrics, supplied oxygen is successfully introduced into La-silicate through the W while additional oxygen is maintaining even after reduction annealing in forming gas.

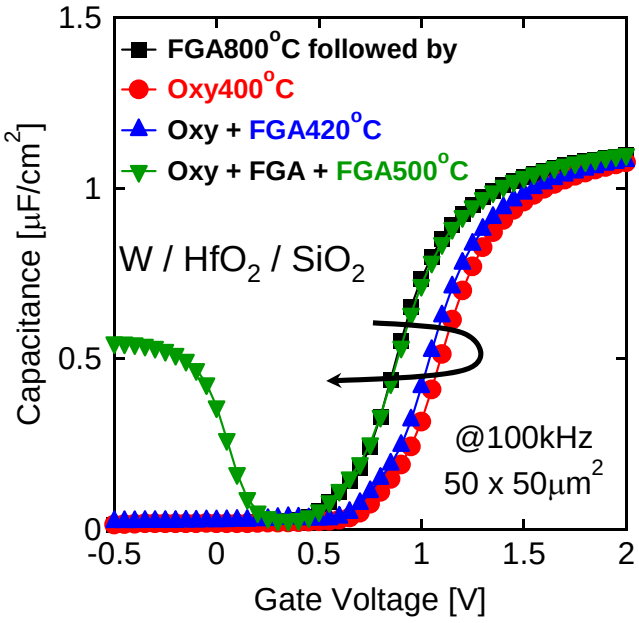
It has been reported that oxygen incorporation is also demonstrated with HfO_2 dielectrics [6.14]. It is called as "Oxygenation". Oxygenation is conducted to obtain the low V_{th} pMOSFETs with $TiN/HfO_2/SiO_2$ gate stacks. Figure 6.26 shows the effect of oxygenation on threshold voltage shift with $TiN/HfO_2/SiO_2$ gate stacks [6.14]. According to their report, oxygen was introduced after sidewall removal as shown in Figure 6.26 (a). This is amazing and interesting method. Figure 6.26 (b) shows the gate length dependence of threshold voltage at various stages in the CMOS process. The threshold voltage becomes lower with decreasing gate length. Gate length dependence of threshold voltage shift indicates the oxygen diffusion mechanisms. Figure 6.26 (c) shows reversible threshold voltage shifts during UHV annealing.



(a) **(b)** **(c)**

Figure 6.26 (a) *Concept of lateral oxygenation,* ***(b)*** *gate length dependence of threshold voltage shift, and* ***(c)*** *reversible threshold voltage shifts during UHV annealing.*

From their research of report shown in Figure 6.26 (c), it was confronted with the question that additional supplied oxygen into HfO_2 could not be preserved. Additional oxygen into HfO_2 would be easily diffused out during UHV or reduction annealing. To investigate a speculation about behavior of oxygen and difference between La-silicate and HfO_2, MOS capacitors with HfO_2 dielectrics was prepared. Device fabrication process is almost same as MOS capacitors with La-silicate dielectrics. However, thermally-grown SiO_2 with about 2nm in thickness was formed prior to HfO_2 deposition. HfO_2 was also deposited by e-beam evaporation in an ultra-high vacuum chamber, followed by *in-situ* W (tungsten) metal deposition by RF sputtering. The experimental sequence is as follows. C-V characteristics were firstly measured after post-metallization annealing at 800 ^{o}C in forming gas. Next, oxygen ambient annealing was performed to supply additional oxygen into gate stacks, followed by C-V measurement. Finally, recovery annealing and C-V measurement were conducted.



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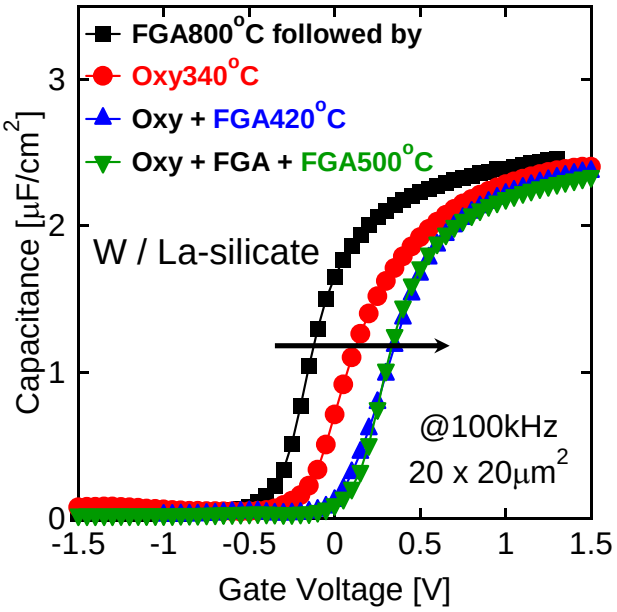
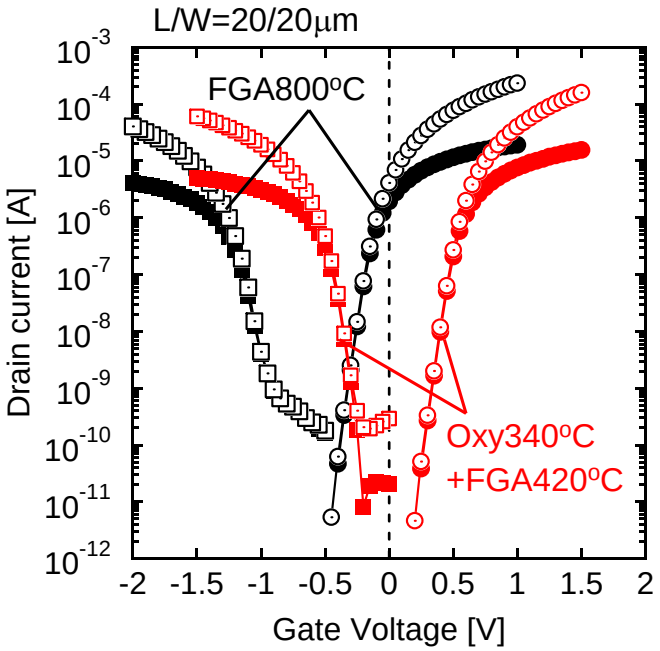


(b)

Figure 6.27 *Comparison of C-V curves between* ***(a)*** *HfO_2 and* ***(b)*** *La-silicate dielectrics.*

Figure 6.27 shows the comparison of C-V curves between HfO_2 and La-silicate dielectrics. Reversible V_{FB} shift after forming gas annealing can be confirmed in Figure 6.27 (a). This result is agreement with previous report [6.14]. On the other hand, in the case of La-silicate, positive V_{FB} shift is maintained after forming gas annealing. It may be considered that this is one of the reasons why the oxygen incorporation is not implemented in device fabrication process. On the other hand, La-silicate has great advantage for defects compensation by oxygen incorporation. The electrical instability of HfO_2 is due to material nature associated with ionic bond while La-silicate may be increased covalent nature by reaction with Si. It is found that oxygen defects can be successfully compensated by oxygen annealing with utilizing covalent feature of La-silicate. It is difficult to form Hf-silicate by reaction with Si substrate. HfO_2 occurs to phase separation by thermal process, resulting in formation of SiO_2 interface. Recent theoretical study also explained the formation mechanisms of different type of interfacial layer between La_2O_3 and HfO_2 [6.15].



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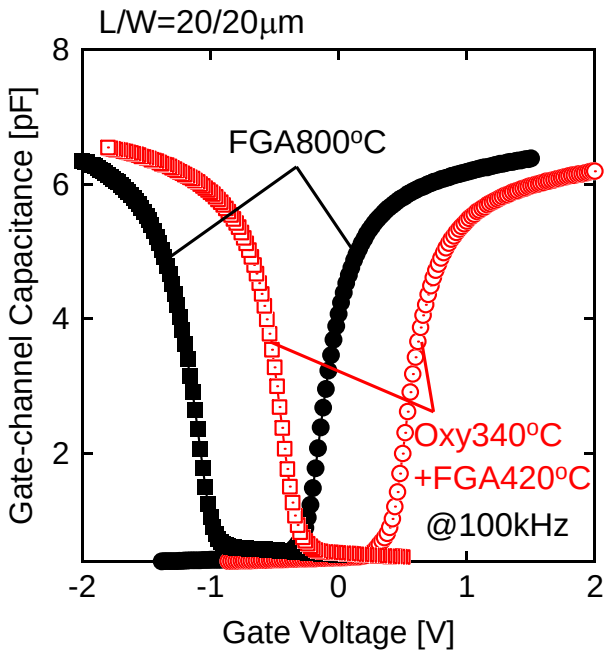
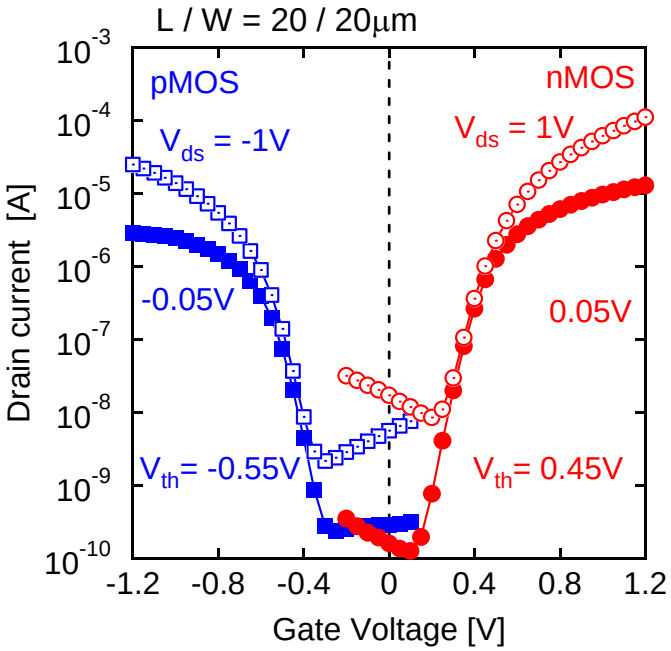


(b)

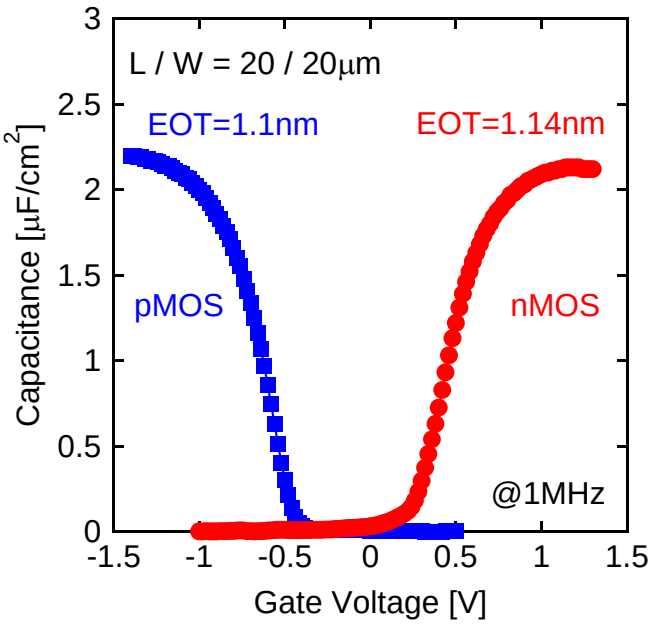
Figure 6.28 *Demonstration of symmetric* ***(a)*** *I_d-V_g characteristics and* ***(b)*** *gate-channel capacitance of n- and p-MOSFETs.*

Benefit of oxygen annealing process was shown in Figure 6.28. As previously shown in Figure 6.23, the positive V_{th} shift by 520mV can be obtained by conjunction with oxygen and forming gas annealing. As the initial V_{th} of pMOSFET is about -1V, it is expected that a symmetric I_d-V_g characteristics of n- and p-MOSFETs with V_{th} equal to ± 0.5V could be obtained by combination of oxygen and forming gas annealing. Figure 6.28 (a) shows the demonstration of symmetric I_d-V_g characteristics of n- and p-MOSFETs. Symmetric I_d-V_g characteristics of n- and p-MOSFETs can be attained by combination of oxygen and forming gas annealing. The sub-threshold slope was not degraded compared with that of FGA 800 ^{o}C. As expected, the threshold voltage after positive shift is about ± 0.5V. No EOT degradation was confirmed from Figure 6.28 (b).

Until now, the MOSFET characterization has been conducted with relatively thick EOT. Effectiveness of oxygen annealing is still unclear in small EOT region. Thus, n- and p-MOSFETs with small EOT were prepared and examined for its availability. Figure 6.29 shows the effect of oxygen and forming gas annealing on n- and p-MOSFETs characteristics with small EOT. Same experimental results compared with Figure 6.28 can be also obtained in small EOT region. Symmetric I_d-V_g characteristics of n- and p-MOSFETs were also confirmed. EOT penalty is less than 1Å.



(a)



(b)

Figure 6.29 *Effect of oxygen and forming gas annealing on n- and p-MOSFETs with small EOT.* ***(a)*** *I_d-V_g characteristics and* ***(b)*** *gate-channel capacitance of n- and p-MOSFETs.*

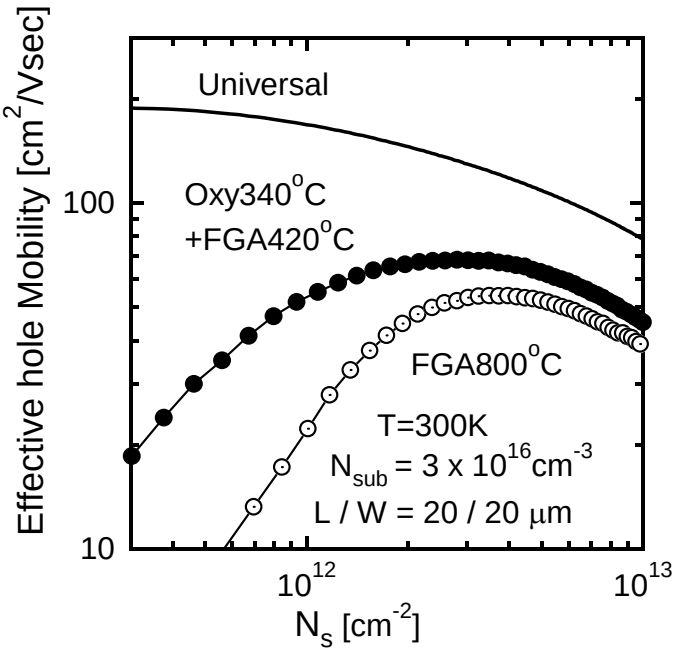
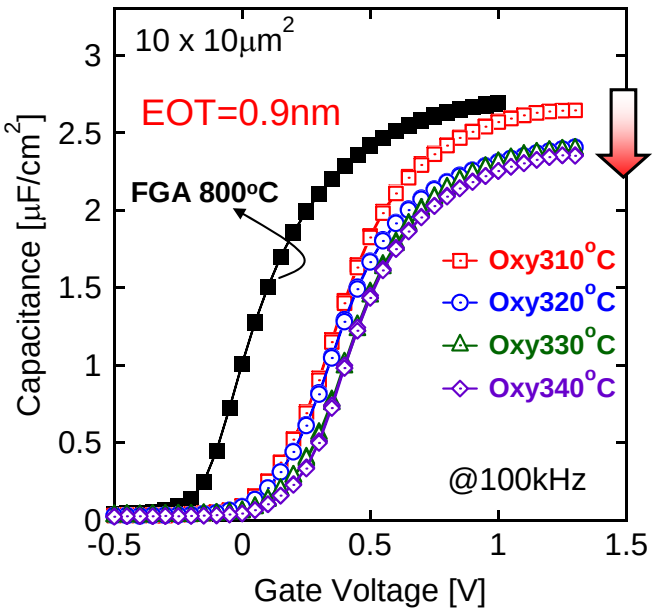


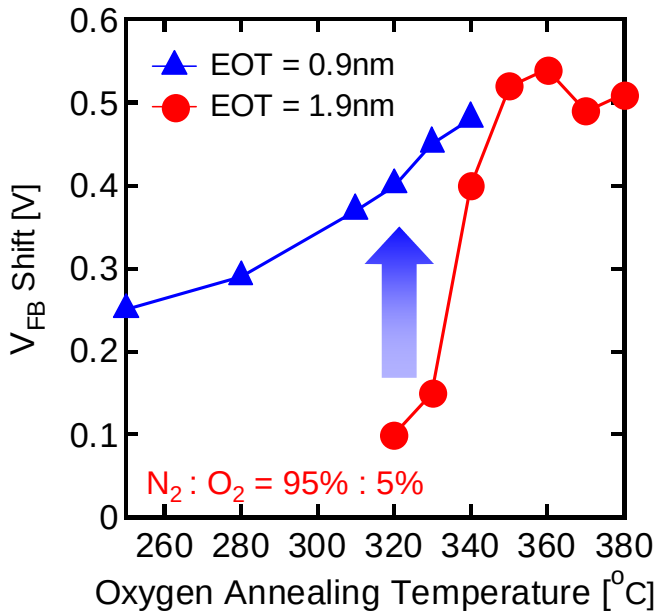
Figure 6.30 *Impact of oxygen ambient annealing on effective hole mobility with small EOT.*

Figure 6.30 shows the effect of oxygen and forming gas annealing on effective hole mobility with small EOT. The hole mobility was also recovered by combination of oxygen and forming gas annealing. It can be concluded that defect compensation by oxygen annealing is also effective in small EOT region.

As previously mentioned, W metal thickness strongly affects on positive V_{FB} shift because of diffusion mechanism through the metal layer. Next, EOT dependence of positive V_{FB} shift was examined. The high-k gate dielectric is basically introduced for EOT below about 1nm region. It is also considered that amount of oxygen defects in high-k layer may depend on EOT or physical thickness. Sample fabrication procedure is completely same as previous experiment.



(a)



(b)

Figure 6.31 (a) *Effect of oxygen ambient annealing on C-V characteristics with EOT of 0.9 nm, and* ***(b)*** *comparison of V_{FB} shift between0.9nm and 1.9nm in EOT.*

Figure 6.31 (a) shows the effect of of oxygen ambient annealing on C-V characteristics with EOT of 0.9 nm. Although positive V_{FB} shift was confirmed with increasing oxygen annealing temperature, the V_{FB} starts to shift toward positive direction at lower annealing temperature than that of thick EOT. Moreover, EOT degradation was also confirmed at temperature below 340 ^{o}C. As previously mentioned, EOT degradation was not observed at temperature of 340 ^{o}C in EOT more than 1nm. Figure 6.31 (b) shows comparison of V_{FB} shift between 0.9nm and 1.9nm in EOT. Positive V_{FB} shift with 0.9nm in EOT can be observed at lower annealing temperature. It is found that positive V_{FB} shift by oxygen incorporation also depends on EOT or physical thickness of high-k gate dielectrics. It appears in EOT less than 1nm. EOT dependence of V_{FB} shift indicates the oxygen diffusion mechanisms in high-k gate dielectrics as well as W layer. Figure 6.32 shows schematic illustrations for oxygen diffusion in gate stacks. First of all, W metal thickness should be less than 10nm to be diffused through the oxygen. An annealing temperature in oxygen ambient is lower with decreasing EOT or physical thickness of La-silicate. Since the oxygen exponentially decay as a certain characteristics length, more amount of oxygen reach at the high-k/Si interface. Excess oxygen induces the EOT degradation as shown in Figure 6.31 (a). It is found that diffusion of oxygen strongly depends on the annealing temperature and physical thickness of both high-k and metal layer.

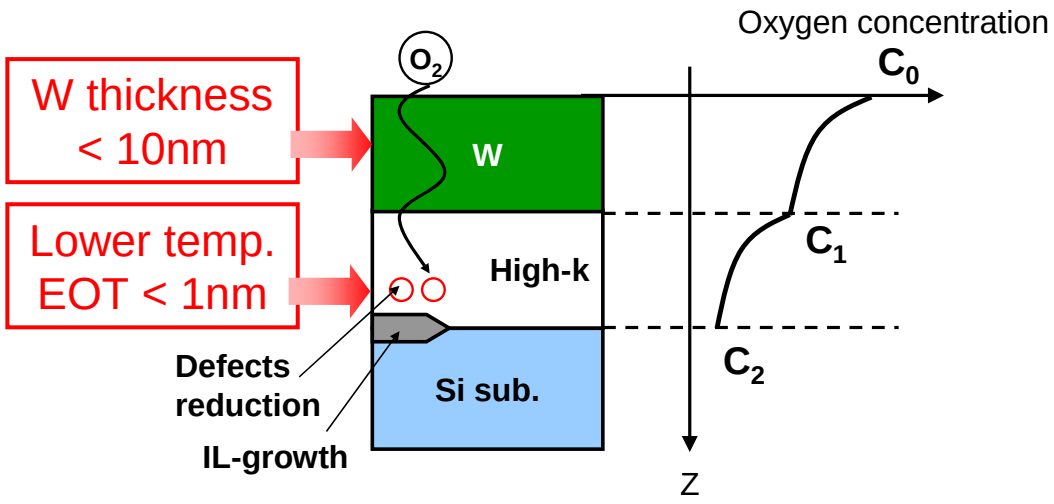


Figure 6.32 *Schematic illustrations for oxygen diffusion in gate stacks.*

6.5 Conclusion

Effect of oxygen ambient annealing for improving effective mobility by compensation of defects in high-k layer was described in this chapter. The details of the findings are as follows.

By optimized oxygen annealing process, positive V_{FB}/V_{th} shift by about 500mV corresponding to a half of Si bandgap energy can be attained without any EOT degradation. It was revealed that the interface properties degraded by oxygen ambient annealing. However, the interface properties can be recovered by conjunction with subsequent forming gas annealing while maintaining positive V_{FB}/V_{th} shift. It is found that effective mobility can be improved by combination of oxygen and forming gas annealing.

It was found that La-silicate has great advantage for defects compensation by oxygen incorporation compared with HfO_2 dielectrics. It can be speculated that advantage of La-silicate over HfO_2 on defects compensation may be due to co-existent of ionic and covalent bond in La-silicate. Using a covalent nature of La-silicate is an important key factor to compensate the oxygen defects for improving the effective mobility.

In this chapter, oxygen ambient annealing was established to improve the effective mobility. There are still many problems remained to be solved. First of all, scaled EOT in less than 1nm should be achieved with maintaining small interface state density and oxygen defects simultaneously. Effect of oxidation of W metal on electrical characteristics is one of concerns issue in scaled MOSFETs. It may be avoidable by deposition of low resistance film. It was demonstrated that supplied oxygen is preserved even after reduction annealing. Integration of low resistance film on W metal may be not so severe problem. Systematic study between V_{th} shift and effective mobility should be also conducted.

6.6 References

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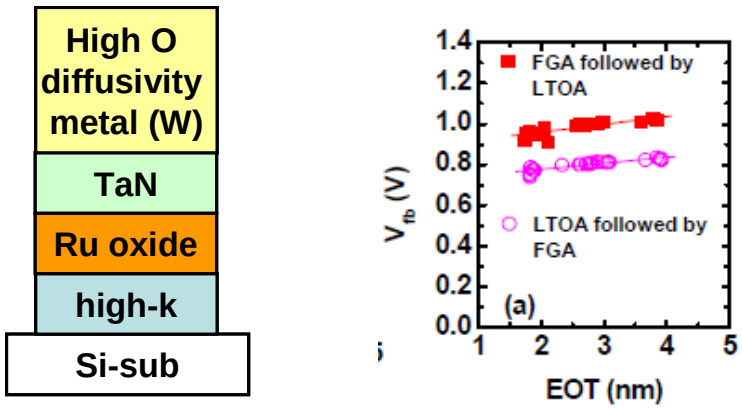
Chapter 7 Selection of Gate Electrode Materials and Structures for Further EOT Scaling

7.1 Introduction

In chapter 5 and 6, device/process technology was established for improving interface properties and compensation of defects, resulting in improvement of effective mobility. However, serious problem is still remained to be solved. Previous experiments were conducted by using relatively thick in EOT more than 1nm. One of the reasons for thick in EOT is robustly examined the electrical characteristics of MOS devices. By scaling EOT, electrical characterization such as C-V measurement or charge pumping measurement, becomes difficult due to excess gate leakage current. That is why MOS devices with EOT more than 1nm were prepared. The other reason is it is difficult to achieve EOT less than 1nm in terms of metal electrode material. In this study, tungsten

(W) metal deposited by RF sputtering is utilized as gate electrode because of its high melting point and easy gate patterning by reactive ion etching with SF_6 chemistry. As previously mentioned, lot of oxygen is contained in sputtered W [7.1]. W electrode plays a role to supply oxygen to gate dielectrics during thermal annealing process. On the other hand, W metal has a material nature of high oxygen diffusivity [7.2]. Figure 7.1 shows the effect of oxidation annealing on flatband voltage (V_{FB}) shift with W metal capping. By oxidation annealing, Ru metal underlying TaN is oxidized from Ru to Ru oxide. It was reported that Ru oxide also shows conductive property. Effective work function of Ru oxide becomes higher than that of Ru. Thus, V_{FB} shifts to positive direction by oxidation annealing. It is expected that lot of oxygen would be incorporated into high-k gate dielectrics through the W metal layer during post-metallization annealing in this experiment. Residual oxygen in rapid thermal annealing furnace may be introduced into La_2O_3 dielectrics. It may induce to excess silicate reaction with Si substrate, resulting in EOT increment.

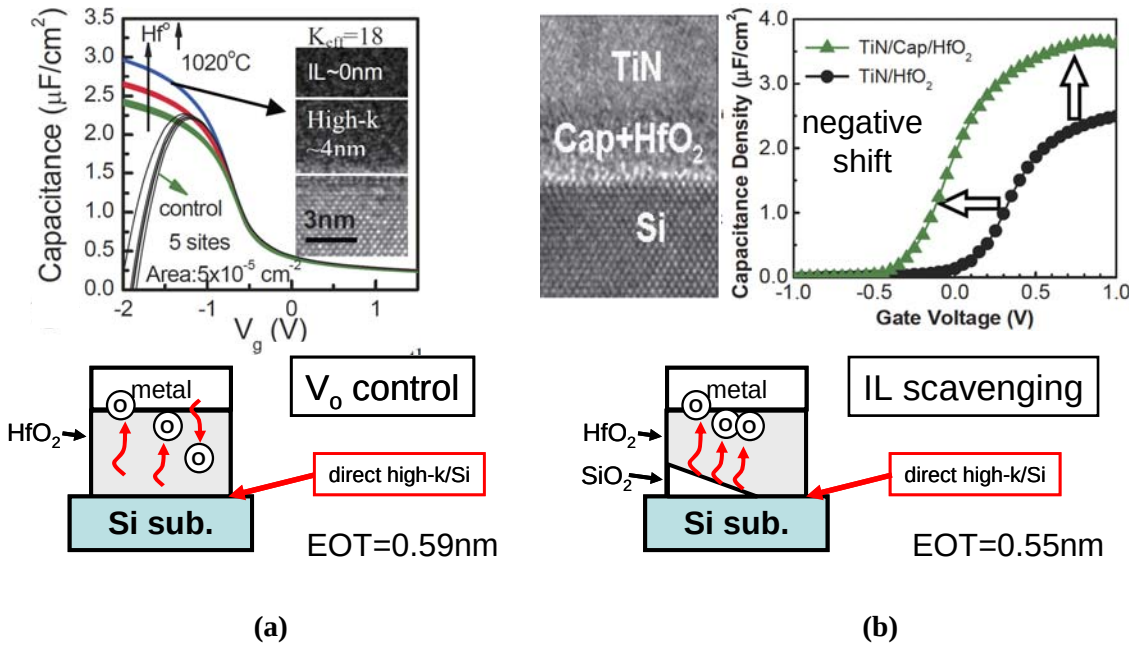


(a) **(b)**

Figure 7.1 *Effect of oxidation annealing on V_{FB} shift with W metal capping.* ***(a)*** *Gate stack structure and* ***(b)*** *V_{FB} shift before and after oxidation annealing.*

Precise oxygen control during fabrication process is essential factor for extremely scaled EOT. Several groups have reported that EOT below 0.6nm can be achieved by using a structure with Hf-based oxides directly in contact with Si by careful high-k deposition and process technique. Figure 7.2 (a) shows precise control of oxygen during HfO_x deposition to inhibit SiO_x interfacial layer growth [7.3]. Figure 7.2 (b) shows interfacial layer scavenging technique for extreme EOT scaling [7.4]. Although the method is quite different between Figure 7.2 (a) and (b), common objective is how to control oxygen during fabrication process. However, both of process techniques are so difficult and complex. It is tough works to optimize the fabrication condition. Moreover, there are not experimental equipments to adopt their proposed methods in present study. Thus, other method for further EOT scaling must be developed. One of the advantages is that La_2O_3 forms not SiO_x interfacial layer but La-silicate. Direct contact structure can be easily attained by La_2O_3 as gate dielectrics.

Purpose of this chapter is to develop the device/process technique for further EOT scaling by controlling amount of oxygen. As previously mentioned, gate metal materials and its structures are focused to inhibit excess incorporation of oxygen in gate stacks. From previous research explained in chapter 5 and 6, the device/process for improving interface properties and compensation of oxygen defects has been established. Therefore, one of the objects of this chapter is hopes to ensure the compatibility with both interface properties and compensation of oxygen defects. Small EOT and would be obtained with maintaining small interface state density. Moreover, defects compensation will be also demonstrated by conjunction with oxygen ambient annealing. The goal of this chapter is summarized in Figure 7.3.



(a) **(b)**

Figure 7.2 (a) *precise control of oxygen during HfO_x deposition to inhibit SiO_x interfacial layer growth, and* ***(b)*** *interfacial layer scavenging technique for extreme EOT scaling.*

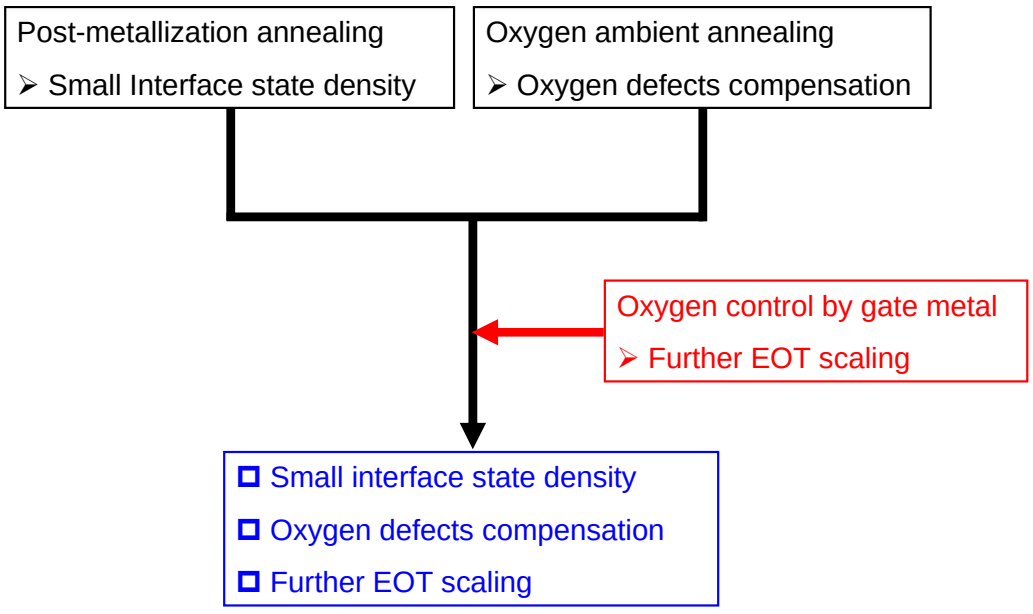
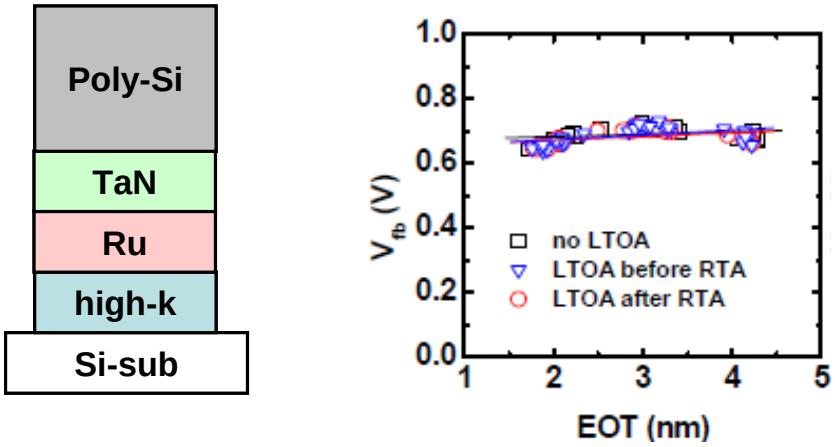


Figure 7.3 *Goal of this chapter*

7.2 Reports of Research and Experimental Procedure

To prevent excess oxygen incorporation into gate stacks, barrier capping layer is one of the effective way. As previously explained, Al film can prevent passage of oxygen. However, the post-metallization annealing at 800 ^{o}C for 30min in forming gas is necessary to improve the interface properties. As melting point of Al is about 600 ^{o}C, Al has poor thermal stability. Barrier layer to prevent passage of oxygen with thermal stability up to 800 ^{o}C must be selected. It was reported that Poly-Si is believed to block the oxygen diffusion toward metal electrode. Figure 7.4 shows the effect of oxidation annealing on V_{FB} shift with Poly-Si capping [7.2]. No V_{FB} shift by oxidation annealing can be confirmed. It indicates that oxygen can not pass through the Poly-Si layer even in oxidation annealing. As Poly-Si is utilized for gate material in conventional MOSFETs, Poly-Si has excellent thermal stability at temperature of activation annealing. Poly-Si is one of the candidates for barrier layer. There is still issue to be solved.



(a) **(b)**

Figure 7.4 *Effect of oxidation annealing on V_{FB} shift with Poly-Si capping.* ***(a)*** *Gate stack structure and* ***(b)*** *V_{FB} shift before and after oxidation annealing.*

As previously shown in Figure 7.3, the aim of this chapter is to combine with oxygen annealing as well as high temperature post-metallization annealing. Even if excess oxygen incorporation could be suppressed with barrier layer on metal electrode during post-metallization annealing, additional oxygen can not be supplied into gate stacks by oxygen annealing. It gives rise to competing goals. Figure 7.5 shows competing problems to achieve small EOT and low oxygen defects in high-k layer simultaneously.

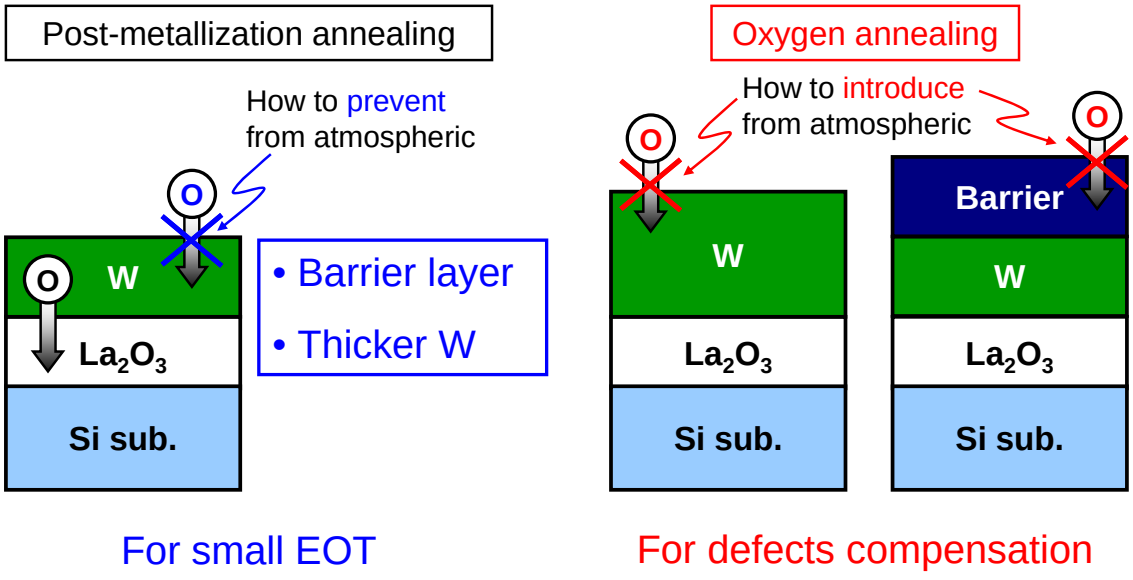


Figure 7.5 *Competing problems to achieve small EOT and low oxygen defects in high-k layer simultaneously.* ***(a)*** *For small EOT, and* ***(b)*** *For defects compensation.*

How to solve this competing problem is most difficult issue in this chapter. To balance competing goals for suppression and introduction of oxygen into gate stacks, several ways were employed to satisfy the competing goals. In chapter 6, Al capping method was conducted to avoid oxidation of W during reactive ion etching process. Post-metallization annealing was performed after Al removal by wet process with TMAH. As also previously mentioned, lateral oxygenation was carried out after sidewall removal. Therefore, this competing problem could be solved by barrier layer removal. As Poly-Si removal has already established for replacement gate process [7.5], Si capping layer is adopted for barrier layer. Figure 7.6 shows device fabrication process. Si layer was deposited by RF sputtering after TiN layer deposition on W. There are some concerns for direct contact of deposited Si with W because of reaction between Si

and W during post-metallization annealing, resulting in formation of silicide like layer (WSi_x). Since Si-based electrode basically prevent the passage of oxygen, it is better to avoid contact between Si and W metal. Therefore, TiN layer was deposited by RF sputtering prior to Si deposition. Si layer can be also easily patterned by reactive ion etching with SF_6 chemistry as well as W metal. Since it was confirmed that TiN layer can be also patterned by RIE with SF_6 chemistry, gate pattering can be performed in one RIE process.

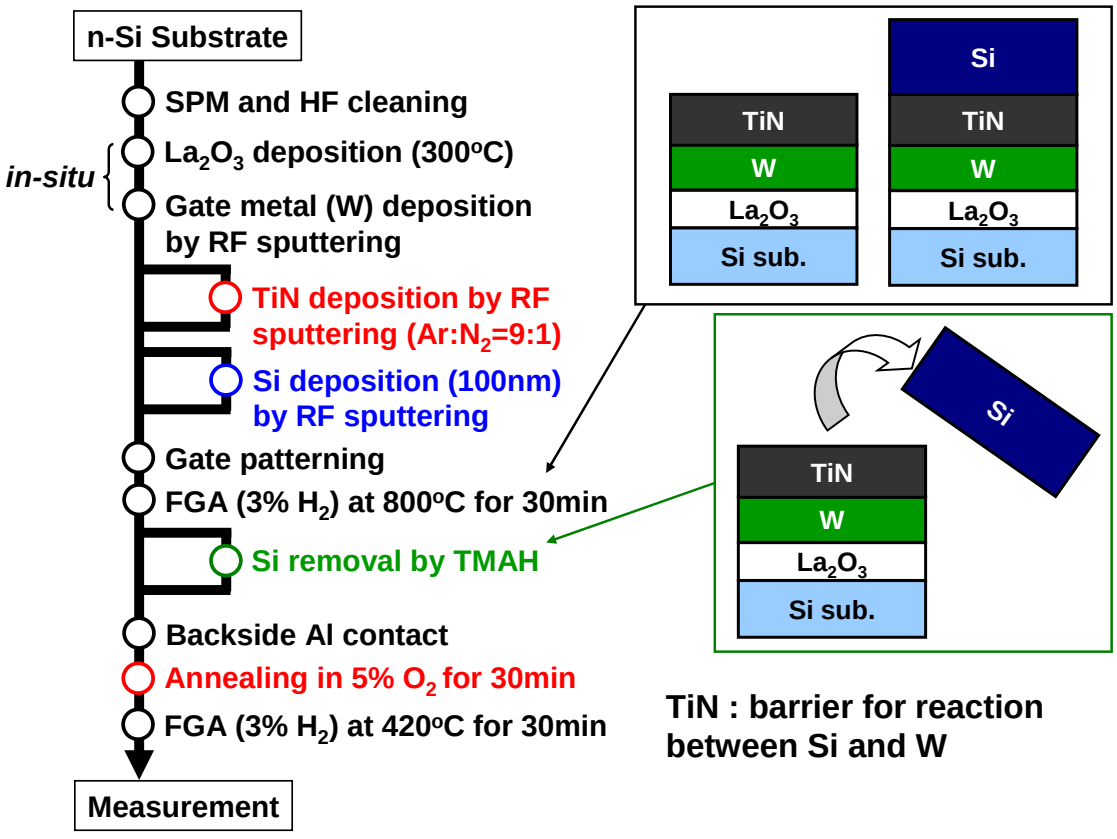


Figure 7.6 *Device fabrication process.*

7.3 Experimental Results of MOS Capacitors

Firstly, whether the additional oxygen is introduced through the TiN/W stack layer was examined. As previously explained in chapter 6, metal thickness strongly affects on oxygen incorporation because of diffusion mechanisms through metal layer. MOS capacitors with various TiN thicknesses were prepared by varying the RF sputtering time. W metal is same as 5nm in thickness. In this experiment, Si was not deposited. MOS capacitor without TiN layer was also fabricated as a reference. Figure 7.7 shows the C-V characteristics as a function of TiN thickness. Increase of EOT after FGA at 800 ^{o}C 30min in forming gas was suppressed with TiN layer on W metal. No hysteresis and little frequency dispersion were also confirmed. Although V_{FB} is slightly shifted with TiN layer, large V_{FB} shift can not be observed. It implies that the effective work function was not varied by reaction between TiN and W. Small V_{FB} shift may be due to fixed charges in high-k gate dielectrics. Figure 7.8 shows the EOT and V_{FB} as a function of TiN thickness. It was found that increment of EOT was independent on TiN thickness down to 5nm. It was considered that TiN below 5nm in Thickness could not play a role on barrier layer for reaction between Si and W metal. Thus, TiN of 5nm in thickness was set to lower limit as a barrier metal.

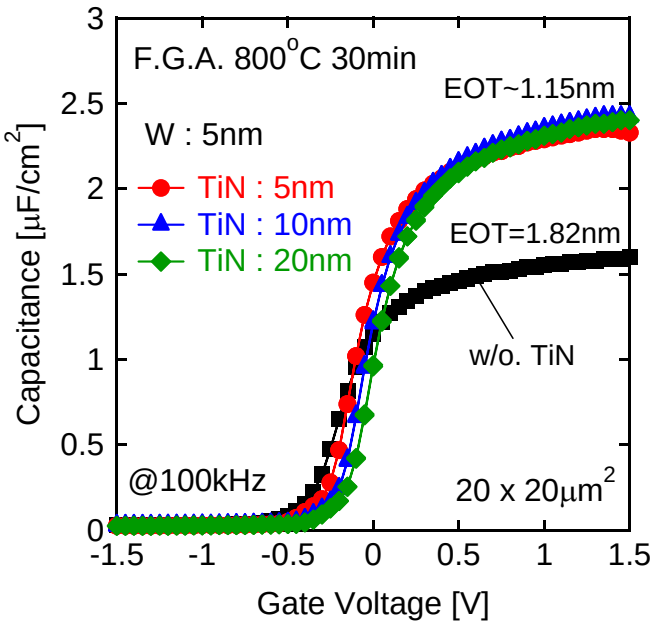


Figure 7.7 *C-V characteristics as a function of TiN thickness.*

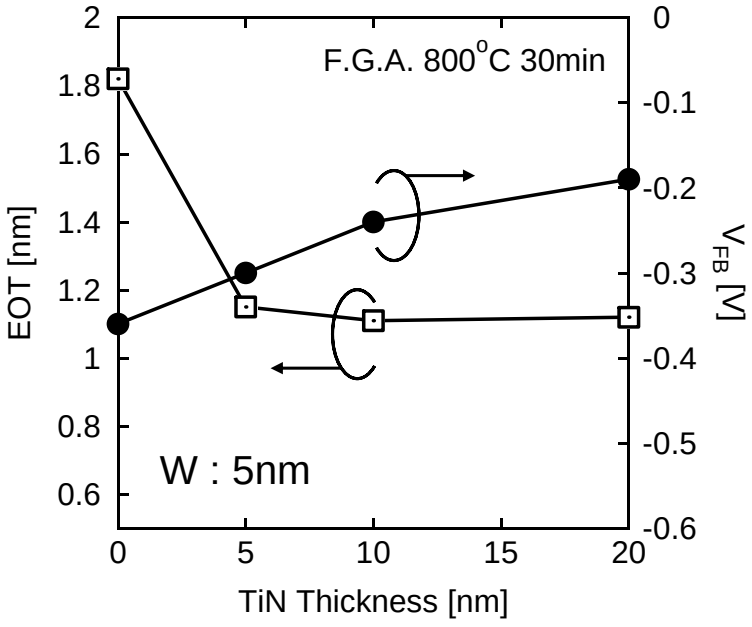


Figure 7.8 *EOT and V_{FB} as a function of TiN thickness.*

Next, oxygen ambient annealing was performed for TiN/W stacked structure. As previously shown in chapter 6, additional oxygen was successfully introduced into HfO_2 dielectrics through TiN of 10nm in thickness [7.6]. W metal also has high oxygen diffusivity. Oxygen incorporation would be also achieved with TiN/W stacked structure. However, re-investigation of annealing condition should be conducted. Figure 7.9 shows the effect of supplied oxygen on C-V characteristics as a function of TiN thickness. Oxygen ambient annealing was performed at 400 ^{o}C for 30min, followed by recovery annealing. The temperature of oxygen annealing is slightly higher than W single layer structure. This is reasonably understood because metal layer becomes thicker by stack structure. Little EOT degradation was also confirmed from C-V characteristics. Although TiN thickness is independent on EOT increase as shown in Figure 7.8, positive V_{FB} shift increased with decreasing TiN thickness. This is the experimental evidence for difference of TiN thickness by varying RF sputtering time. It was found that additional oxygen was also introduced through the TiN/W stack layer.

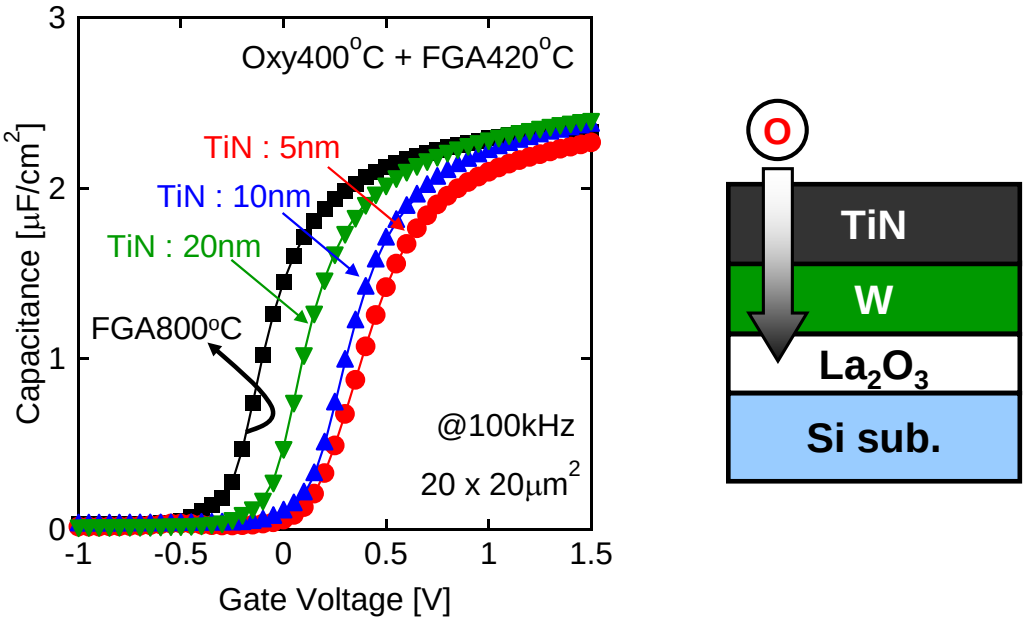


Figure 7.9 *Effect of supplied oxygen on C-V characteristics as a function of TiN thickness.*

In this experiment, Si removal process is most important issue. Selective Si etching on metal layer must be conducted. It was reported that SOI layer can be etched by wet process using TMAH [7.7]. It is straightforwardly expected that deposited Si could be also removed by using TMAH. To investigate whether deposited Si can be selectively removed underlying TiN or not, samples with Si deposited on TiN metal were prepared without field oxide. The samples were annealed at 800 °C for 30min in forming gas. Although wet process for Si etching by TMAH at 60 °C was performed, Si layer was partially remained on TiN layer. Since SiO_2 is hardly etched by TMAH, formation of native oxide at Si surface may be one of the causes for remaining Si on TiN layer. Figure 7.10 shows the reconstructed device fabrication process. Wet process with 1% HF for removal of native oxide was performed prior to TMAH for Si etching. Deposited Si etching by TMAH at 60 °C was completely removed by conjunction with wet process

by 1% HF. This additional wet process is so important. It takes about 1min to remove Si of 100nm in thickness.

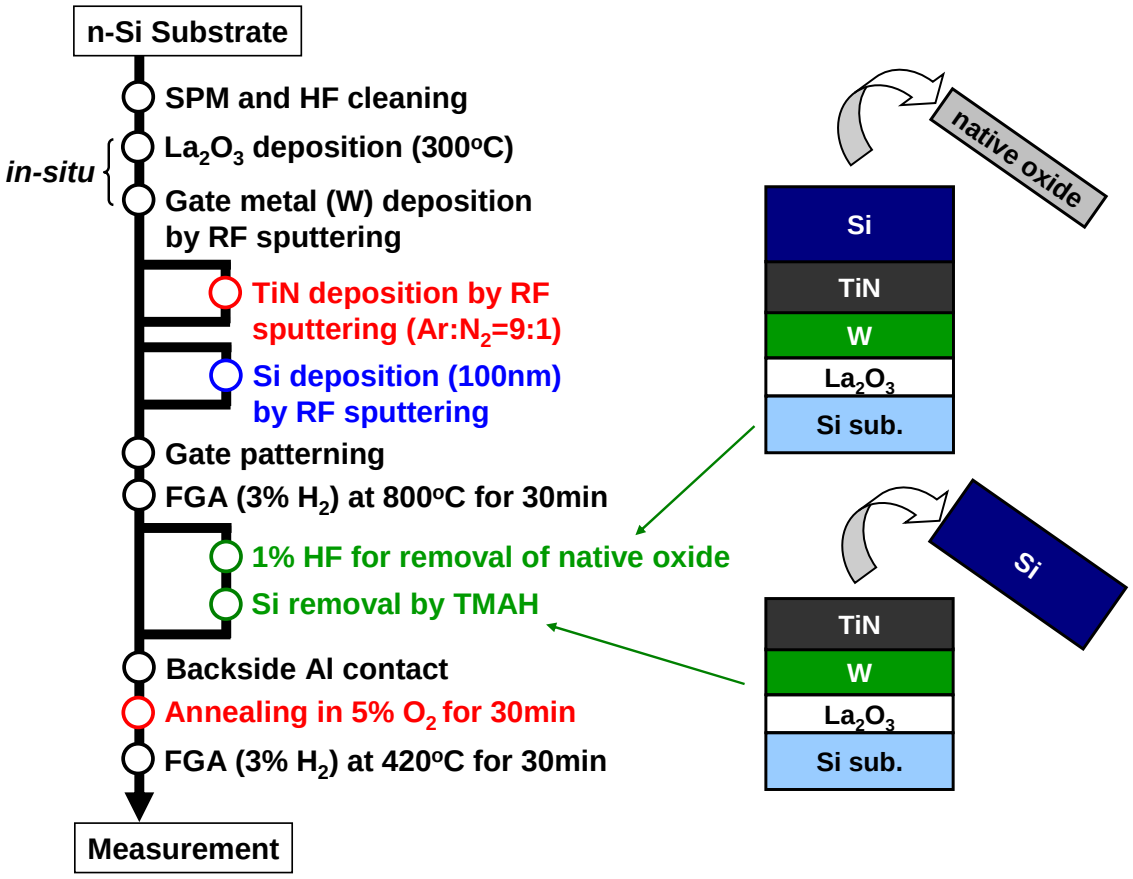


Figure 7.10 *Reconstructed device fabrication process.*

As Si etching process on TiN layer was established, electrical characteristics of MOS capacitors were investigated. Post metallization annealing was performed with Si layer at 800 ^{o}C for 30min in forming gas. C-V measurement was employed after Si removal process. Figure 7.11 shows the C-V characteristics after Si removal as a function of TiN thickness. Capacitance value after Si removal dramatically increased, indicating decreasing EOT. V_{FB} is almost identical in all MOS capacitors. It implies that effective

work function is not varied as well as Figure 7. 7. EOT of 0.75nm can be attained after annealing at 800 ^{o}C for 30min with Si capping. It was revealed that TiN metal can play a role to block layer down to 5nm in thickness.

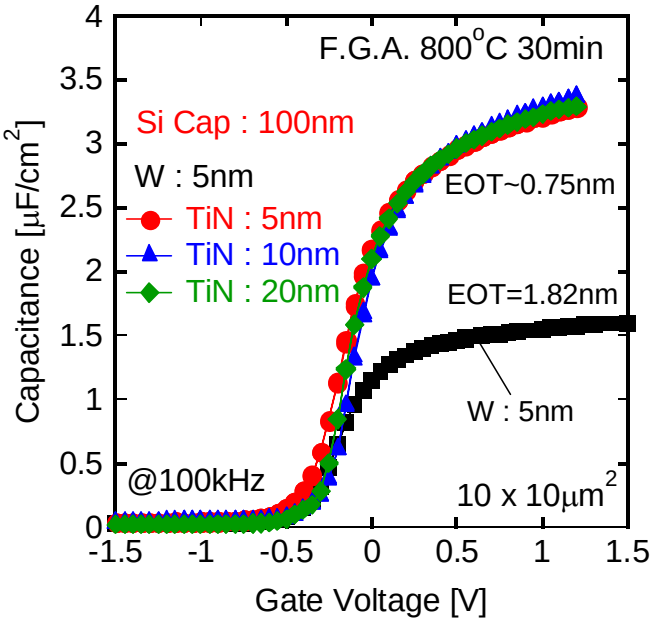


Figure 7.11 *C-V characteristics after Si removal as a function of TiN thickness.*

Figure 7.12 shows the comparison between ideal and experiment C-V characteristics. The measured C-V curve is fairly nice agreement with ideal C-V curve calculated by NCSU CVC, indicating excellent interface properties. It was demonstrated that C-V characteristics close to the ideal C-V curve can be also achieved with 0.69nm of EOT by high-temperature annealing with Si capping layer. As previously mentioned, precise oxygen control is necessary for further EOT scaling by careful deposition or special technique. In this experiment, more simple method to control for amount of oxygen was presented. As Poly-Si, TiN and W has been already utilized in conventional MOSFET

process, technical issue may be not so severe. This thick Si stacked structure is called as metal inserted Poly-Si (MIPS) structure. Recent research of reports has been adopted MIPS structure [7.5]. The advantage for MIPS structure is to utilize the conventional CMOS process. Device structure is almost identical to conventional MOSFETs with Poly-Si/SiO_2 gate stacks. Structure similar to conventional Poly-Si/SiO_2 MOSFETs is quite important in terms of fabrication process such as etching. It was demonstrated that control the amount of oxygen for scaled EOT can be attained by metal inserted Poly-Si (MIPS) structure not to introduce the special technique. This is simpler and easier process compared with previous report.

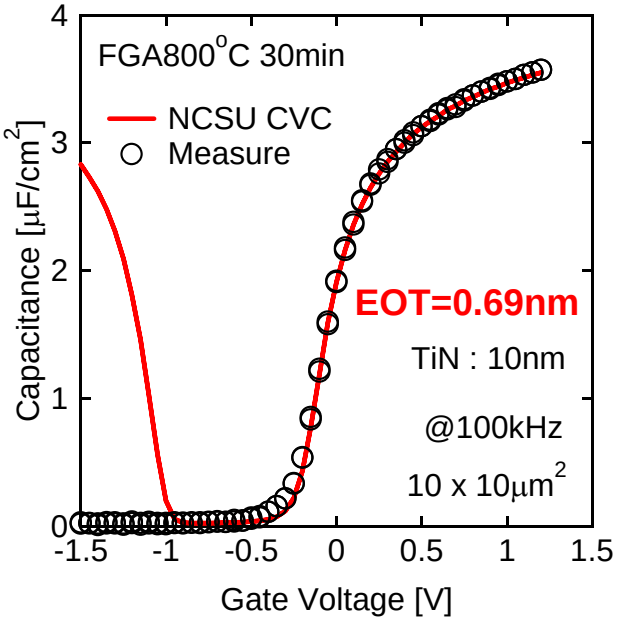


Figure 7.12 *Comparison of C-V characteristics between ideal and experiment.*

Figure 7.13 shows the comparison of C-V characteristics with and without Si layer. The EOT with Si removal process is less than half that of W single layer structure.

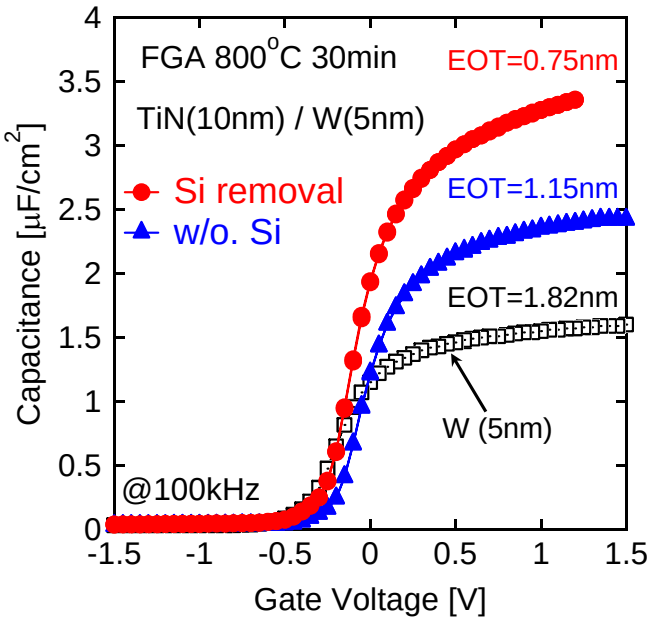


Figure 7.13 *Comparison of C-V characteristics with and without Si layer.*

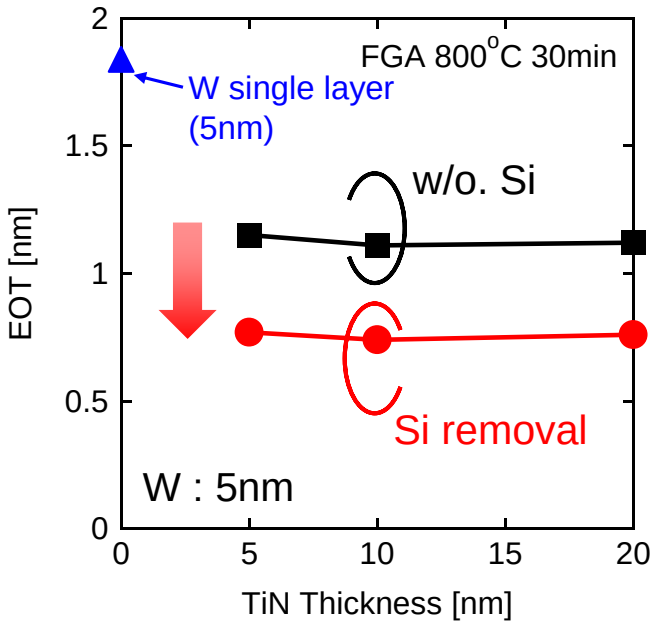


Figure 7.14 *EOT as a function of TiN thickness with and without Si layer.*

Figure 7.14 shows the EOT as a function of TiN thickness with and without Si layer. It was confirmed that TiN layer is also effective to inhibit the increment of EOT. EOT increment was dramatically suppressed by Si capping layer on TiN. On the other hand, impact of TiN thickness on EOT increase is so small. By considering the results for oxygen incorporation through TiN/W stacked layer shown in Figure 7.9, it can be concluded that TiN thickness less than 10nm is suitable for applying the oxygen ambient annealing.

Oxygen annealing with TiN/W stack structure was performed after Si layer removal by wet process using TMAH. Temperature of oxygen annealing is 400 ^{o}C as well as previous results as shown in Figure 7.9. The only difference is with and without Si capping layer during post-metallization annealing. Oxygen ambient annealing was performed except for 20nm of TiN thickness because V_{FB} shift is smallest after oxygen annealing as shown in Figure 7.9. Figure 7.15 shows the C-V characteristics before and after oxygen annealing at 400 ^{o}C. Although the oxygen ambient annealing was performed at 400 ^{o}C, positive V_{FB} shift is quite small compared with that of without Si capping as shown in Figure 7.9. It indicates that additional supplied oxygen was rarely introduced by oxygen annealing after Si removal by wet process using TMAH. This is completely different in previous experimental results. Little positive V_{FB} shift was also observed with TiN of 10nm in thickness. The cause of little positive V_{FB} shift may be due to Si capping and removal process because positive V_{FB} shift was obtained by TiN/W stacks without Si capping. C-V characteristics were measured irrespective of before and after oxygen annealing. Thus, it can be speculated that metal with low oxygen diffusivity may be formed at TiN surface. The plausible matter is formation of silicide-like layer at the TiN surface during forming gas annealing at 800 ^{o}C for 30min

with Si layer. It was reported that Si is diffused from Poly-Si into TiN layer in metal inserted Poly-Si stack structure [7.8]. Moreover, Ti-silicide by reaction between Ti and Si was also utilized in previous MOSFET process [7.9]. Si-based gate electrode, such as Poly-Si or silicide, has a nature to block the oxygen diffusion.

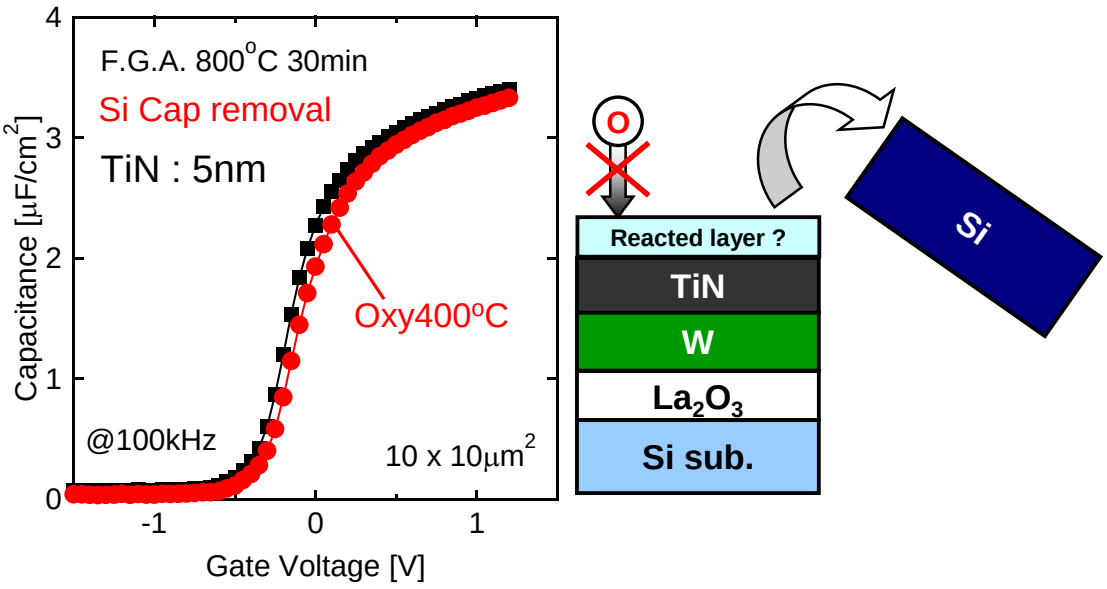


Figure 7.15 *C-V characteristics before and after oxygen annealing at 400 °C.*

Low oxygen diffusivity layer must be removed as same as Si layer to supply additional oxygen into gate stacks. RIE process is not available because all of metal layer is removed. Wet etching is better to selectively remove the top surface. Although the origin for little V_{FB} shift is still unclear, wet etching was experimented with 1% HF on MOS capacitor after oxygen ambient annealing. Figure 7.16 shows the demonstration of positive V_{FB} shift by oxygen incorporation after Si removal. After wet etching with 1% HF, positive V_{FB} shift can be clearly observed. The positive V_{FB} shift by 490mV is in

good agreement with previous experimental results in chapter 6. Although decreasing of capacitance can be also observed by oxygen ambient annealing, EOT degradation is 0.8Å extracted by NUSC CVC. Defects compensation by oxygen annealing can be successfully attained with EOT penalty less than 1Å in sub-1nm EOT region. This experimental result suggests that effective mobility could be improved with scaled EOT.

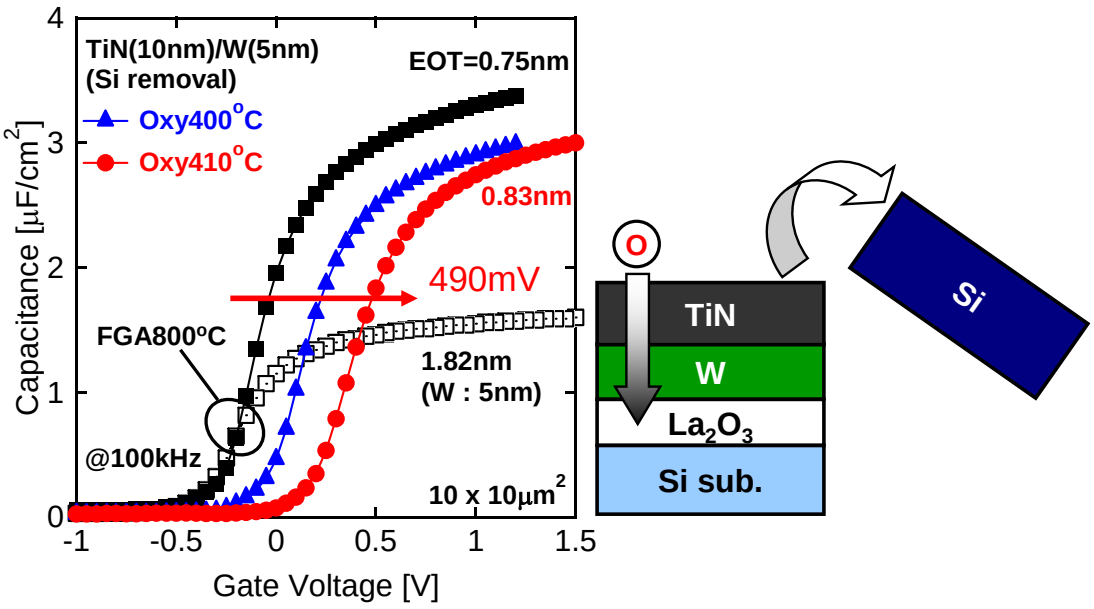


Figure 7.16 *Demonstration of positive V_{FB} shift by oxygen incorporation after Si removal.*

7.4 Experimental Results of nMOSFETs

Next, the impact of MIPS structure on MOSFET characteristics was examined. It has been reported that effective mobility is reduced with decreasing the EOT [7.10]. Recovery of effective mobility with scaled EOT is challenge to be addressed in high-k/metal gate stacks. In previous section, close to the ideal C-V characteristics can be attained with a combination of MIPS structure and high temperature annealing. It suggests that excellent interfacial property is obtained. It is of great interest to evaluate the effective mobility of MOSFET. Thus, nMOSFET was fabricated in the same process as MOS capacitors mentioned in previous section. Figure 7.17 shows the fabrication process of nMOSFETs with MIPS structure. Post metallization annealing at 800 ^{o}C for 30min in forming gas was performed with MIPS structure. Si capping layer was removed after post metallization annealing by wet etching using TMAH. Finally, recovery annealing was performed at 420 ^{o}C for 30min in forming gas. Split C-V method was employed to measure the effective mobility.

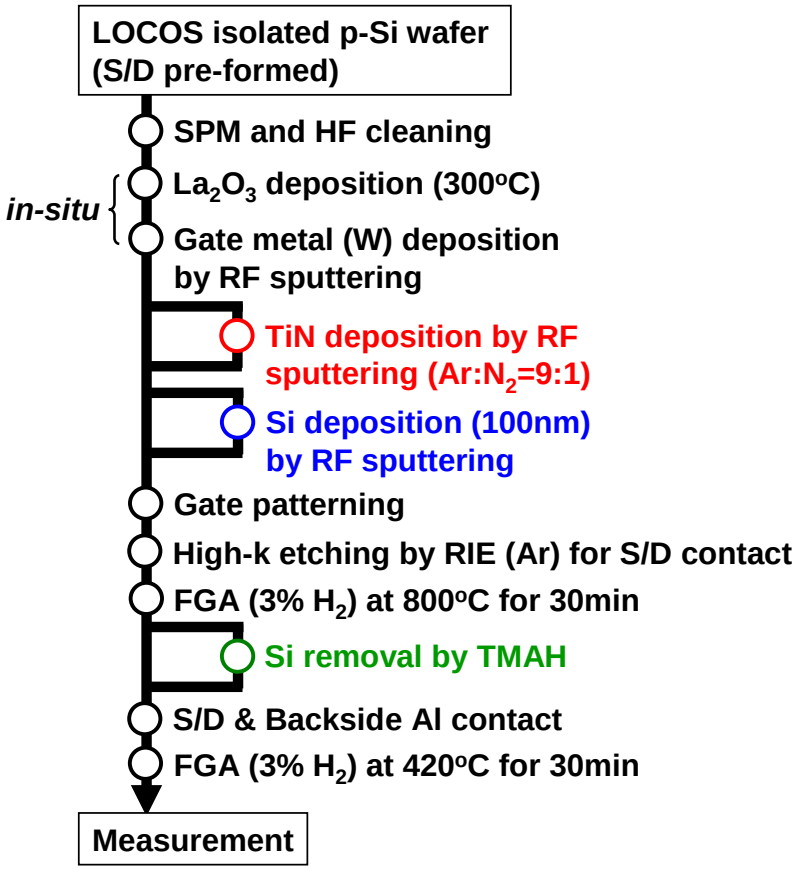


Figure 7.17 *Fabrication process of nMOSFETs with MIPS structure.*

Figure 7.18 shows the comparison of gate-channel capacitance with various metal gate structures. The EOT of 0.71nm is in good agreement with the result of MOS capacitors. Since the C-V measurement becomes difficult with decreasing the EOT due to excess gate leakage current, gate area is also shrank to evaluate the C-V characteristics. On the other hand, all of these C-V characteristics were measured with same gate area, namely L /W = 20 / 20 um. It indicates that the gate leakage current is dramatically suppressed even EOT of 0.71nm.

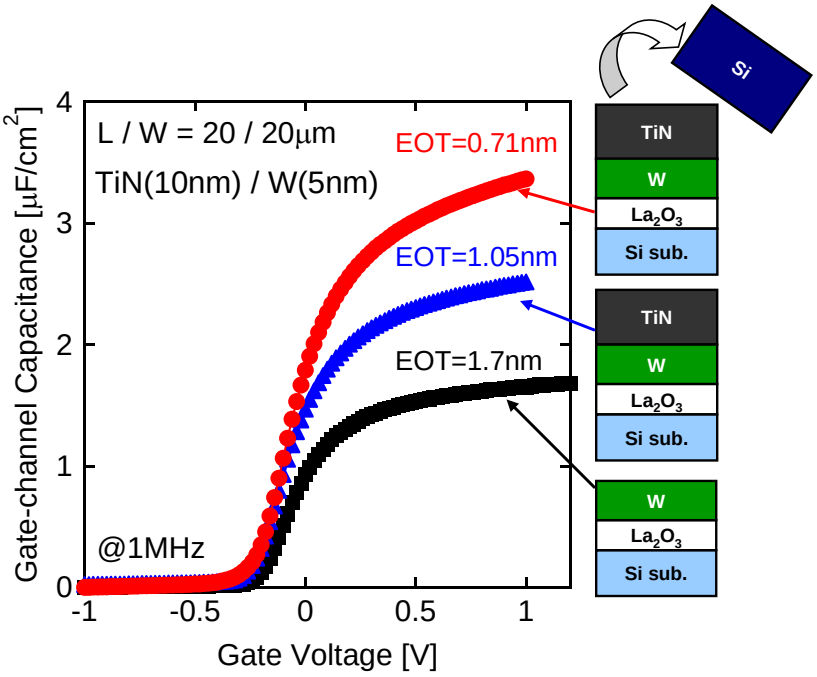


Figure 7.18 *Comparison of gate-channel capacitance with various metal gate structures.*

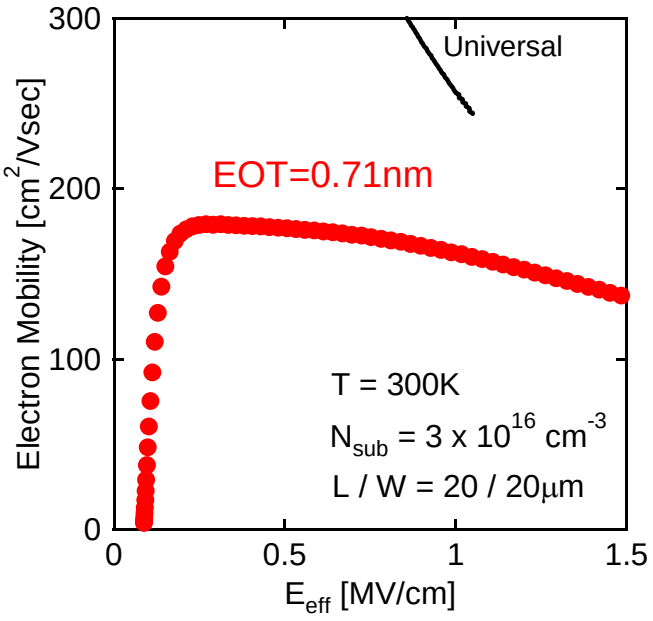


Figure 7.19 *Effective electron mobility with MIPS structure.*

Figure 7.19 shows the effective electron mobility with MIPS structure. Effective field was calculated from gate-channel and gate-body capacitance measured by split C-V characteristics. The depletion charge was estimated from gate-body capacitance by integral from V_{FB} to inversion with respect to the gate voltage.

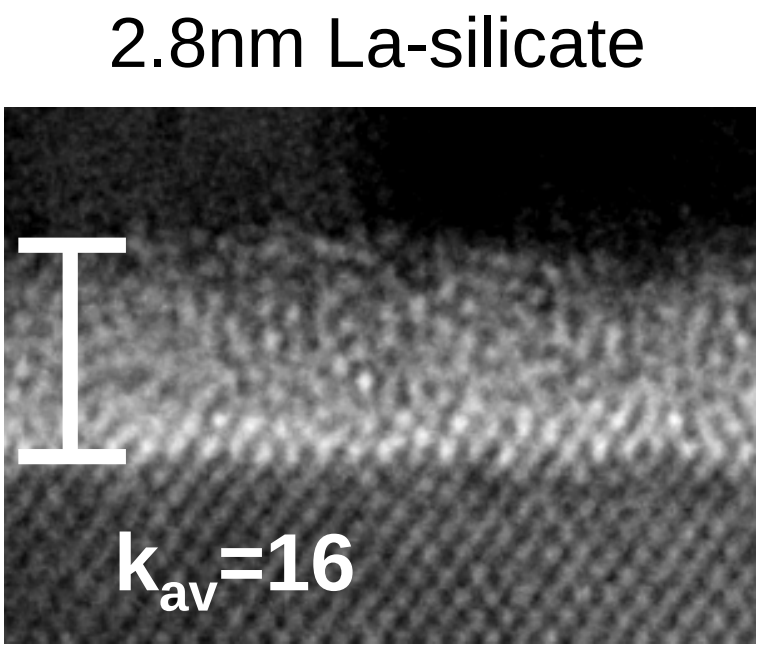
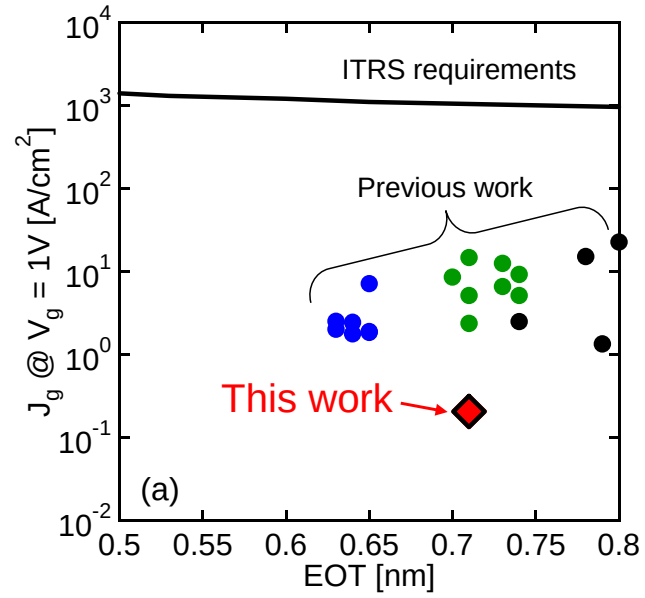
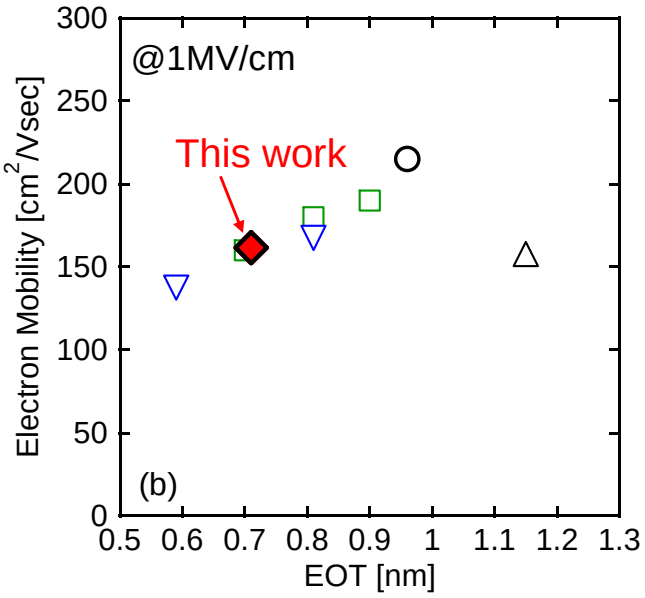


Figure 7.20 *Cross section of TEM image.*

Figure 7.20 shows the cross section of TEM image of measured nMOSFET. The physical thickness of La-silicate is 2.8 nm. Thus, average dielectric constant overall the La-silicate is 16. Moreover, amorphous form was observed over the entire structure. Crystalline form was not observed. It was reported that the La-silicate formed by high temperature annealing is amorphous structure [7.11]. Amorphous form is suitable for gate insulator application to obtain the high effective mobility and low gate leakage current [7.12, 7.13].



(a)



(b)

Figure 7.21 *Benchmark of this work.* ***(a)*** *Gate leakage current and* ***(b)*** *effective electron mobility, respectively.*

Figure 7.21 (a) and (b) show the benchmark of gate leakage current and effective electron mobility, respectively. Gate leakage current is about one order of magnitude less than previous result with rare earth oxides [7.14]. Moreover, effective electron mobility is comparable to previous report with Hf-based oxides proposed by IBM group [7.15]. Their result is a record mobility with scaled EOT in my knowledge. High electron mobility in scaled EOT can be attained with La-silicate gate dielectrics in conjunction of MIPS structure and high temperature annealing. On one the reason for achieving high effective mobility with low gate leakage is due to the amorphous structure of La-silicate.

7.5 Conclusions

Selection of gate electrode materials and structures for further EOT scaling were described in this chapter. The details of the findings are as follows.

It was found that increment of EOT due to post-metallization annealing was dramatically suppressed by control the amount of oxygen with Si capping layer (MIPS structure). Scaled EOT and small interface state density was achieved at the same time by combination of high temperature annealing with Si capping layer. The simpler and easier method was established to obtain the small EOT.

It was revealed that additional oxygen can be also supplied to high-k layer through TiN/W stack structure as well as W single layer. Moreover, the EOT degradation was suppressed less than 1Å. It was demonstrated that oxygen incorporation with scaled

EOT can be attained simultaneously by combining oxygen ambient annealing with Si removal process.

High electron mobility in scaled EOT can be achieved with La-silicate dielectrics by combination of MIPS structure and high temperature annealing. Advantage of La-silicate for high electron mobility was experimentally demonstrated in scaled EOT.

In this chapter, metal gate materials and its structure for further EOT scaling was developed. The problems remained to be solved are as follows.

Improvement of effective mobility by oxygen annealing should be investigated with scaled EOT. Evaluation of hole mobility with same process should be also conducted.

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Chapter 8 Conclusions

8.1 Conclusions of This Study

In this thesis, various problems related to the reduced mobility with high-k/metal gate stacks explained in Chapter 1 are experimentally investigated. Concepts to solve those problems are proposed. Such attempts have been effective for improving effective mobility with direct contact of high-k/Si structure

In Chapter 8, the studies referred to in this thesis are summarized and their importance is described.

a) Fundamental properties of La_2O_3 gate dielectrics (Chapter 3)

In chapter 3, realization of MOSFETs in direct contact of high-k/Si structure was described. The electrical characteristics of MOS devices with La_2O_3 as gate dielectrics were investigated. The main findings and contributions of this work are summarized below.

La_2O_3 is necessary to achieve direct contact of high-k/Si structure because of its material nature to form La-silicate between La_2O_3/Si interface by reaction with Si substrate. W metal is suitable for gate electrode with La_2O_3 dielectrics in terms of its thermal stability and device fabrication process such as etching. It was found that lowering effective work function of metal was observed in direct contact of high-k/Si structure as same as high-k/SiO_2 structure. IT is considered that lowering effective work function is inherent material properties of La_2O_3. It was revealed that threshold voltage of nMOSFET with W/La_2O_3 gate stacks is almost identical to that of Al/SiO_2 gate nMOSFET. Thus, effective work function of W on La_2O_3 becomes near the conduction bandedge.

b) Complex and Stacked Structure based on La_2O_3 for Gate Insulator Application (Chapter 4)

In chapter 4, material-based approach for improving effective mobility was described. Based on La_2O_3 dielectrics, effect of complex and stack structures on effective mobility were experimentally investigated. The main findings of this work are summarized below.

It was found that the V_{FB} can be modulated by composition ratio between La_2O_3 and Sc_2O_3. By increasing ScO concentration, V_{FB} shifts toward positive direction. However, window of V_{FB} tuning becomes narrower. On the other hand, lower interface state density was confirmed with increasing LaO concentration.

It was revealed that crystallization of high-k layer can be suppressed by HfO_2/La_2O_3 stacked structure. Moreover, EOT increment by thermal annealing process can be inhibited by stack structure. However, effective mobility is reduced by stack structure compared with La_2O_3 single layer. Through this work, it was concluded that simple device structure and process is desirable to improve effective mobility.

It was accidentally found that C-V characteristics can be improved by high temperature annealing while increasing EOT.

c) Impact of annealing process on MOS devices with La_2O_3 gate dielectrics (Chapter 5)

In chapter 5, device and process-based approach for improving mobility was described. The gate stack was W/La_2O_3/Si. Effect of annealing condition on electrical characteristics was investigated. The main findings and contributions of this work are summarized below.

It was found that C-V characteristics close to ideal C-V curve can be attained by post-metallization annealing at 800 ^{o}C for 30min in forming gas ambient. It was revealed that the La-silicate formed by high temperature annealing shows the excellent interface properties. The effective electron mobility can be recovered by high temperature annealing in same EOT value due to its nice interface properties. However, it was also found that large amount of coulomb scattering sources was existed in oxides by low temperature mobility measurement.

The weaker N_s dependence of electron mobility for La-silicate MOSFET was observed. The strange mobility behavior appears in the high N_s region may be explained by analogy to oxynitride gate dielectrics. The effective mobility is also degraded with direct contact of high-k/Si structure by decreasing the EOT.

d) Compensation of oxygen defects in high-k gate dielectrics (Chapter 6)

In chapter 6, effect of oxygen ambient annealing for improving effective mobility by compensation of defects in high-k layer was described. Optimum device structure and process condition were investigated. The main findings and contributions of this work are summarized below.

Positive V_{FB}/V_{th} shift by about 500mV corresponding to a half of Si bandgap energy can be attained without any EOT degradation. Since oxygen vacancy is positively charged, V_{FB}/V_{th} shift toward positive direction is experimental evidence for defects compensation. It was revealed that the interface properties degraded by oxygen ambient annealing. However, the interface properties can be recovered by conjunction with subsequent forming gas annealing while maintaining positive V_{FB}/V_{th} shift. It was found that effective mobility can be improved by combination of oxygen and forming gas annealing.

It was found that La-silicate has great advantage for defects compensation by oxygen incorporation compared with HfO_2 dielectrics. It can be speculated that advantage of La-silicate over HfO_2 on defects compensation may be due to co-existent of ionic and covalent bond in La-silicate. Using a covalent nature of La-silicate is an important key factor to compensate the oxygen defects for improving the effective mobility.

e) Selection of gate electrode materials and structure for further EOT scaling (Chapter 7)

In chapter 7, control the amount of oxygen due to gate electrode material and structure for further EOT scaling were described. Gate stacks is as well as previous experiment, namely, W/La_2O_3. The main findings and contributions of this work are summarized below.

It was found that increment of EOT due to post-metallization annealing was dramatically suppressed by control the amount of oxygen with Si capping layer (MIPS structure). Scaled EOT and small interface state density was achieved at the same time by combination of high temperature annealing with Si capping layer. The simpler and easier method was established to obtain the small EOT.

It was revealed that additional oxygen can be also supplied to high-k layer through TiN/W stack structure as well as W single layer. Moreover, the EOT degradation was suppressed less than 1Å. It was demonstrated that oxygen incorporation with scaled EOT can be attained simultaneously accompanied by oxygen ambient annealing and Si removal process.

High electron mobility in scaled EOT was experimentally demonstrated with La-silicate dielectrics by combination of MIPS structure and high temperature annealing. It is comparable to previous result reported by IBM group.

8.2 Prospects for Further Study

Based on this study, further study of high-k/metal gate stacks with La-silicate is described. One of the most concern issues is the goal of EOT scaling. Although ITRS requires the EOT of 0.5nm in future, EOT scaling may be also predicted to encounter a practical limit due to a technological limit or an economic limit. However, high performance and low power consumption is still quite important. Especially, reduction of power supply voltage is indispensable for ultra low power application. Serious problem of lowering power supply voltage is V_{th} variability. EOT scaling with high-k/metal gate is effective to reduce the V_{th} variability. Thus, the lower supply voltage requires the scaled EOT. In this study, EOT of 0.69nm was demonstrated with La-silicate. The silicate reaction is basically triggered by the presence of oxygen. Control the oxygen corresponds to the control of silicate reaction. Further EOT scaling may be achieved by systematic study including physical analysis. How amount of oxygen in gate stacks should be investigated. Although e-beam evaporation is utilized to deposit the La_2O_3 in this study, the concept is the same if the other method is employed such as ALD or CVD. First La-silicate is formed by the high temperature annealing under rigorous control of oxygen. Then, additional oxygen is introduced into La-silicate. The EOT is determined by the high temperature annealing for La-silicate formation. The MOSFET performance can be improved by additional oxygen incorporation. As previously mentioned in this study, oxygen control is most important issue. In the past, various downsizing difficulties were expected. However, all such difficulties were overcome by the introduction of new technologies. Although there are still many

problems remained in La-silicate dielectrics, it may be solved on the basis of this study.

In conclusion, the original studies referred to in this thesis provide useful information and further understanding for high-k/metal gate system. These studies are also expected to contribute to the future progress of LSIs.

Publications and Presentations

a) Publications

[1] ○T. Kawanago, K. Tachi, J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Electrical Characterization of Directly Deposited La-Sc Oxides Complex for Gate Insulator Application", *Microelectronic Engineering*, Elsevier, vol. 84, issue. 9-10, pp. 2235-2238, 2007

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b) International Presentations

[1] ○T. Kawanago, K. Tachi, J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Electrical Characterization of Directly Deposited La-Sc Oxides Complex for Gate Insulator Application", *INFOS2007*, Session 17.5-Dielectrics & Metal Gates-2, Ref.No.249, Athens, Greece, June, 2007

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c) Domestic Presentations

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