Structural Effects of Channel Cross-section on a Gate Capacitance of Silicon Nanowire Field-Effect Transistors

S. Sato\textsuperscript{a}, K. Kakushima\textsuperscript{b}, P. Ahmet\textsuperscript{a}, K. Ohmori\textsuperscript{c}, K. Natori\textsuperscript{a}, K. Yamada\textsuperscript{c}, and H. Iwai\textsuperscript{a}

Frontier Research Center\textsuperscript{a}, Interdisciplinary Graduate School of Science and Technology\textsuperscript{b}, Tokyo Institute of Technology. Graduate School of Pure and Applied Sciences, University of Tsukuba\textsuperscript{c}. 

Event, Venue information
For suppression of off-state leakage current

Structure and technology innovation (ITRS 2007)

Nano-wire FET

HK/MG stack → EOT Scaling

Silicon nanowire FET is a promising candidate for future CMOS at the scaling limit.
Expectation for the increase of gate capacitance

Increase of the gate capacitance of Gate-around structure is expected using cylindrical conductor model.
Purpose of this work

✓ To investigate the effects of SiNW cross-sectional shapes on gate capacitance of SiNW FET.

✓ To compare the experimental results with the simulation results.
Computer simulation scheme

- Cross-sectional shape of SiNW FET in this work

- The amount of inversion charge was normalized by the peripheral length (the sum of side surfaces and top surface)

- Quantum-mechanical effect approximation: Modified Local Density Approximation method.

- Oxide thickness: Uniform around SiNW channel

- Calculation of the gate capacitance: 
  \[ C_{gate} = \frac{\partial Q_{gate}}{\partial V_{gate}} \]
High inversion carrier density regions around corners because of electric-field concentration

High inversion carrier regions were observed around the corners of SiNW cross-section because of concentration of electric-field.
Effects of corner radius on inversion charge density of SiNW nFETs

- Corner radius was less effective on inversion charge density of SiNW FET with rectangular cross-section.
Effects of cross-sectional dimensions on $Q_{inv}$ and EOT of SiNW nFETs with rectangular cross-sections

As the channel width decreased, EOT decreased.
Structural advantage of SiNW nFETs on gate capacitance

✓ Advantage of SiNW structure is valid down to sub-1 nm region.
✓ Larger gain of gate capacitance was obtained in sub-1nm region.
Comparison of simulation result with experimental results

- Experimental results were confirmed with simulation.
- Larger EOT with experiments were due to thicker oxide at the sides of SiNW cross-sections.

*Oxide thickness at the top of SiNW cross-section was measured.*
Enhancement of the short channel effect immunity by reduction of oxide thickness

As the gate oxide thickness decreased, off-characteristics improved.
Conclusions

✓ Structural advantage of SiNW FET on the gate capacitance is investigated.

✓ As the cross-sectional dimensions decreased, structural gain of the gate capacitance increased.

✓ EOT advantage was confirmed down to sub-1.5 nm by both simulation and experiments.

✓ SiNW FET is more suitable for improvement of $I_{ON}/I_{OFF}$ characteristics than planar FET with the same oxide thickness with respect to the gate capacitance.
Acknowledgement

The authors thank all members of ASKA II line and the researchers in the front-end program in the R&D Department 1, Selete, Tsukuba for device fabrication and fruitful discussions. This work was supported by the program ‘Development of Nanoelectronic Device Technology’ of the New Energy and Industrial Technology Development Organization (NEDO).