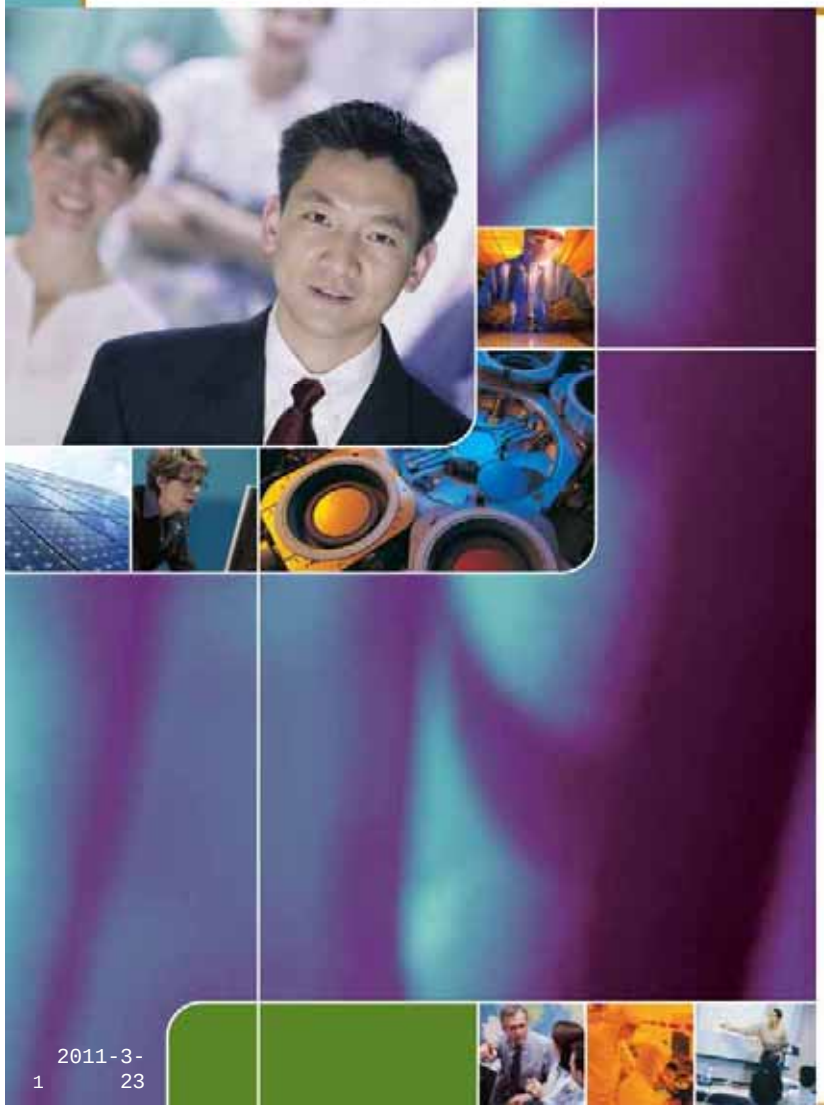
# Structural Effects of Channel Cross-section on a Gate Capacitance of Silicon Nanowire Field-Effect Transistors



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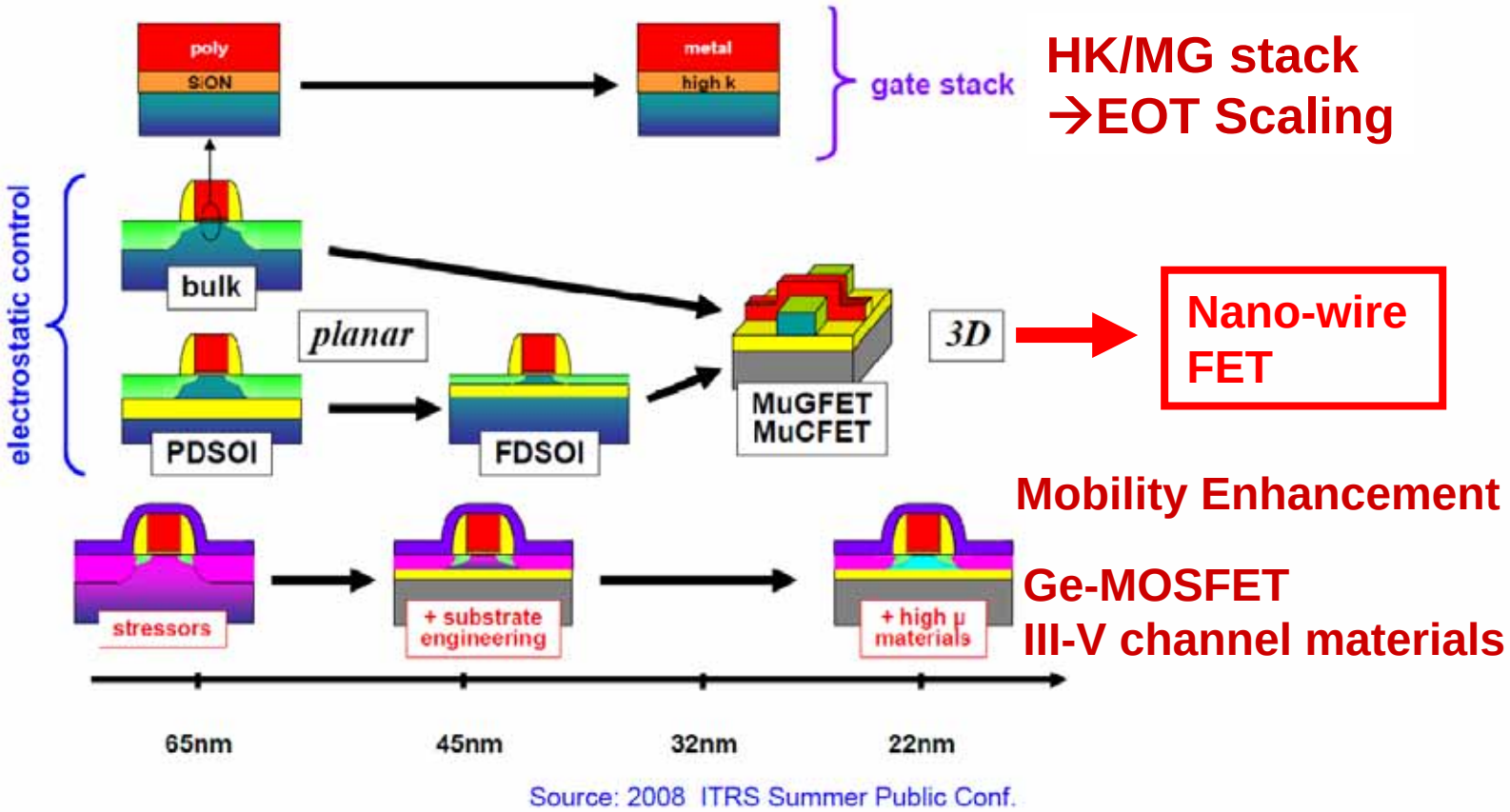
# For suppression of off-state leakage current

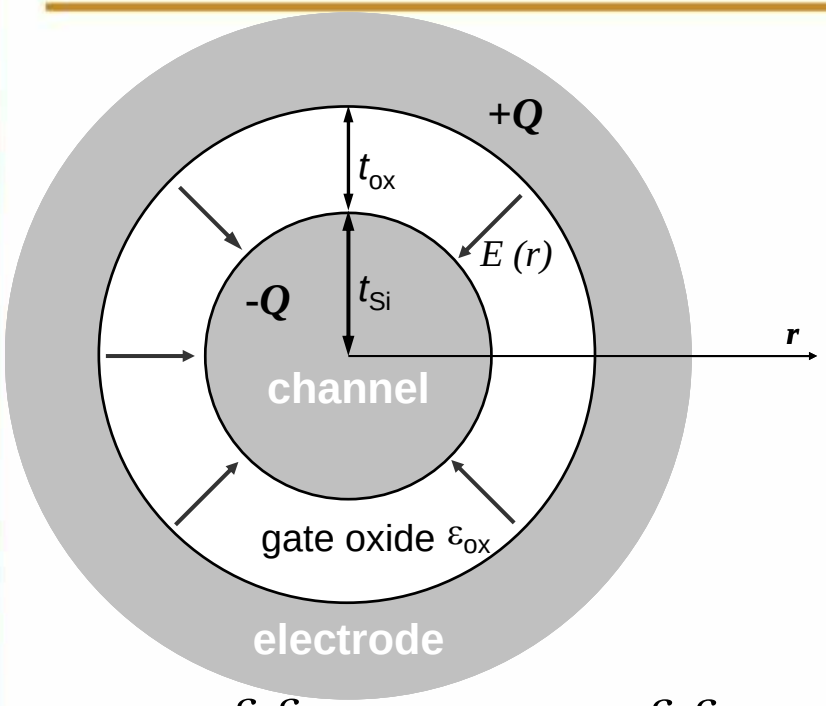
Structure and technology innovation (ITRS 2007)

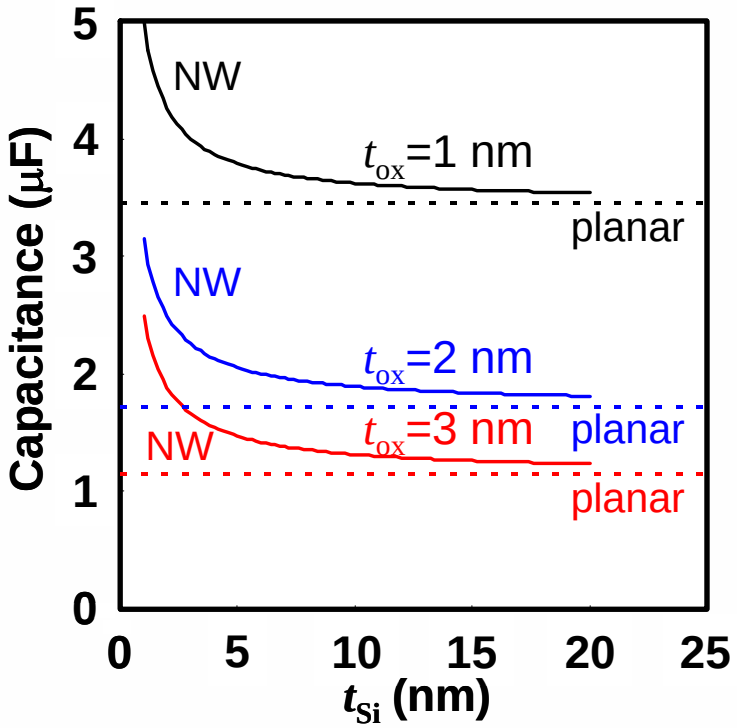



Source: 2008 ITRS Summer Public Conf.

✓Silicon nanowire FET is a promising candidate for future CMOS at the scaling limit.

# Expectation for the increase of gate capacitance




$$C_{NW} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{Si} \cdot \ln\left(1 + \frac{t_{ox}}{t_{Si}}\right)} \qquad C_{planar} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}$$

✓**Increase of the gate capacitance of Gate-around structure is expected using cylindrical conductor model.**

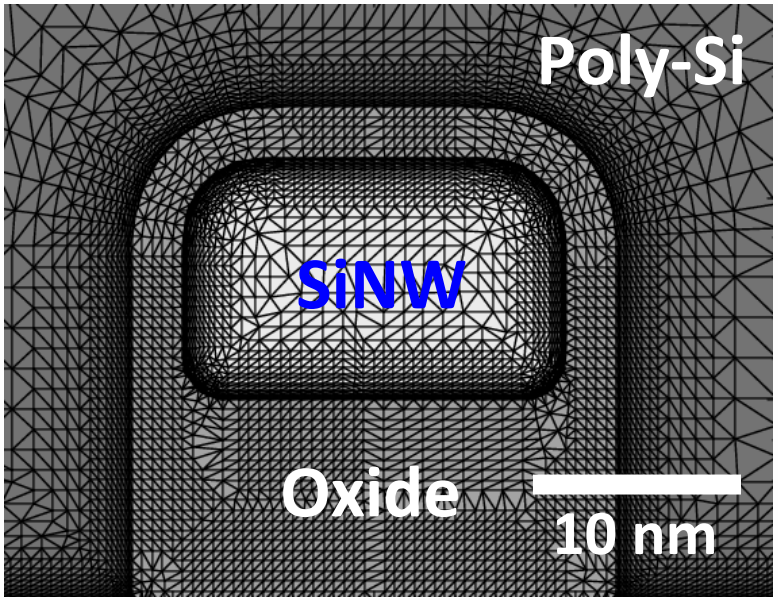
# Purpose of this work

✓To investigate the effects of SiNW cross-sectional shapes on gate capacitance of SiNW FET.

✓To compare the experimental results with the simulation results.

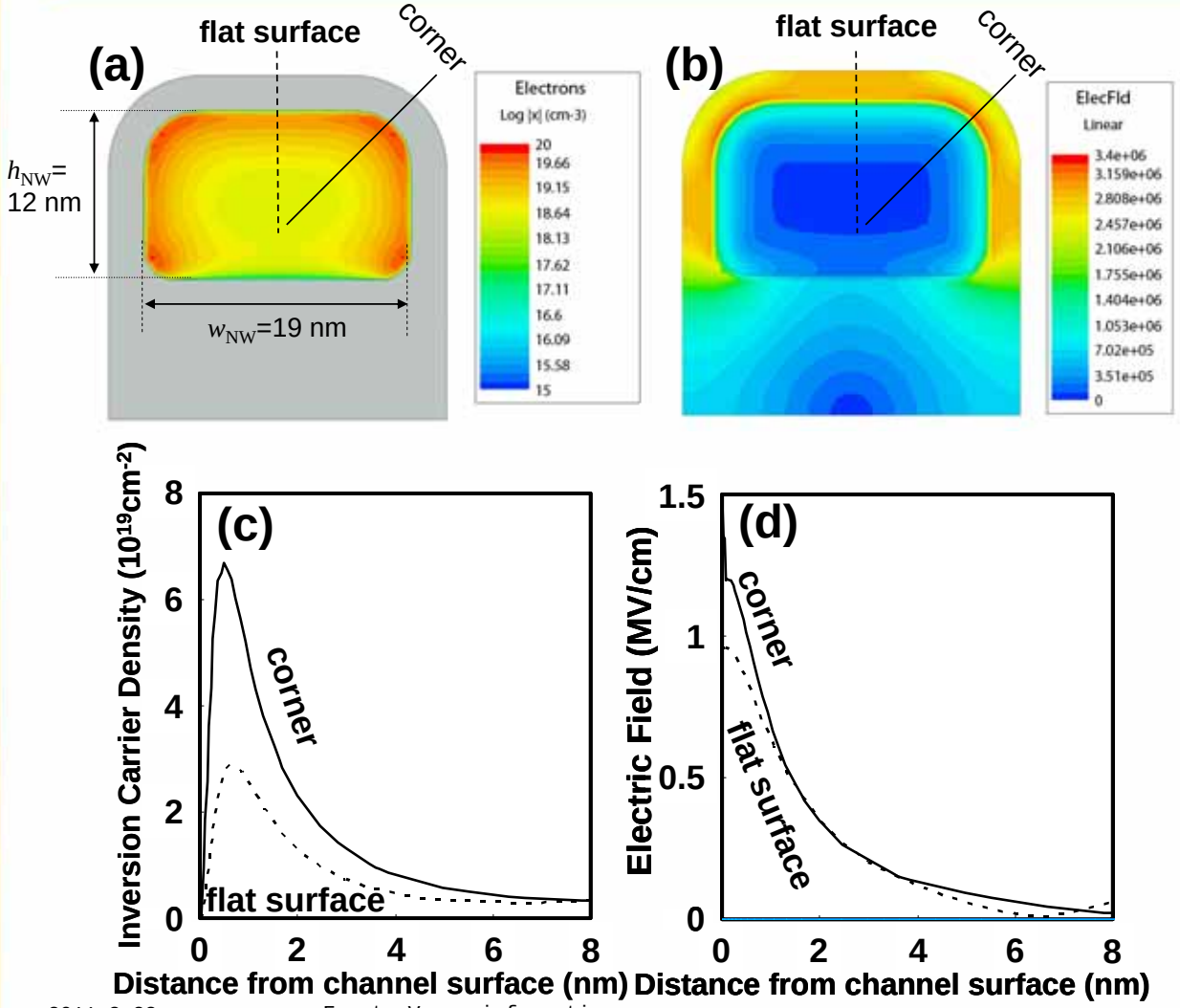
# Computer simulation scheme

➢Cross-sectional shape of SiNW FET in this work



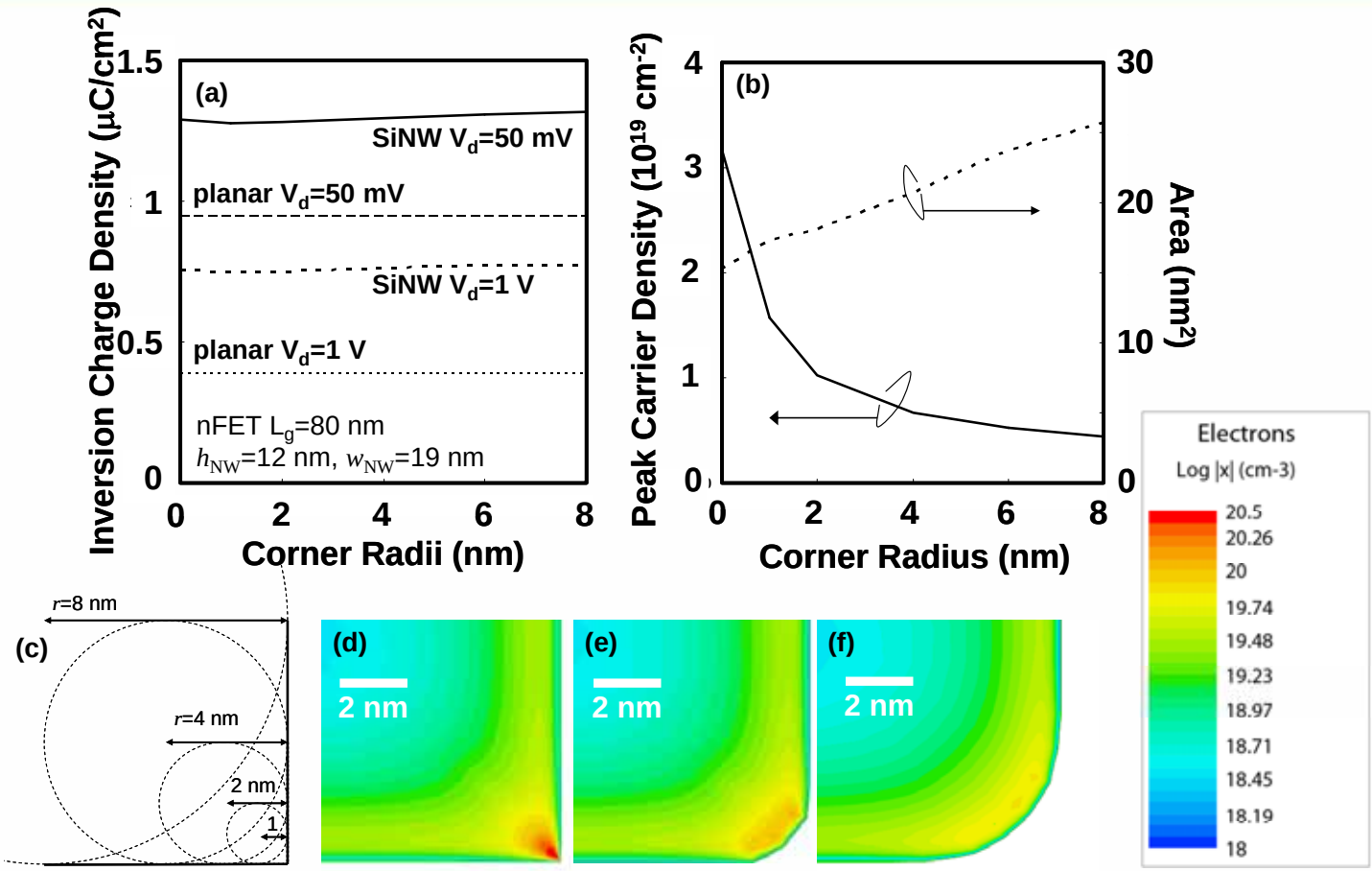

- ✓The amount of inversion charge was normalized by the peripheral length (the sum of side surfaces and top surface)
- ✓Quantum-mechanical effect approximation: Modified Local Density Approximation method.
- ✓Oxide thickness: Uniform around SiNW channel
- ✓Calculation of the gate capacitance: $C_{gate} = \frac{\partial Q_{gate}}{\partial V_{gate}}$

# High inversion carrier density regions around corners because of electric-field concentration



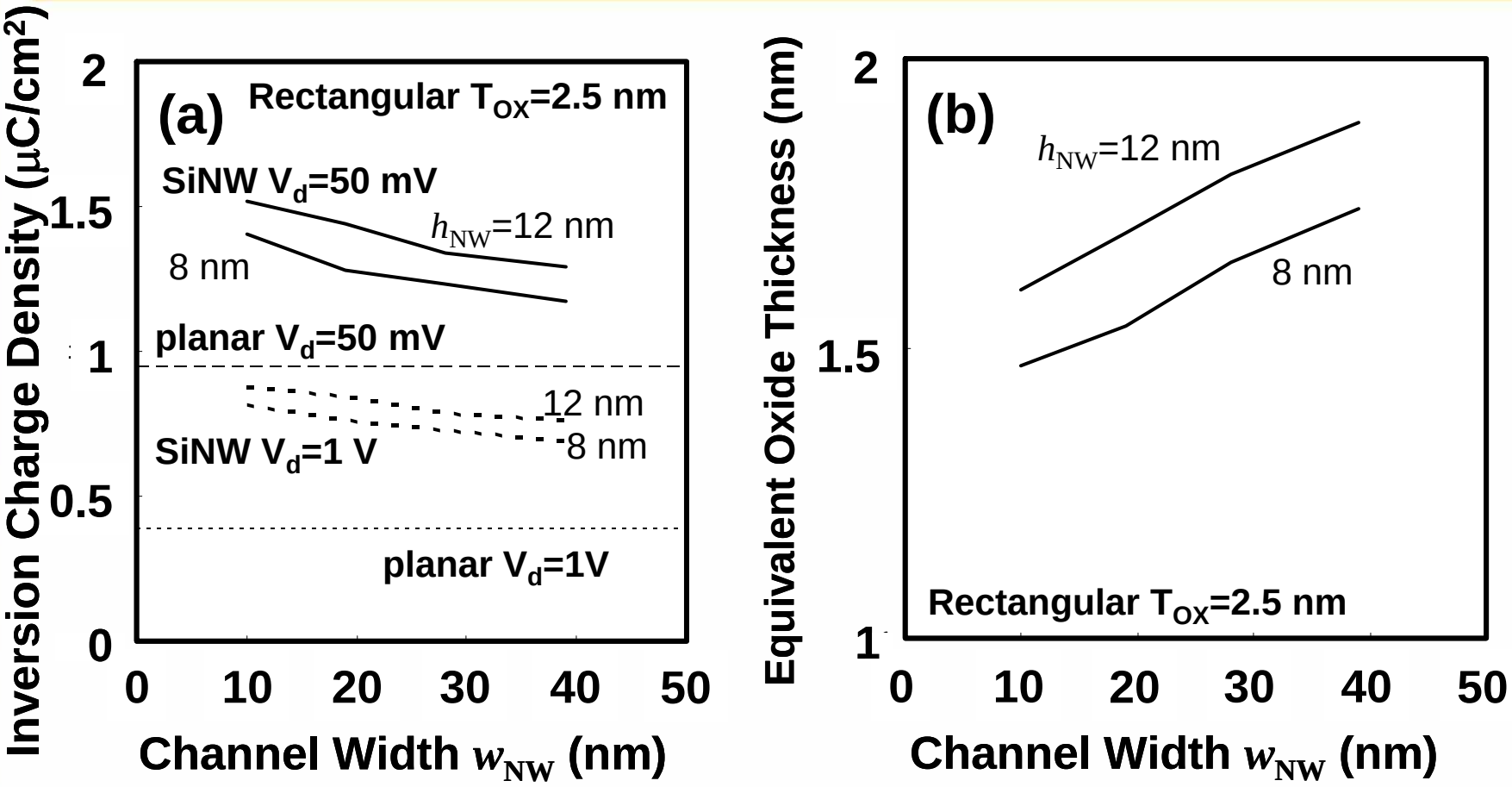

✓**High inversion carrier regions were observed around the corners of SiNW cross-section because of concentration of electric-field.**

# Effects of corner radius on inversion charge density of SiNW nFETs



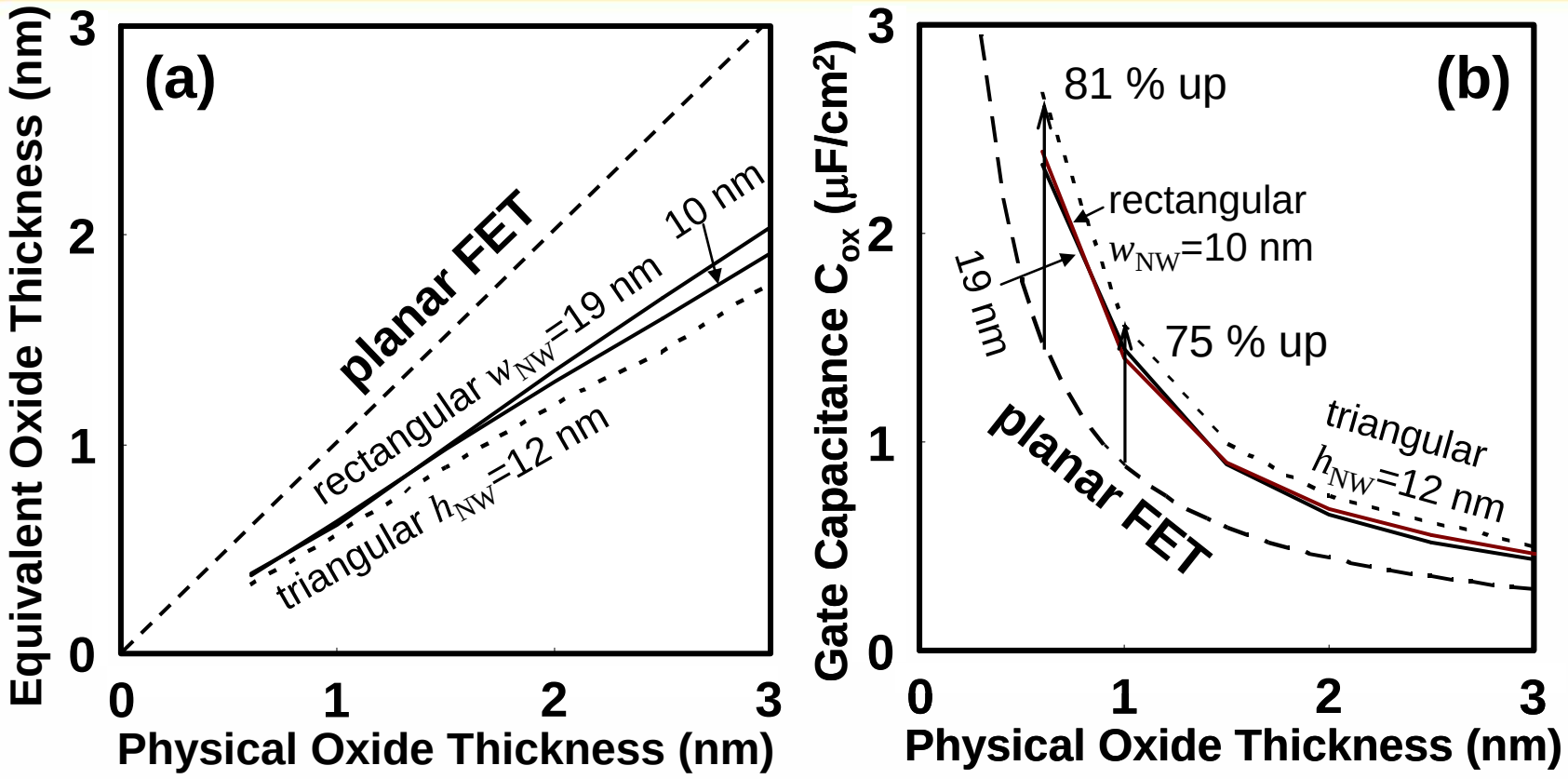

✓Corner radius was less effective on inversion charge density of SiNW FET with rectangular cross-section.

# Effects of cross-sectional dimensions on $Q_{inv}$ and EOT of SiNW nFETs with rectangular cross-sections



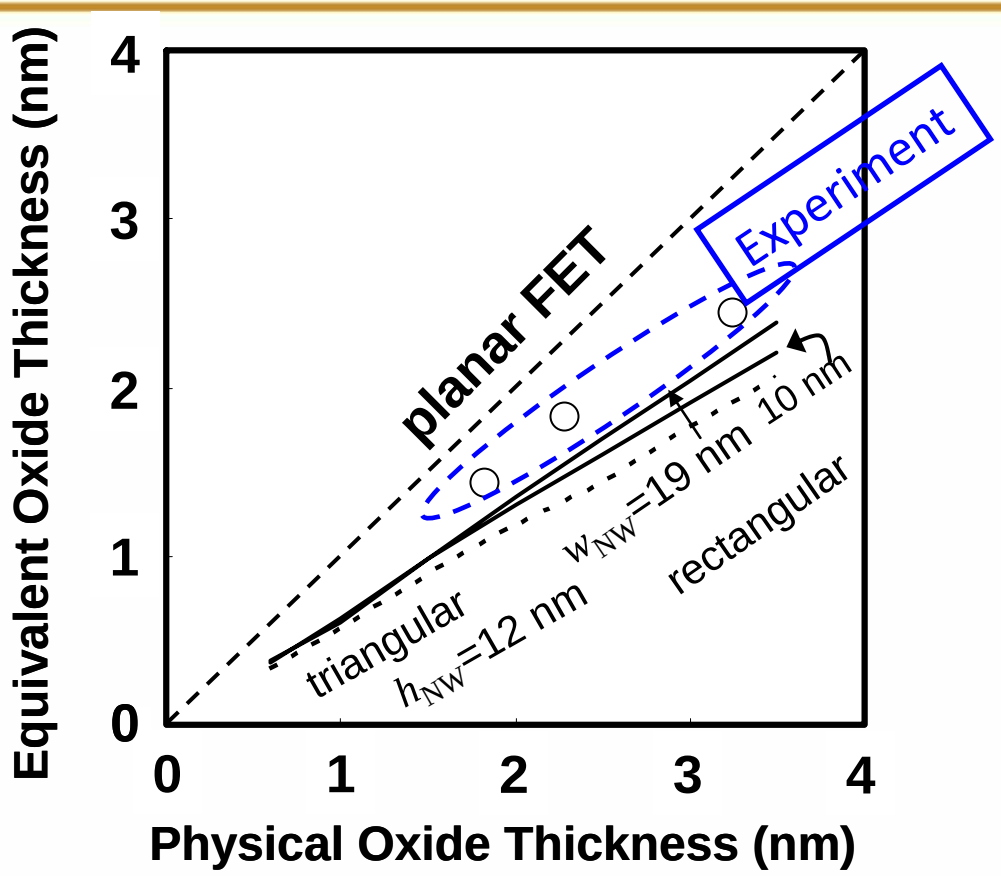

✓As the channel width decreased, EOT decreased.

# Structural advantage of SiNW nFETs on gate capacitance

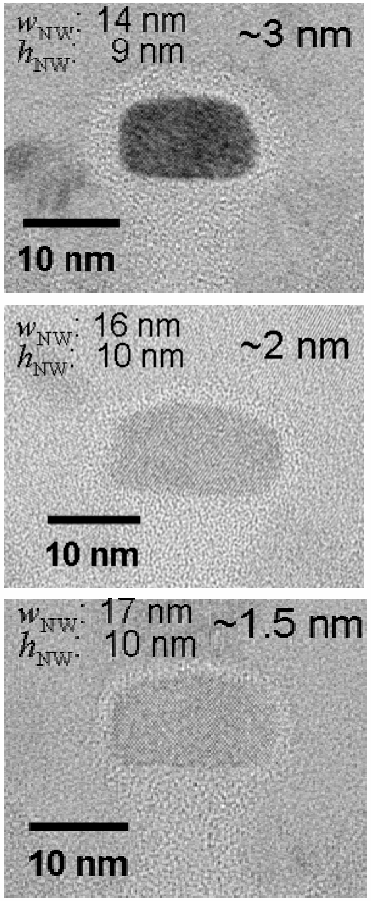



- ✓Advantage of SiNW structure is valid down to sub-1 nm region.
- ✓Larger gain of gate capacitance was obtained in sub-1nm region.

# Comparison of simulation result with experimental results




➢XTEM images

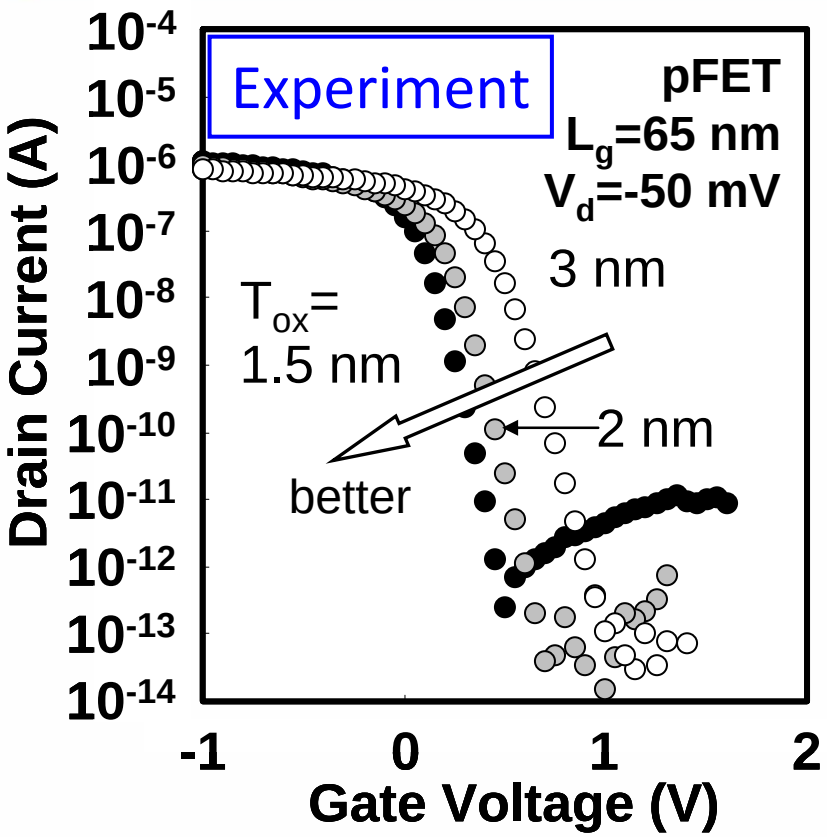


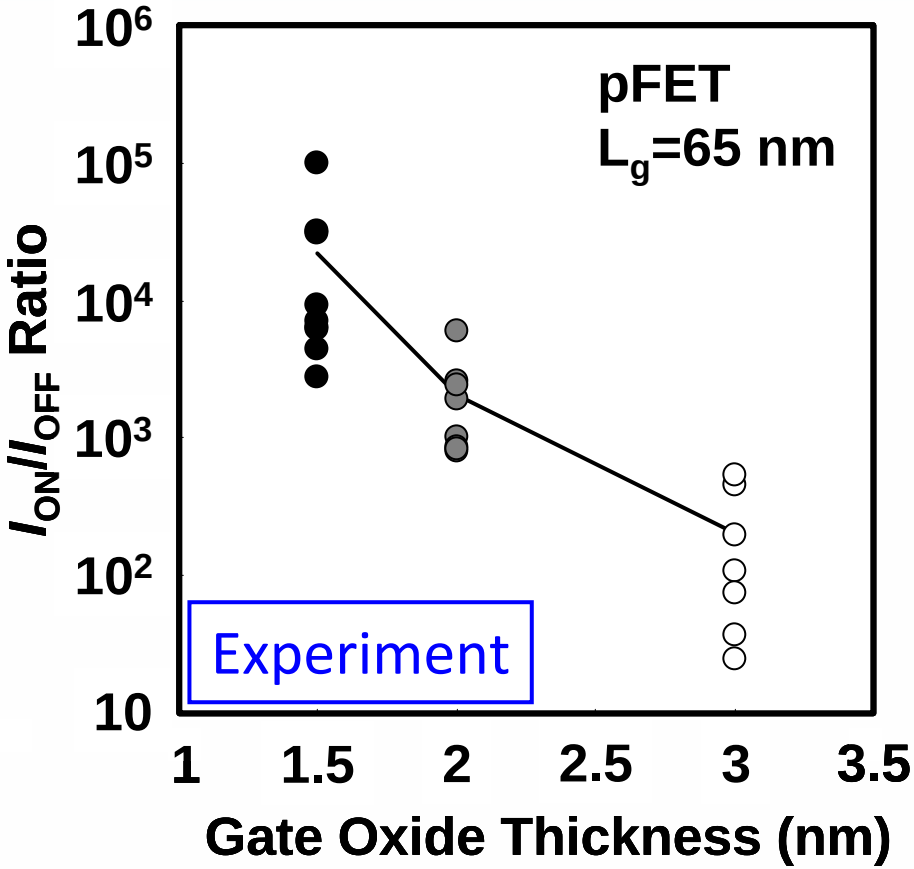

✓Experimental results were confirmed with simulation.

✓Larger EOT with experiments were due to thicker oxide at the sides of SiNW cross-sections.

*Oxide thickness at the top of SiNW cross-section was measured.

# Enhancement of the short channel effect immunity by reduction of oxide thickness




✓As the gate oxide thickness decreased, off-characteristics improved.

# Conclusions

✓Structural advantage of SiNW FET on the gate capacitance is investigated.

✓As the cross-sectional dimensions decreased, structural gain of the gate capacitance increased.

✓EOT advantage was confirmed down to sub-1.5 nm by both simulation and experiments.

✓SiNW FET is more suitable for improvement of $I_{ON}/I_{OFF}$ characteristics than planar FET with the same oxide thickness with respect to the gate capacitance.

# Acknowledgement

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