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TiN/W/La_2O_3/Si High-k Gate Stack for EOT below 0.5nm

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Electrical properties of TiN/W/La_2O_3 high-k gate stack were studied by fabricating MOS capacitors. Obtained results showed that a W layer inserted at the interface between TiN and La_2O_3 is the key factor in suppression of the equivalent oxide thickness (EOT) increment during the annealing process. An EOT of 0.43nm was achieved with a 3nm W inserted layer after annealed at 800°C in a forming gas ambient. Our results show that TiN/W/La_2O_3 gate stack is one of the promising candidates for realizing high-k gate stack with EOT of 0.5nm and beyond.

Introduction

As the result of continues scaling in CMOS technology, required equivalent oxide thickness (EOT) in MOSFETs is expected to down to a thickness of less than 0.5nm in the near future. For such a small EOT, a directly contacted of high-k/Si structure is required because of a SiO_x based interfacial layer at the interface between high-k and Si will limits the EOT value obtainable with the high-k gate dielectrics. However, realizing a high quality interface between directly contacted high-k dielectric and Si substrate bring about a great challenge, because of the interface between gate dielectric and Si substrate has always been SiO_2/Si or SiON/Si in the past. Recently, several types of high-k gate stacks without any SiO_x based interfacial layer at the interface between high-k and Si were investigated [1-4], however, further reduction of EOT to beyond 0.5nm with a high quality interface is still the major obstacle in the future high-k gate stack technology.

In this paper, we report our approaches in realizing EOT of 0.5nm and below by using La_2O_3 as the high-k dielectric and employing TiN/W as the gate electrode. An EOT of 0.43nm has been achieved with TiN/W/La_2O_3 gate stack after annealed at 800°C by optimizing the thickness of the W layer. Our results show that a proper gate electrode structure is one of the most important factors for realizing EOT below 0.5nm in La_2O_3 high-k gate stack.

Experimental

La_2O_3 thin films were deposited by e-beam evaporation in an ultra-high vacuum chamber on HF-last n-Si substrates. After the deposition of La_2O_3 thin films, the substrates were transferred into a sputter chamber without breaking the ultra-high vacuum. Tungsten (W) and TiN gate electrodes were deposited by RF sputtering and

reactive RF sputtering, respectively. After patterned by lithography and reactive ion etching (RIE), post-metallization annealing was carried out in a forming gas ambient (H_2:N_2 = 3:97%) at various temperatures. Back side contacts were formed by Al deposition. The samples were evaluated by electrical measurements and the EOT values of the samples were calculated by NCSU CVC program [5].

Results and Discussion

A schematic illustration of the structure of deposited samples and a cross sectional TEM image of the fabricated gate stack after annealed at 800°C for 2 seconds in a forming gas ambient are shown in Figure 1. No any SiO_x like interfacial layer was observed at the interface between La_2O_3 high-k dielectric and the Si substrate after such a temperature thermal processing.

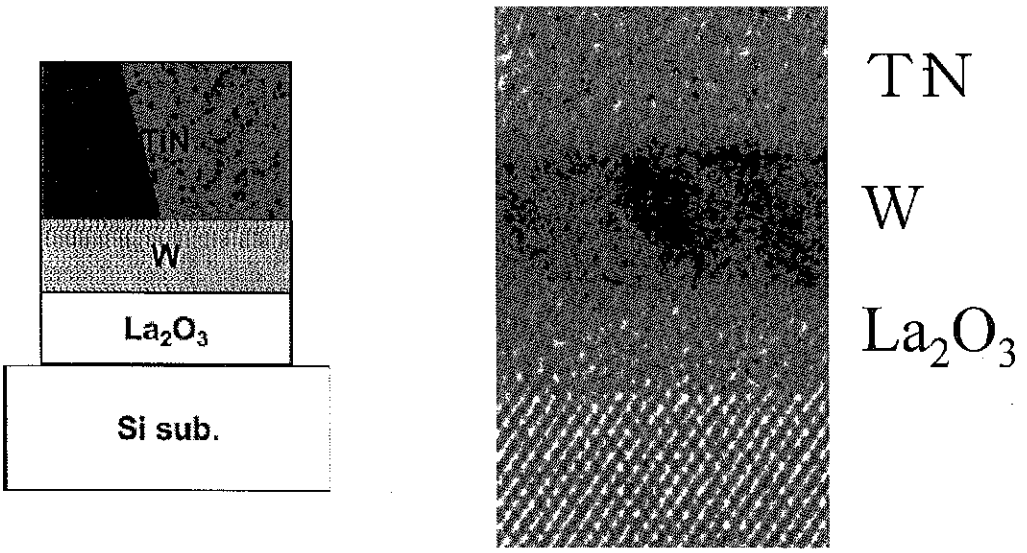

Figure 1. Schematic illustration of the structure of deposited samples and a cross sectional TEM image of the gate stack after annealed at 800°C for 2 seconds in a forming gas ambient.

Obtained lowest EOT from TiN(45nm)/W/La_2O_3(3nm)/n-Si MOS capacitors with different thicknesses of W layer are shown in Figure 2. These samples were annealed at 700°C in a forming gas ambient for 30 minutes. A minimum EOT of 0.57 nm was obtained with a 3nm W layer. The samples annealed at 800°C in a forming gas ambient for 2seconds also a give similar result where a minimum EOT of 0.43 nm was obtained with a 3nm W layer. Obtained EOTs without a W layer insertion were 2.3 nm for 700°C in a forming gas ambient for 30minutes and 1.5 nm for 800°C in a forming gas ambient for 2seconds (not shown). The huge difference in obtained EOT between the capacitors with and without a W layer insertion indicating that the W layer inserted at the interface between La_2O_3 high-k dielectric and TiN electrode plays the crucial role in suppression of the EOT increment during annealing process. Figure 2 also shows a low EOT can be obtained by optimizing the inserted W layer thickness.

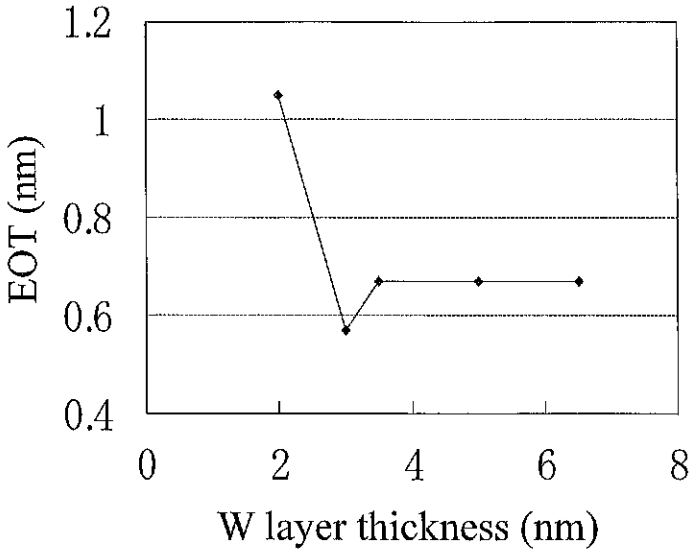

Figure 2. Obtained lowest EOT from TiN(45nm)/W/La_2O_3(3nm)/n-Si MOS capacitors with different W layer thicknesses. (Samples were annealed at 700°C in a forming gas ambient for 30min)

Figure 3 show the measured Capacitance-Voltage (C-V) curves from TiN(45nm)/W(3nm)/ La_2O_3(3nm)/n-Si MOS capacitors annealed at 500°C and for at 700°C for 30 minutes, and at 800°C for 2 seconds in an forming gas ambient. The C-V characteristics at higher voltages also show that the gate dielectric film quality was better in the samples annealed at 700°C for 30 minutes compare to that of the samples annealed at 500°C for 30 minutes. No significant reduction in k-value of the dielectric film was observed during the annealing process performed at 700°C for 30 minutes compare to the annealing process performed at 500°C for 30 minutes. Lowest EOT of 0.43nm was obtained when the samples annealed at 800°C for 2 seconds, however, the hysteresis was not as negligibly-small as those observed with the samples annealed at 500°C and 700°C for 30 minutes.

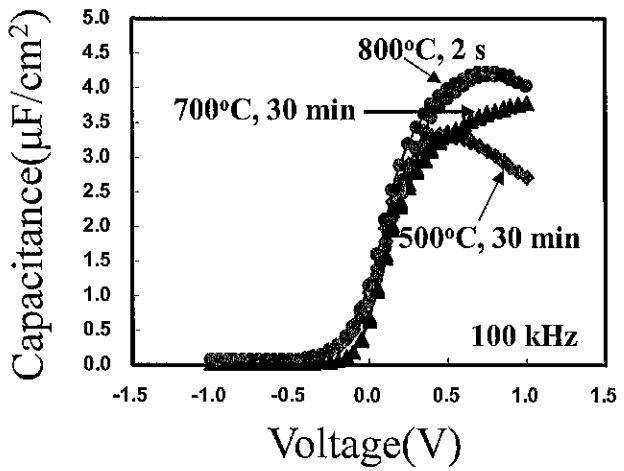

Figure 3. C-V characteristics of TiN(45nm)/W(3nm)/La_2O_3(3nm)/n-Si MOS capacitor annealed in an forming gas ambient at 500°C for 30minuts, 700°C for 30minuts and 800°C for 2 seconds (with hysteresis).

The results above show that the thermal stability properties of La_2O_3 and Si interface can be significantly improved by the TiN/W gate electrode. The results also show that there is a great possibility to overcome the thermal stability problems of high-k materials on Si by developing a proper gate electrode structure.

Summary

The importance of the gate electrode structure in realizing EOT of 0.5nm and below was demonstrated. Our results show that a W layer inserted at the interface between TiN and La_2O_3 is the key factor in suppression of the EOT increment during high temperature annealing process. An EOT of 0.43nm was achieved with TiN/W(3nm) /La_2O_3(3nm)/n-Si gate stack after annealed at 800°C in a forming gas ambient. An EOT of 0.57 nm was also obtained with TiN(45nm)/W(3nm)/La_2O_3(3nm)/n-Si MOS capacitor even after an annealing process was performed at 700°C for as long as 30 minutes. Our results also showed the possibility to overcome the thermal stability problems in extremely scaled high-k gate stack with EOT of 0.5nm and beyond by developing a proper gate electrode structure.

Acknowledgments

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