Metal Inserted Poly-Si Stacks with La_2O_3 Gate Dielectrics for Scaled EOT and V_{FB} Control by Oxygen Incorporation

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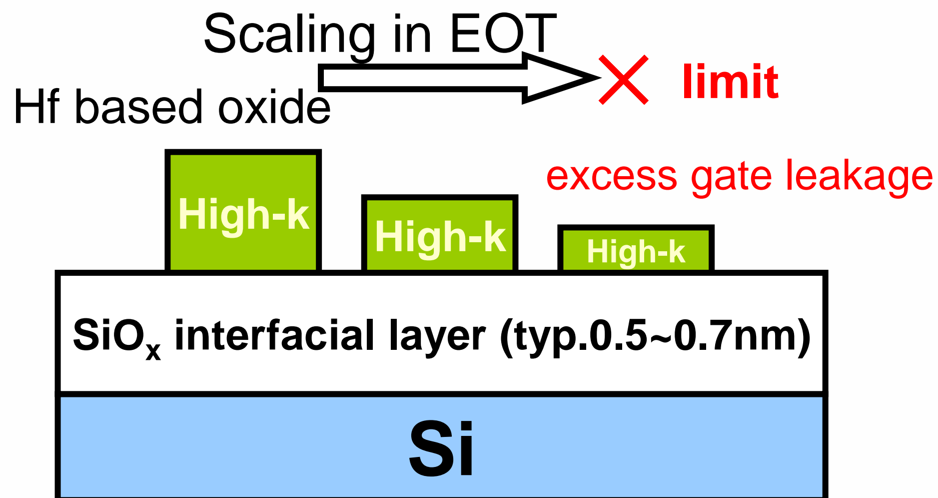
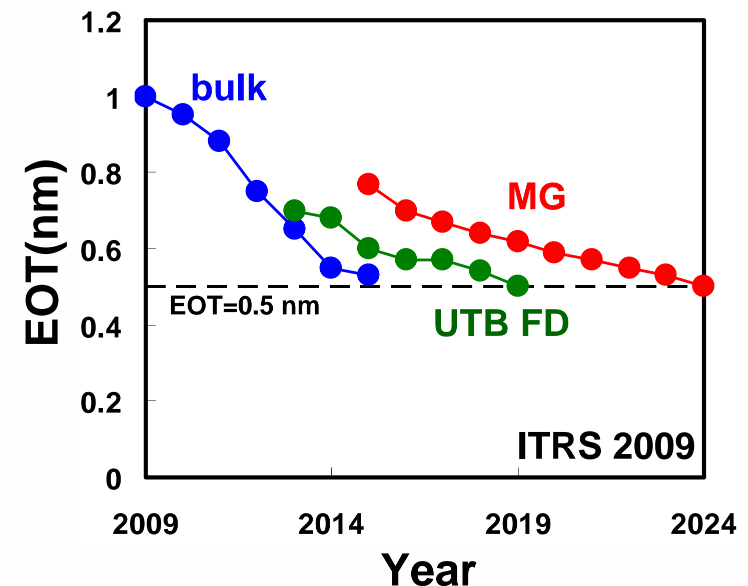
Event, Venue information

Outline

- Direct contact high-k/Si Structure
- MIPS stacks for scaled EOT with La_2O_3 dielectrics
- C-V characteristics of MOS capacitors
- Flatband voltage control by oxygen incorporation
- Conclusions

Scaling issue in high-k gate dielectrics



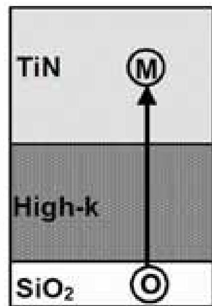


SiO_2 interfacial layer inserted or re-grown for

- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

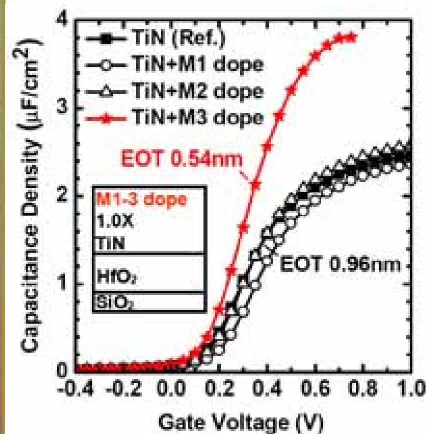
SiO_2-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm

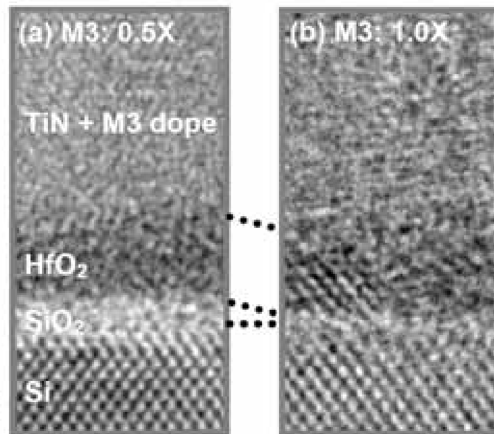
Reports on direct contact of high-k/Si



IL scavenging

T. Ando, et al., IEDM. p.423 (2009).





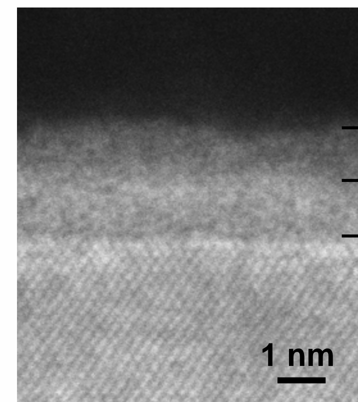
Control of oxygen atoms

Direct HfO_2/Si structure

Our approach

500 °C, 30 min

K. Kakushima, et al., ESSDERC2009

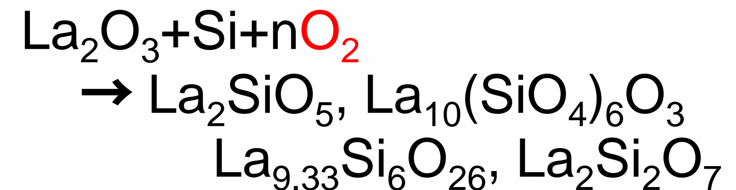


W

La_2O_3 k=23

La-silicate k=8~14

Silicate formation



$La_2O_3 + Si + nO_2$
$\rightarrow La_2SiO_5,\ La_{10}(SiO_4)_6O_3$
$La_{9.33}Si_6O_{26},\ La_2Si_2O_7$

La_2O_3 can easily achieve direct contact of high-k/Si

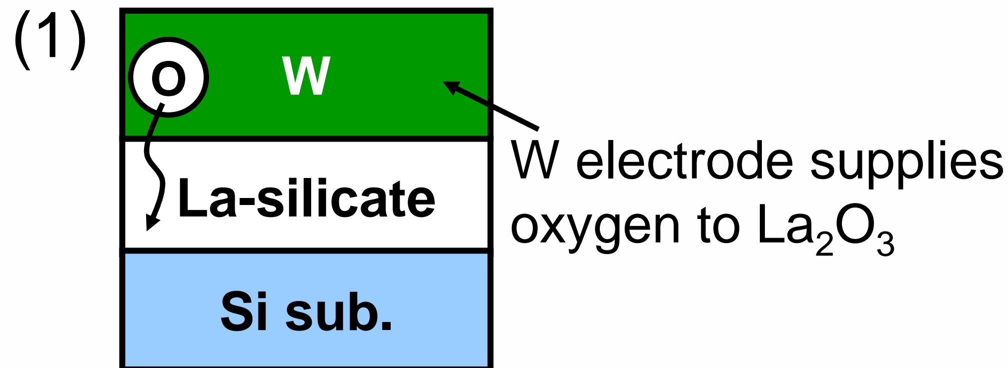
Motivation & Objective

- Improvement of interfacial property at high-k/Si interface is essential
- V_{FB} tuning is also important issue in high-k /metal gate stacks

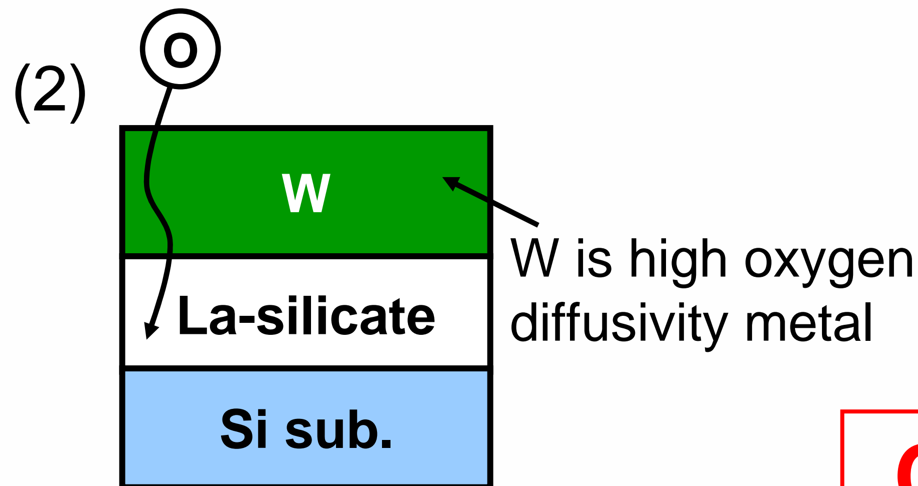
How to improve interfacial property accompanied by scaled EOT with La_2O_3 dielectrics

V_{FB} control by oxygen incorporation

Problems for scaled EOT with La_2O_3



E. J. Preisler, et al., Appl. Phys. Lett., vol.85, p.6230(2004)



C. S. Park et al., SSDM 2007, p.14

Excess oxygen

Excess silicate formation (EOT increase)

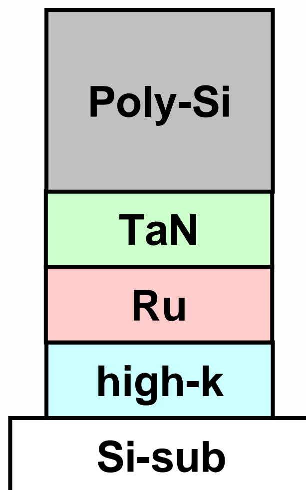
Deficient oxygen

Oxygen vacancy (reduced mobility, gate leakage)

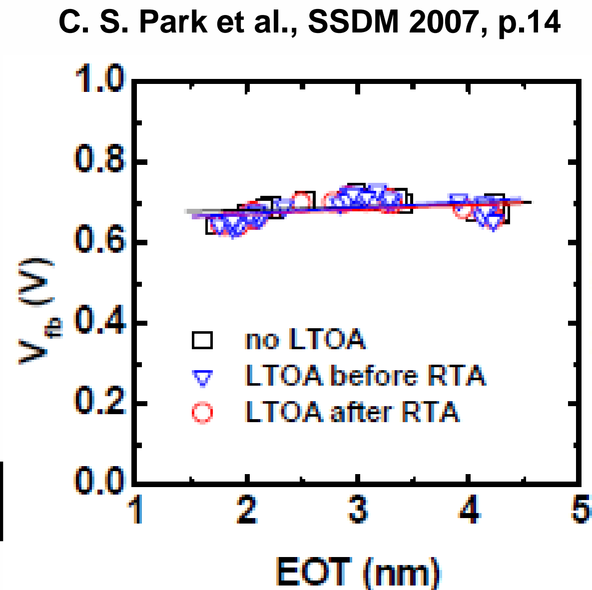
Control of oxygen

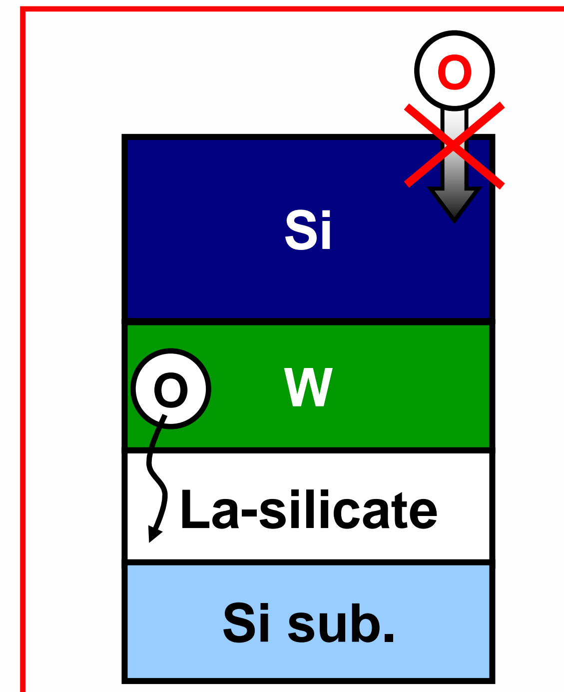
Strategy & Concept

Oxygen trigger the silicate reaction



C. S. Park et al., SSDM 2007, p.14

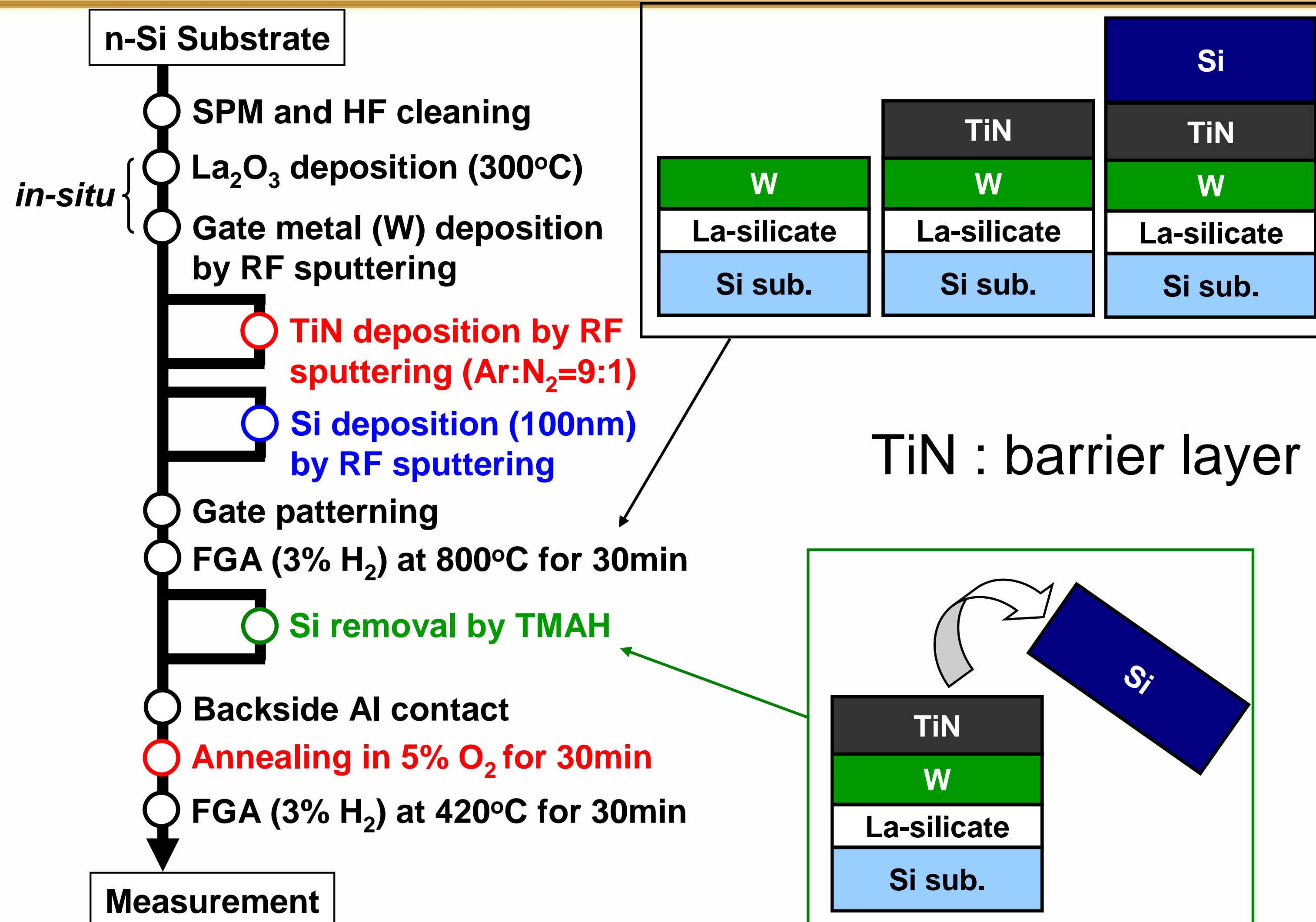




Poly-Si prevent the oxygen diffusion

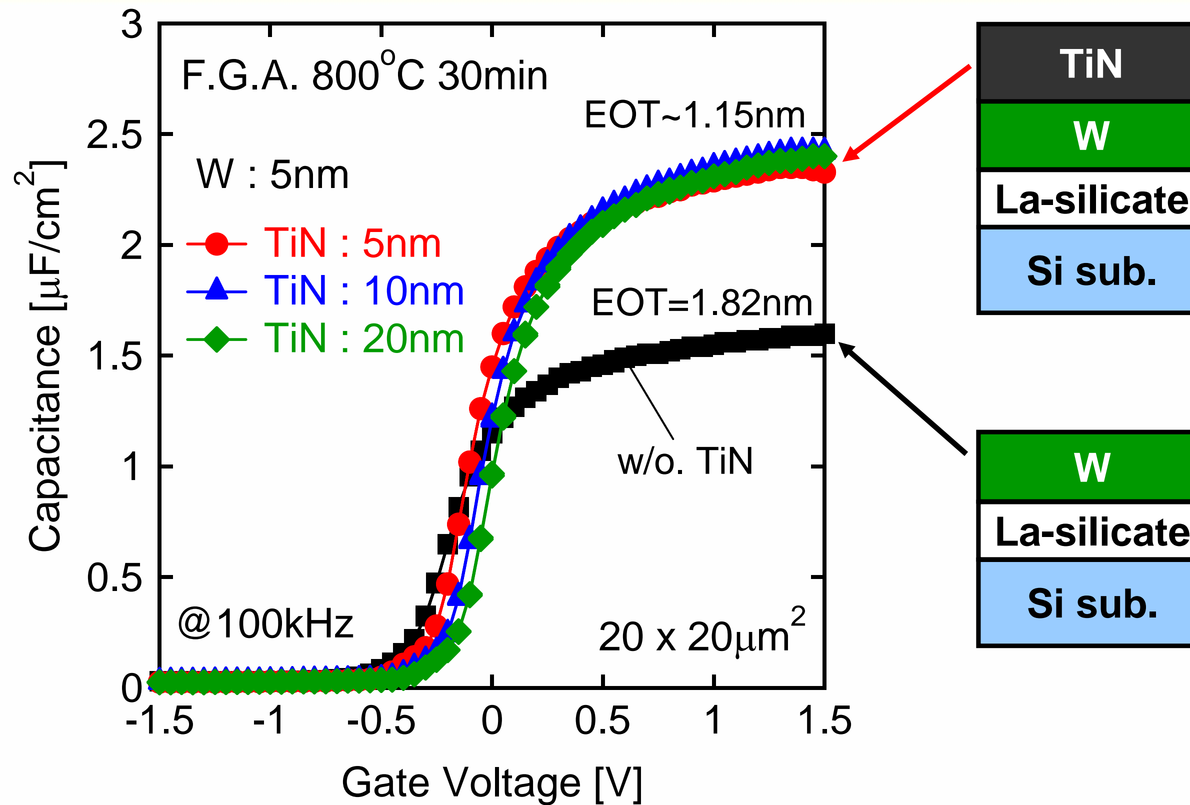
Oxygen in W metal is consuming during annealing process

Experimental procedure



TiN : barrier layer

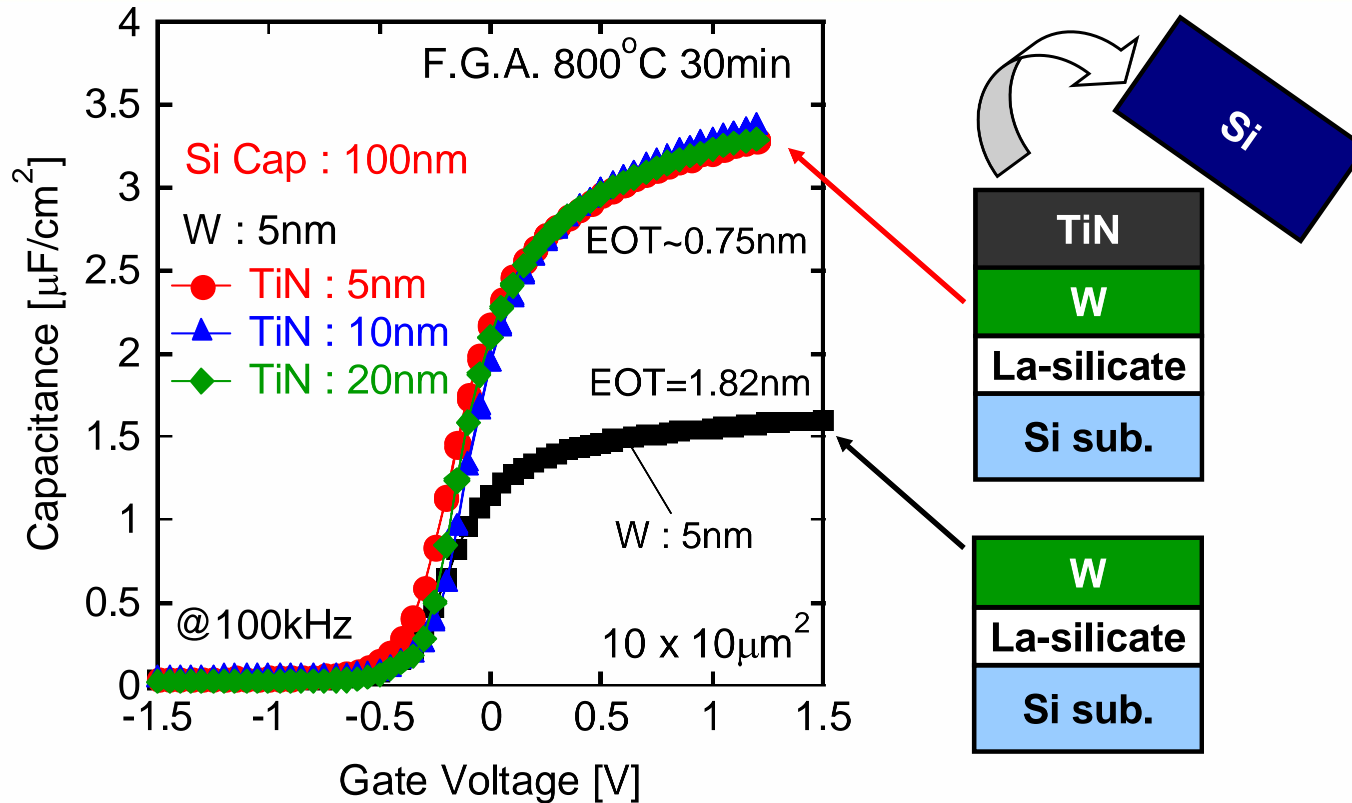
C-V characteristics ~TiN/W~



TiN layer is effective to suppress the increase in EOT

Barrier layer or Oxygen getter

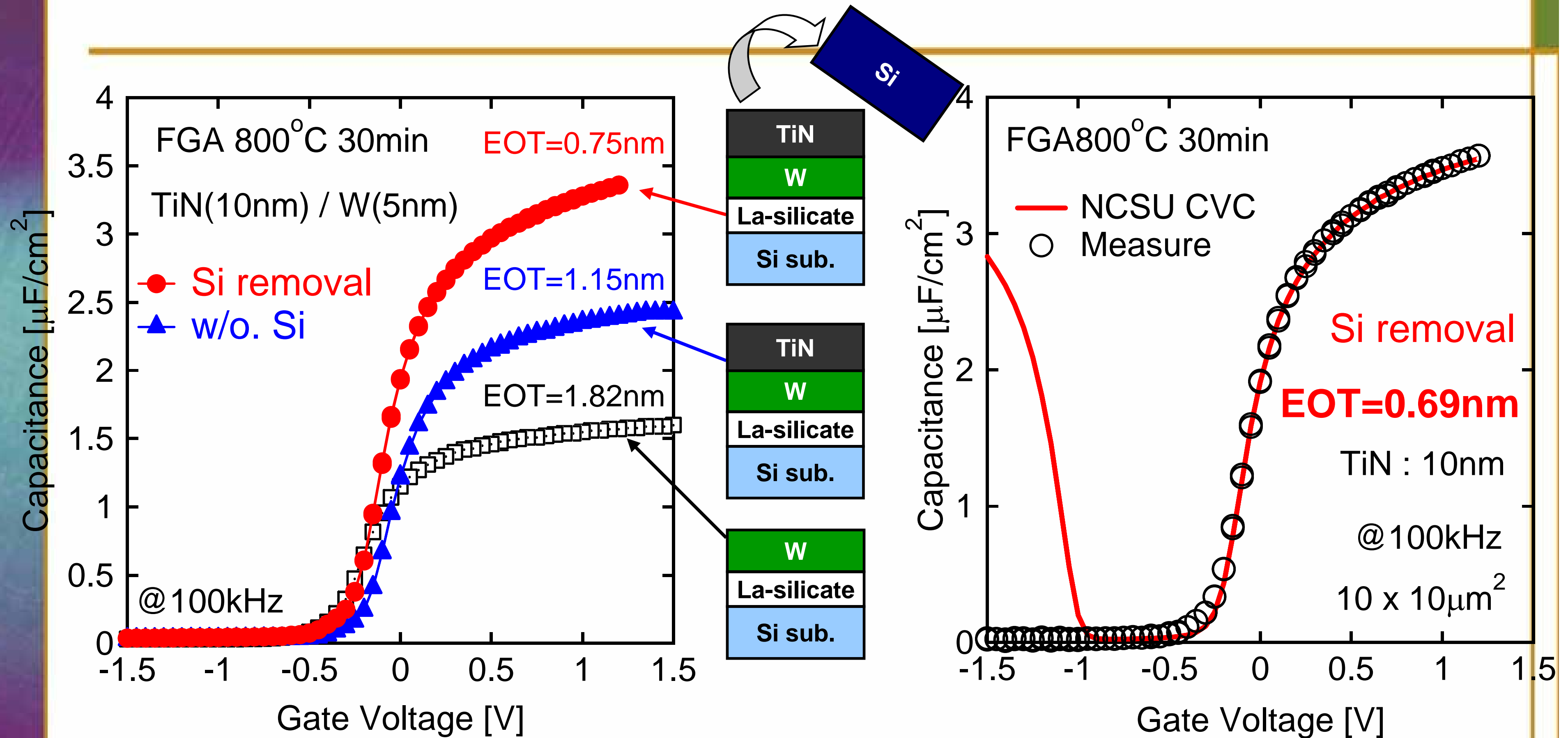
C-V characteristics ~MIPS~



EOT increase is dramatically suppressed with MIPS

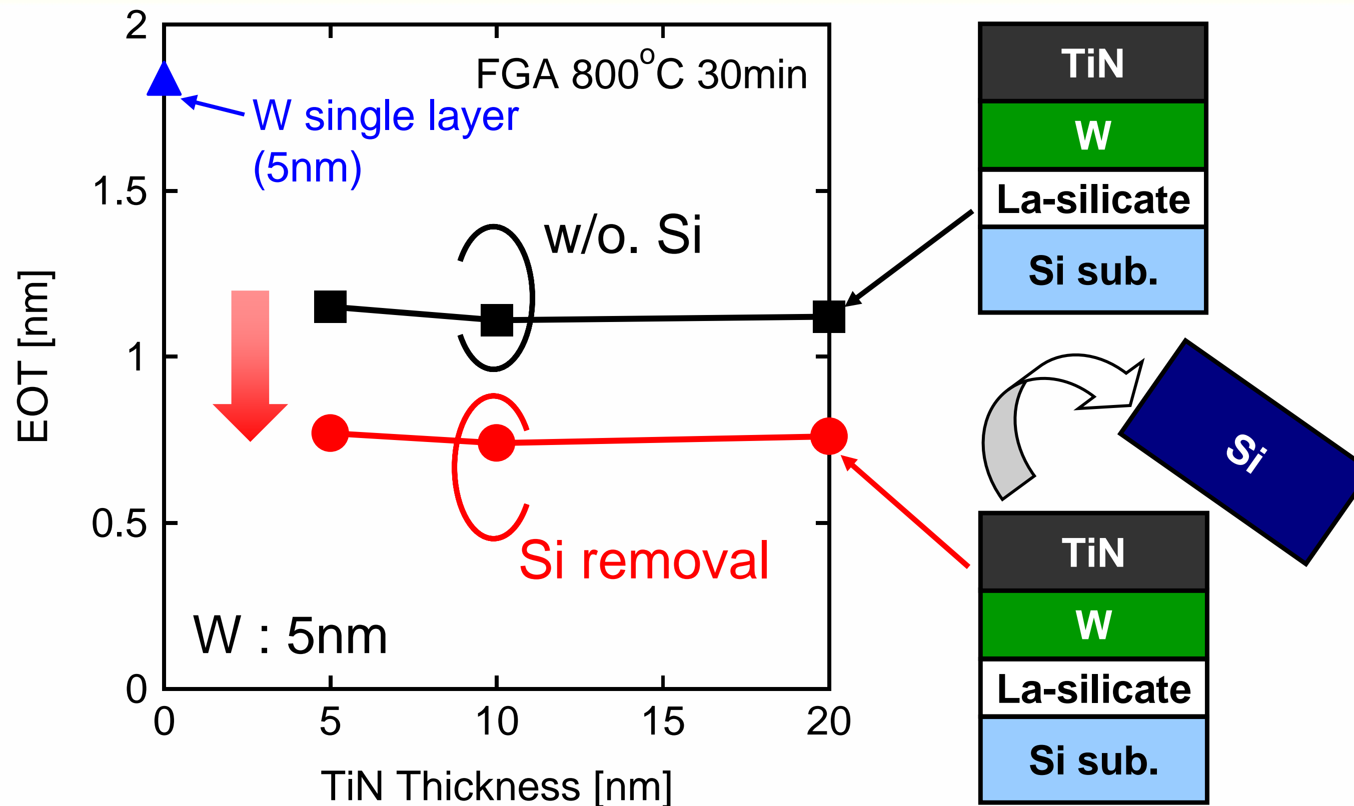
V_{FB} is almost identical

Comparison of C-V characteristics



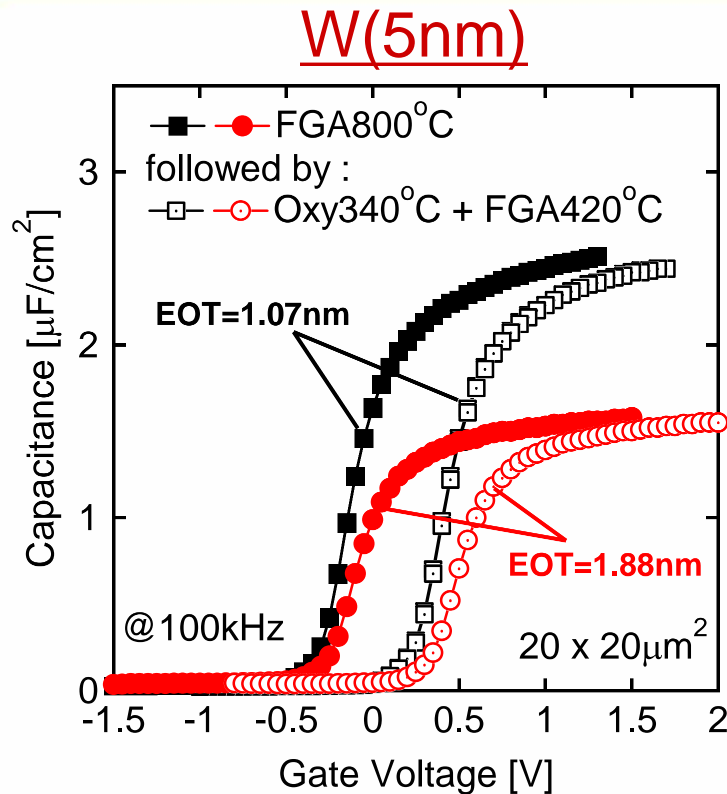
EOT of 0.69nm can be attained with a combination of MIPS structure and FGA 800 °C 30min

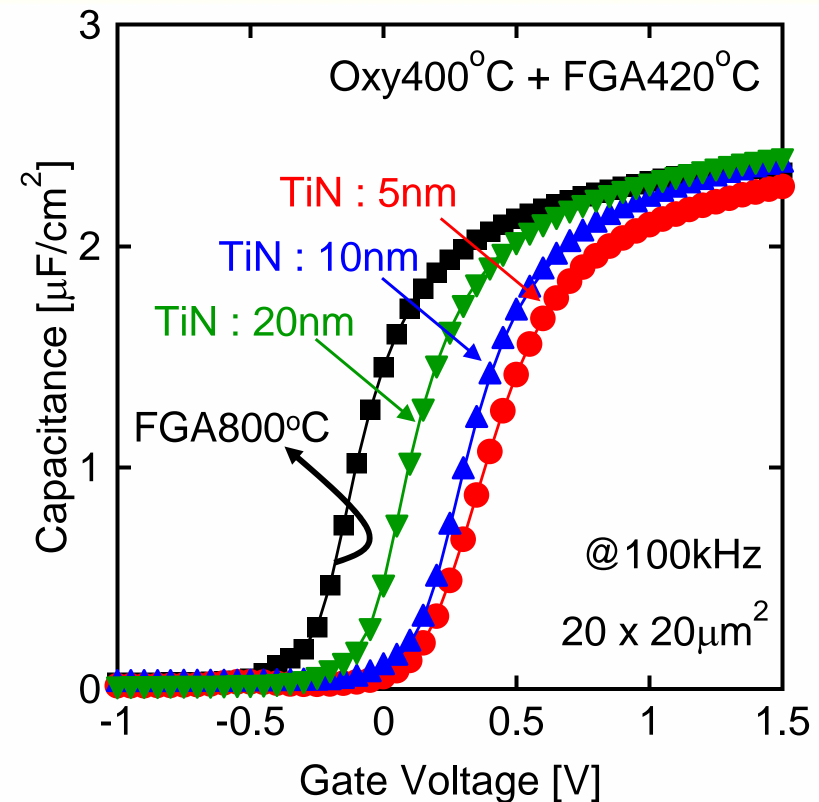
Effect of gate metal structure on EOT



Si Cap layer can prevent the excess oxygen incorporation from atmospheric

Oxygen incorporation through TiN/W

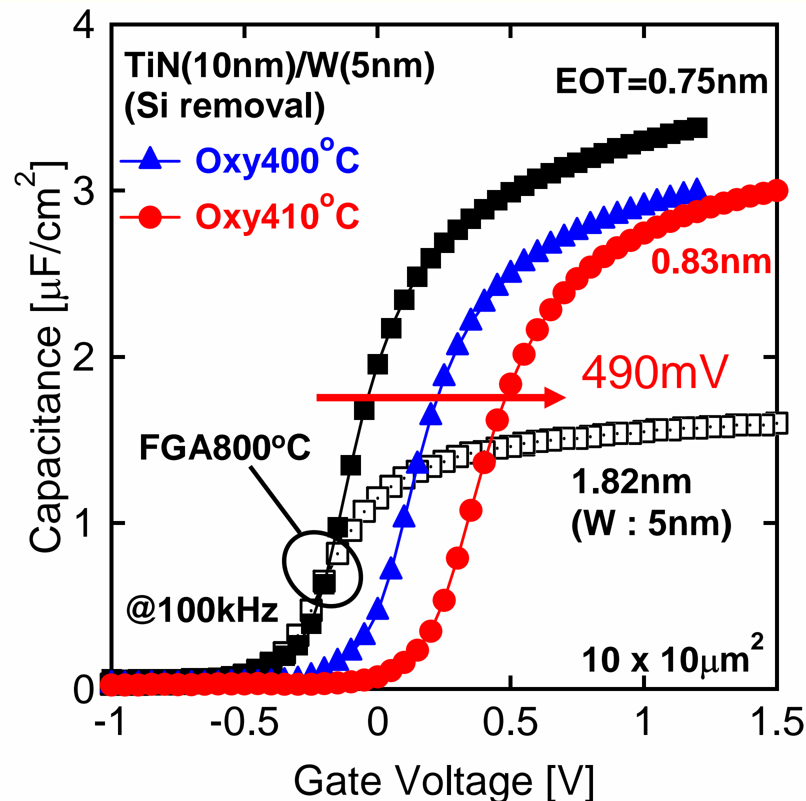


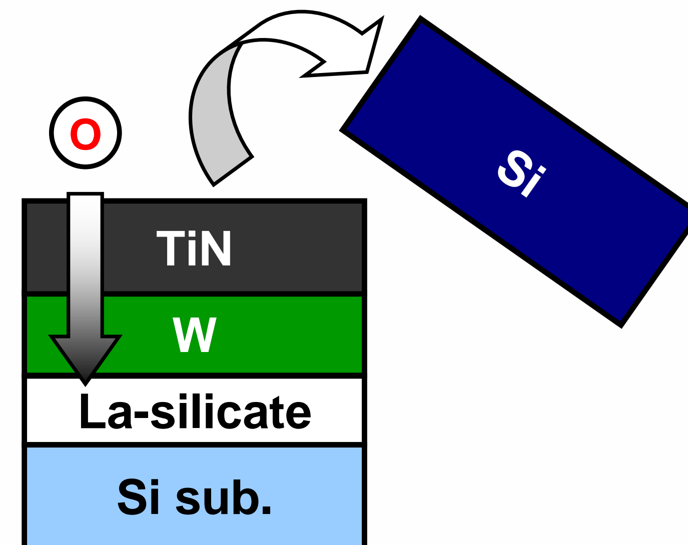


T. Kawanago, et al., ESSDERC2010

Positive V_{FB} shift increase with decreasing the TiN thickness

Oxygen incorporation after Si removal





Positive V_{FB} shift by 490mV can be observed

EOT degradation is less than 1Å

Conclusions

- MIPS with high temperature annealing is extremely effective to improve interfacial property accompanied by scaled EOT simultaneously
- Close to the ideal C-V curve with EOT of 0.69nm can be achieved
- Oxygen incorporation after Si removal yields positive V_{FB} shift by 490mV while EOT penalty is less than 1Å

Acknowledgements

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Thank you for your attention!