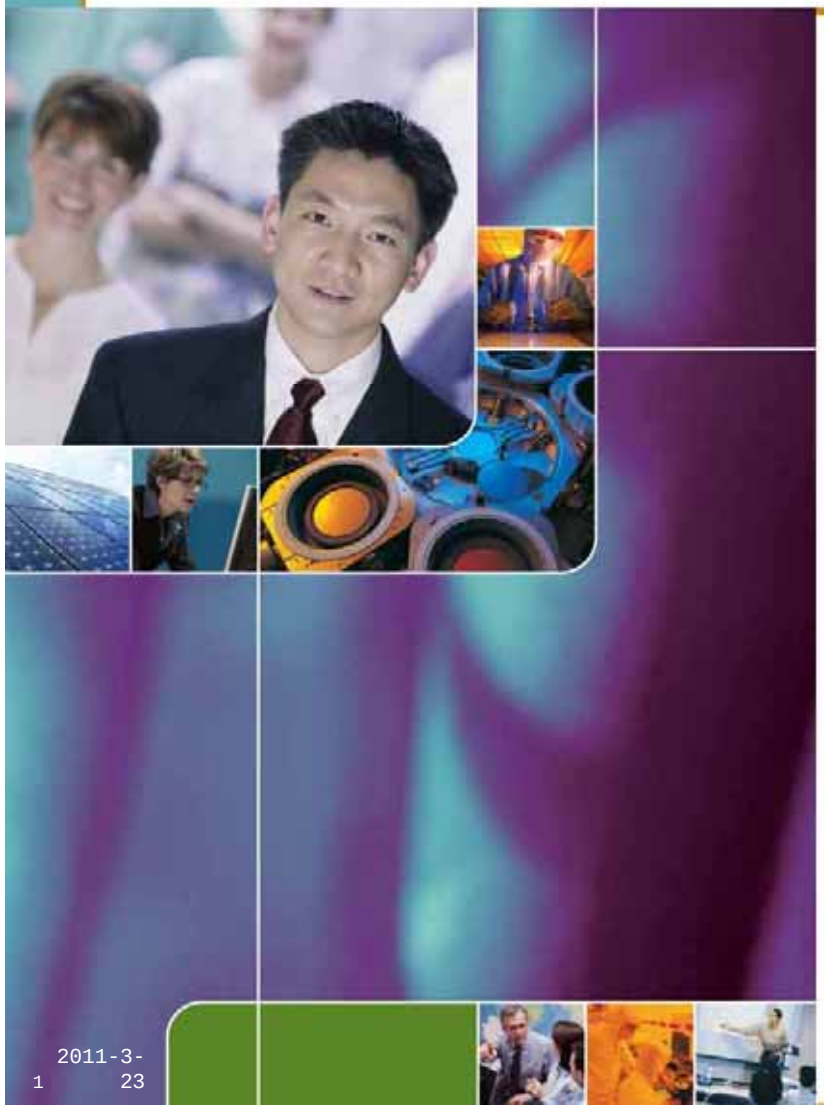
Annealing Effect on the Electrical Properties of La_2O_3/InGaAs MOS Capacitors



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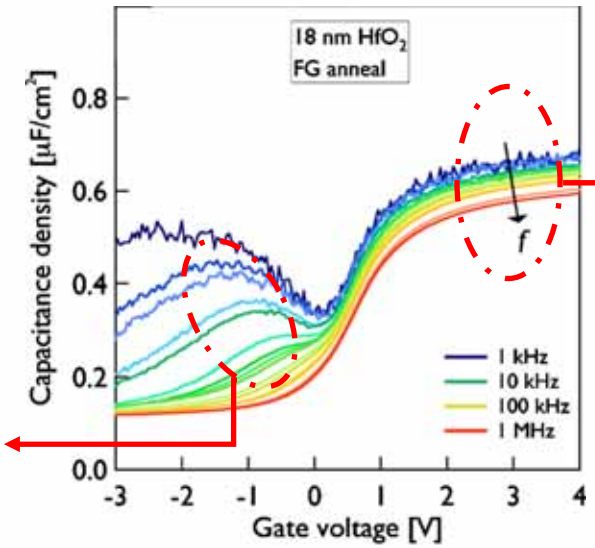
Background of InGaAs

MOS devices with III-V channels, especially InGaAs, have been of great interest as one of the promising candidates for future MOSFET, owing to high electron mobility.

	Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electron Mobility (cm^2/Vs)	600	4600	7800	20000	30000
Electron Saturation Velocity ($\times 10^7$ cm/s)	1	1.2	0.8	3.5	5
Ballistic Mean Free Path (nm)	28	80	106	194	226
Energy Band-gap (eV)	1.12	1.42	0.72	0.36	0.18

Electron mobility
$In_{0.53}Ga_{0.47}As$
~ 7800 cm^2/Vs



Frequency dispersion in accumulation.

Bump of C-V curves in inversion and depletion.

InGaAs MOS devices lack good electrical properties.

Ref. Y. Hwang *et. al*, Applied Physics 108 (2010)

High-*k* materials

Al_2O_3 has been reported to have small interface state density with reduced hysteresis.

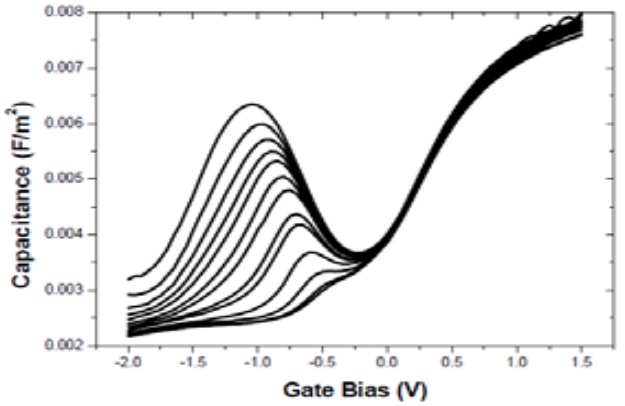
Al_2O_3 (*k* ~9)

Higher *k*-value dielectrics are needed for further scaling.

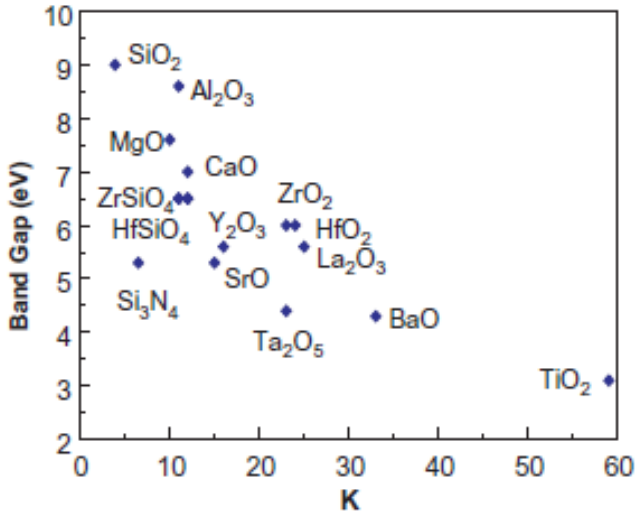
La_2O_3 (*k* ~23)

High *k*-value and large band gap

La_2O_3 has been identified as a good candidate for Si-MOSFET.



Ref. E O'Connor *et. al*, ECS Transaction (2010)



Ref. J. Robertson, Solid-State Electronics (2005)

Purpose

Investigation of annealing effects on the electrical characteristics of La_2O_3/InGaAs MOS capacitors

Annealing
Temperature : 300 - 450 ^oC
Duration : 30 sec, 5 min, or 30 min
Ambient gas : Forming gas (F.G.) (N_2:H_2=97%:3%)

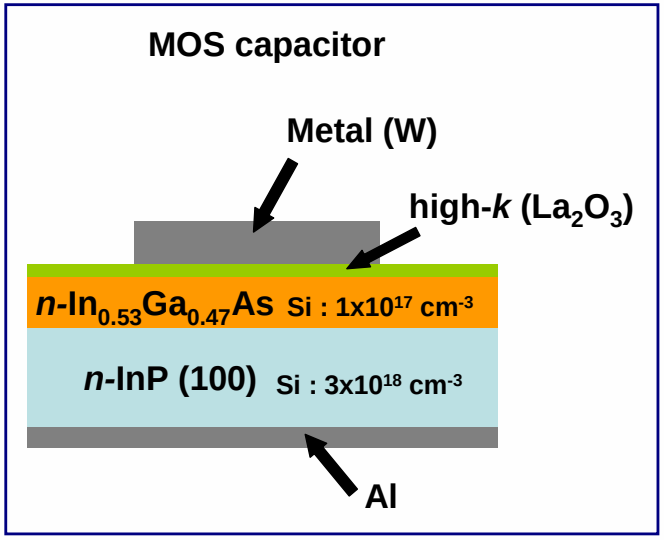
Fabrication Process

W/La_2O_3 (8 nm)/$In_{0.53}Ga_{0.47}As$/*n*-InP (100)

300 nm thick $In_{0.53}Ga_{0.47}As$ on *n*-InP wafer

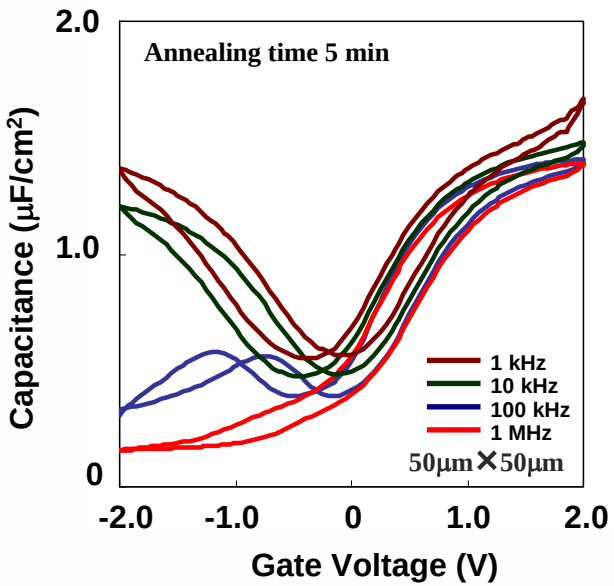
- **Acetone and ethanol cleaning**
  HF 20% (3 min) treatment
- **High-*k* (La_2O_3) e-beam deposition @ R.T**
  in-situ
- **Gate metal (W) deposition by sputtering**
- **Reactive ion etching (RIE) of W gate**
- **Backside Al contact**
- **Annealing in F.G. from 300 to 450 °C for 30 sec, 5 min, or 30 min**

Electrical Characterization

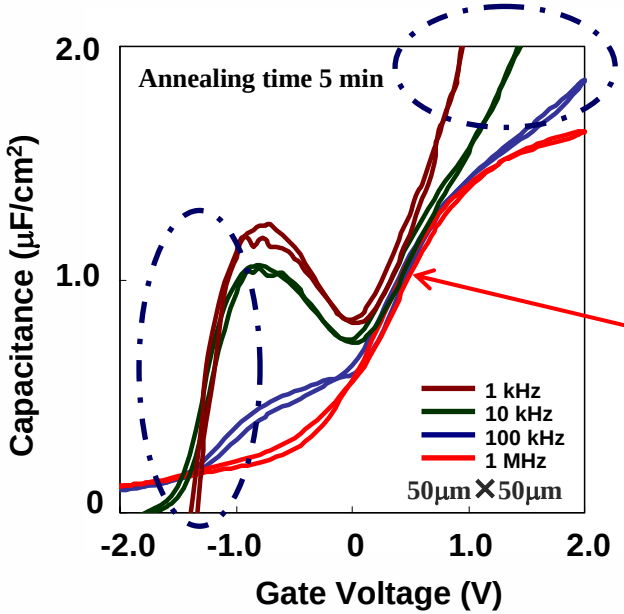


Annealing temperature effect

300 °C

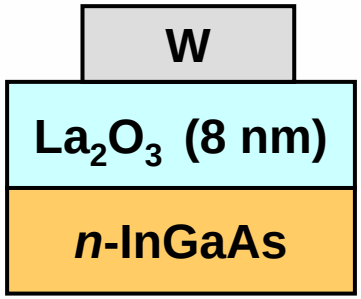


450 °C



Effect of leakage current

Improvement in the hysteresis

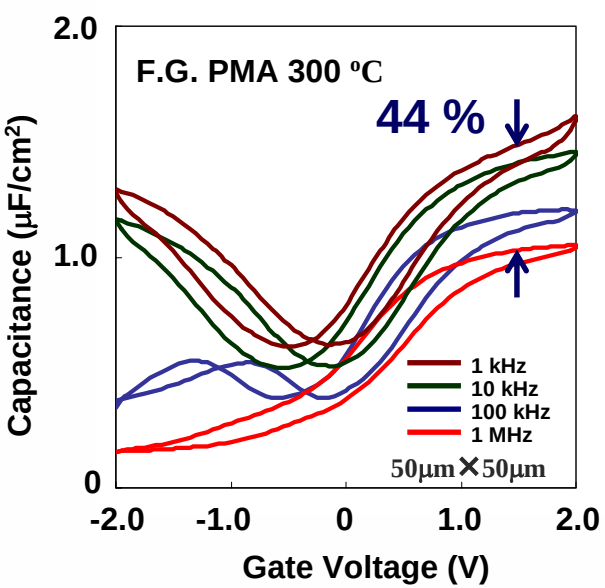


Higher annealing temperature could reduce the hysteresis, but increase the leakage current.

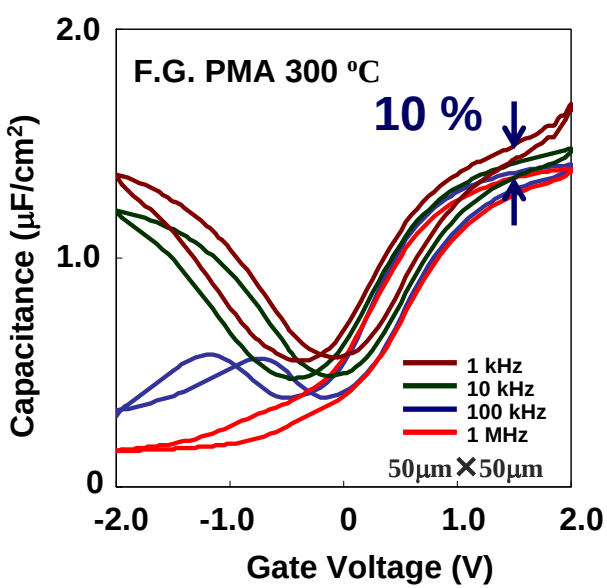
Lower annealing temperature is preferable.

Annealing time effect

0.5 min

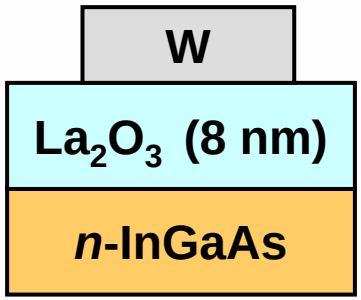


5 min



Improvement in the frequency dispersion

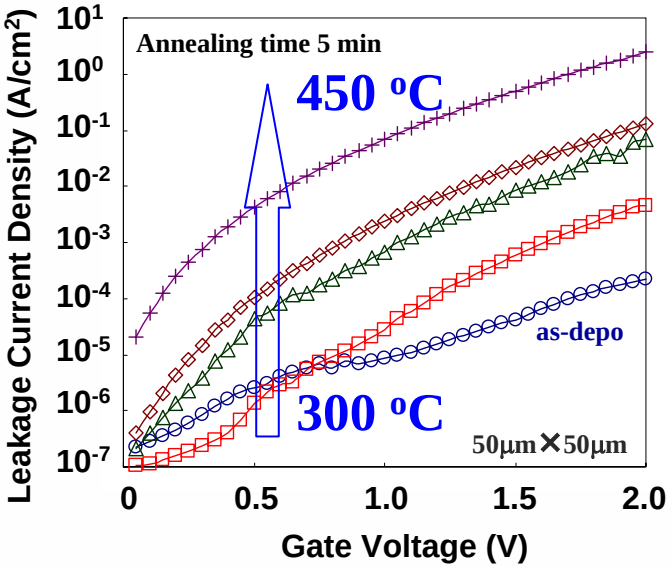
No change more than 5 min.



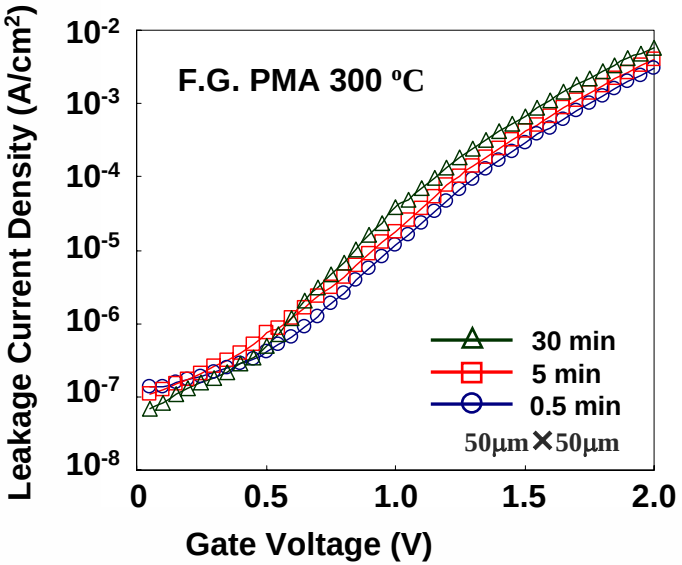
Annealing at 300 °C for 5 min and over reduces the frequency dispersion in accumulation.

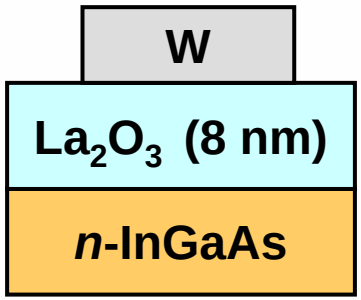
Longer annealing time is preferable for low annealing temperature.

Leakage current



Annealing time effect at 300 °C



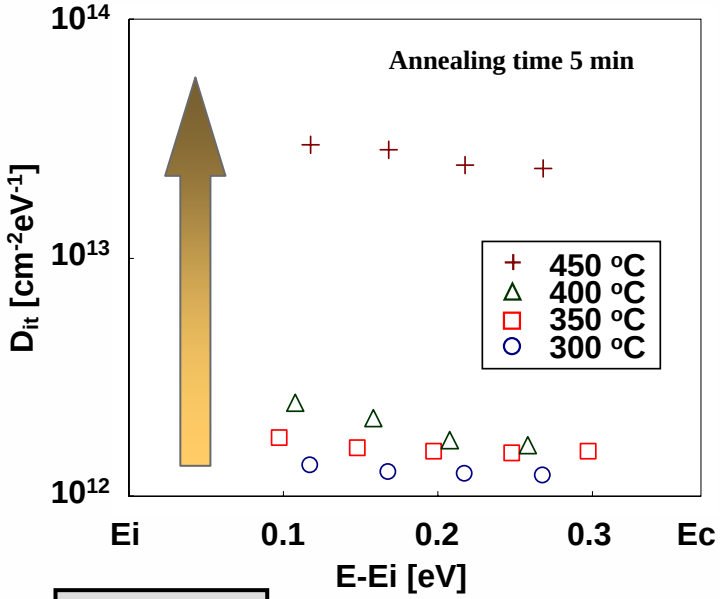


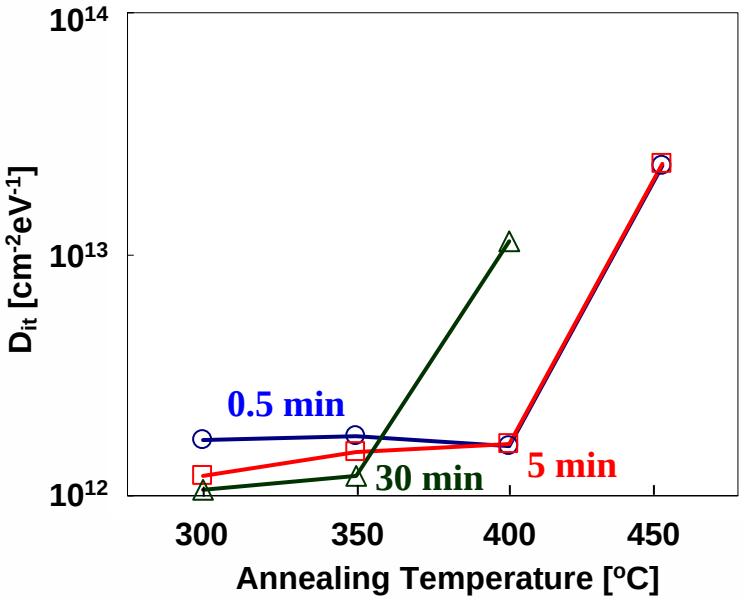
Leakage current at PMA 300 °C is independent from annealing time.

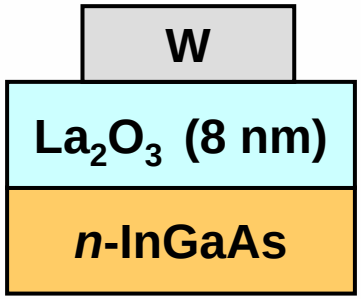
Low annealing temperature suppresses the leakage current.

Interface state densities

Values of D_{it} gradually increase with increasing the annealing temperature.







Low annealing temperature and long annealing time is preferable for reducing the D_{it}.

Summary

We have investigated the annealing effect on the electrical properties of La_2O_3 /InGaAs MOS capacitors upon various annealing temperatures ranging from 300 to 450 ^oC with duration of 0.5, 5, or 30 minutes in F.G ambient.

The process of low annealing temperature and long annealing time is preferable for reduction frequency dispersion and D_{it}, and suppression leakage current.

Acknowledgements

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