# SOI opportunities
## to speed up, save energy and memorize

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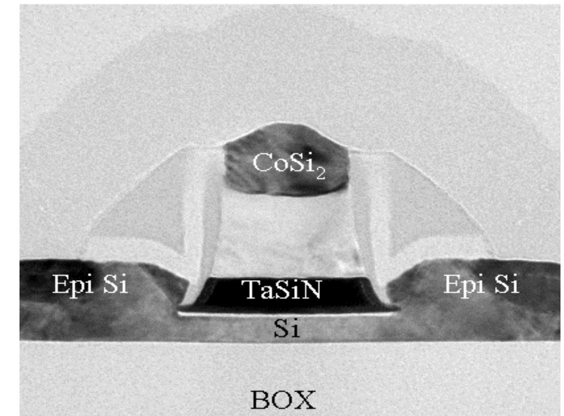
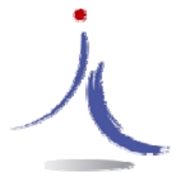
Grenoble SOI Mafia : SOITEC, IMEP, LETI, STMicroelectronics

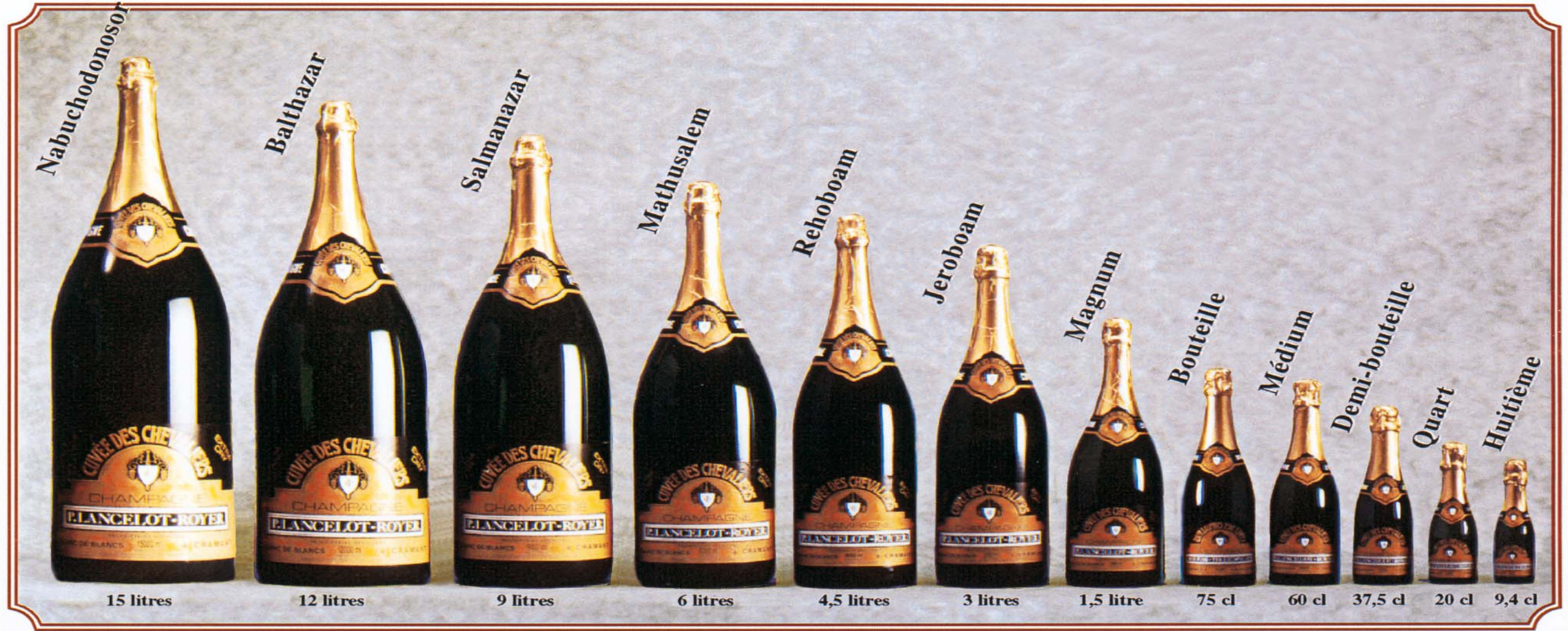
# Outline

- Context: why SOI, what for, how good…?
- SOI technology and advanced boosters
- A few memories: SOI 1T-DRAMs
- Conclusions
  - SOI is HOT: performance & scalability
  - SOI is GREEN: power & voltage saving
  - SOI is versatile: new devices



# CMOS and SOI Evolution

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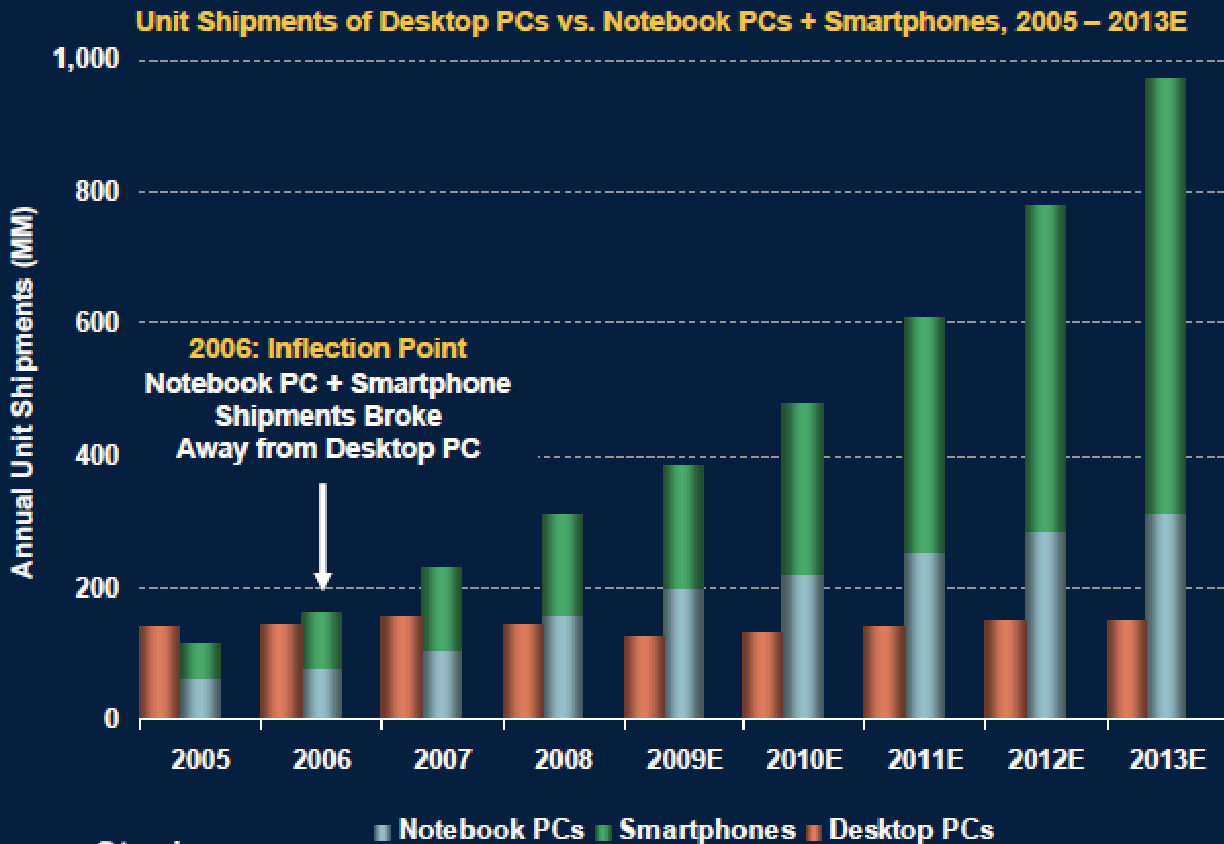
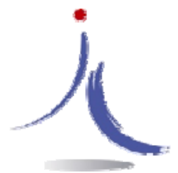
# SOI for Portable Devices




## Market evolution

**Predictions from Morgan Stanley, December 2009**



# Power Inflation

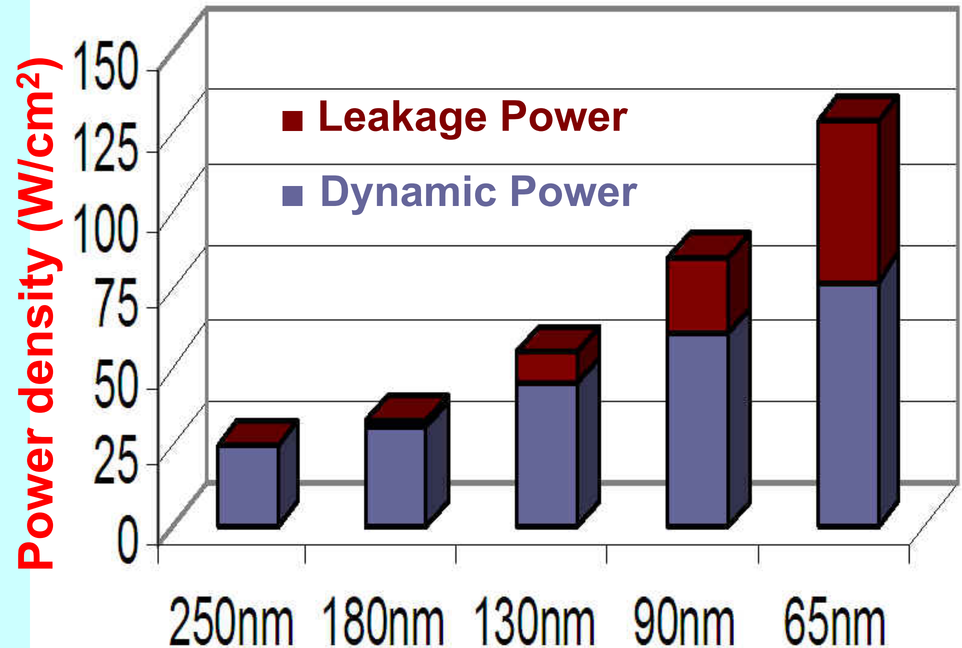
Power consumption tends to increase with scaling:

- The circuit density increases:
  more devices per $mm^2$
- The clock frequency increases:
  more activity per $mm^2$
- The leakage current increases
  in shorter transistors

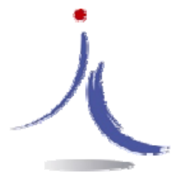
More power means:

- The chip T increases and
  heat has to be evacuated
- Battery lifetime becomes insufficient
- Dramatic increase of energy
  consumption worldwide

Is Google going to build a nuclear plant?




SOI can help !



# SOI key value

☺ Power

- Lower $V_{min}$
- Reduced variability
- SRAM stability & FOM = +35%
  (Bulk SRAM falls apart due to RDF)
- Lower leakage

☺ Scaling

- Difficult for Bulk at 20 nm
- OK via FD CMOS

☺ Speed

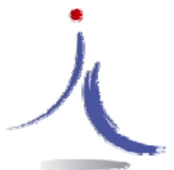
**SOI MOSFETs**

Excellent subthreshold swing
(< 80 mV/decade)

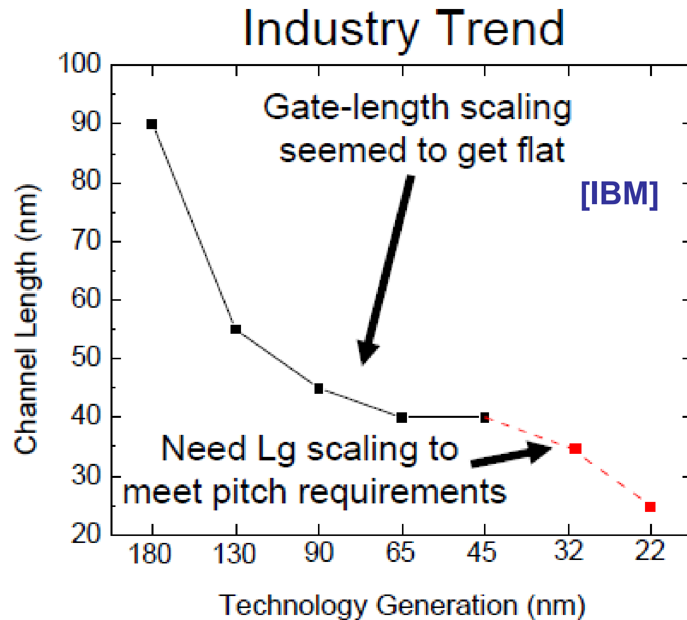
Superior short-channel control
(DIBL < 100 mV/V)

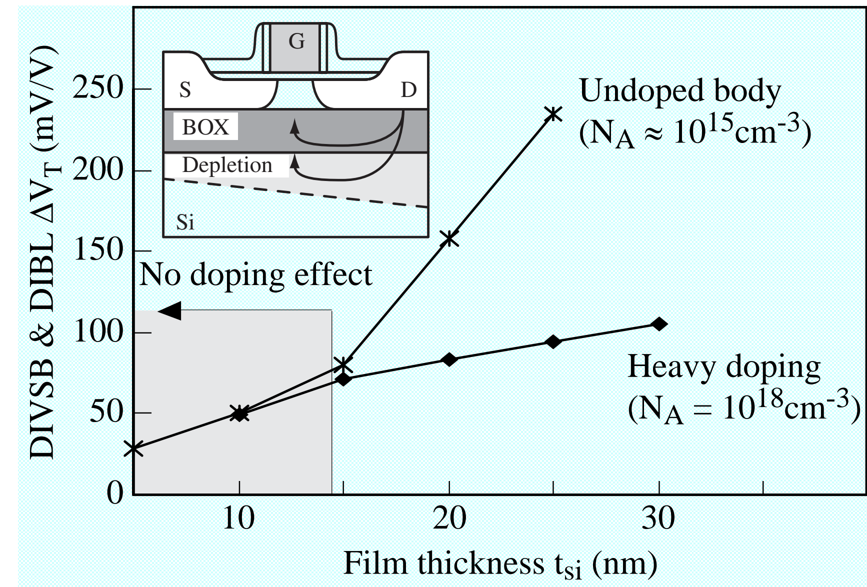
Low $I_{off}$ and GIDL
Difficult for Bulk to meet specs at LP 20 nm without increasing junction leakage and GIDL

Ultrathin FD SOI
has demonstrated excellent SCE
and performance at L < 25 nm



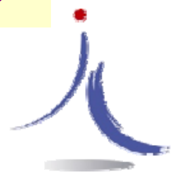
# HOT SOI: Scaling



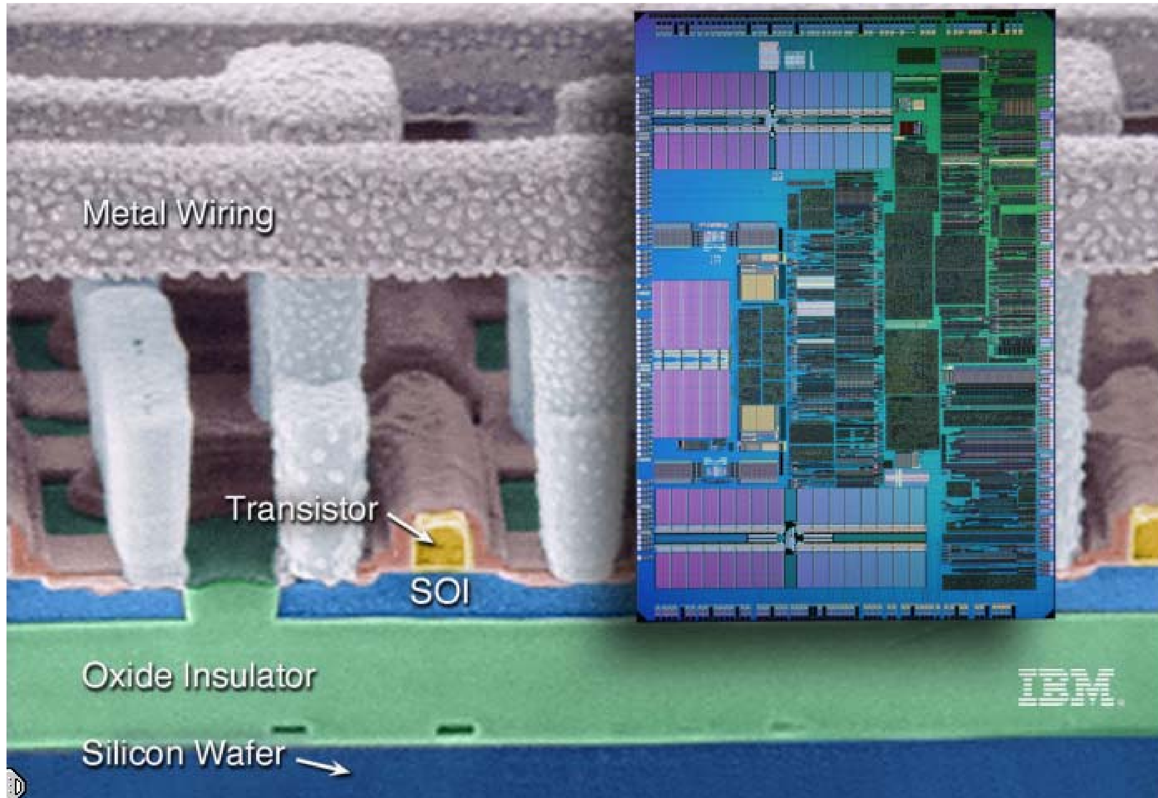

**Bulk: Doping based**
- Huge doping level
- Issues:
  variability, mobility, BTBT

**SOI: Thickness based**
- No doping effect
- Thin Si film: $T_{si} \approx L/4$
- Thin BOX & Ground-plane



# HOT SOI: Performance

## Top 10 super-computers: 9 are SOI-based!

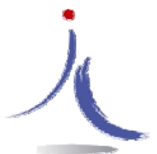



**SOI Products:**

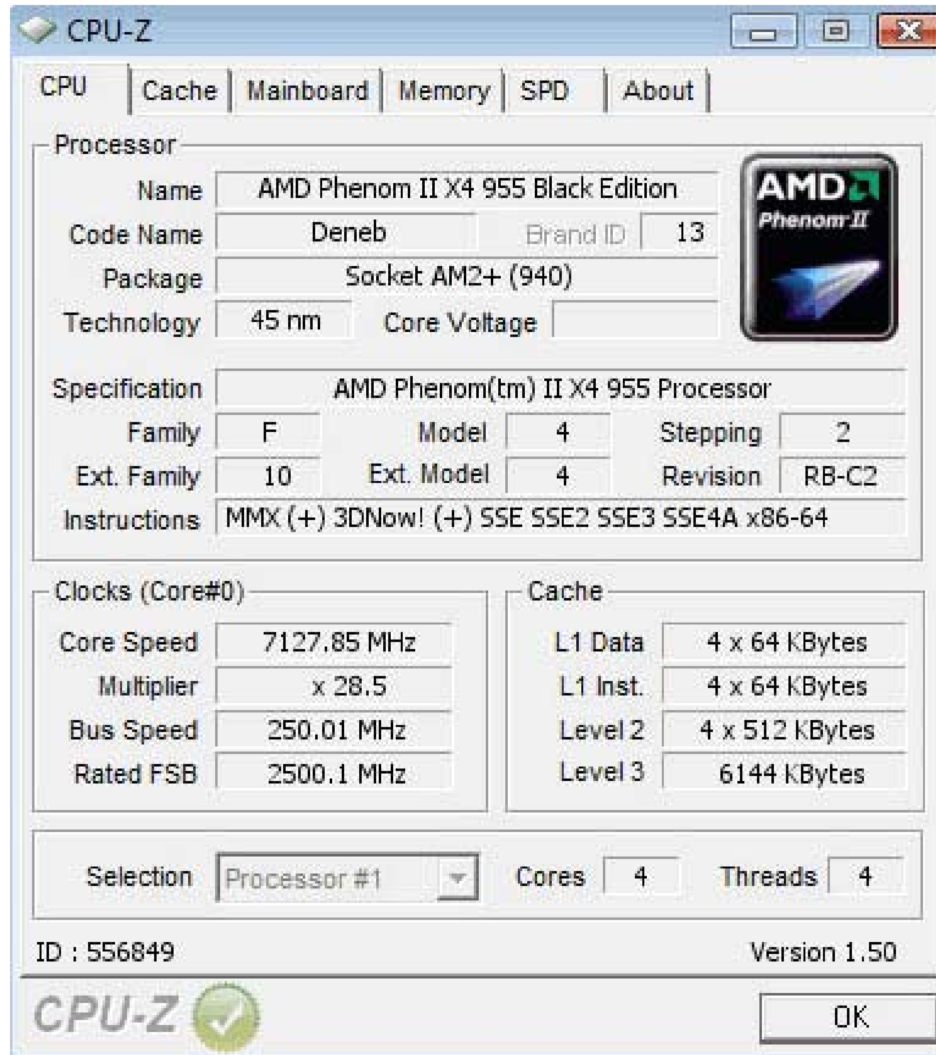
µprocessors

(AMD, IBM, Sony, ARM, …)

+ ultralow power (watches)
+ medium/high voltage & HT
(lightening & car electronics)
+ RF devices
+ imagers
+ MEMS & sensors

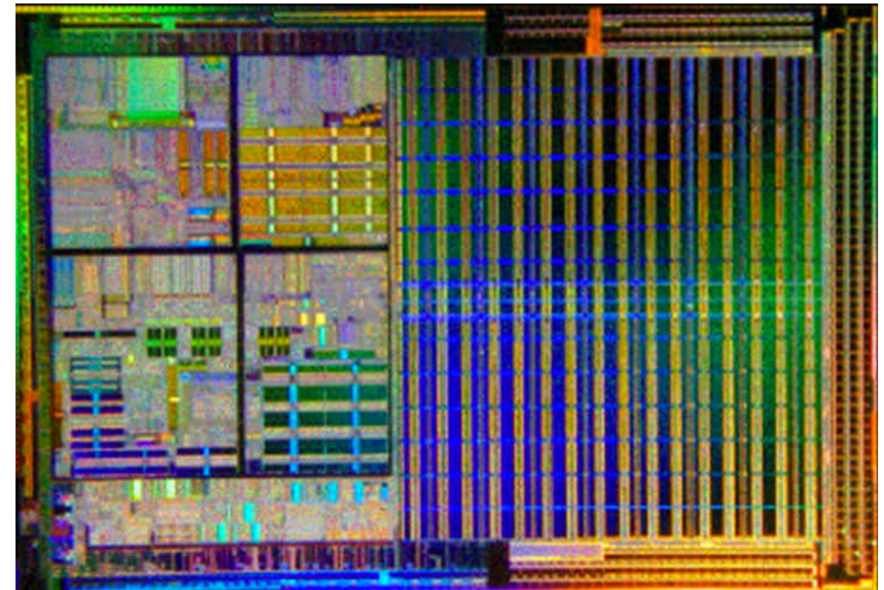


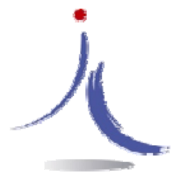
# HOT SOI: Performance




**News on 5/05/2009:**

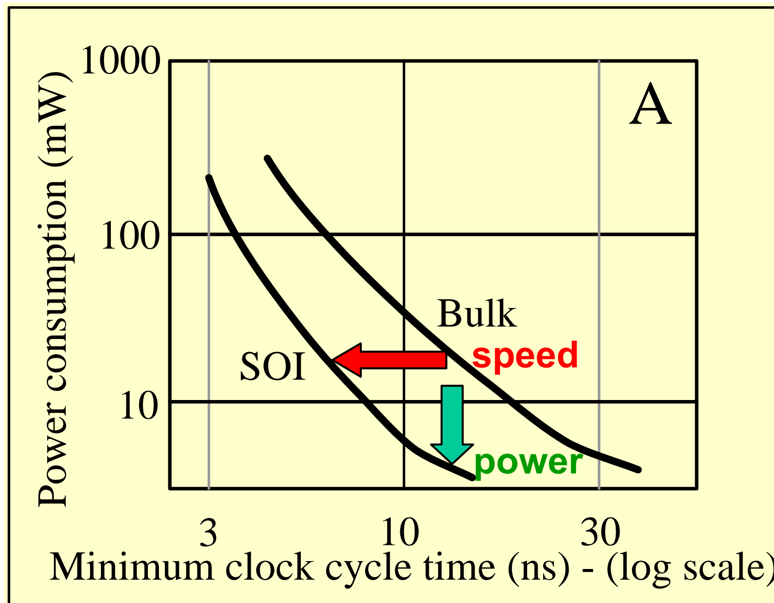
***AMD smashes the 7.1 GHz barrier with SOI Phenom 2 !***

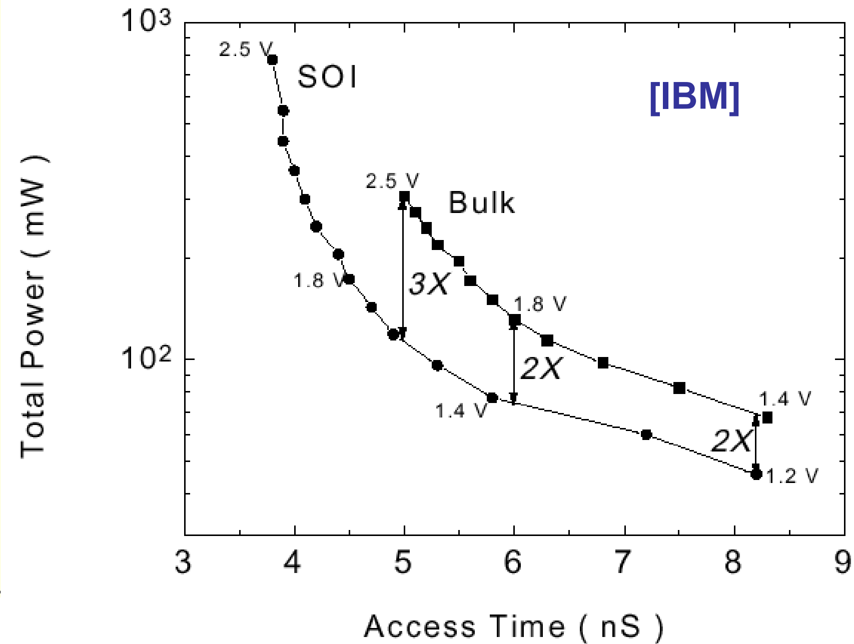




http://brightsideofnews.com/news/2009/5/5/amd-smashes-the-71-ghz-barrier-with-phenom-ii-955-cpu!.aspx

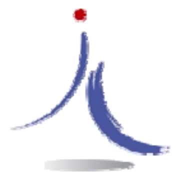
# GREEN SOI: Power Saving




[Colinge'05]

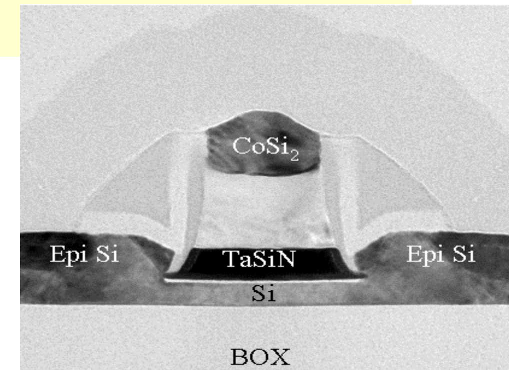
**Repeatedly demonstrated performance gain**



# Sake-winning bet for beyond *'Beyond-CMOS'*

***In 2035, our computers will still contain lots of MOSFETs with***

- Traditional Chinese medication = silicon
- Generic pills = Si surrogates (Ge, GaN, …)




## What can we do to embellish MOSFETs ?

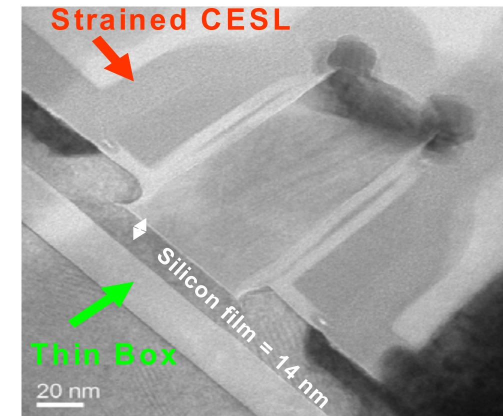
**- Enhance electrostatic control**

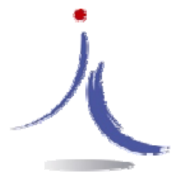
**For ultimate scaling: FD SOI**

- Ultrathin film
- No doping
- Thin BOX
- Ground Plane
- Multiple gates

**- Improve transport properties:**

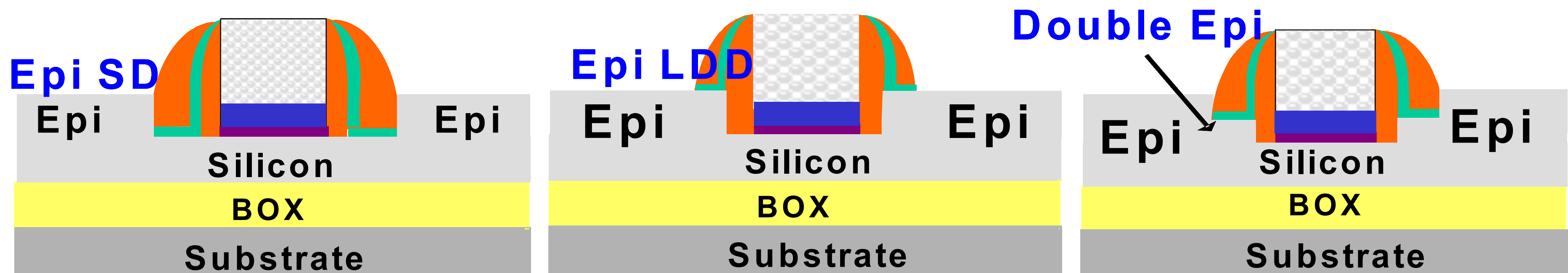
- Ad-hoc boosters: $R_{SD}$, strain, high-K, metal gate



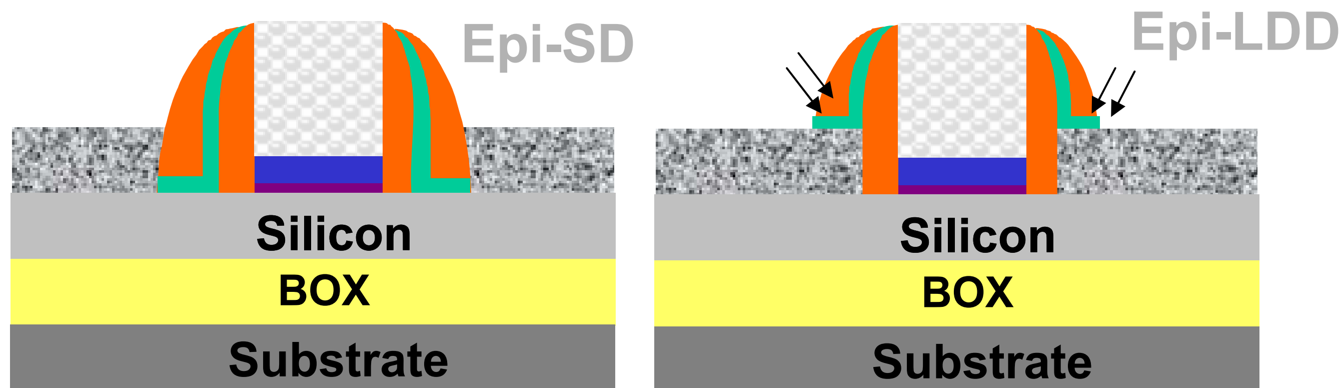



# Booster 1: Low Series Resistance

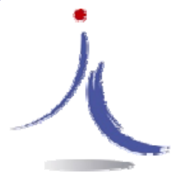
- Junction engineering via Selective Epitaxial Regrowth
  - several options for raised terminals




- Source-drain Ni silicidation



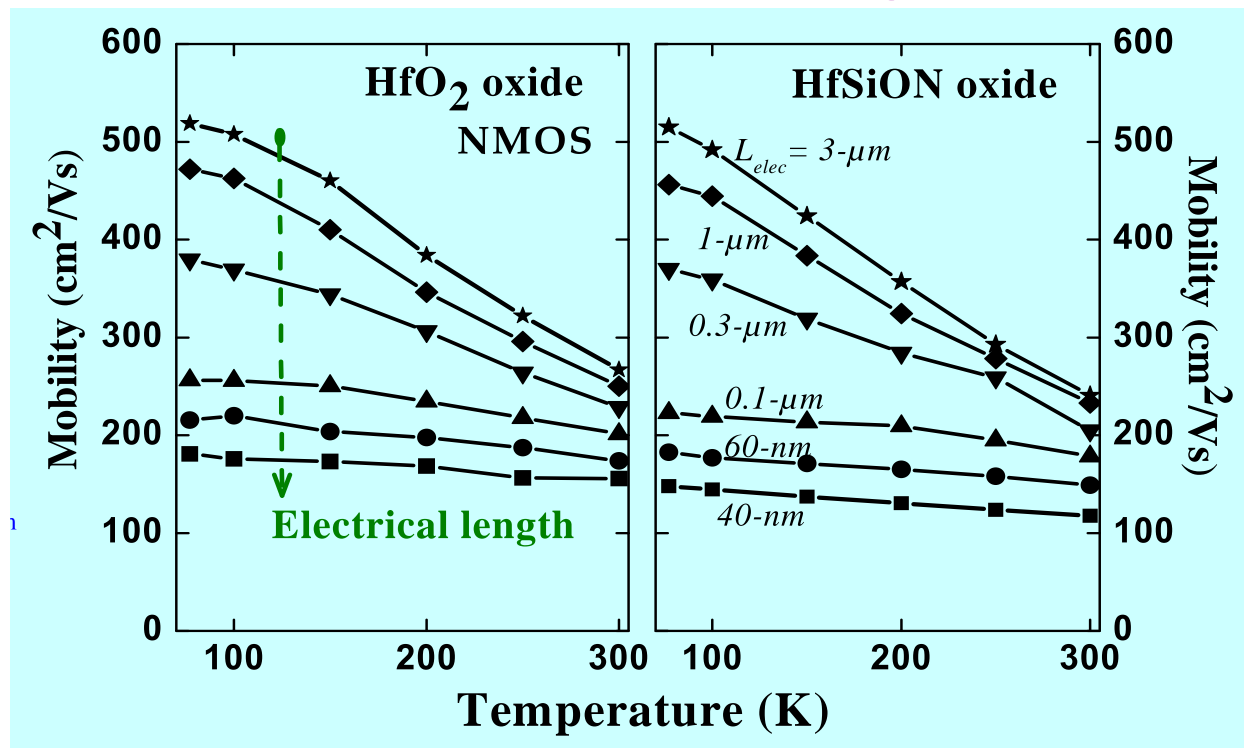

Greatly improved $R_{SD}$



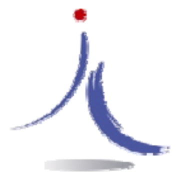
# Booster 2: High K Dielectrics

- Similar mobility behavior for $HfO_2$ and HfSiON
- Long channels: acoustic phonon scattering prevails ($\mu \sim T^{-0.7}$)
- Short channels: degraded mobility & attenuated T dependence

Additional scattering mechanisms?



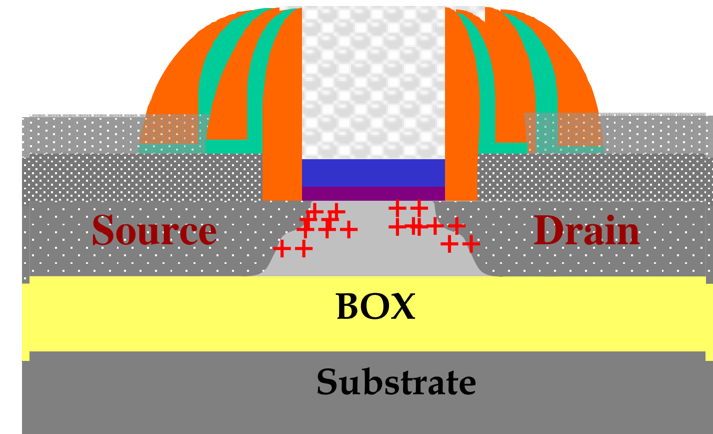

8 nm thick
FD SOI MOSFET

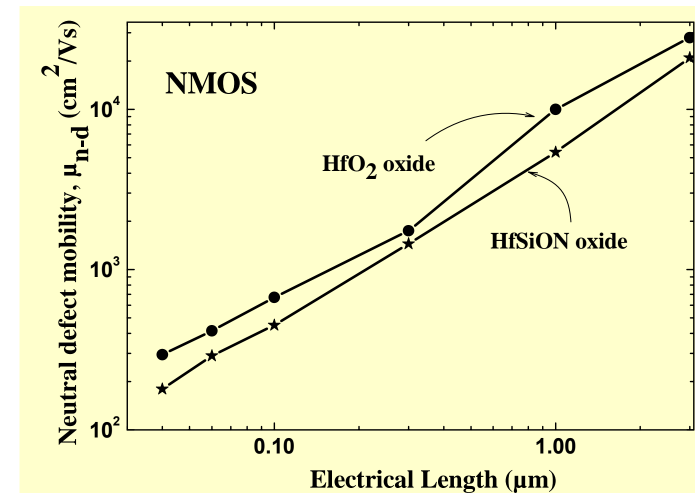


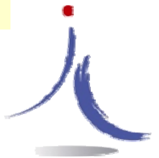
# Additional Scattering Mechanisms

- Short L : saturated μ(T) variation
  → presence of defects
- Neutral defects are induced, at the channel extremities, by S/D implantation and gate formation
- More important contribution of neutral defects in short-channel

$$\frac{1}{\mu_{measured}} = \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{Coulomb}} + \frac{1}{\mu_{defect}}$$



# In-Situ Comparison of High-K vs $SiO_2$

Two channels can be activated at the front and back interfaces

In-situ comparison:
Si-$SiO_2$ vs. Si-high K

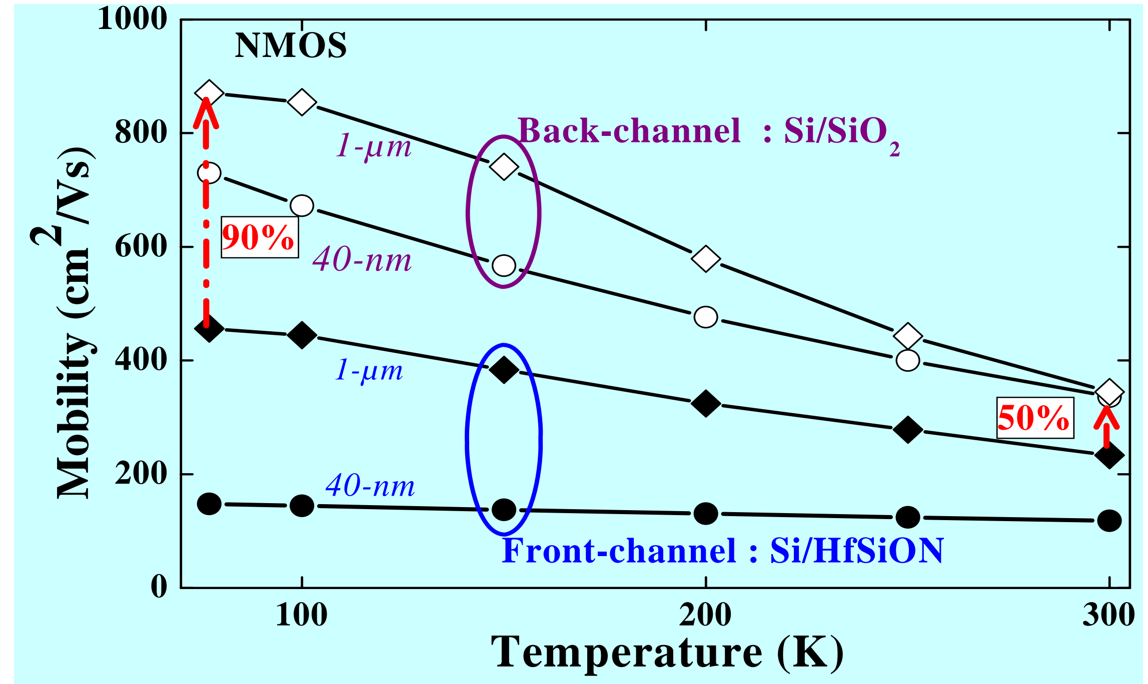
Back interface transport:
high mobility
phonon scattering
low impact of neutral defects

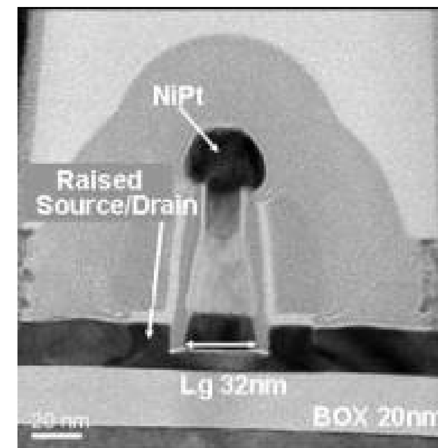
Mobility degradation in top channel :

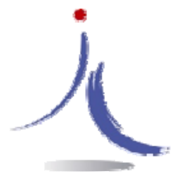
$$1/\mu_{HK} = 1/\mu_{SiO2} + 1/\mu_{ADD}$$

Remote Coulomb scattering

[Vandooren et al'02, Pham-Nguyen'08]



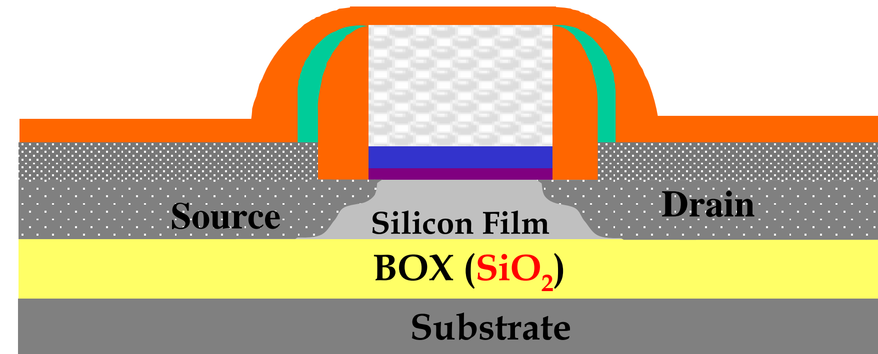



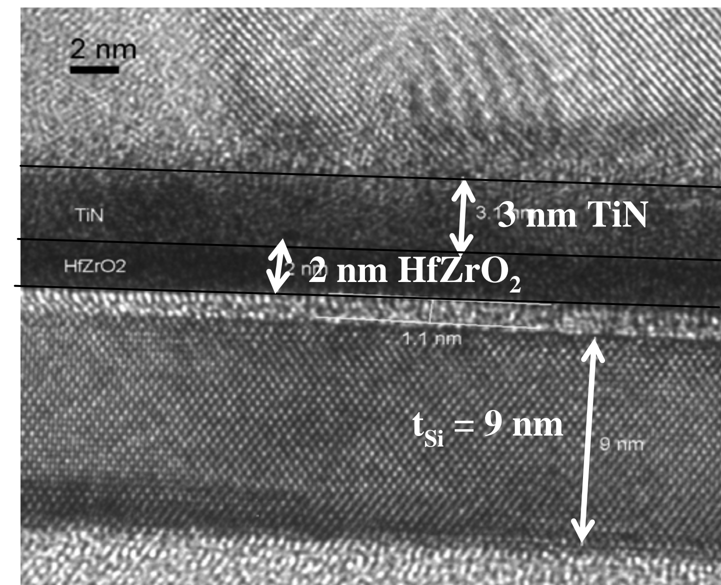
# Booster 3: Metal Gate

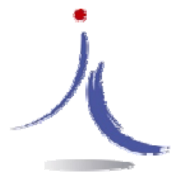
- TiN vs TaN
- ALD vs PVD deposition
- Gate thickness from 3 to 10 nm

**Benefits**

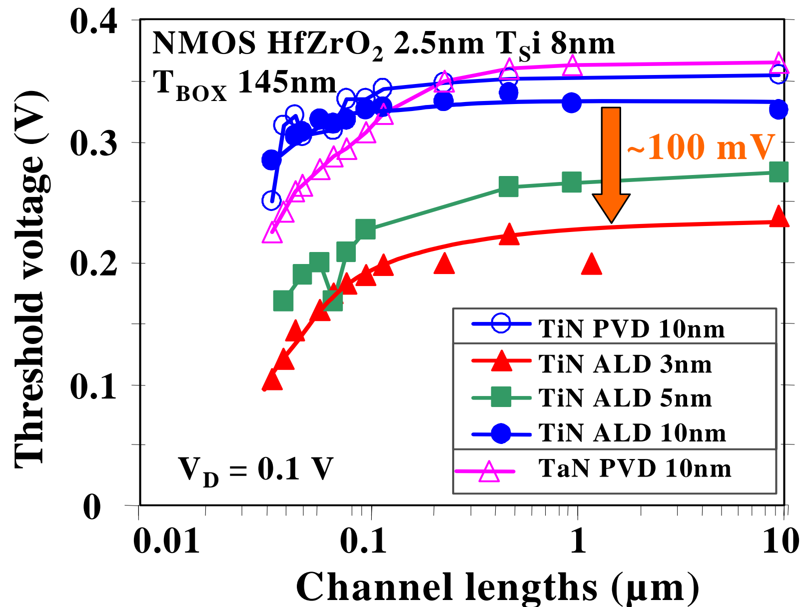
- No poly depletion
- $V_T$ tunning

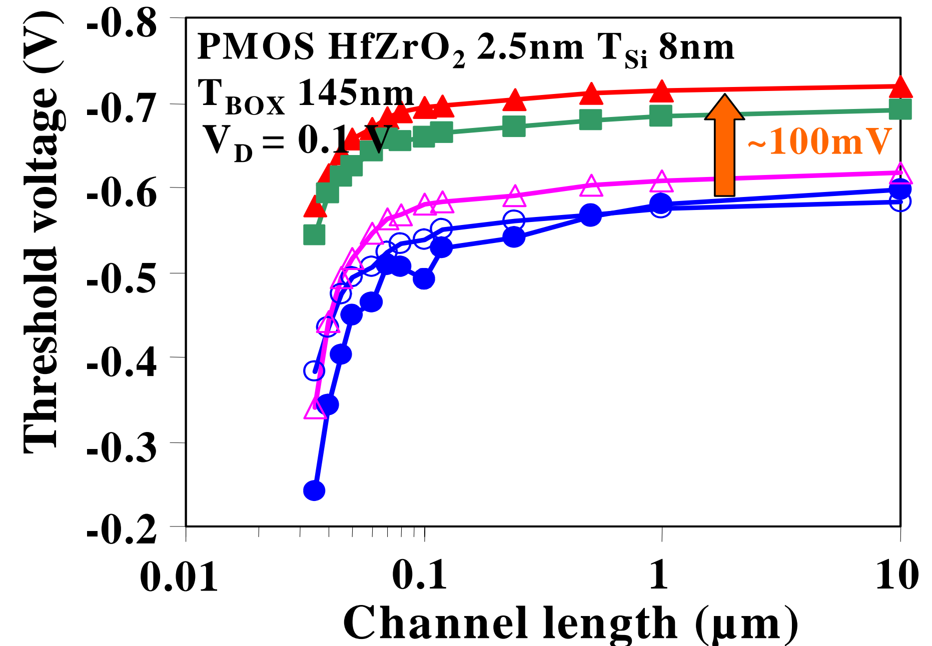


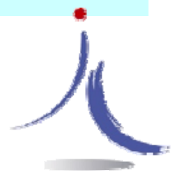



# Threshold voltage modulation



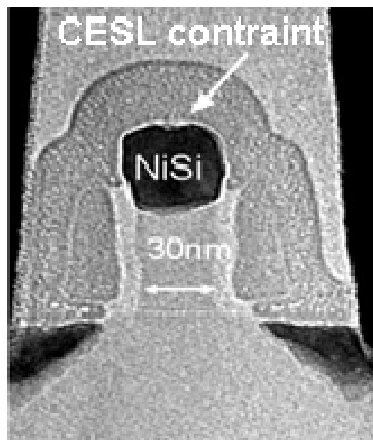

- $V_T$ tuning : 100 mV shift by decreasing TiN thickness from 10 nm to 3 nm
- Similar shift for NMOS and PMOS
- No significant impact of deposition techniques (ALD or PVD) or metal materials (TiN or TaN)

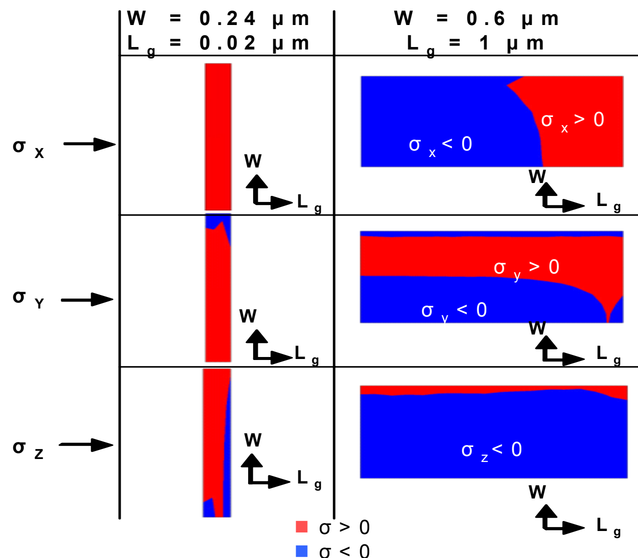


# Booster 4: Strain in SOI

1 – Biaxial strain at wafer level
2 – Process-induced uniaxial strain:

- Isolation techniques (STI, SiGe, …) – compressive or tensile
- Source-Drain engineering – SiGe for PMOS and SiC for NMOS
- Stress Memorization Transfer (SMT) from gate and/or capping layer
- Contact Etch Stop Layer (CESL) – compressive (for holes) or tensile (electrons)

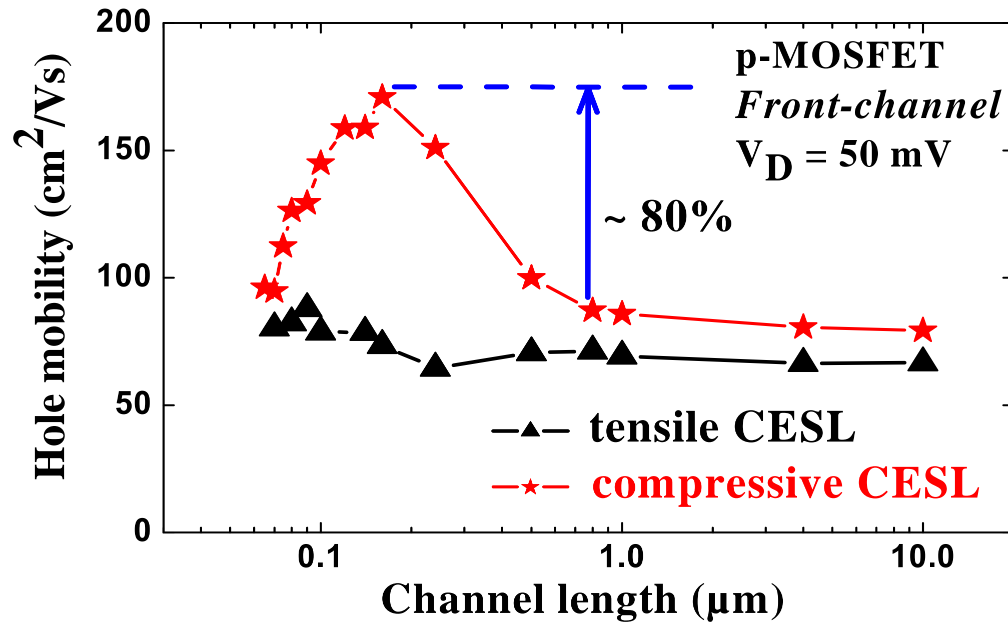


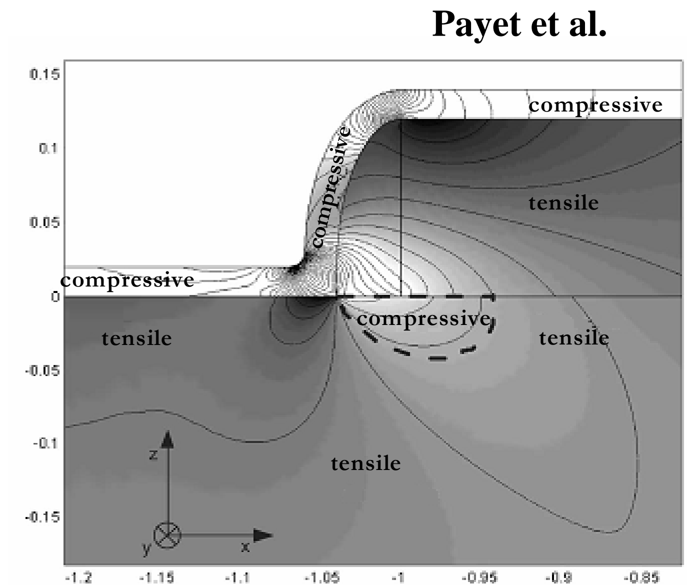




- Regions with compressive or tensile strain can coexist in the body of one SOI MOSFET. This effect disappears for small L.
- Different effects according to CESL location:
  - on top of the gate
  - on gate edges
  - on spacers
  - on extensions

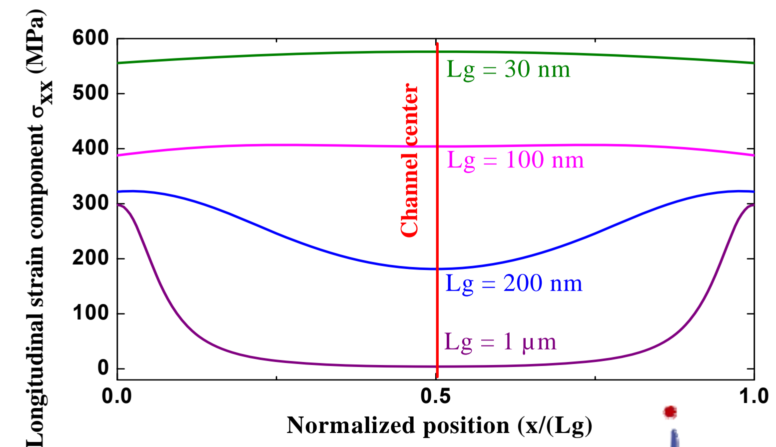
[Gallon'07]

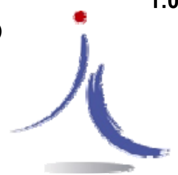
# Hole mobility: compressive CESL




- No hole mobility enhancement in t-CESL
- Strong gain in c-CESL with selected lengths
  - L ≈ 100 nm : $\mu_{max}$ = 180 cm²/Vs (+80% !!)
  - Stress pocket effect
  - Very short channels: Mobility gain is competed by other mechanisms

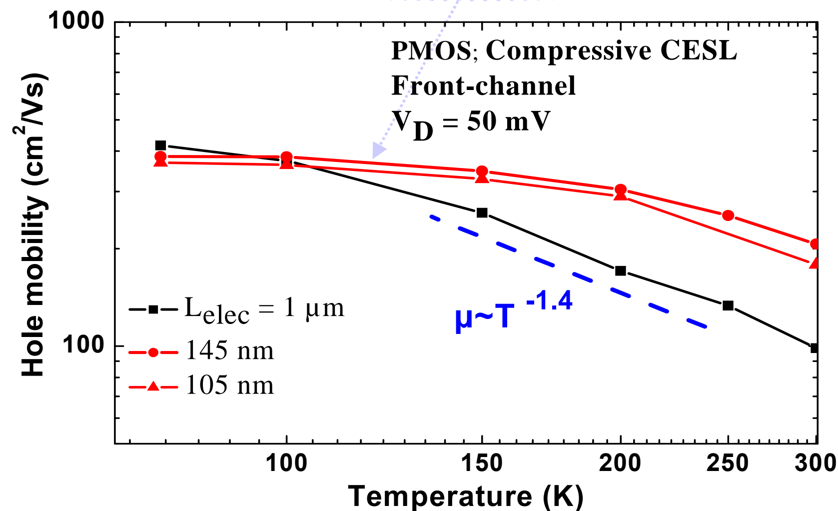


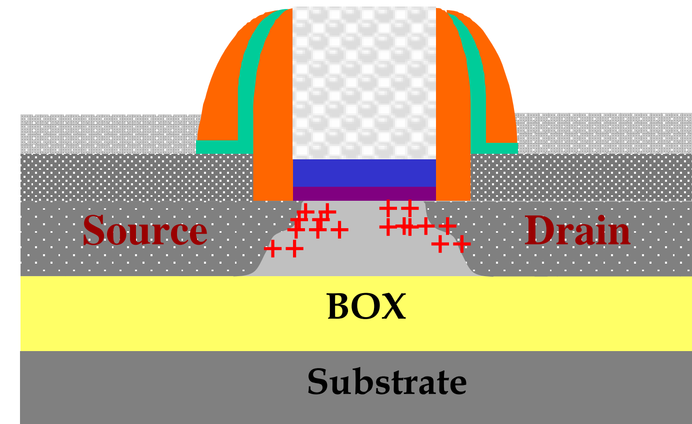



# Competing mechanisms

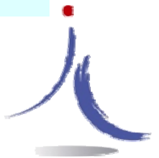
- Neutral defects, strain and source/drain scattering are inhomogeneous along the channel
- Competing effects

Saturated μ variation → presence of defects




- Neutral defects and strain are located at the channel extremities
- More effective contributions of neutral defects and strain in short-channel



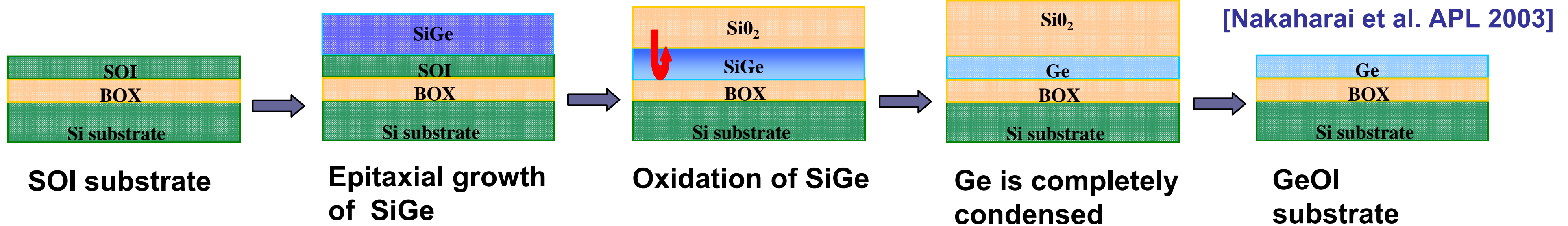
# Booster 5: Advanced Materials (Film)

**Germanium** for higher mobility

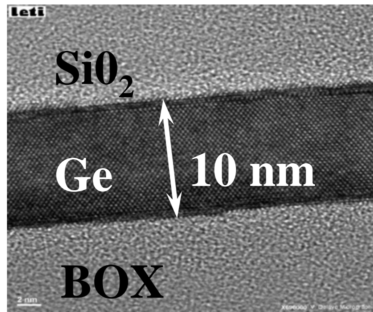
GeOI by Smart Cut or Condensation

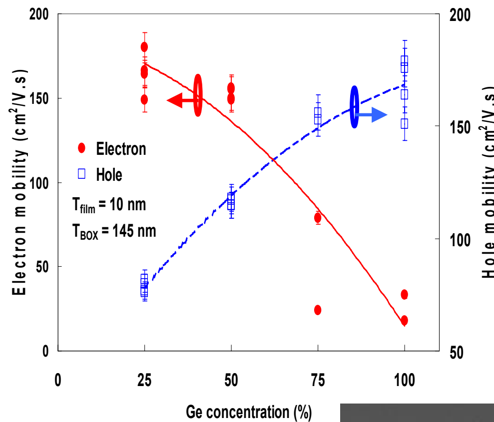
**GaN** for power, RF, photonics

[Nakaharai et al. APL 2003]

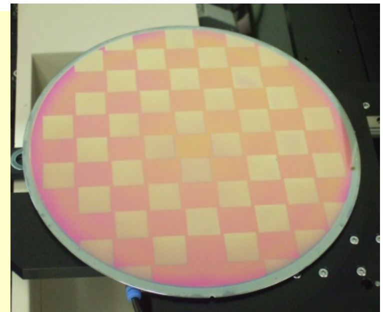


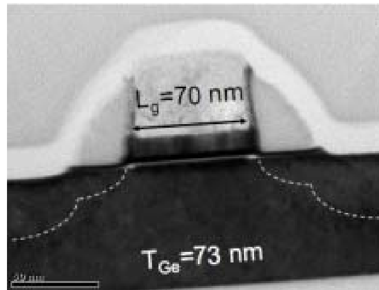

SOI substrate | Epitaxial growth of SiGe | Oxidation of SiGe | Ge is completely condensed | GeOI substrate



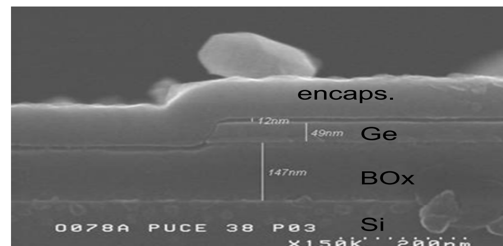



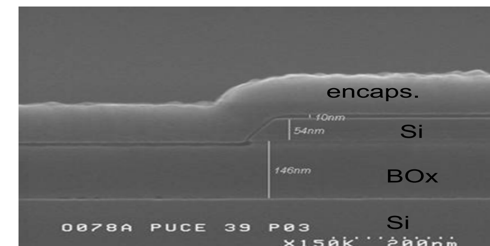

- **Excellent hole mobility**
  400 $cm^2/Vs$
  750 in strained GeOI
- **Poor electron mobility**
- **Solution: co-integration**
  p-MOS on GeOI and n-MOS on SOI

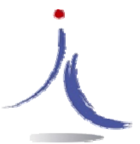





[Nguyen, 2007]
[Le Royer, 2009]



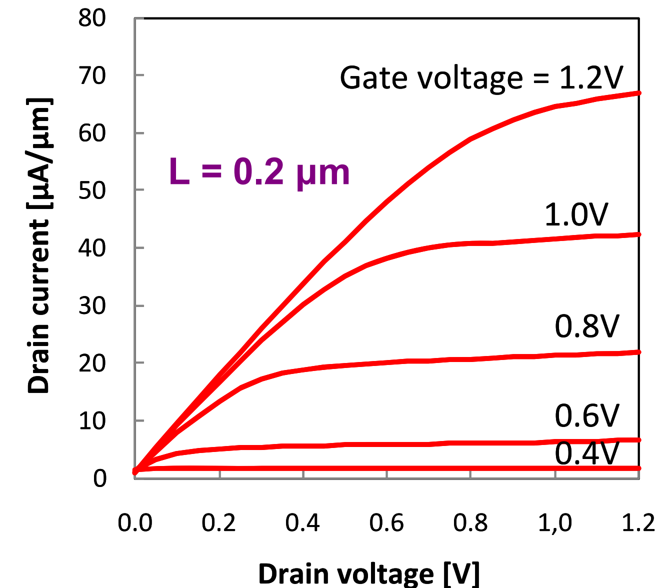
# Booster 5: Advanced Materials (BOX)

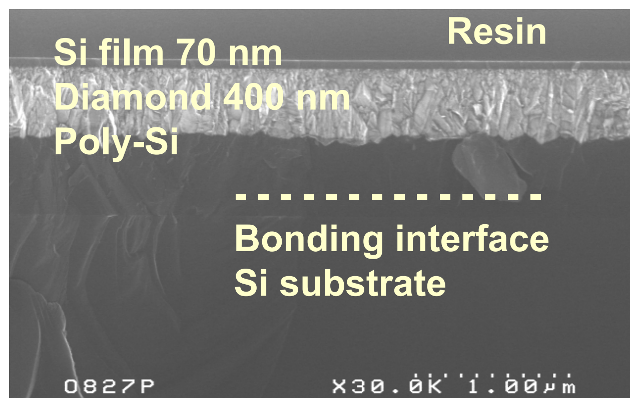
## Functionalize the BOX

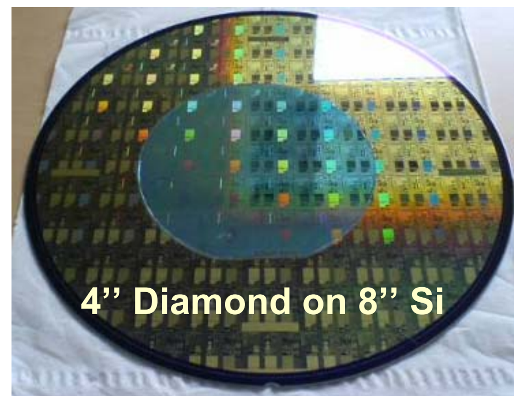
- generate strain: $Si_3N_4$
- store charges (EEPROM): ONO
- optical applications: glass, quartz
- RF devices: $Al_2O_3$

## Eliminate heat:

- reduce self-heating: diamond, alumina, AlN



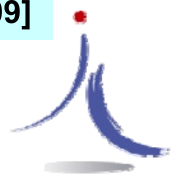




## SOD MOSFET

- Good characteristics
- No mobility degradation
- No self-heating
- Much lower thermal R

[Mazellier et al, 2009]

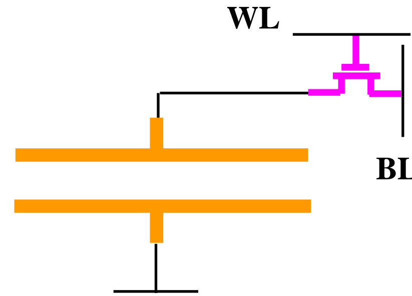


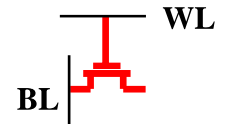
# From DRAM to 1T-DRAM

## DRAM (1C + 1T)

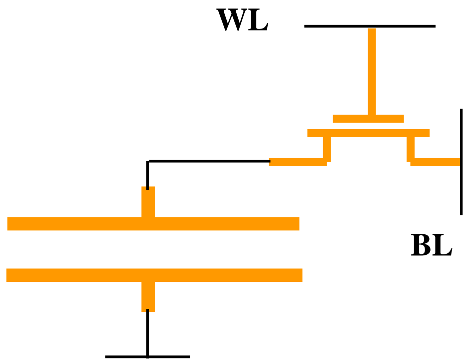
Scalable transistor

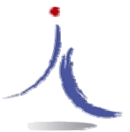
Unscalable capacitor



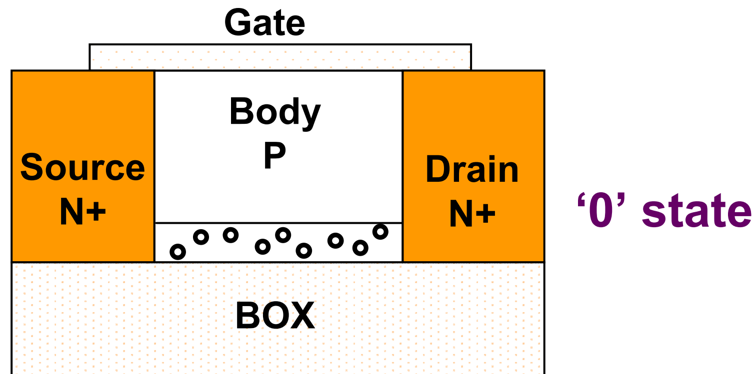
1T-DRAM





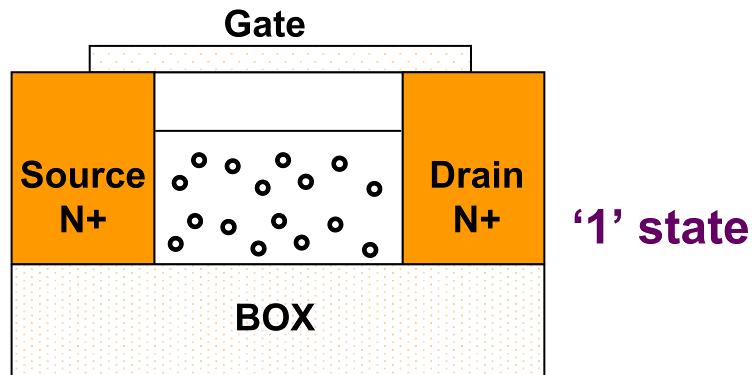
# SOI 1T-DRAM Basics

## PD SOI MOSFET structure




'0' state

Lack of holes : $V_{TH1}$ ↗ : $I_D$ ↘



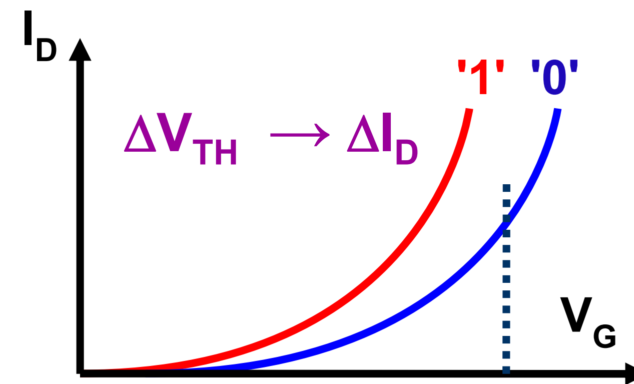

'1' state

Excess of holes : $V_{TH1}$ ↘ : $I_D$ ↗

## Z-RAM: Zero-capacitor RAM

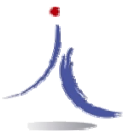
Takes advantage of floating body effect

Okhonin S. et al., EDL '02



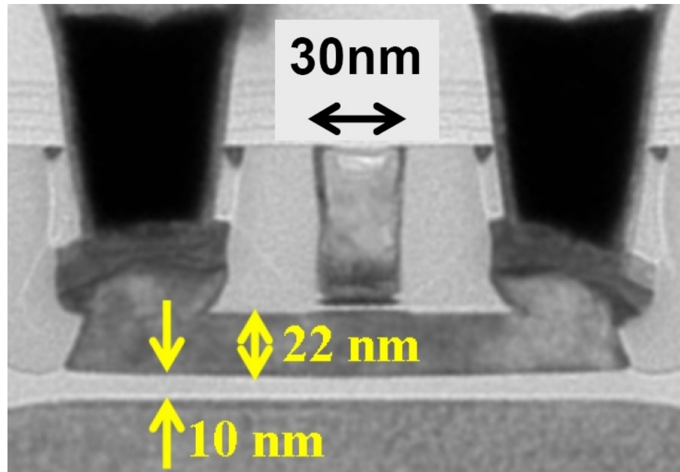

**Advantages:**

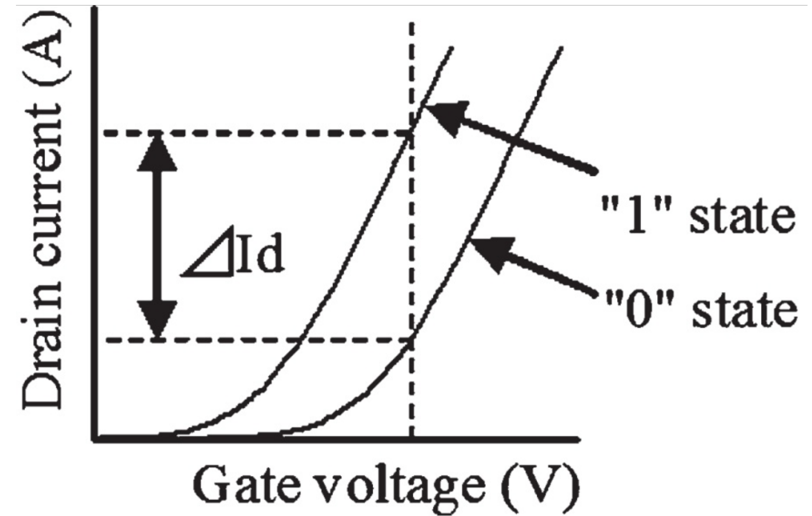
- no capacitor
- smaller surface: easy scaling
- low power
- high speed

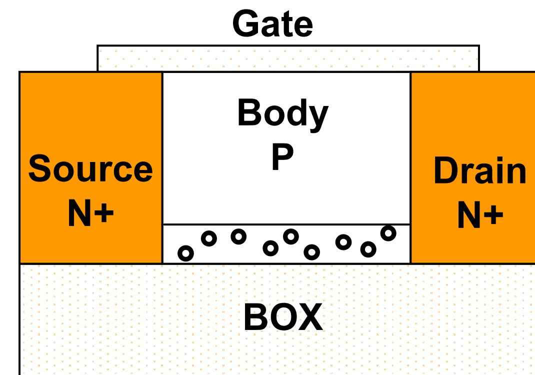


# Example of FD SOI 1T-DRAM

## Intel



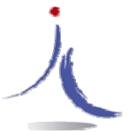




- Prog. Methods: I.I. and FB1
- 45nm, stand alone cell
- LDD and high k dielectric, low doped channel
- $T_{BOX}$= 10nm ($V_{G2}$=-2V), $T_{SI}$= 22nm
- $\Delta V_{TH}$ = 400 mV and $T_R$= 25 ms at 85°C

$V_{G2} < V_{FB2} < 0$

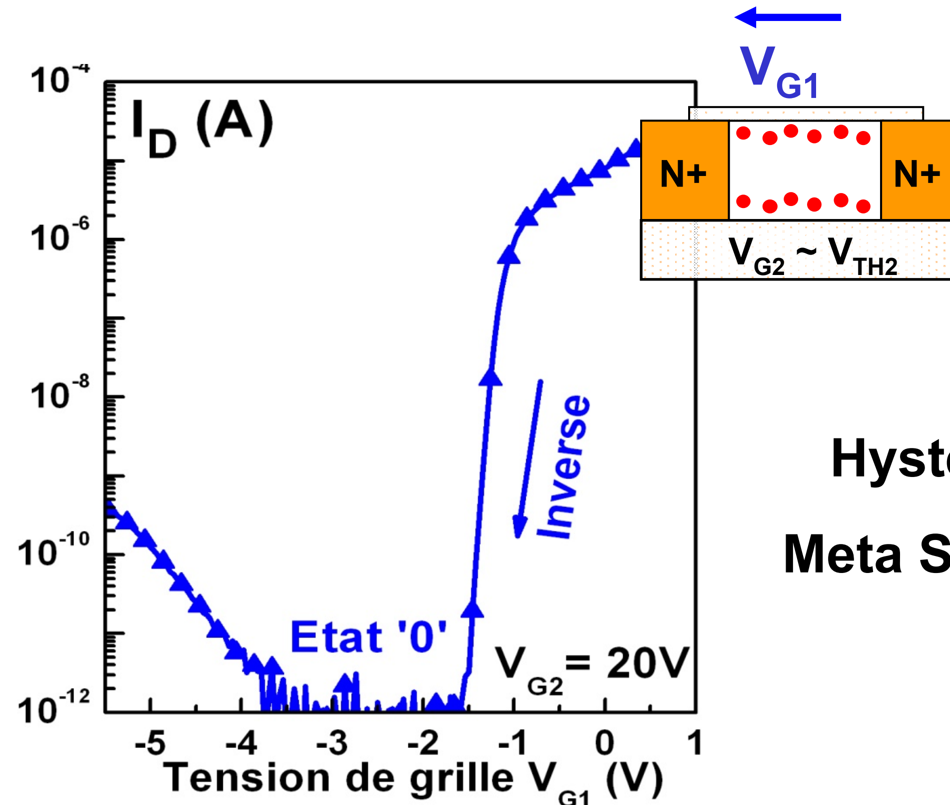
To attract holes



# ‘New’ FBE: Meta-Stable Dip (MSD)

## Dynamic coupling and drain current hysteresis

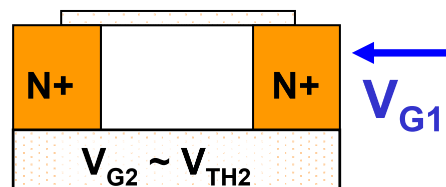
- electron
- hole




Hysteresis = Memory effect

Meta Stable Dip (MSD)= DRAM

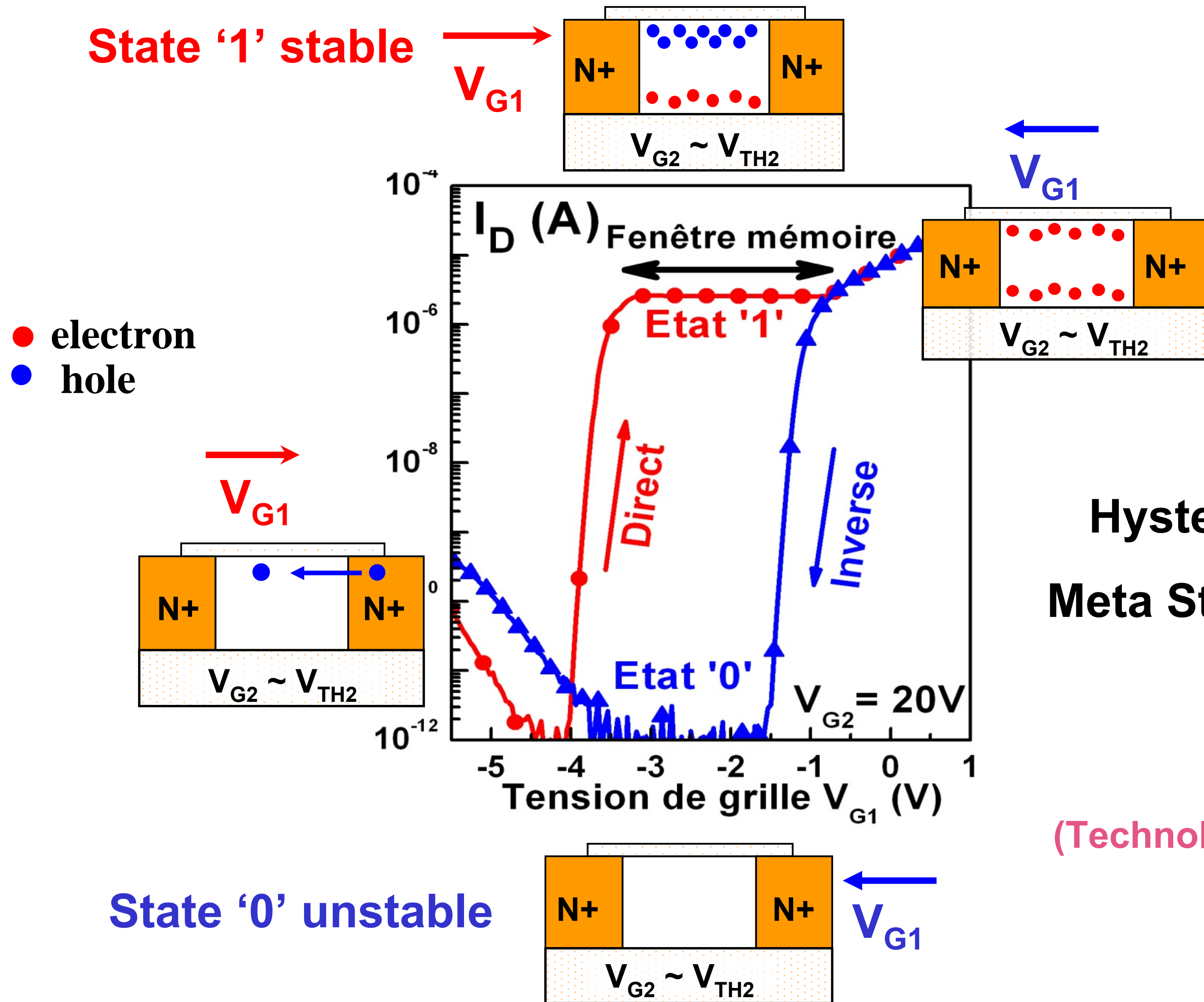
State ‘0’ unstable




*" M. Bawedin et al. SSE 2006, EDL 2008 "*

# ‘New’ FBE: Meta-Stable Dip (MSD)

## Dynamic coupling and drain current hysteresis




**Hysteresis = Memory effect**

**Meta Stable Dip (MSD)= DRAM**

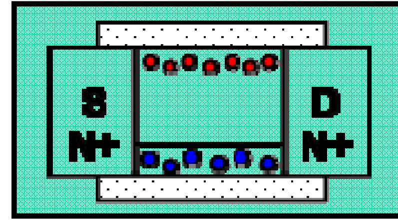
(Technology transfert in progress)

*" M. Bawedin et al. SSE 2006, EDL 2008 "*

# MSDRAM: Double-Gate MOSFET

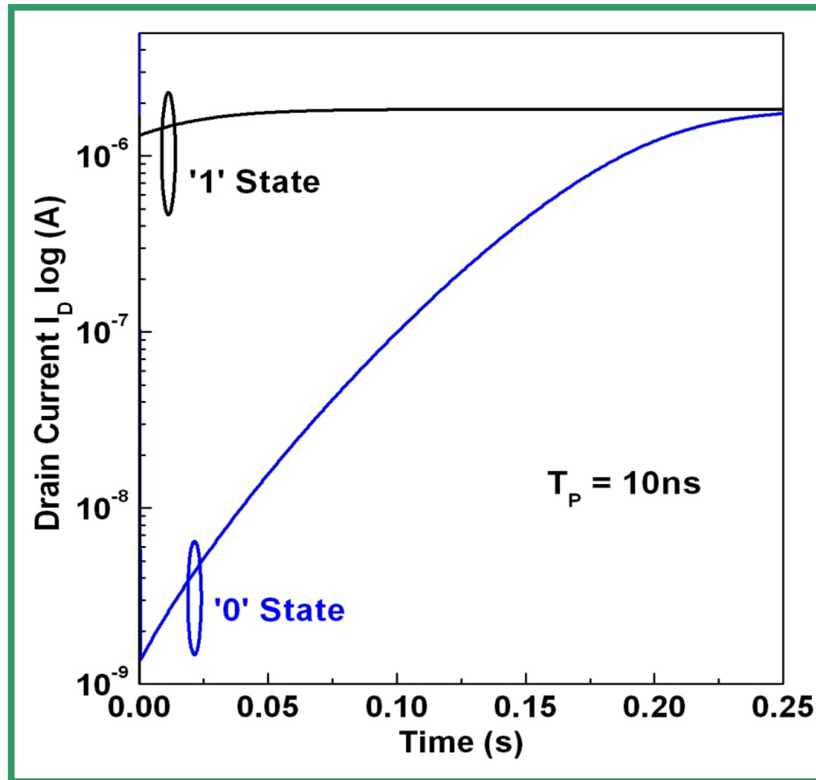
**Non Optimized:**

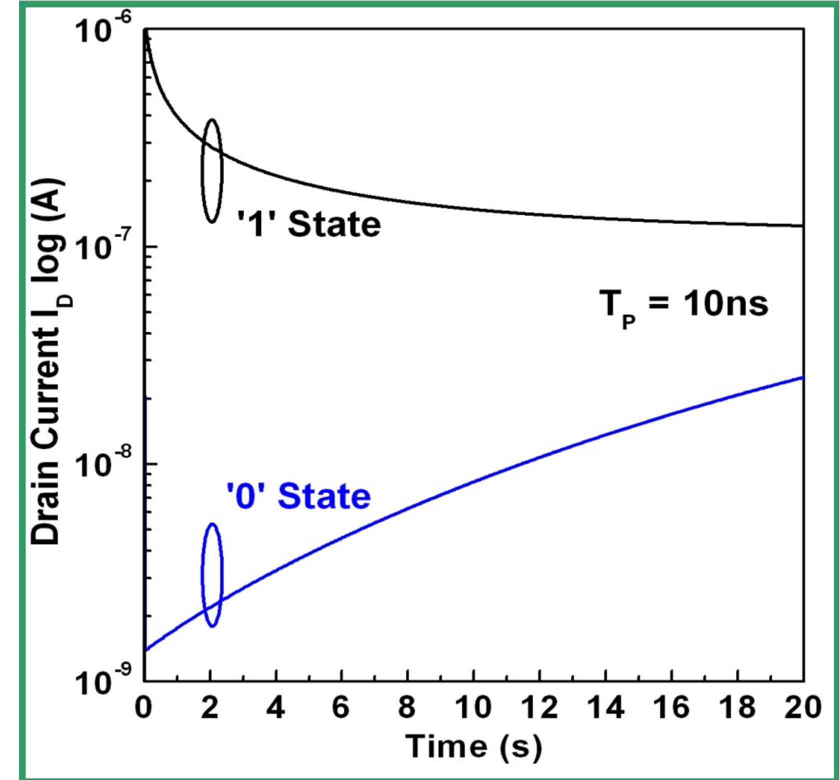
$I_1/I_0=10 \Rightarrow T_R \cong 100ms$



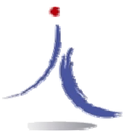

**Optimized S/D:**

$I_1/I_0=10 \Rightarrow T_R \cong 20s$

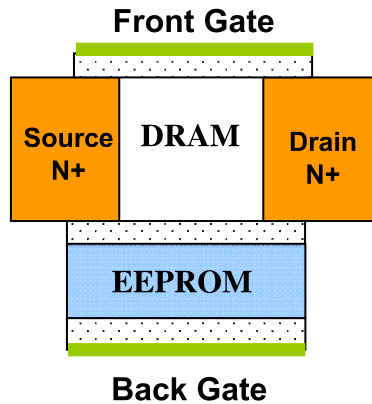


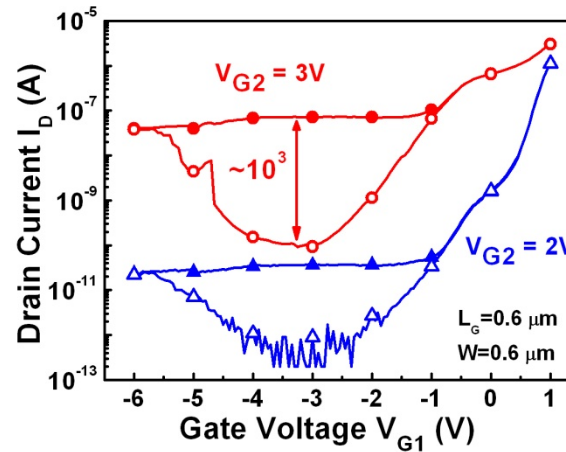

[Bawedin et al, patent 2009]



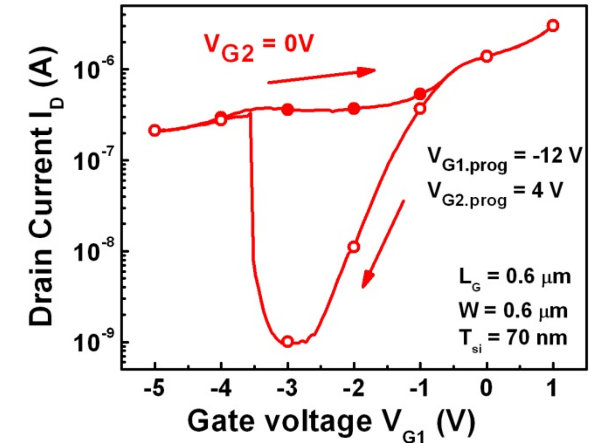
# MSDRAM: Nonvolatile Function




## Double-gate mode




## Single-gate mode

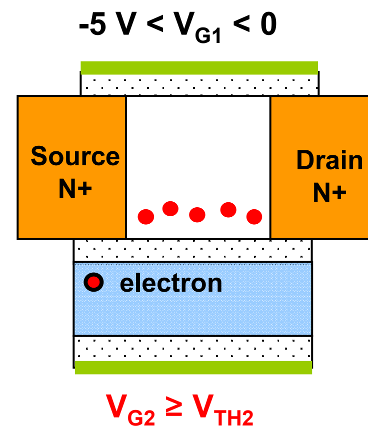


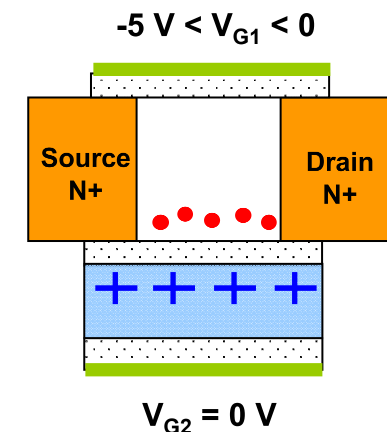

**ONO as BOX:**

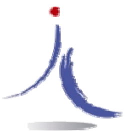
**1 - To store holes**
**Replacement of back gate**

**2 - To store electrons**
**Unified memory:**
**combined MSDRAM + EEPROM**

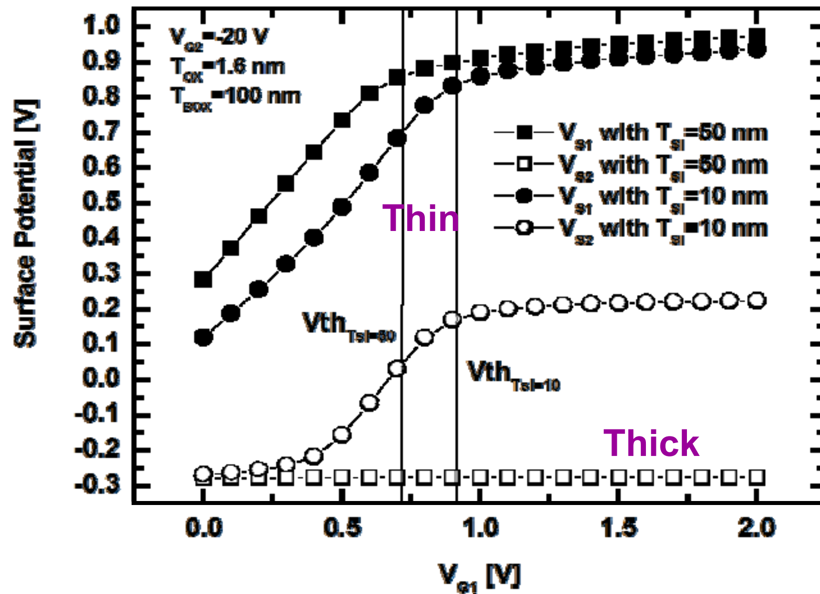
[Park, Bawedin et al, 2010]

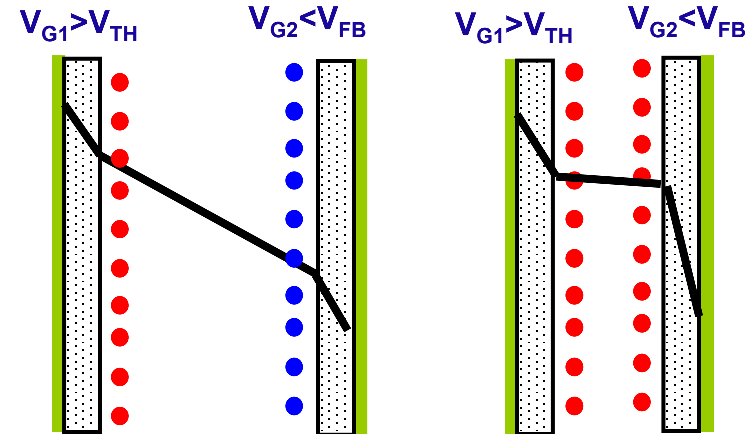


# Super-Coupling in Ultra-Thin MOSFETs

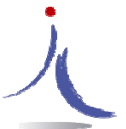


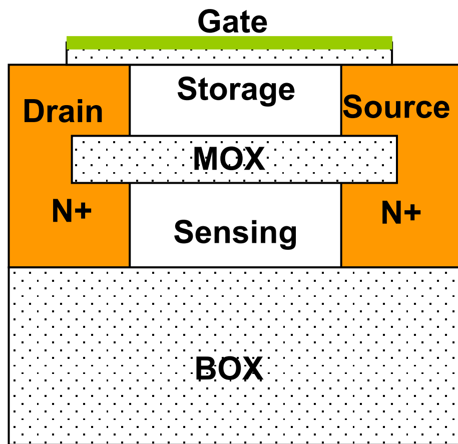

**In MOSFETs with sub-critical thickness :**

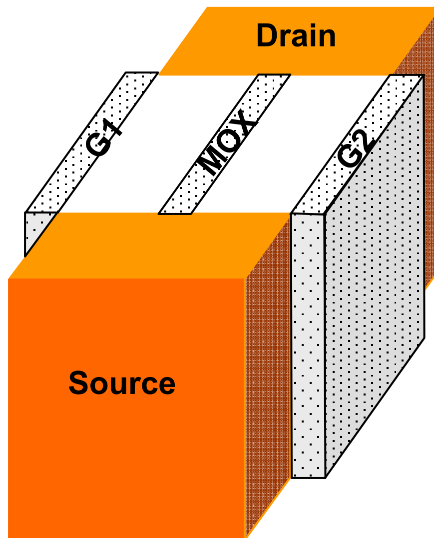
- it is not possible to **accumulate** one channel while **inverting** the opposite channel
- the back surface potential follows the front gate voltage: **volume inversion**
- the film behaves as quasi-rigid **rectangular well**, with flat potential

[Eminente et al'06]

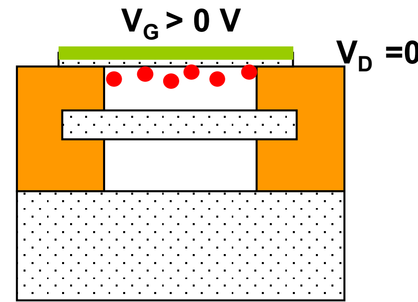


# A-RAM: Multi-body DRAM

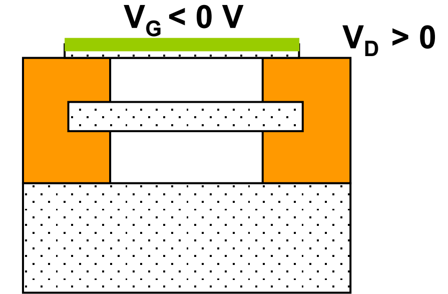



State '0'

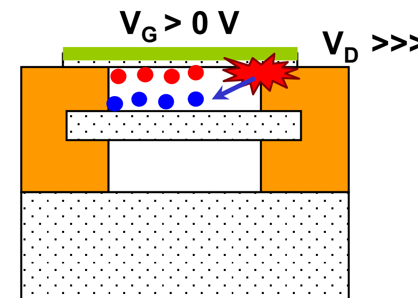



Program

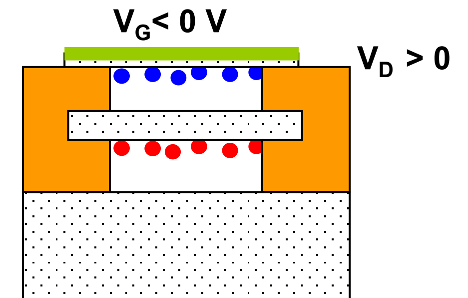



Read

State '1'




Program




Read

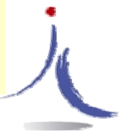
**Two bodies:**

1 – for hole storage
2 – for $I_D$ sense

[Rodriguez et al, patent 2009]

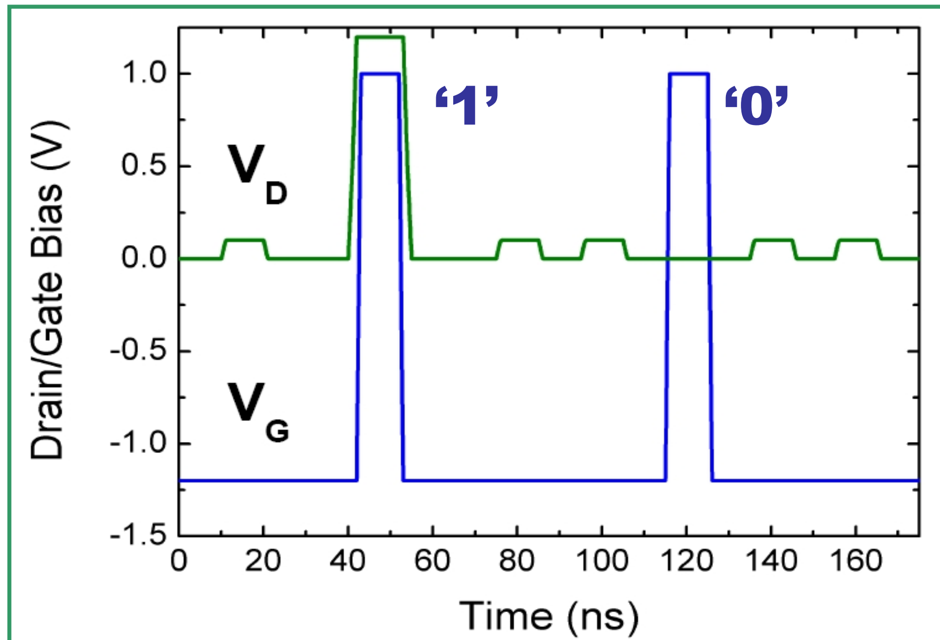
**Advantages:**

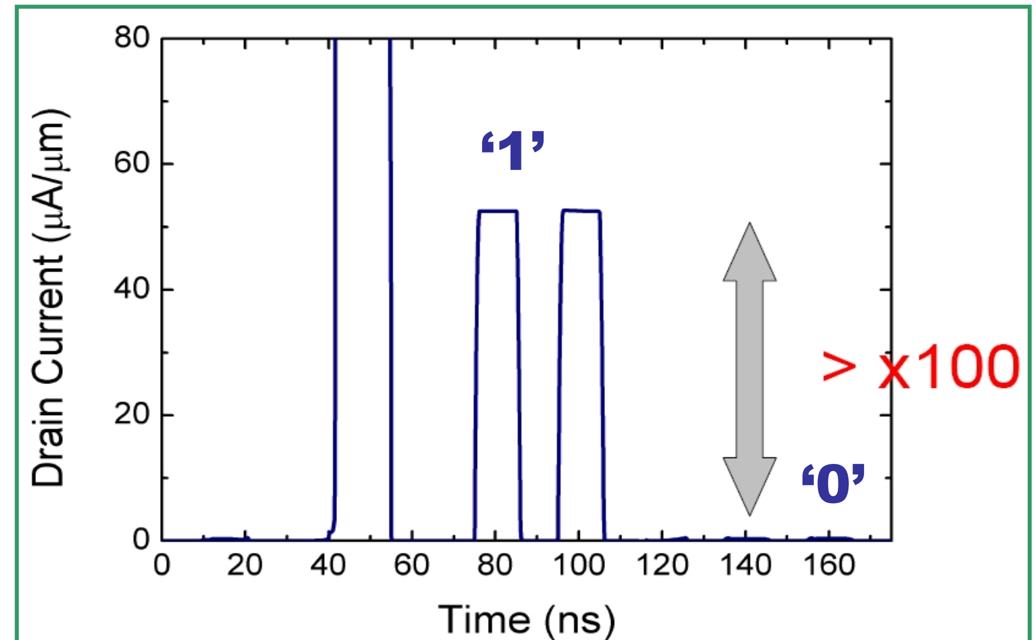
- Scaling
- Ultrathin: no super-coupling
- Single-gate operation
- Simple Word/Bit line signals



# A-RAM ...

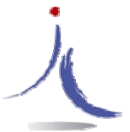
## Programming/ Reading cycles



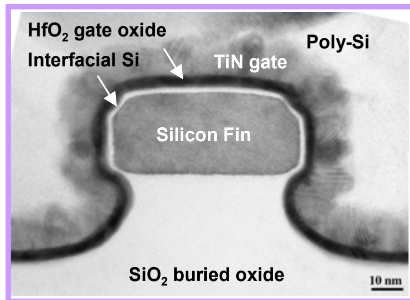

- $T_{Si}$ and MOX engineering can enhance the bit margin over a factor of 100
- Simple writing/reading signals
- Retention is controlled by the transistor gate

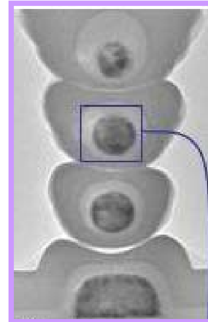
[Rodriguez et al, patent 2009]



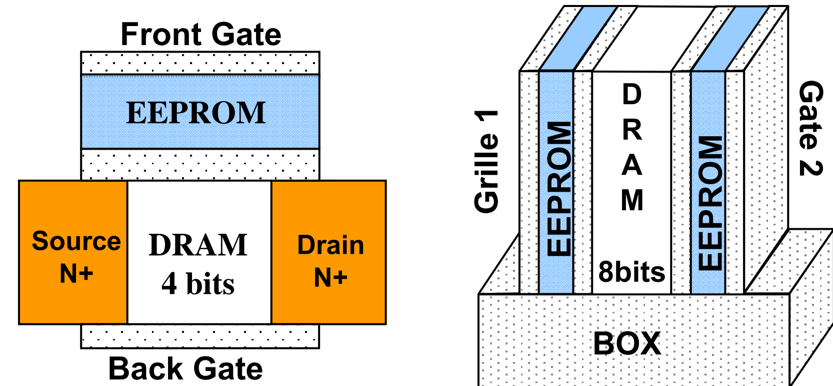
# Novel Architectures & Concepts

## FinFETs, Triple-Gates & 3D Nanowires

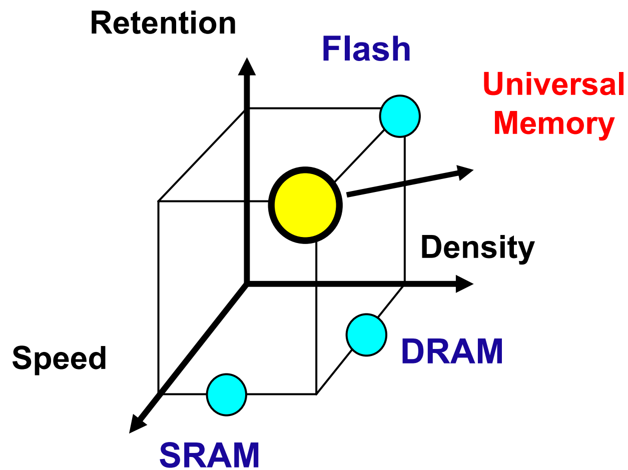


## URAM: Unified Memory

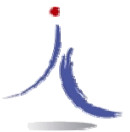



**Multi-bit memory: 2n states**



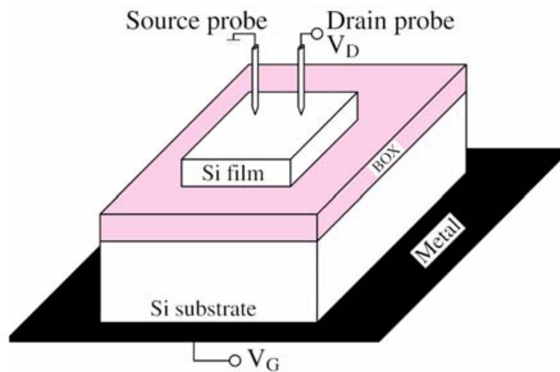

**Challenges:**

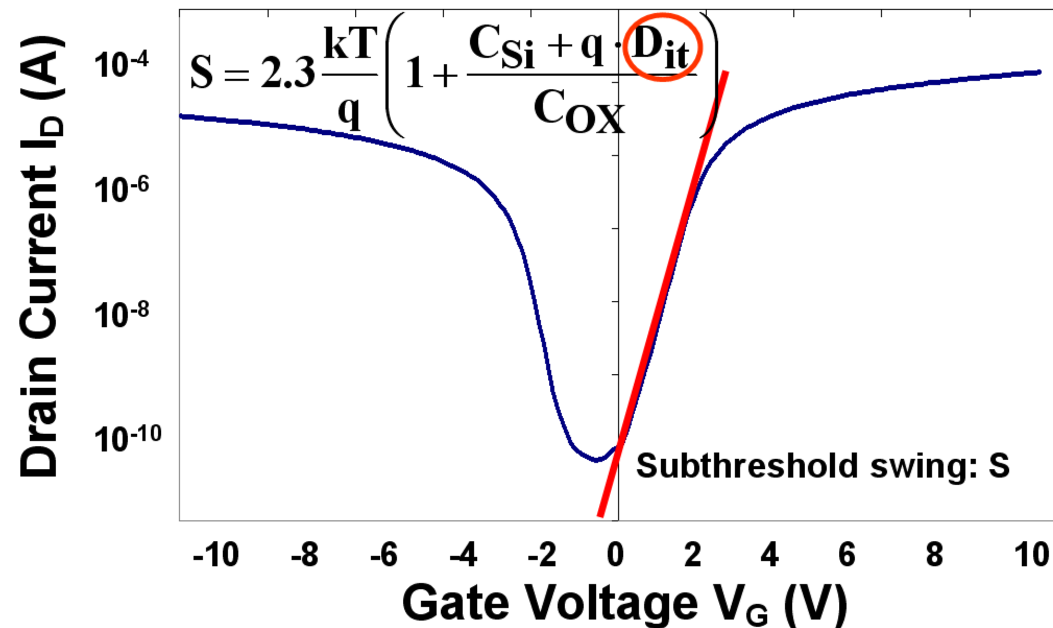
- Get 4 - 8 distinct levels of current
- Lower time and bias for programming
- Select appropriate materials and architectures



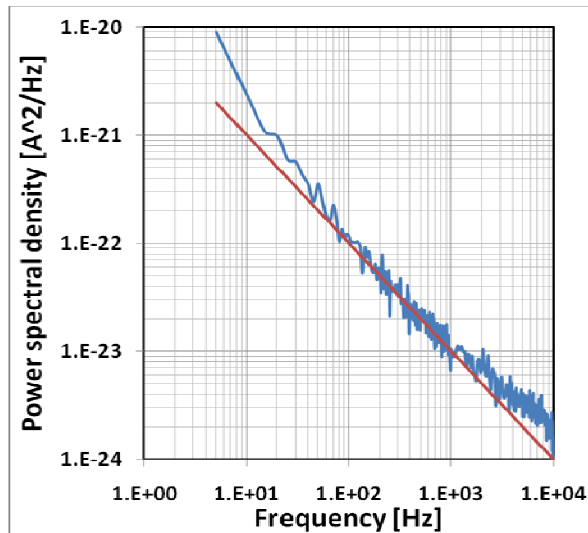
# Puzzle 1: Noise in Ψ-MOSFET

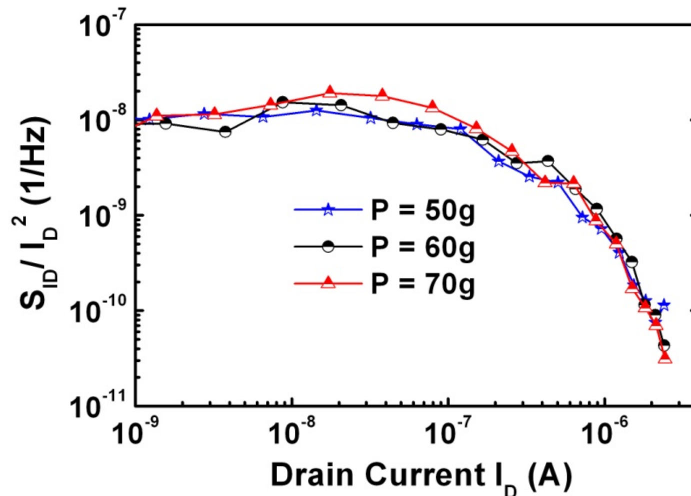
- Very powerful technique to probe the quality of SOI wafers
- The density of interface traps is determined from the sub-$V_T$ swing
- Noise is sensitive to traps
- Can we have a more sensitive tool for detecting $D_{it}$ ?



# Puzzle 1: Noise in Ψ-MOSFET

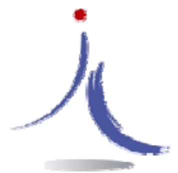



- First time noise measurements
- Noise is *1/f*
- Normalized noise follows the McWhorter's model

$$\frac{S_{Id}(f)}{I_d^2} = \frac{g_m^2}{I_d^2} \frac{\lambda k T q^2 N_{it}}{WLC_{ox}^2 f^{\gamma}} = \frac{g_m^2}{I_d^2} S_{VG}$$

- The noise is due to carrier number fluctuations via trapping
- The noise does not depend on series resistances
- It decreases in longer Ψ-MOSFETs



# Puzzle 1: Noise in Ψ-MOSFET

- Calculated trap density is huge : $5x10^{13}$ $cm^{-2}$
- 2 orders of magnitude larger $D_{it}$ than from the swing

## Puzzle: Why is $D_{it}$ overestimated ??

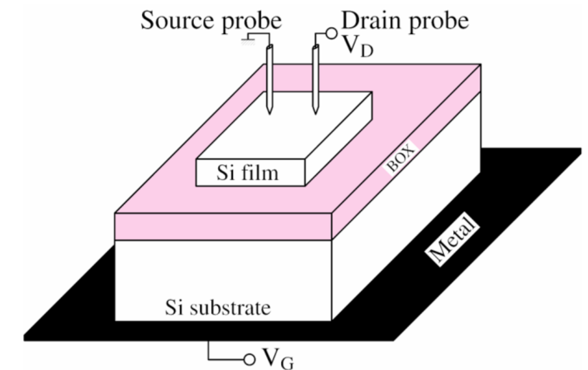
Trapping area:

- The aspect ratio of the P-MOSFET is W/L = 0.75

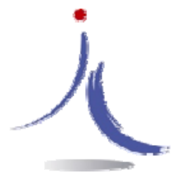
- The channel surface is $WxL = 0.75\ L^2$

- Inversion and trapping occur on the whole sample surface (much larger)

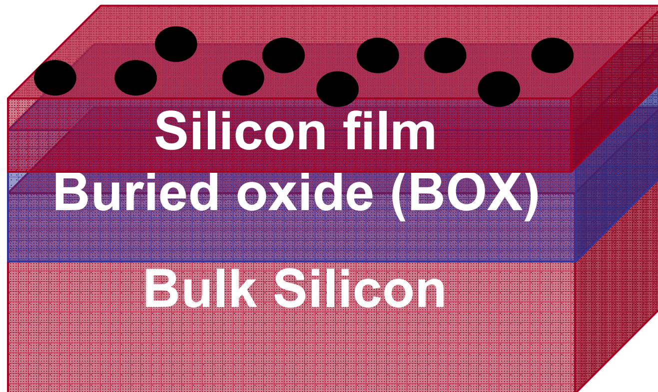
- Why the effective surface for noise and current is not the same?




Parasitic trapping at the unpassivated top surface?

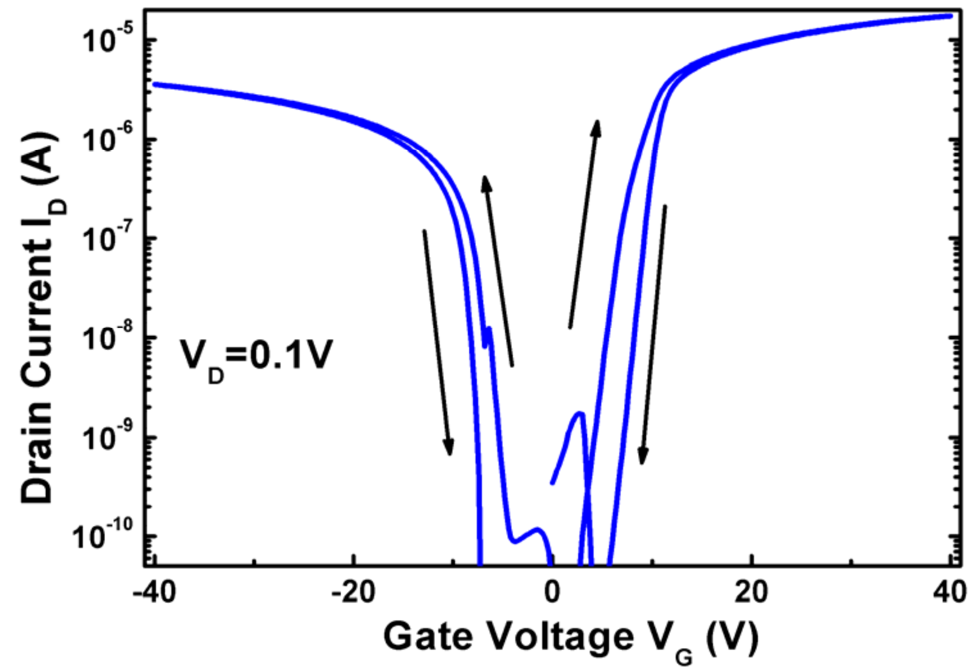


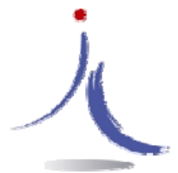
# Puzzle 2: Golden Ψ-MOSFET




Gold nanoparticles deposited on the surface

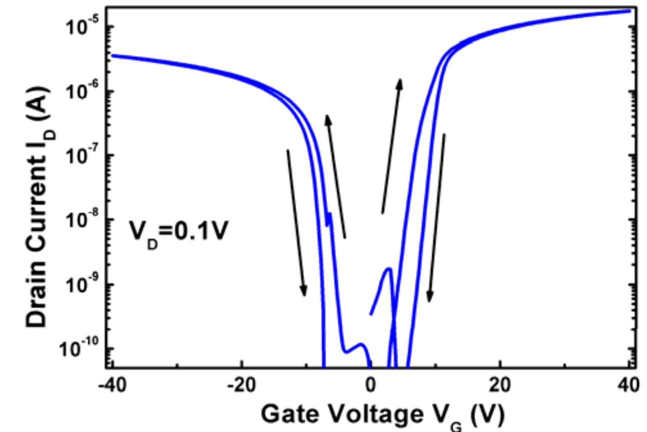
Hysteresis in $I_D(V_G)$ curves: $\Delta V_T = 3$ V



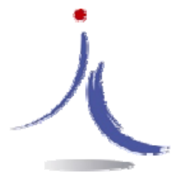



# Puzzle 2: Golden Ψ-MOSFET

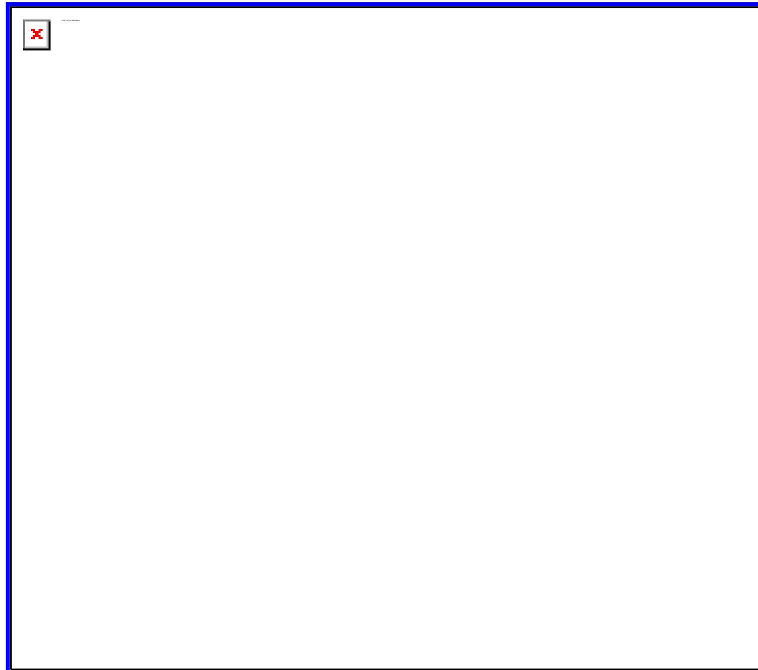
- Hysteresis: due to gradual charging of nanoparticles
- Do the nanoparticles behave as $D_{it}$ or $Q_{ox}$ ?
- $\Delta V_T$ increases
  - in thinner films
  - for higher density of nanoparticles

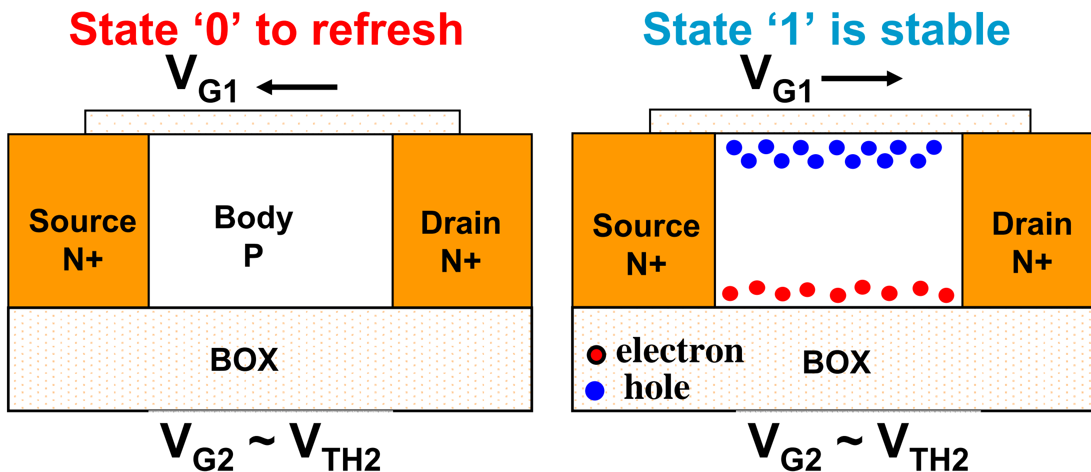



- $\Delta V_T$ = 3 V corresponds to $6\times10^{11}$ charges/cm$^2$
- Coupling coefficient = $1 + C_{it}/C_{si}$
- Au nanoparticles: diameter = 5–50 nm and density = $4 \times 10^8$ cm$^{-2}$
- Each 50 nm ball can trap $10^3$ electrons
- Is this analysis correct?
- What is the maximum charge the balls can accommodate?
- For ultimate sensitivity: larger or more numerous golden balls?



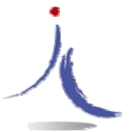
# Puzzle 3: Hysteresis in FinFET



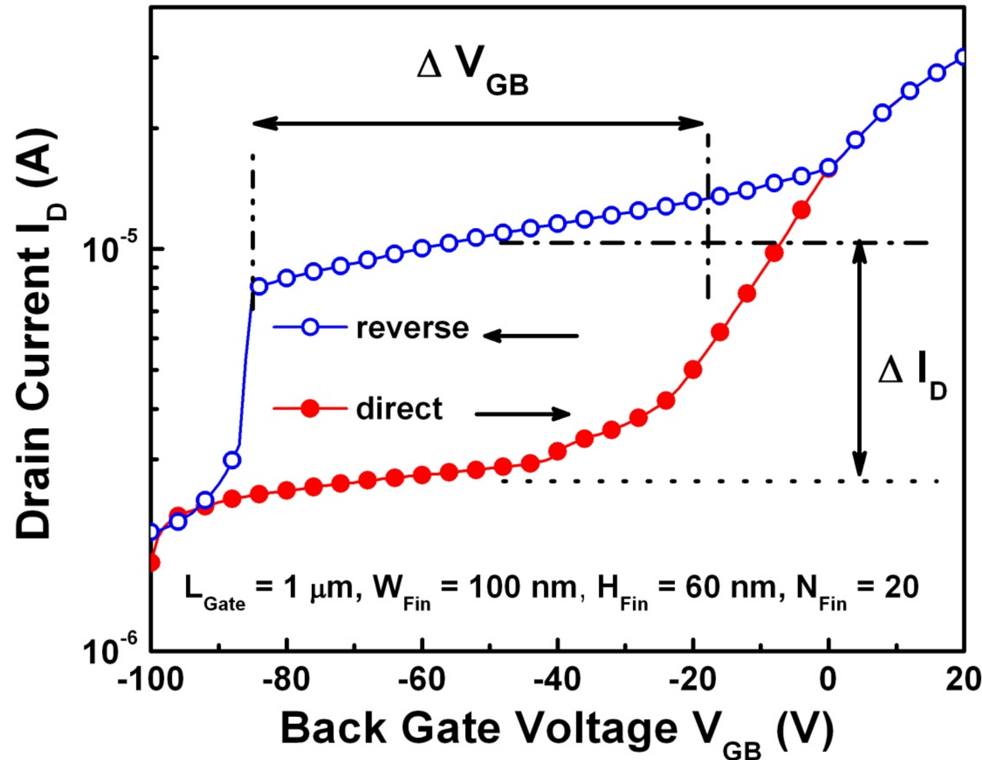


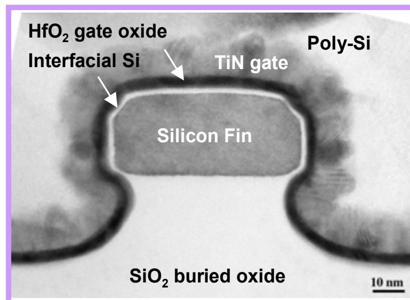

## MSD Effect:

- Planar FD MOSFET with $V_{GB}$
- Hysteresis = memory effect
- Combined effects:
  Interface coupling +
  Floating body +
  Transient
- Capacitor-less DRAM



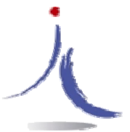
# Puzzle 3: Hysteresis in FinFET




## Reversed MSD Effect:

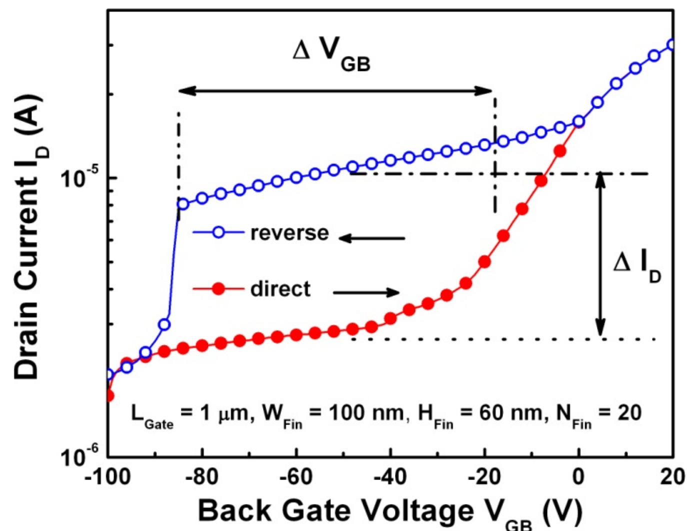
- FinFET with $V_{GB}$ scan; $V_{FG} \geq V_{T1}$
- Direct scan:
  - Back interface accumulated, high $V_{T1}$
  - Equilibrium
  - Front current increases by coupling: $V_{T1}$ decreases with $V_{GB}$
- Reverse scan:
  - No holes available
  - Depleted back interf: lower $V_{T1}$, higher $I_D$
  - Where is the deep-depletion effect gone?
- Experimental clues:
  Hysteresis suppressed for illumination or narrow fins

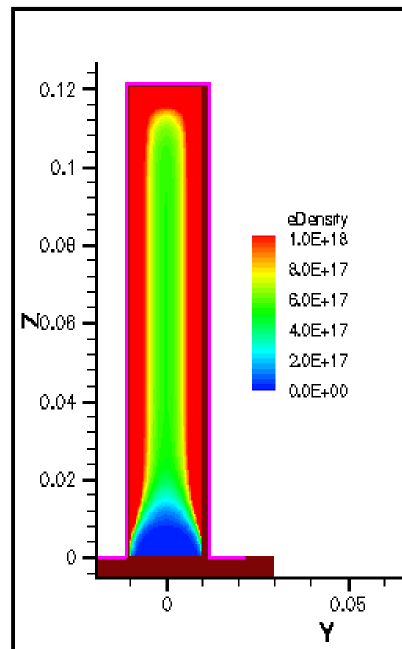


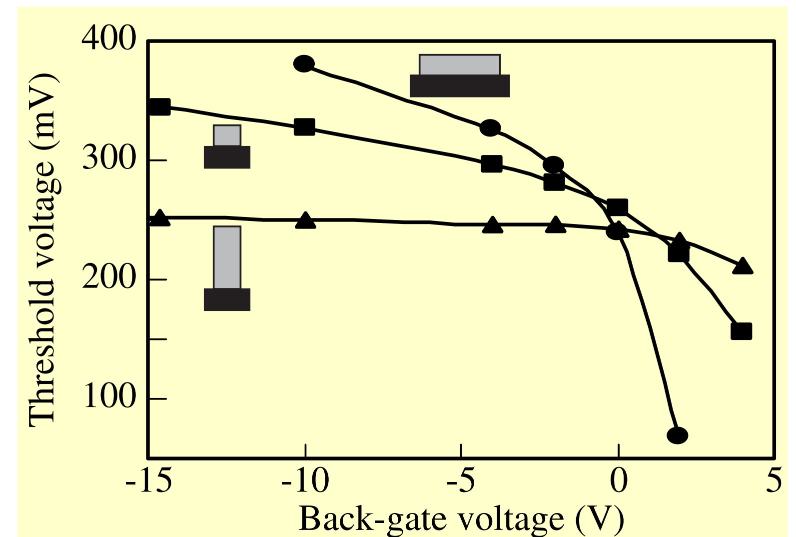
# Puzzle 3: Take-away Questions

**Why is MSD effect upside-down in FinFETs?**

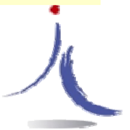
**Why is the front current unaffected by deep depletion?**



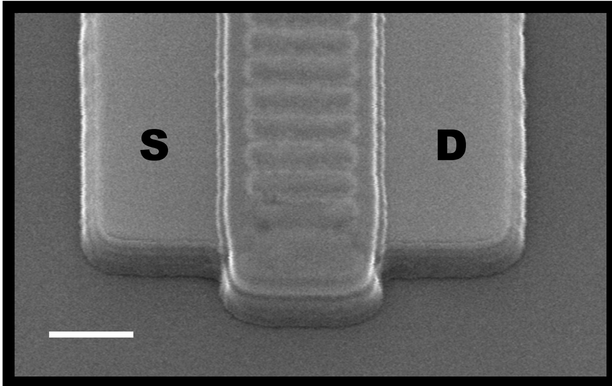




**Competition between lateral and vertical coupling?**



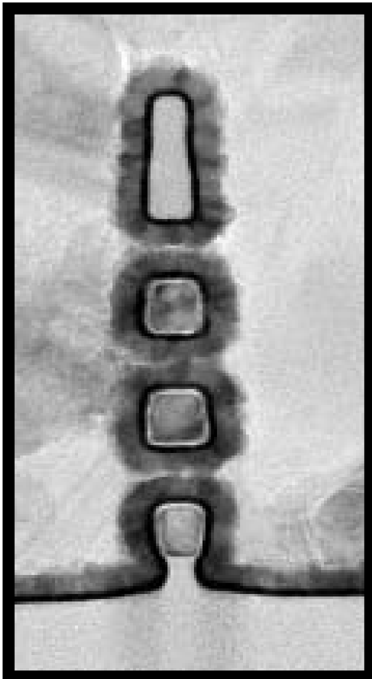
# Puzzle 4: Mobility in Nanowire FETs

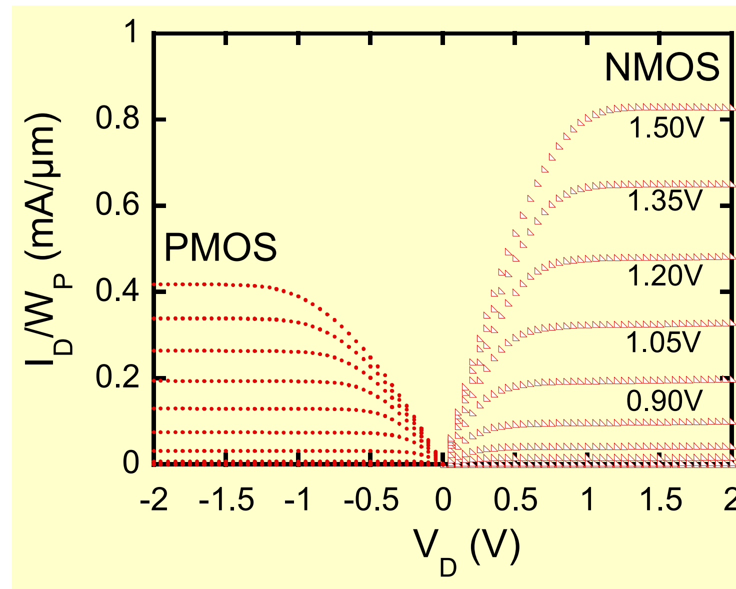



3 levels vertically stacked

50 nanowires in parallel

Various geometries

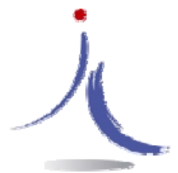




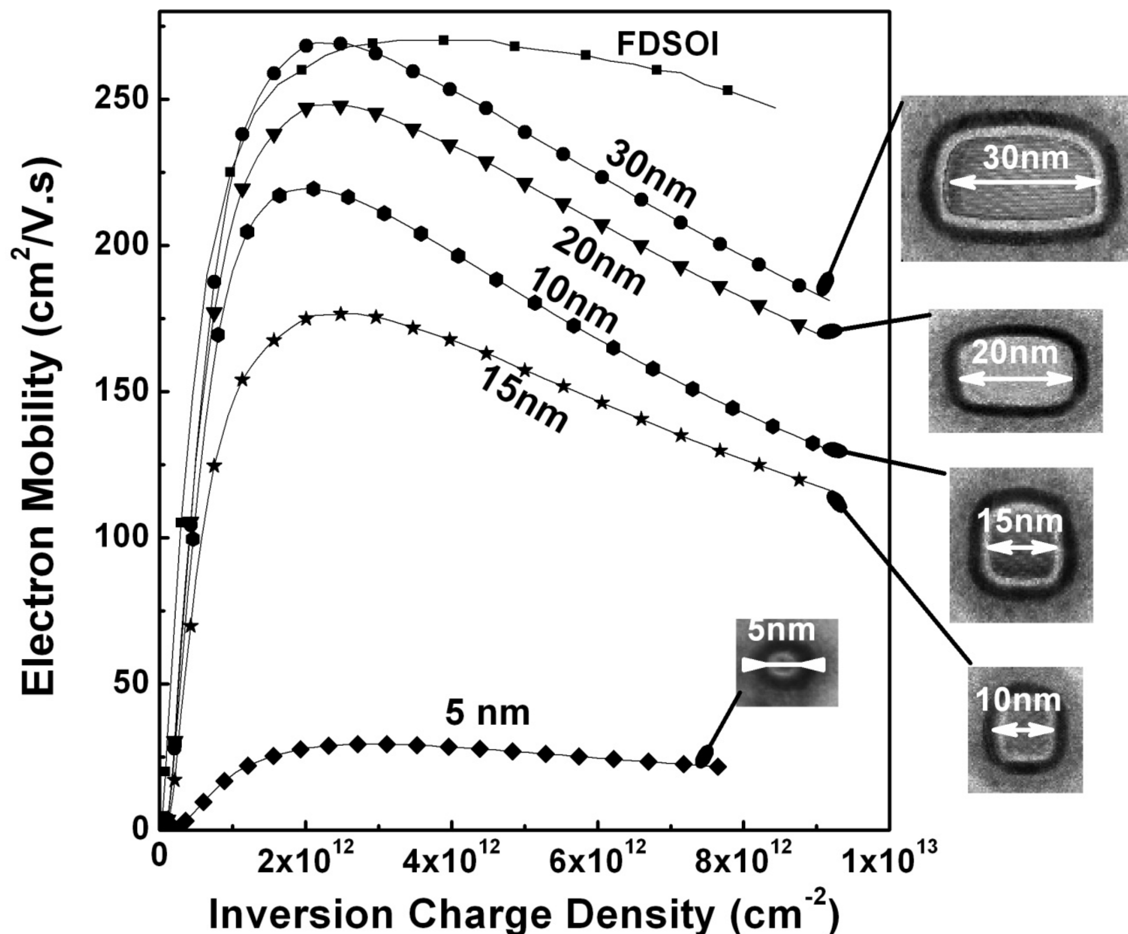

Well behaved characteristics

Excellent subthreshold swing

Reasonable mobilities



# Puzzle 4: Mobility in Nanowire FETs

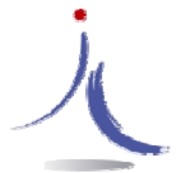



**Puzzle:**

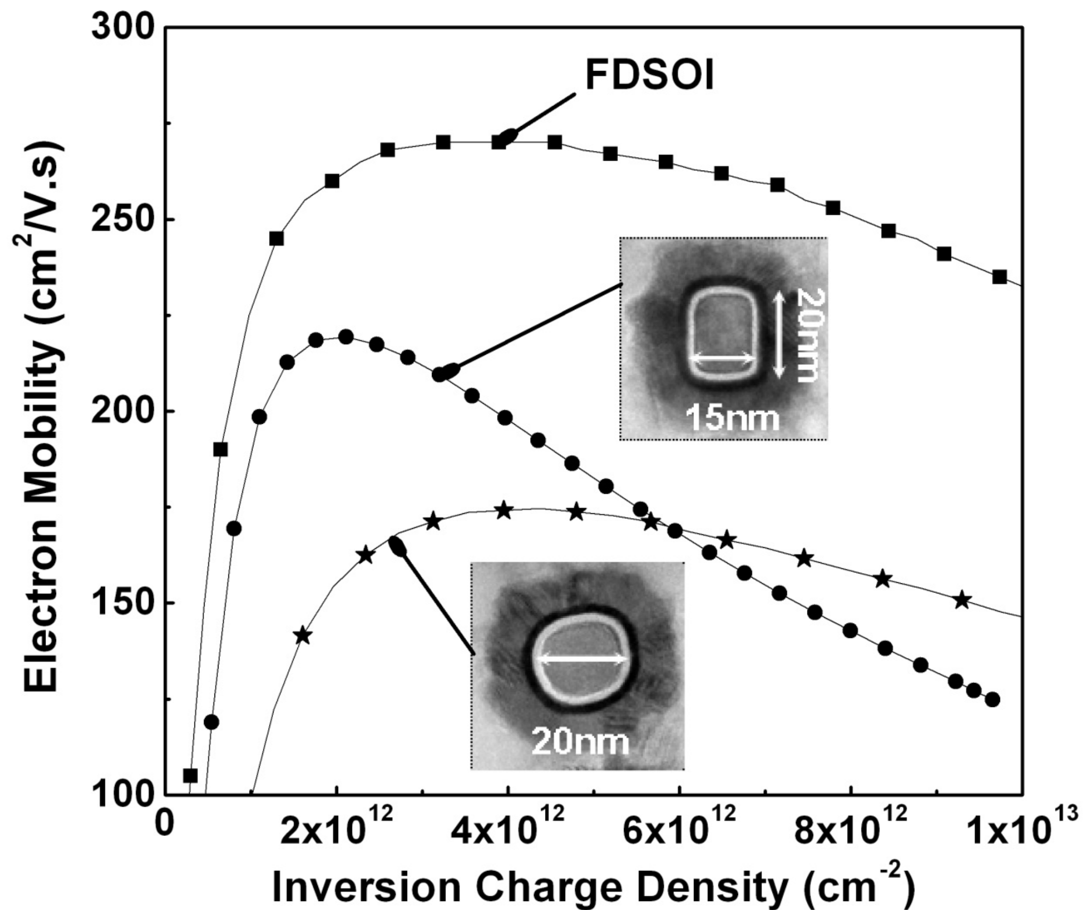
**Why is the mobility degraded in 5 nm nanowires?**

**Hints:**

- Subband splitting
- Phonon & carrier confinement
- Technology



# Puzzle 4: Mobility in Nanowire FETs



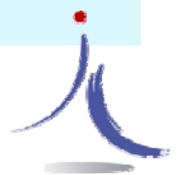

## Puzzles:

**Why is the low-field mobility degraded in circular nanowires?**

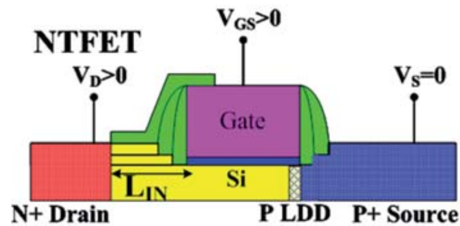
**Why is the high-field mobility improved?**

## Hints:

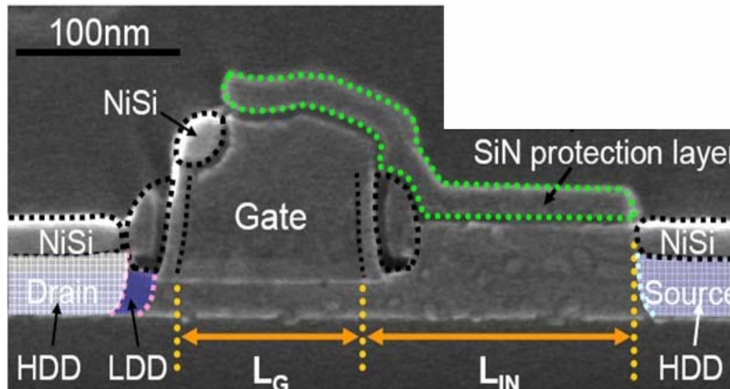
- Charge pumping shows higher $D_{it}$
- Varying surface orientation
- Surface roughness improved by H anneal



# Final Puzzle: Tunneling FETs

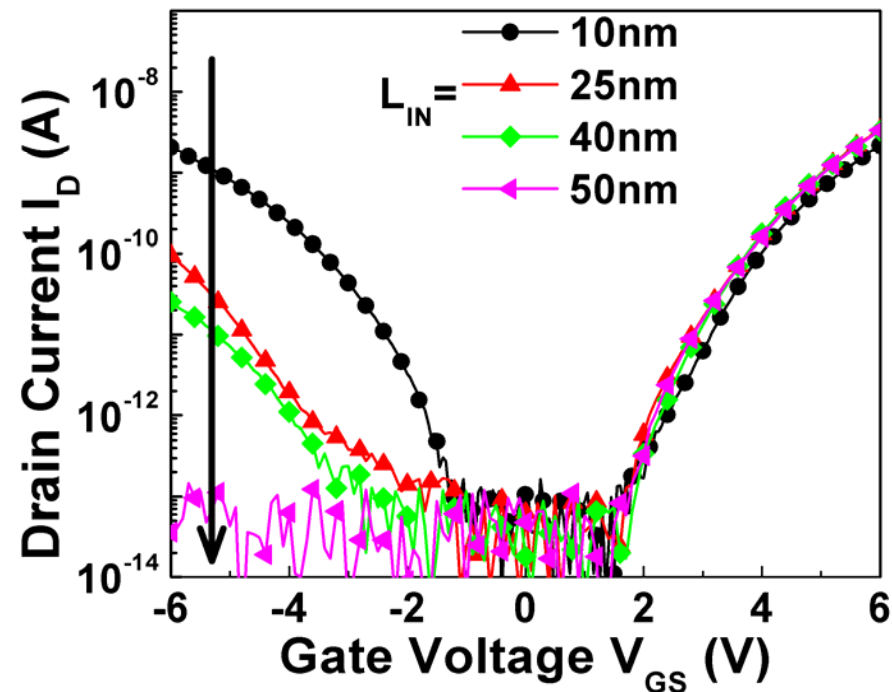


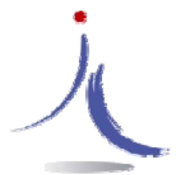

- TFET = Gated PIN diode
- Reversed biased
- B2B tunneling: small switch (SS < 60 mV/decade)




$L_{IN}$ = 0: symmetric TFET
Tunneling at both S & D

$L_{IN}$ = 50 nm: suppressed ambipolar conduction

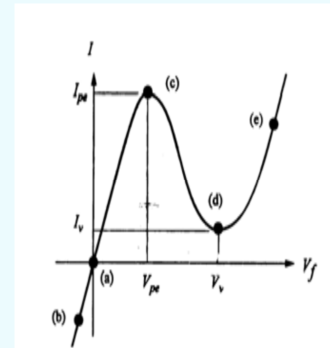


# Final Puzzle: Tunneling FETs

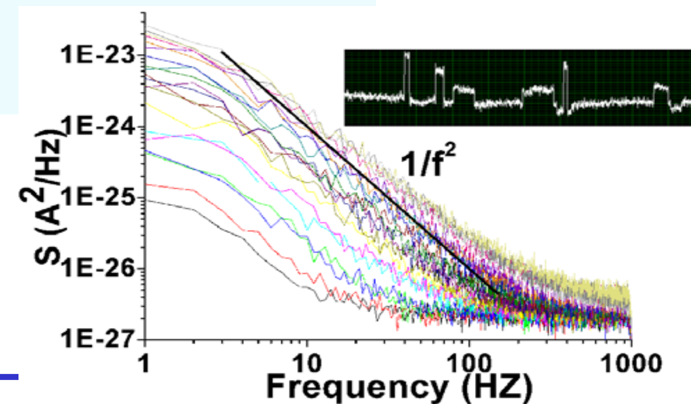
## Puzzles:

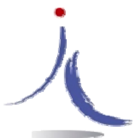
- Why is the swing larger than 60 mV/decade?
- Why is the current smaller than predicted by simulations? Even in Ge…
- No negative resistance in $I_D(V_D)$ curves? Why?
- Is the current due to B2B tunneling exclusively?




### Hints:

- $V_T$ and swing do not depend on channel length
- Noise is RTS with *1/f²* spectrum (discrete number of traps)



# Conclusions

- SOI is HOT: performance & scalability
- SOI is GREEN: power & voltage saving
- SOI is versatile: new devices
- Puzzles selected to develop curiosity & thinking