The future of Nanoelectronics by Scaling of CMOS and Functional Diversification

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on NAnometer CMOS Technology (WIMNACT 26)
Yokohama, February 9, 2011

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Since 2005: A complete set of research platforms…

CEA LETI (1600 CEA researchers)
collaborating
in MINATEC campus (3000 researchers)

MicroTechs for bio

200mm 'CMOS' new concepts & Beyond CMOS

300mm CMOS Integration & adv. modules

Design

More Than Moore 200mm

Advanced Research 100-200mm

Nanoscale Characterization

Incubation

Education

interacting daily with R & D platforms worldwide
(ST Crolles, IBM Albany, …)

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Outline

- Introduction : Trends and Hot Topics in Nanoelectronics
- Nanoelectronics scaling and use of the 3rd dimension to continue Moore's law.
- Interfacing the Multiphysics World (More Than Moore) thanks to functional diversification
- Building new systems and their packaging with a 3D tool box at a wafer level.
- Conclusions

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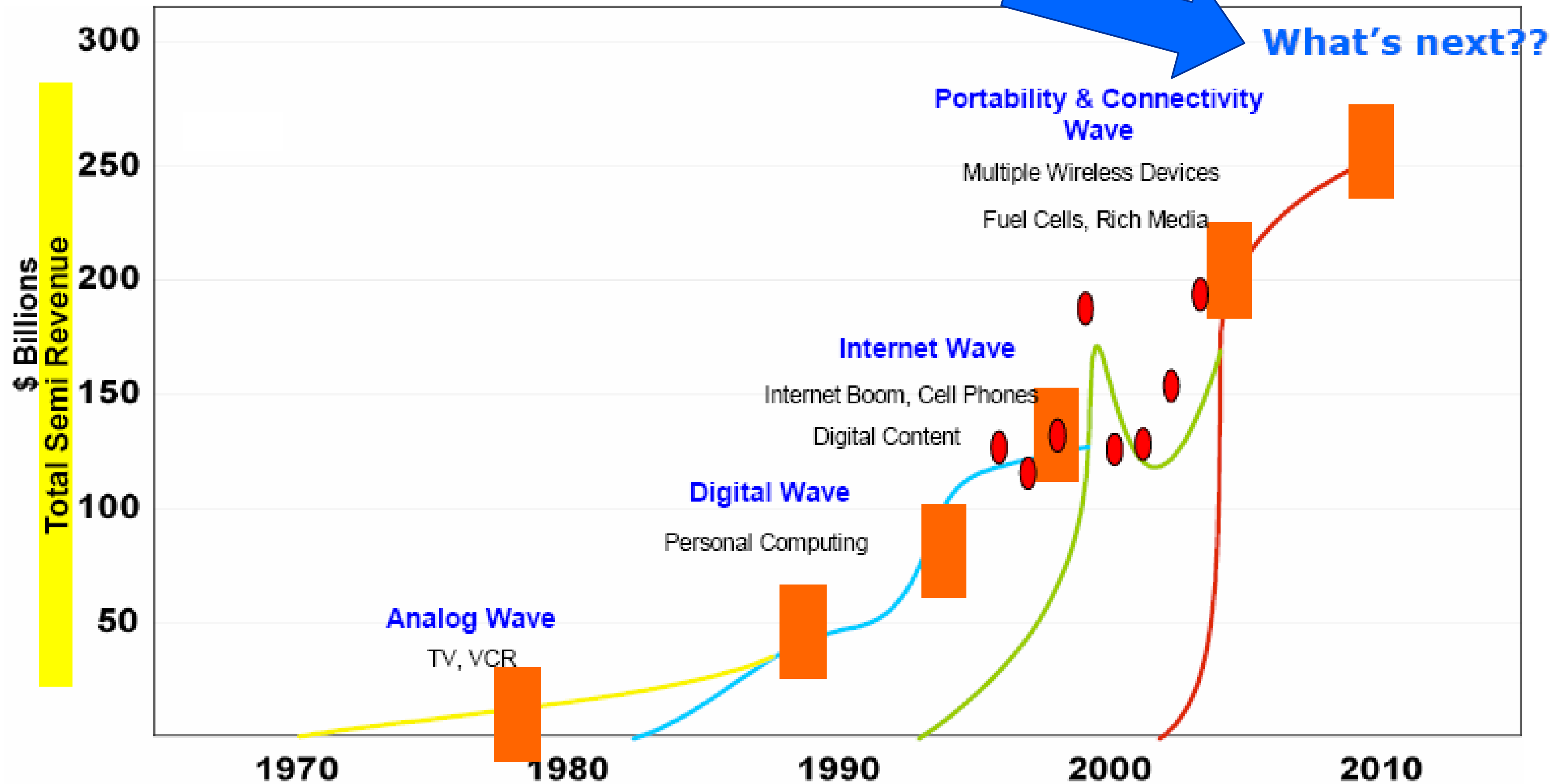
Semiconductor Market applications successive waves

Quality of life, Social, Environment, Health, Energy, …associated to ICT



Source : Semico Research Corp. May 2004 IPI Report

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Ecological Footprint of ICTs

reported by Intergovernmental Panel Climate Change(IPCC) *Source: TU Dresden*

- **Currently, 3 % of the world-wide energy is consumed by the ICT infrastructure**
  - which causes about 2 % of the world-wide CO_2 emissions
  - comparable to the world-wide CO_2 emissions by airplanes or ¼ of the world-wide CO_2 emissions by cars
- **ICT: 10% of electrical energy in industrialized nations**
  - 900 Bill.. kWh / year = Central and South Americas
- **The transmitted data volume increases approximately by a factor of 10 every 5 years**

For ICTs, keep in mind:

$P = P_{stat} + P_{dyn}$ $\quad P_{stat} = V_{dd} x I_{off}$ and $P_{dyn} = CV_{dd}^2 f$

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Scaling: a success story…thanks to innovation

INSTITUT CARNOT CEA LETI
MINATEC

Moore's law: 2Xdevices/year

Convergence
Portable Internet
Digital Camera
Home PC
Office PC
Main Frame
VCR Defense
C.T.V.

1 billion
10 millions

dynamic memories(DRAM)
1k 4k 16k 64k 256k 1M 4M 16M 64M 128M 256M 512M 1G 2G 4G

microprocessors
4004 8080 8086 80286 i386 i486 Pentium Pentium II Pentium III Pentium IV Itanium

ULK(11 lev met)
polymers +ALD (10 lev met)
HiK +metal gate
Cu+H(M)SQ (9 lev met)
Cu (7 lev met)
FSG(6 lev met)
damascene(5 lev met)
vias « plugs »,CMP(4 lev met)
STI, salicide
contacts « plugs »(3 lev met)
polycide
poly gate

Number of transistors per chip: 1,00E+00 1,00E+01 1,00E+02 1,00E+03 1,00E+04 1,00E+05 1,00E+06 1,00E+07 1,00E+08 1,00E+09 1,00E+10

Date: 1958 1963 1968 1973 1978 1983 1988 1993 1998 2003 2008 2013 2018

Critical Dimension: 100µm 10µm 1µm 0,10µm 10 nm

Electronic Device Architectures for the Nano-CMOS Era
From Ultimate CMOS Scaling to Beyond CMOS Devices
Editor: S.Deleonibus, Pan Stanford Publishing, Oct 2008

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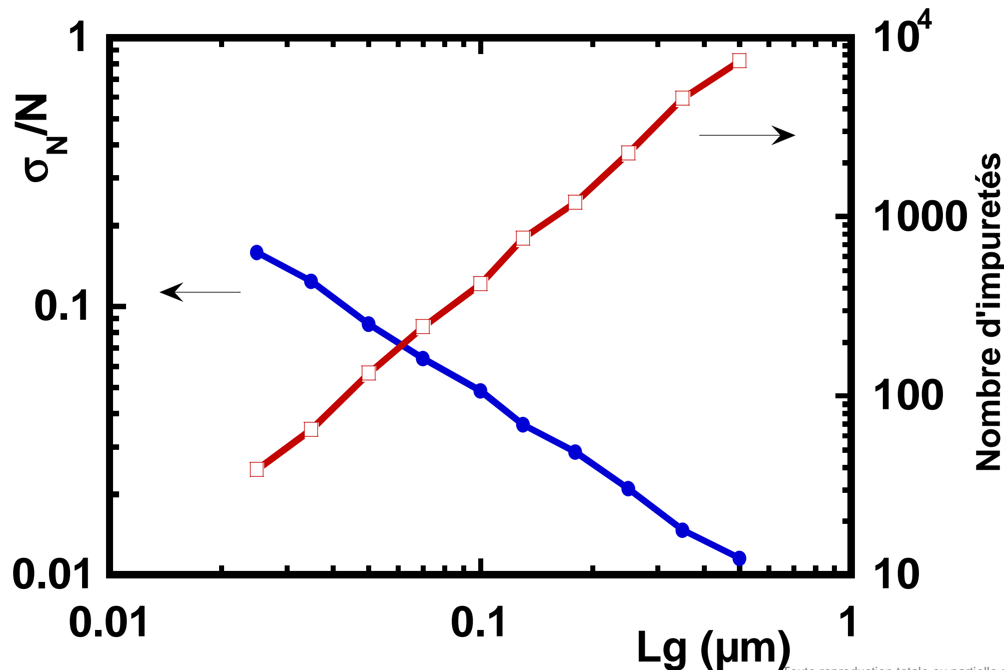
Hot Topics: parasitic effects in MOSFET technology

- Introduction of HiK and metal gate allows continued scaling and relaxes SiO2 gate leakage current related issues - Ig added to SCE, DIBL, subthreshold leakage(LETI IEDM 2002, Intel IEDM 2005)
- Statistical dopant variability
  - number of dopants in the active area decreases with scaling
  - random distribution of channel dopants

  Poisson's law. Standard deviation:

$$\sigma_{doping} = \left(\frac{N}{Volume} \right)^{1/2}$$



Statistical fluctuations of threshold voltage: 150 mV decay for VT=200mV(Lg=25nm) !!

Major interest for Low Doped channels

S.Deleonibus et al. ESSDERC 1999

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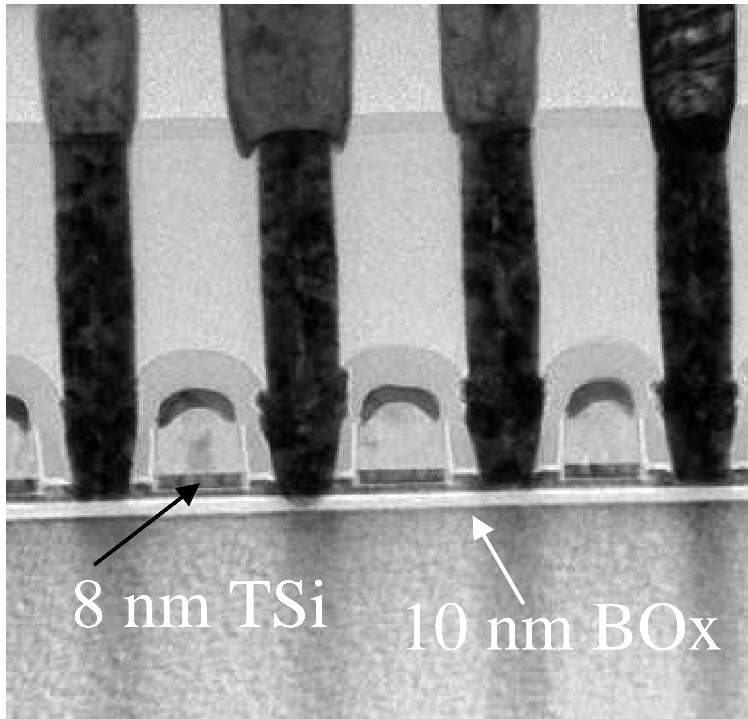
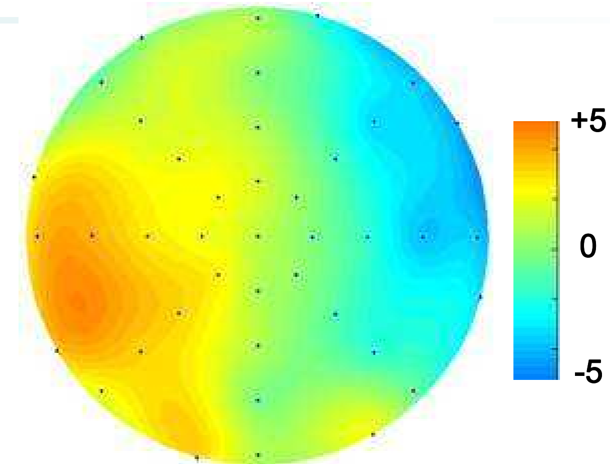
32nm Low Power FDSOI Undoped channels

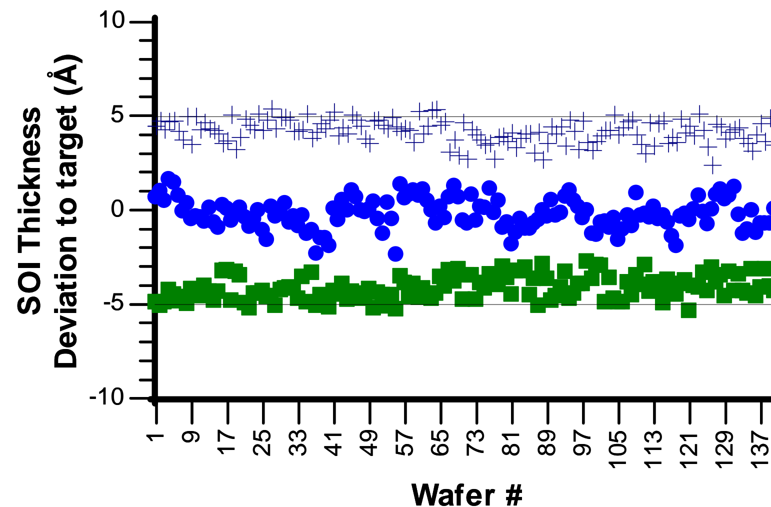
6T SRAM

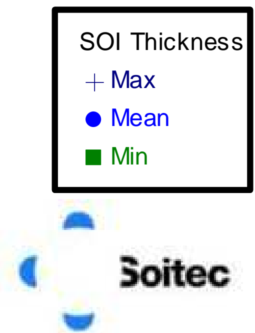
300mm wafers





Range = ±4 Å!





0.248µm² SNM (1.2V)=140mV

0.179µm² SNM (1.2V)=230mV

VDD=1V Ioff=6pA/µm

C.Fenouillet Beranger et al., IEDM 2007, VLSI Symp 2010

V.Barral et al., IEDM2007

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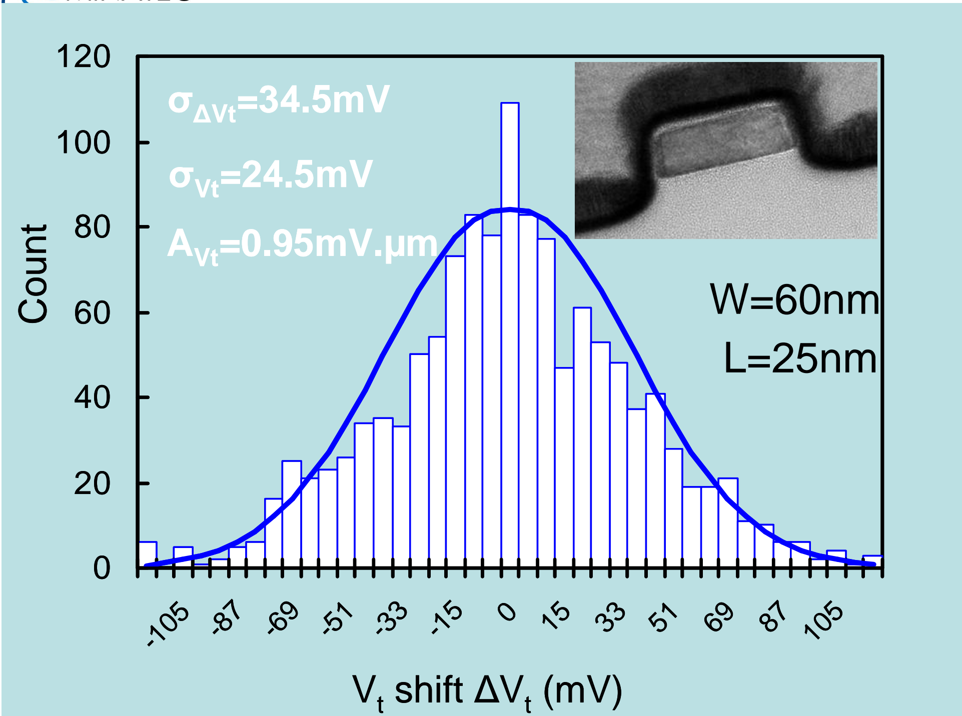
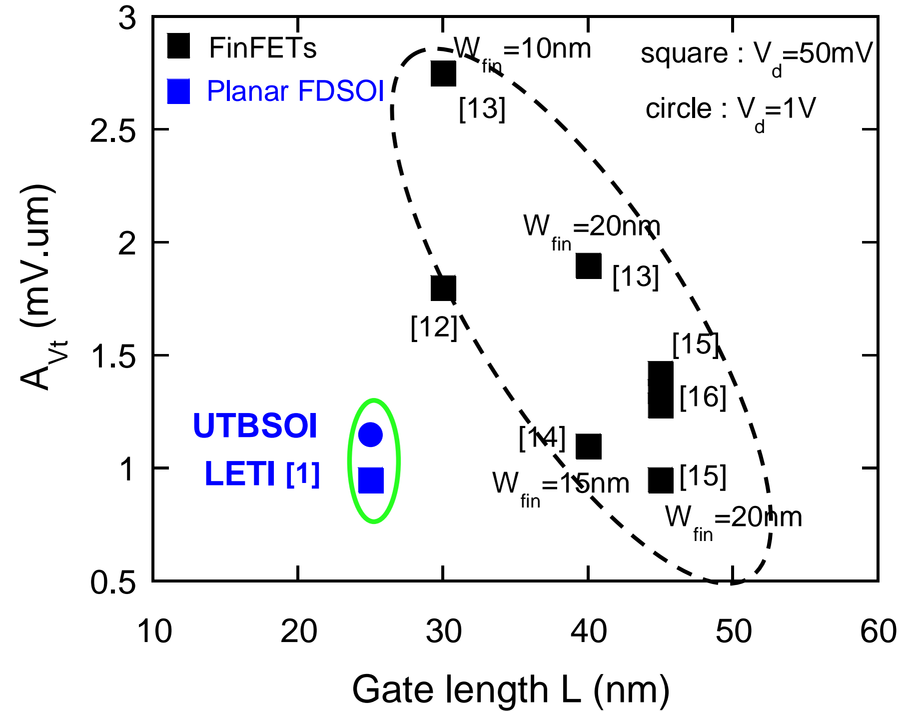
Record-high V_T matching performance

FDSOI Undoped channels vs.FinFET





O.Weber et al., IEDM 2008

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

($\sigma_{Vt}=\sigma_{\Delta Vt}/\sqrt{2}$ to compare measurements on pairs and on arrays of transistors in the literature)

Best trade-off between V_T variations and gate length scaling compared to bulk MOSFETs and FinFETs

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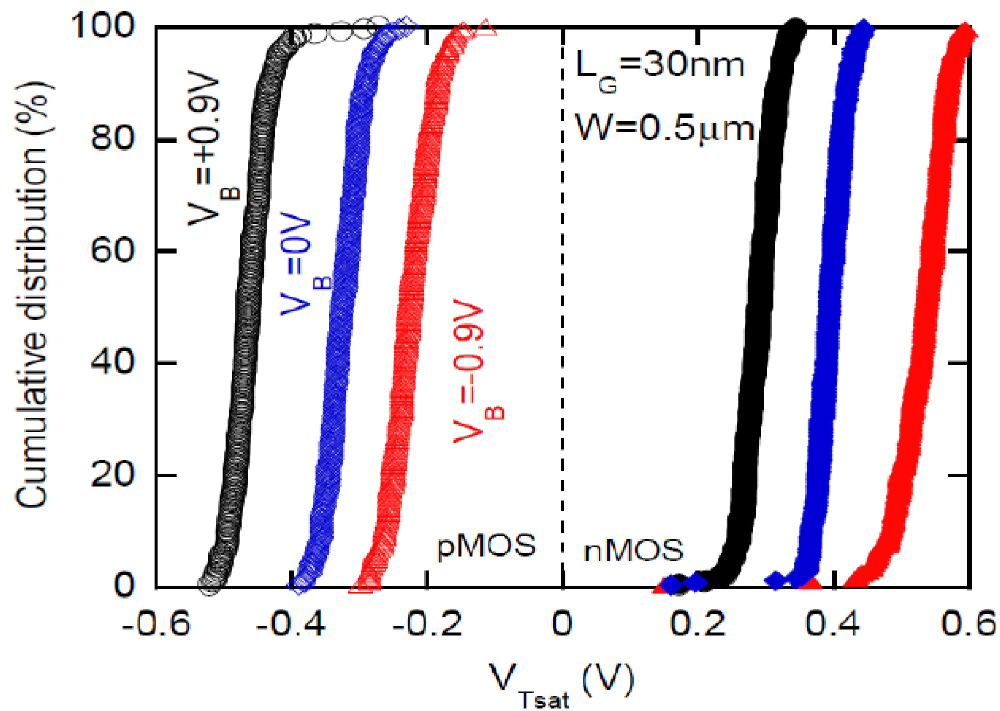
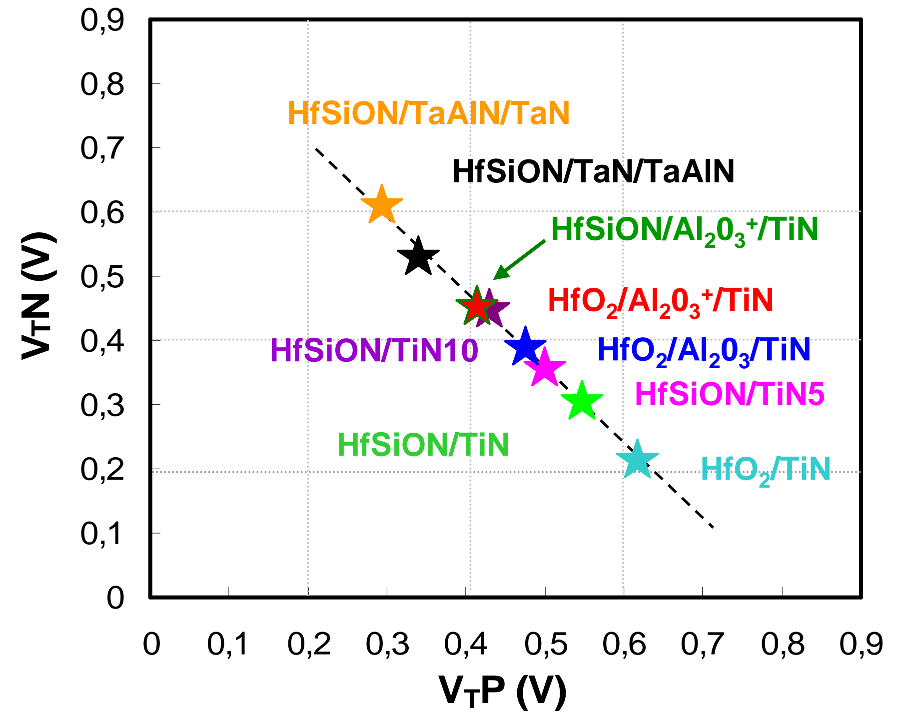
Multi VT solutions for SOC design
UTBOX + Back bias ; Gate stack engineering





BOX = 10nm and VBB/ Ground Plane
N and PMOS: VT modulation of ≤200mV

VT tuning by gate stack engineering

F.Andrieu et al. , VLSI 2010 Honolulu
O.Faynot et al., IEDM 2010 San Francisco, invited talk

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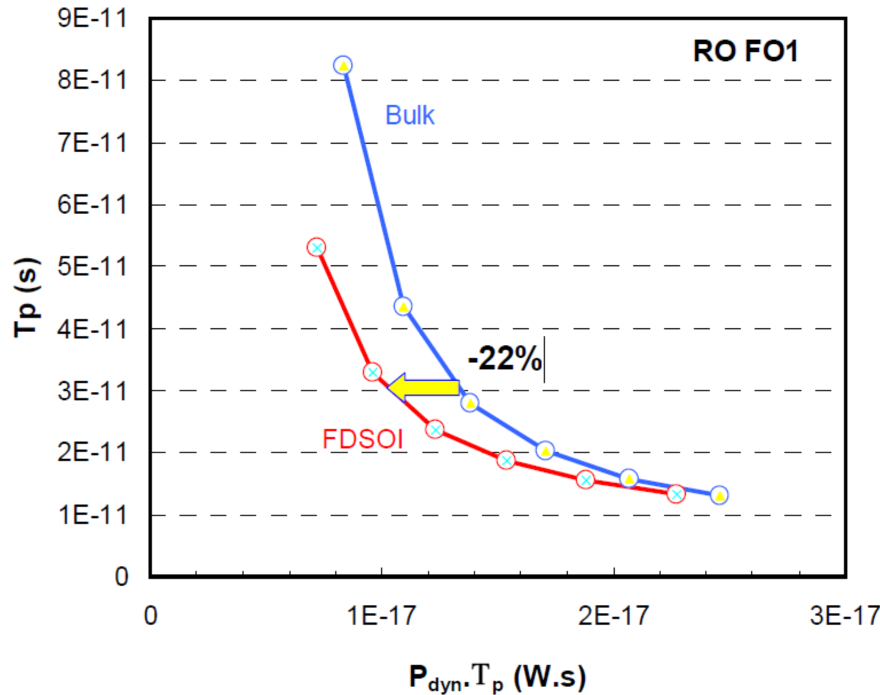
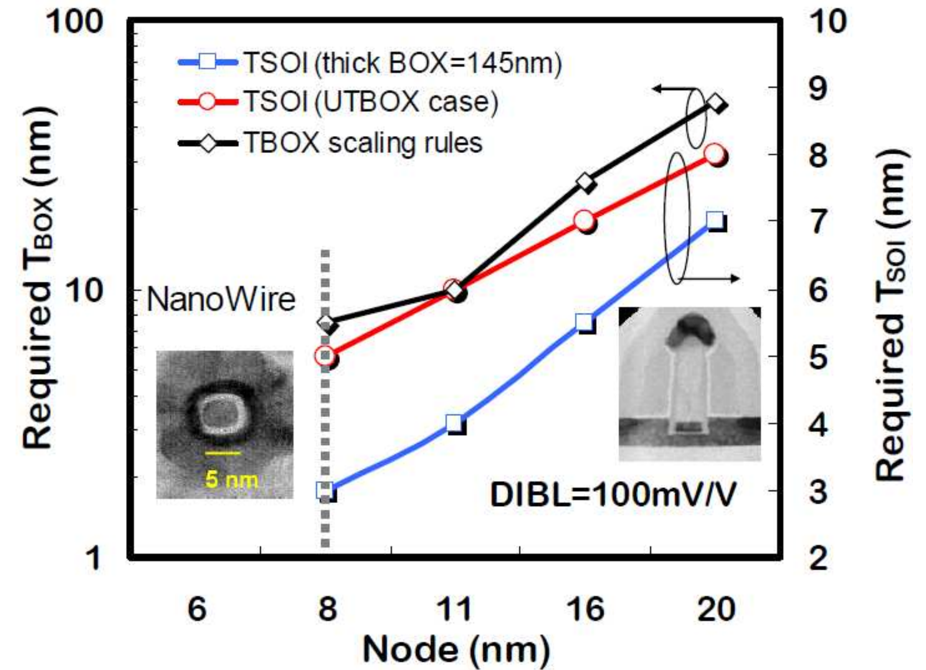
Merits of FDSOI

Delay vs. Power x Delay
22% improvement/bulk (20nm)



Reachable Scaling rules
(TSi, TBOx)



O.Faynot et al, IEDM 2010, invited talk

L.Clavelier et al, IEDM 2010, invited talk

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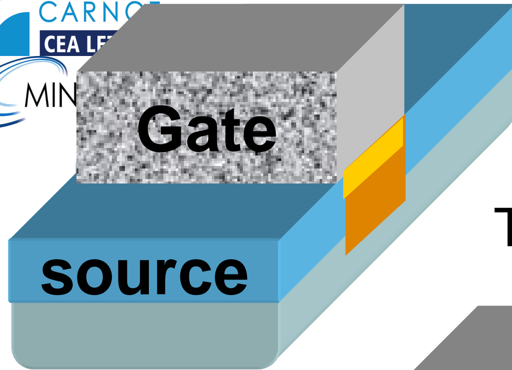
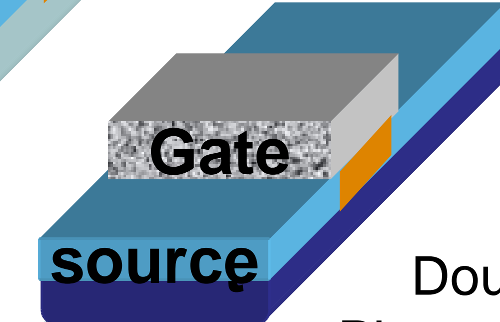
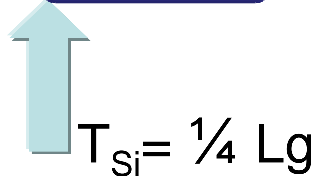


Bulk or thick SOI

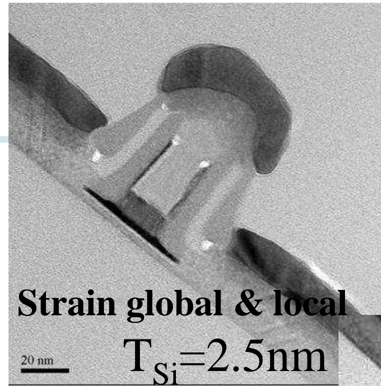
Planar

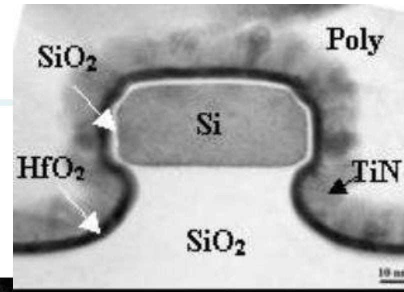


ThinSOI

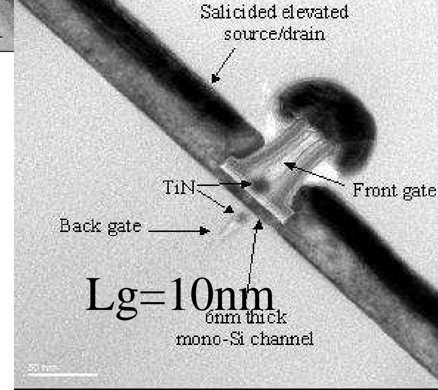


T_{Si}= ¼ Lg





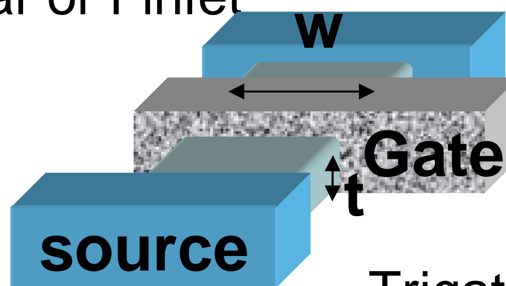
Jahan et al. VLSI2005



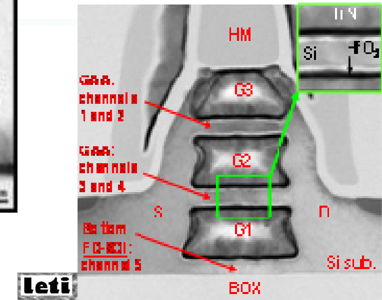
Barral et al. IEDM2007

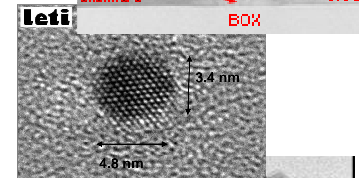
Andrieu et al VLSI2006

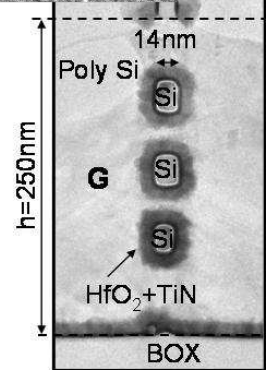
Double-gate Planar or Finfet



Vinet et al. EDL 2005





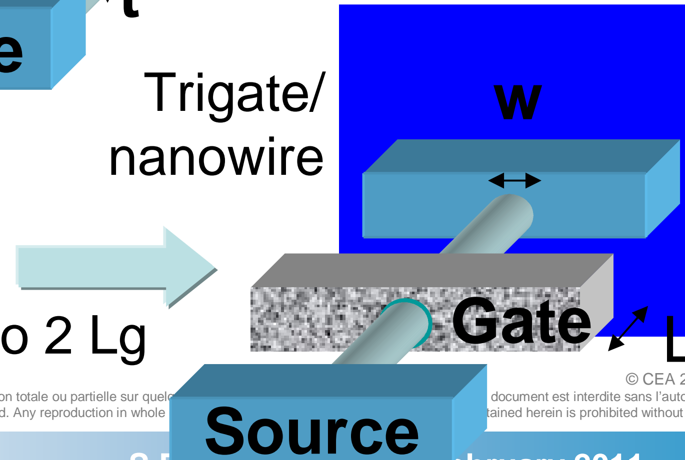


Thin Films Devices

Relaxing optimization scaling rule by architecture

T_{Si}= ½ Lg

Trigate/ nanowire



T_{Si}= 1 to 2 Lg

Bernard et al VLSI 2008

Dupré et al. IEDM 2008

Ernst et al. IEDM 2008

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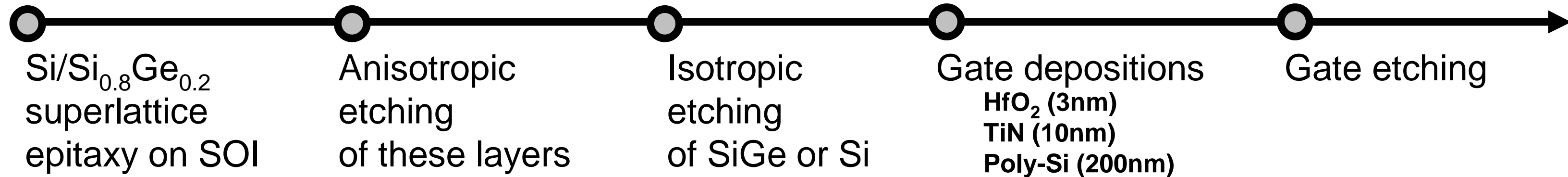
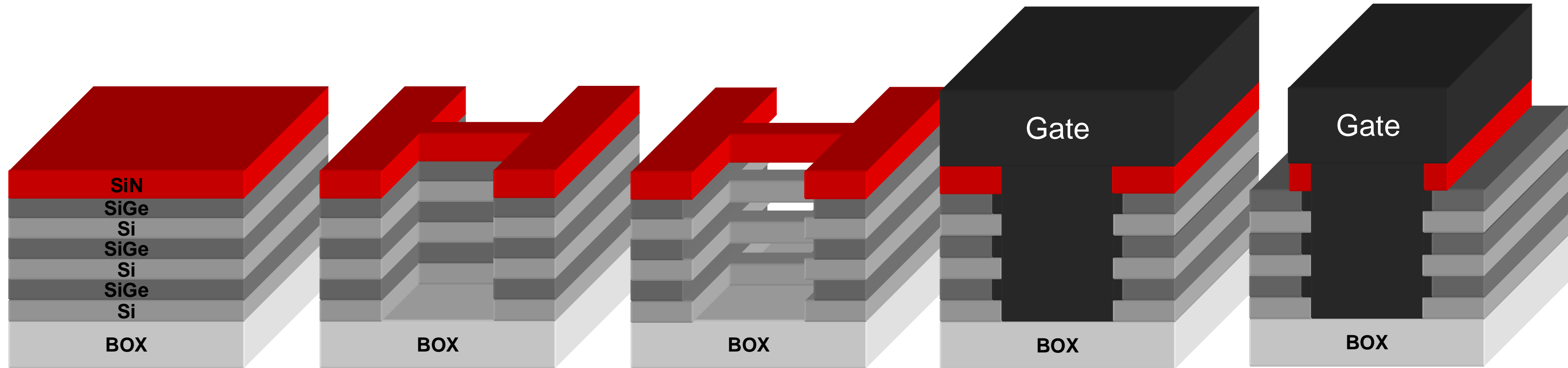
Device fabrication

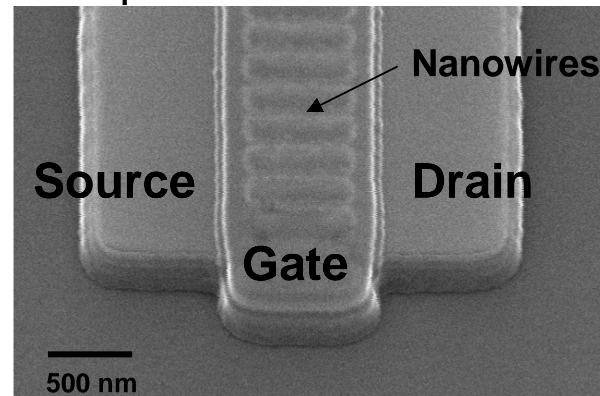




S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of-Line Processes

Top view of our device



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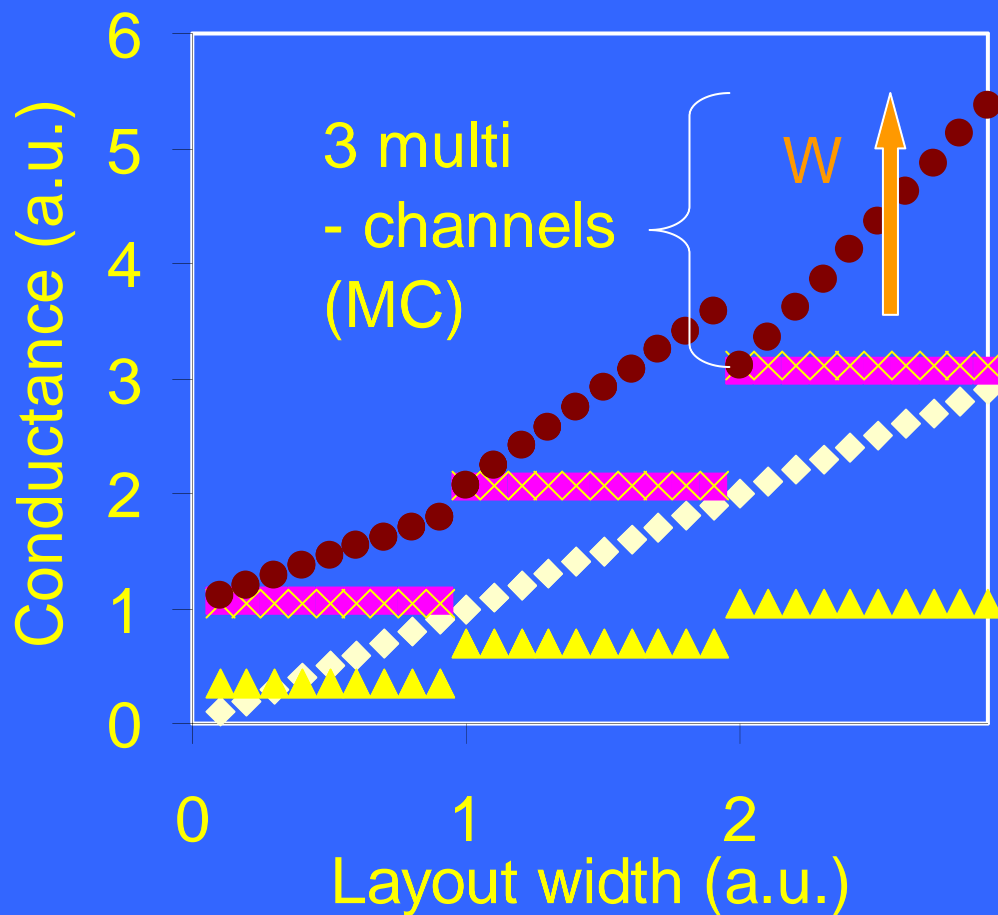
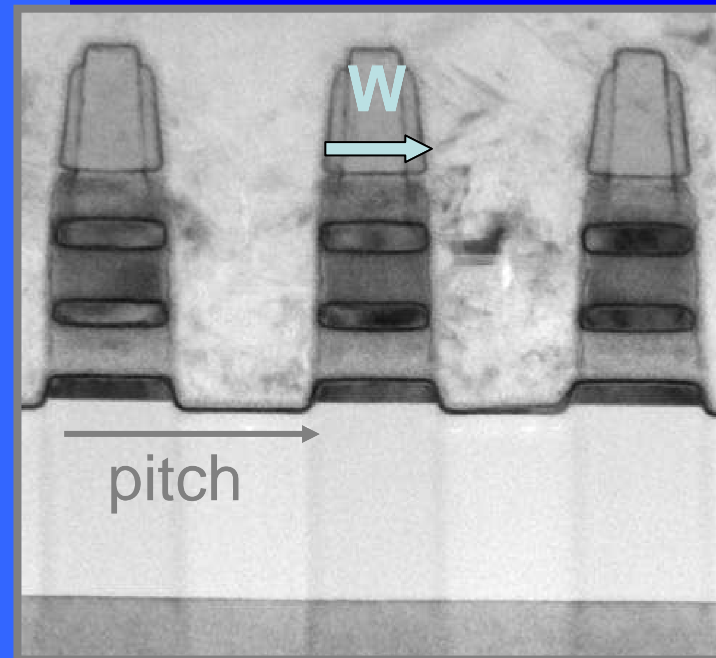
Tunable width

Design flexibility to tune the conductance





See for details:
T. Ernst et al, IEDM'06,'08 SSDM'07, ICIDT'08
E. Bernard et al. VLSI'08, ESSDER'07
C. Dupré et al, IEEE SOI Conference 07

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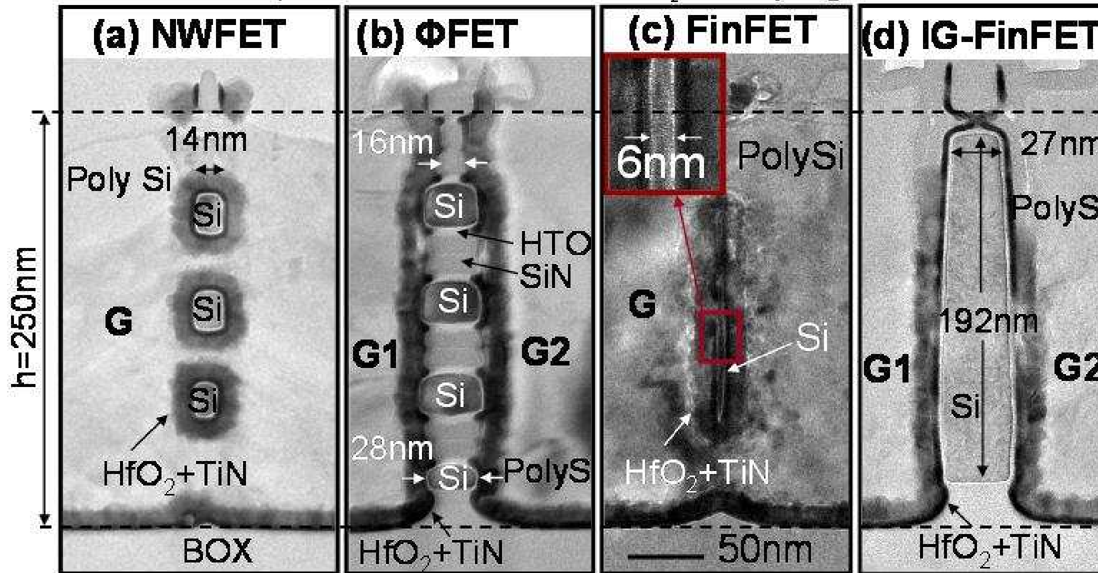
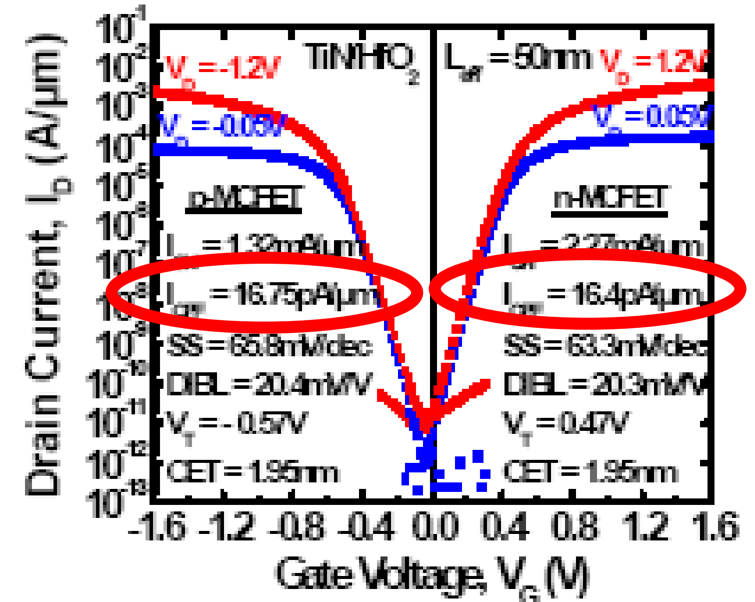
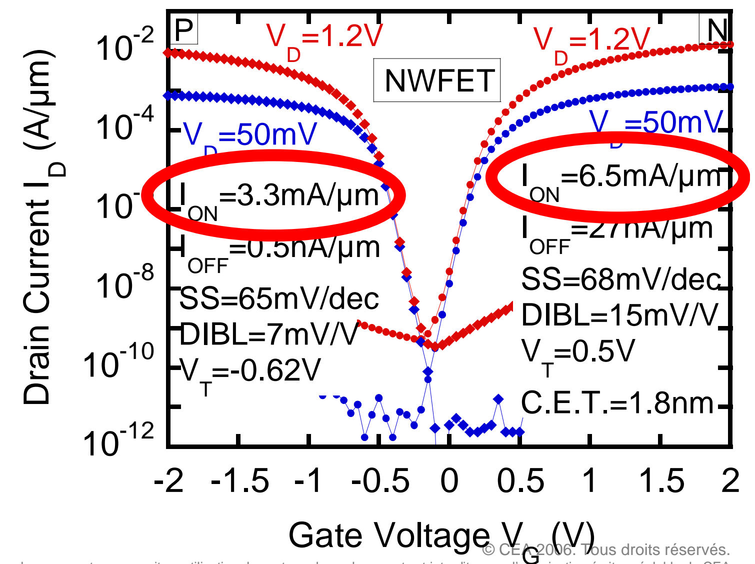
Stacked Multichannels and MultiNanowires « Top-Down » approach







LETI top down approach for Low Power and High performance

- CV/I outperforms Planar in loaded environment
- Improved voltage gain (8GHz) wrt Planar
- Gate separation possible

LETI: Dupré et al. IEDM 2008, San Francisco(CA)
Ernst et al., Invited talk IEDM 2008, San Francisco(CA)
Bernard et al, VLSI Symposium 2008 Honolulu
K.Tachi et al., IEDM 2010, San Francisco

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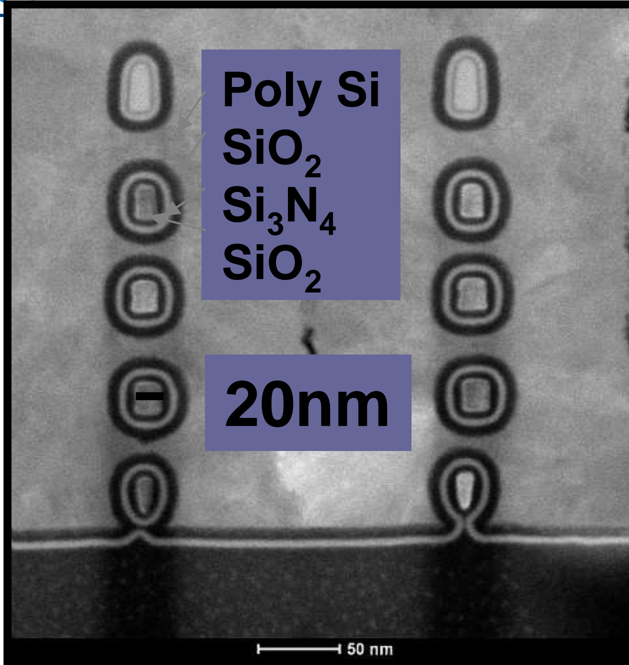
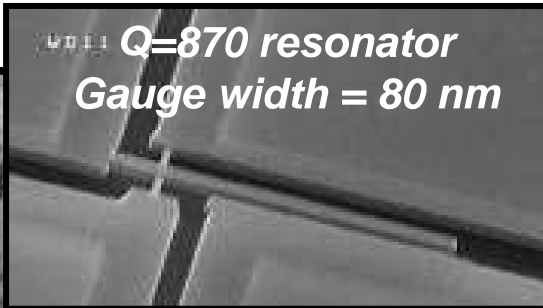
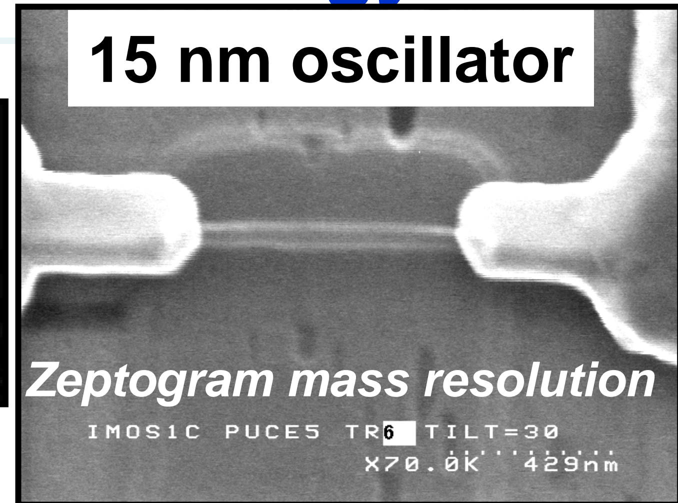
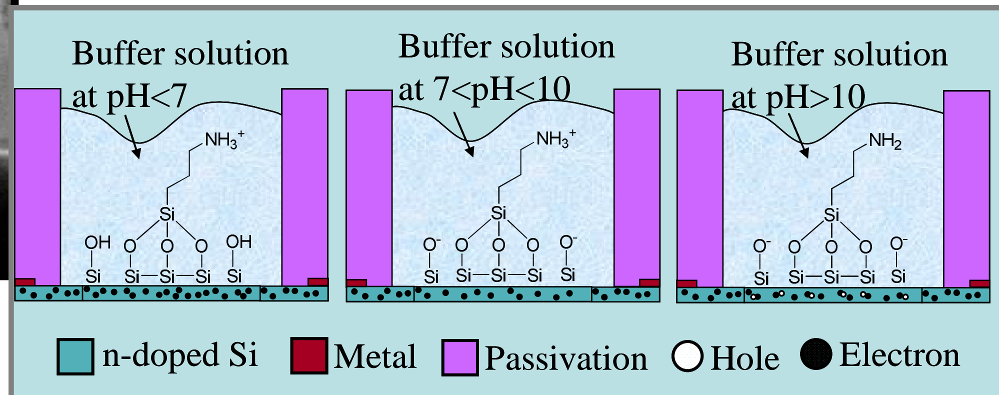
Pervasion of Nanowire technology

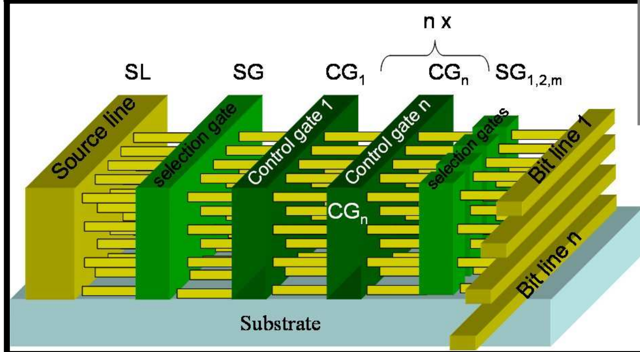
Mass detection



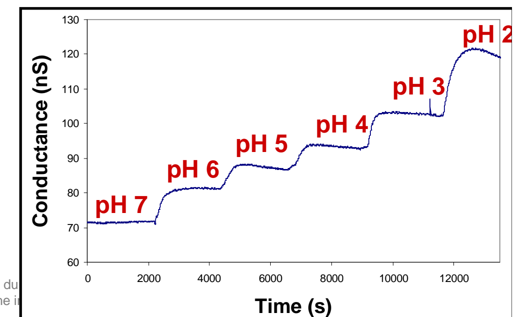








Chemical sensing



3D NAND Flash Memories

T.Ernst et al., IEDM 2008
Hubert et al., IEDM 2009

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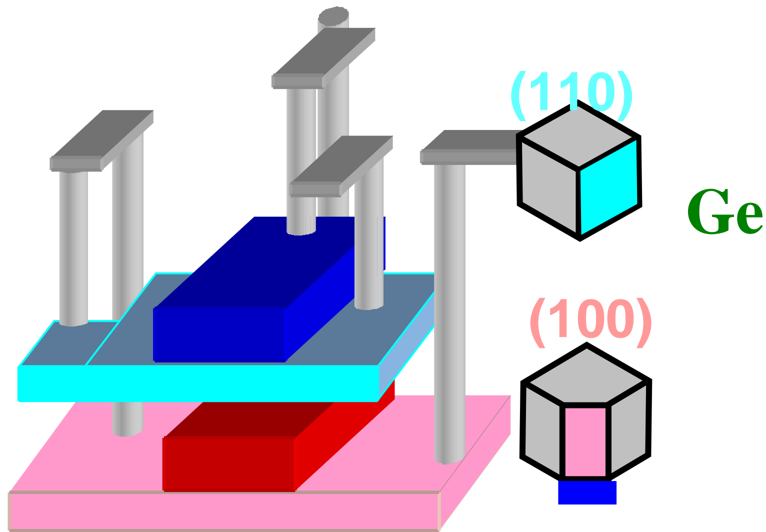
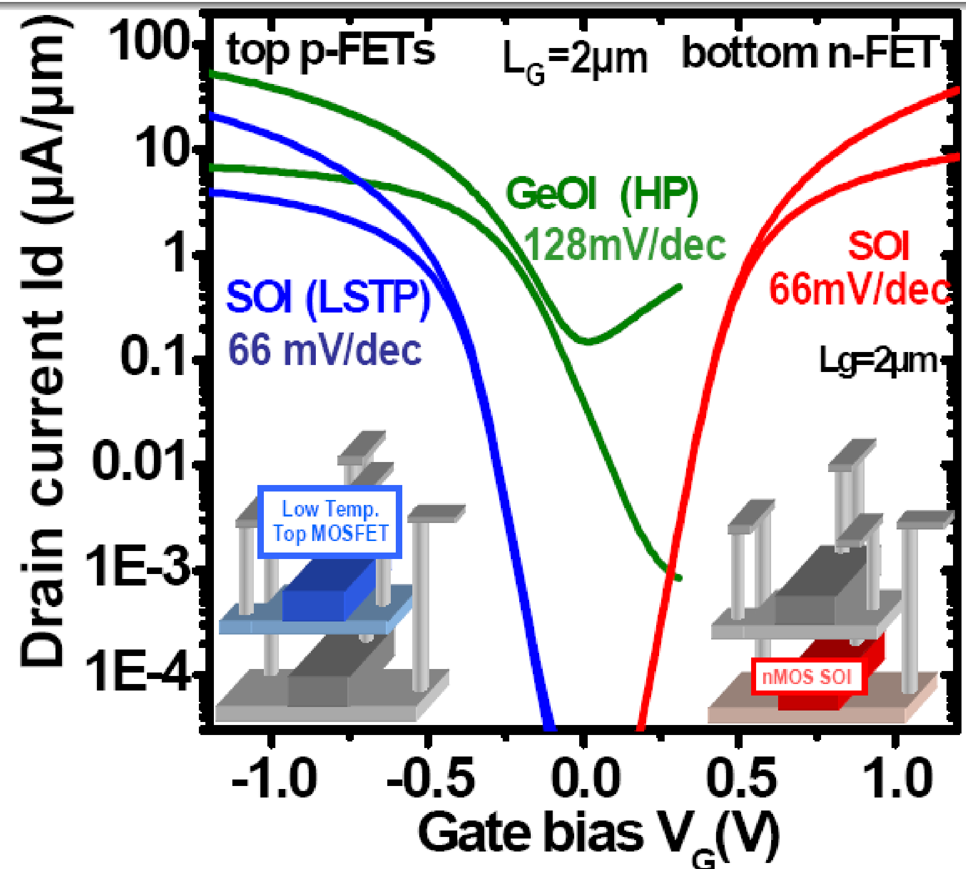
3D sequential process

Co-Integrating Heterogeneous orientation or materials





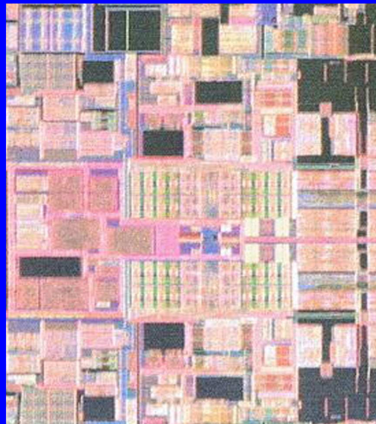
-4T SRAM
- cold end process(bonding).
Opportunities for other SC(Ge,III-V,...)
- improved layout (40% area SRAM cell)
-dynamically controlled VT:
improved RNM and SNM

P.Batude et al., Best student Paper Award, IEDM 2009

First heterogeneous orientation in 3D Si sequential integration
Enabled by use of wafer bonding by keeping low thermal budget

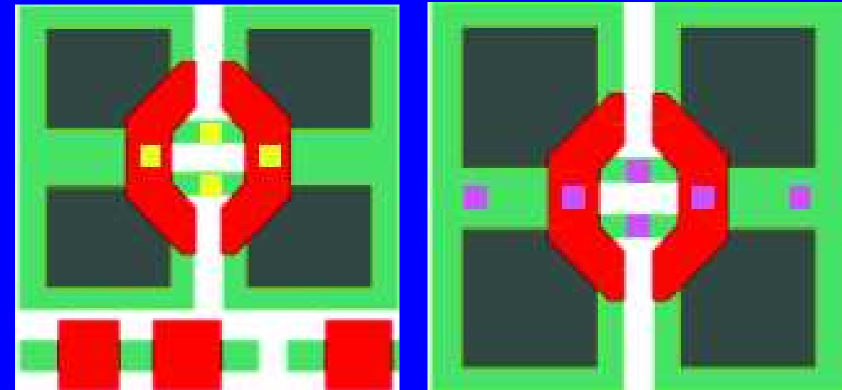
Sequential 3D: Potential and Demonstrated Applications

High density logic applications



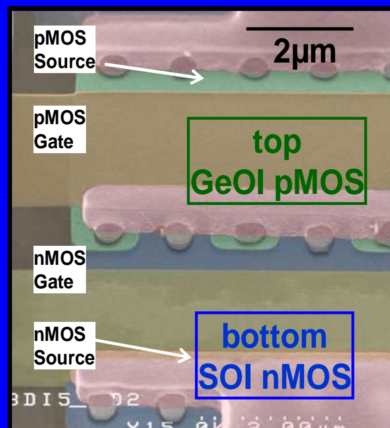
~ 1 node gain with same design rules for Front end levels

Highly miniaturized CMOS imagers pixels



P. Coudrain et al, IEDM 08,

Heterogeneous integration

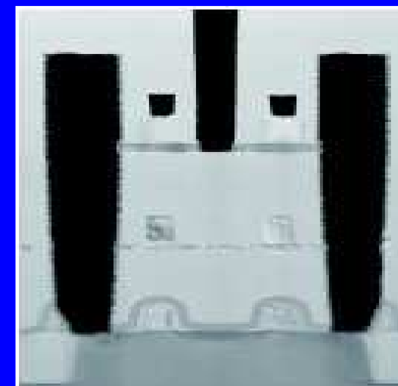


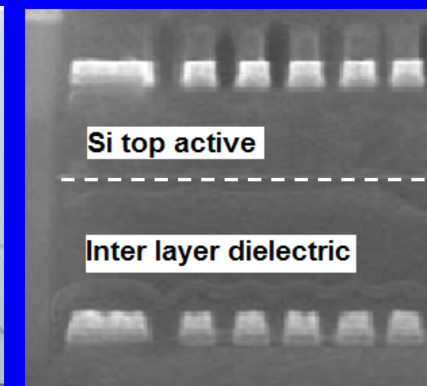
P. Batude et al,VLSI09

- Nanoelectronics & Photonics applications with Si-Ge Co-integration
- SRAM on top SOI logic, I/Os, analog on bottom bulk
- …

3D memories

- SRAMs
- FLASH

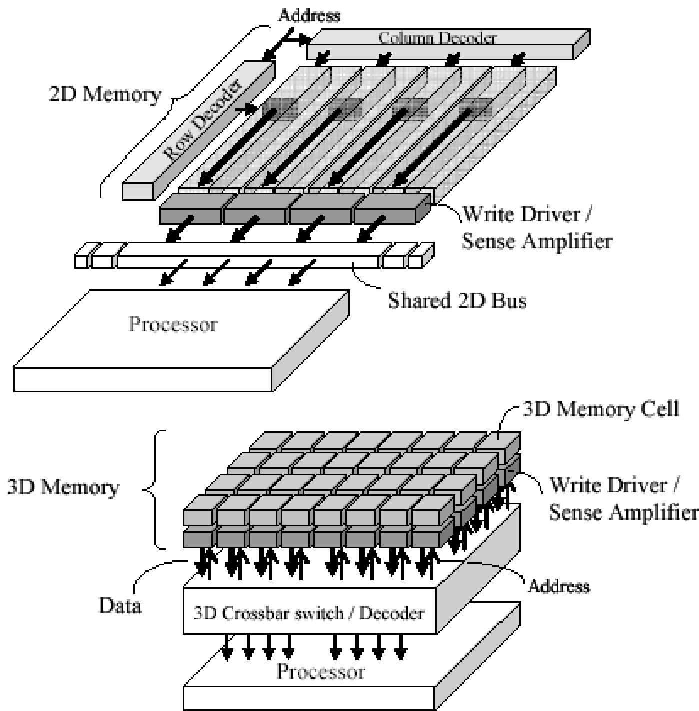


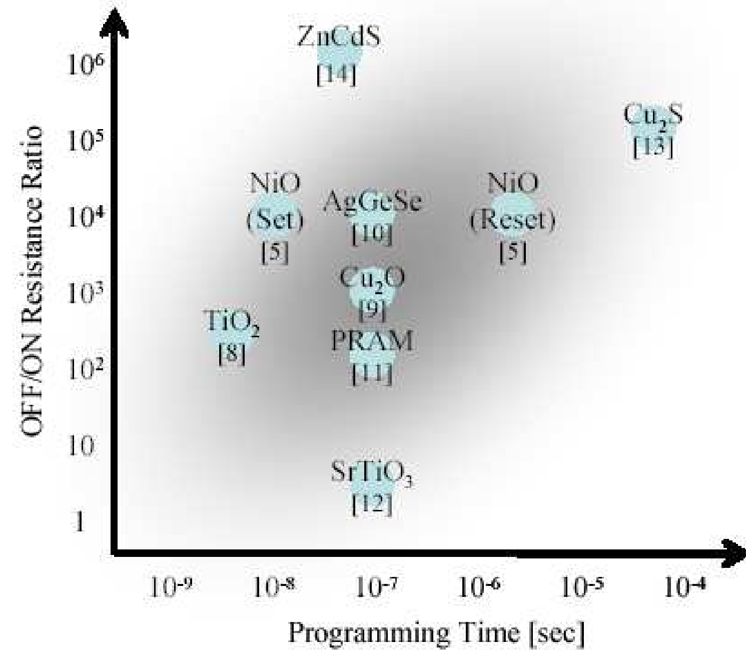


Y-H. Son et al, VLSI 07, Jung et al, IEDM 2006

P.Batude et al., IEDM 2009, Best Student Paper Award

3D-Xbar Memory stacked on Logic: towards NV Logic





Resistive switches

Toshiba, Stanford Univ.: K.Abe et al, ICICDT 2008

proven in 2D with
Magnetic Tunnel Junctions,
FeRAM ***Tohoku Univ., Hitachi: S.Matsunaga et al., Appl.Phys. Express(2008); ROHM***

Logic + Stacked NVM:
- High bandwith,
- Reduced Power consumption,…
- Reconfigurability
- ex: 32 nm node : > 1TB/s per 1mm^2

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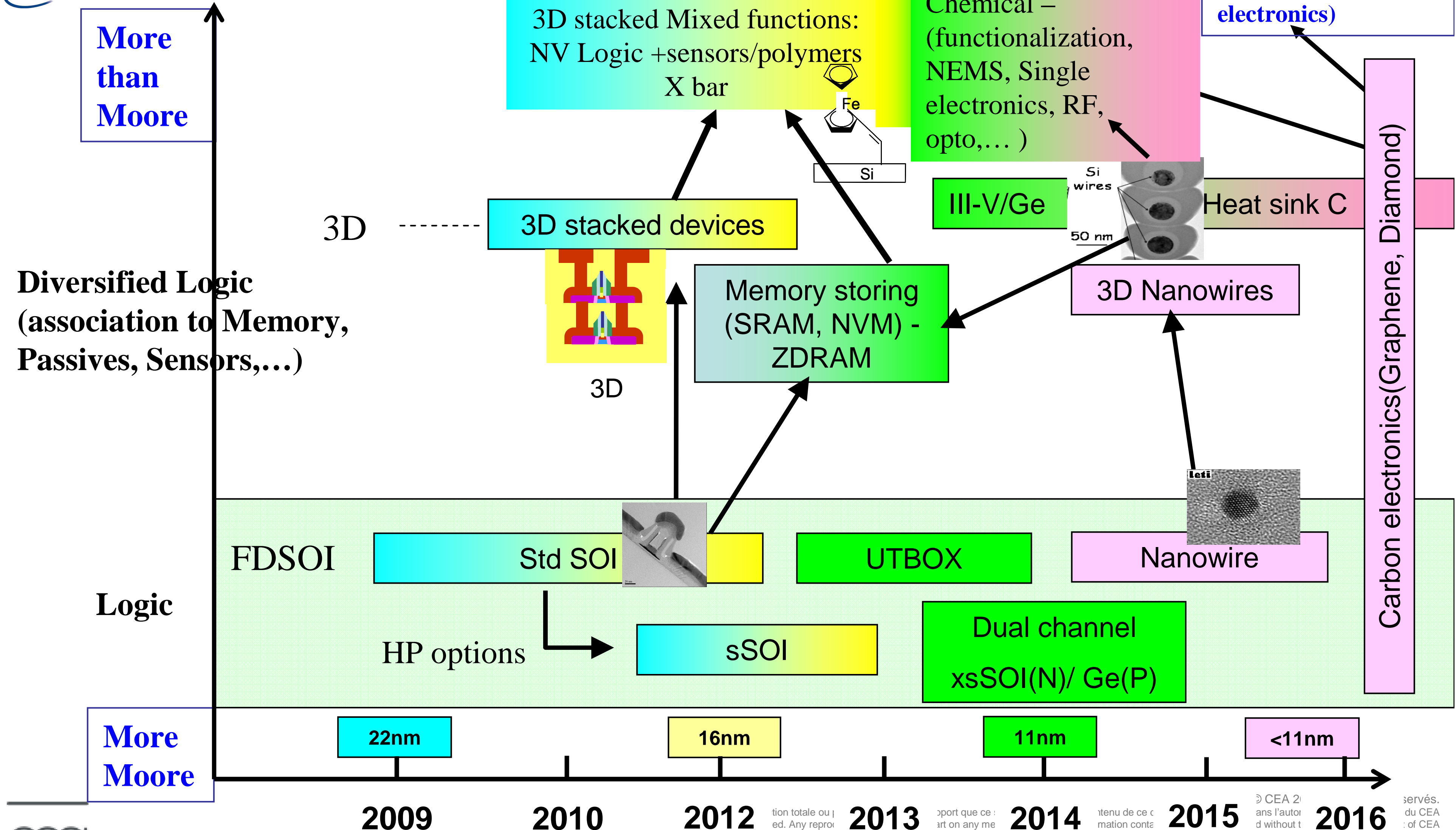
Advanced Devices and Systems Future Vision



Outline

- Introduction : Trends and Hot Topics in Nanoelectronics
- Nanoelectronics scaling and use of the 3rd dimension to continue Moore's law.
- Interfacing the Multiphysics World (More Than Moore) thanks to functional diversification
- Building new systems and their packaging with a 3D tool box at a wafer level.
- Conclusions

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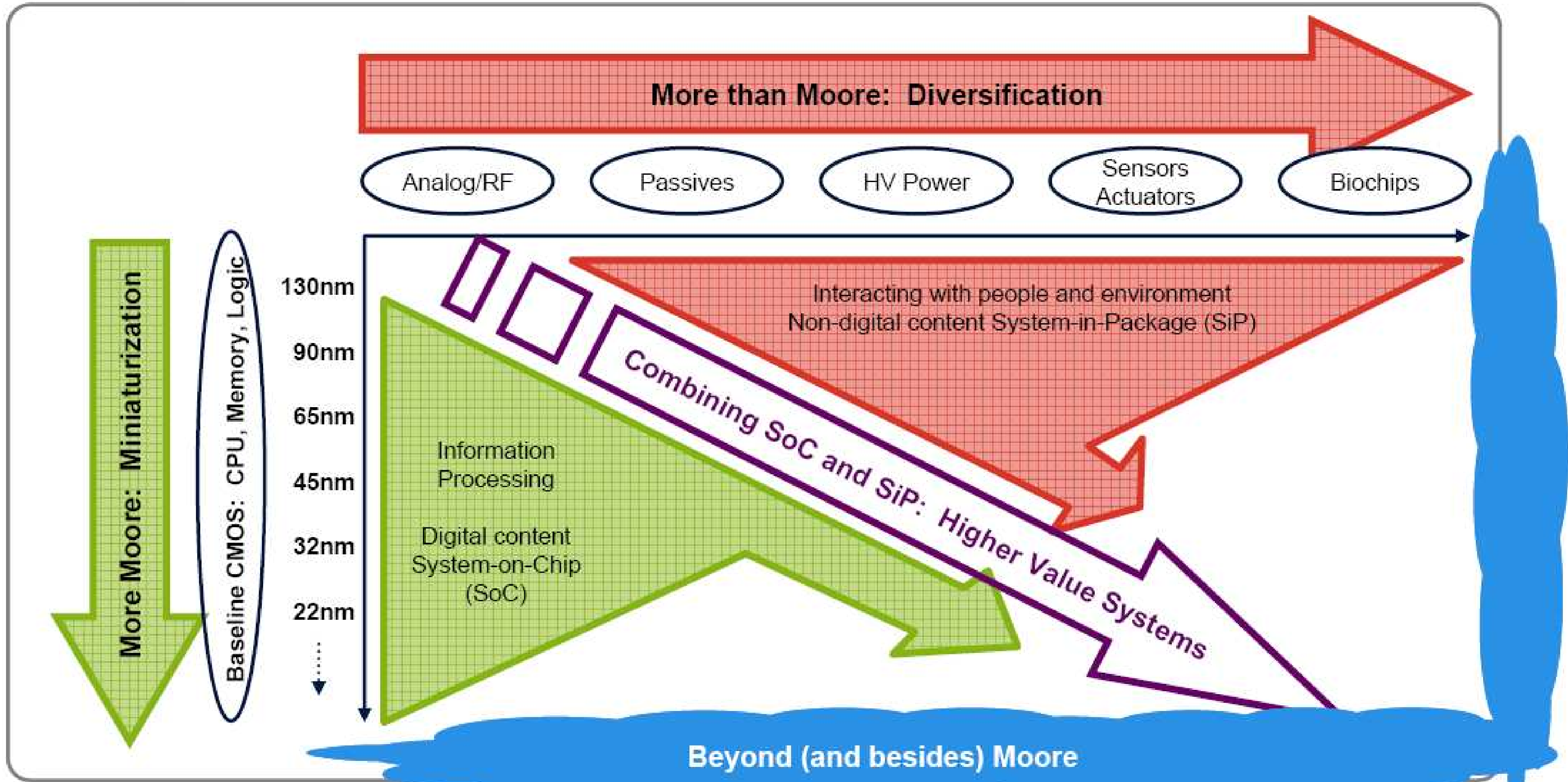
« More, More than, Beyond Moore »

Tomorrow’s top added value markets



High growth with ‘More than Moore’ technologies:
they require **expertise** in all technical domains and in-depth knowledge of the targeted markets *ITRS 2009*

niac

ITRS

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NEMS scaling laws: is it worth?

- resolution increases
- sensitivity decreases (SBR,SNR) => arrays, actuation,…
- figures of merit pressure and vacuum quality dependent

$$\delta m = \frac{M_{eff}}{Q} \cdot 10^{-(DR/20)}$$

$$DR \propto \sqrt{\frac{\sum S_{noise}}{P_{act}}} = \frac{1}{SNR}$$

ML Roukes et. al. APL (2005)

Parameter	Scaling rule
mass	k^3
stiffness	k
resonant frequency	k^{-1}
mass responsivity	k^{-4}
energy consumption	k^3 [rough estimate]

$$M_{eff} \propto l \cdot w \cdot t$$

$$\kappa_{eff} \propto w \cdot \frac{t^3}{l^3}$$

$$f_0 \propto \sqrt{\frac{\kappa_{eff}}{M_{eff}}} \propto \frac{t}{l^2}$$

$$\Re = \frac{\partial f_0}{\partial M_{eff}} = -\frac{f_0}{2M_{eff}}$$

$$E_P \approx \frac{1}{2}\kappa_{eff} \cdot x_{Max}^2$$

and $x_{Max} \propto t$

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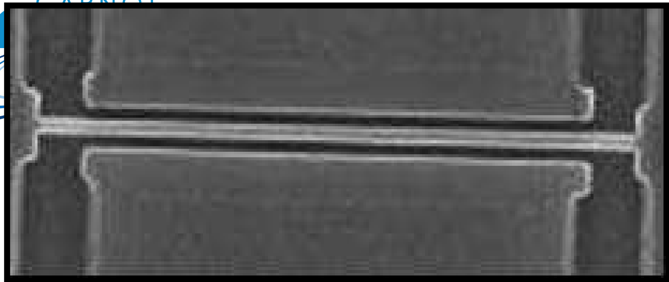
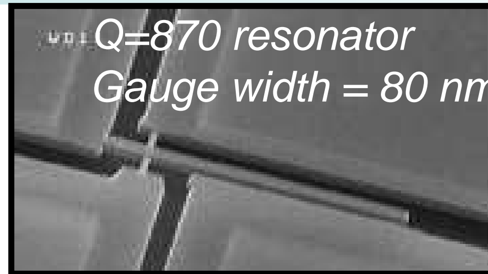
Nanowire used for mass detection

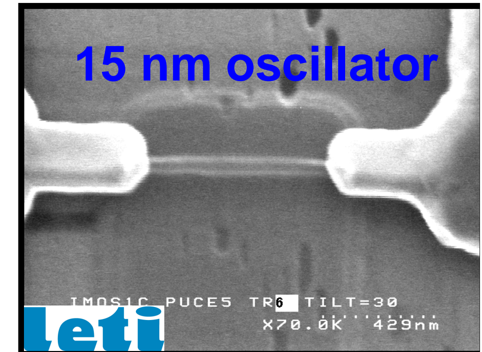


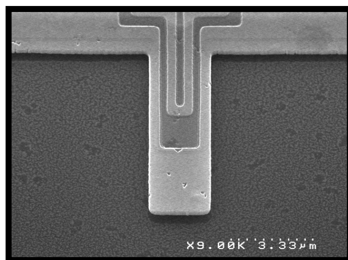
Capacitive actuation & detection



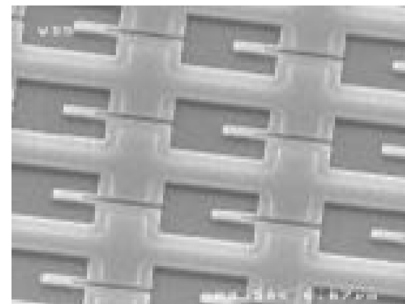
Capacitive actuation & piezo-resistive detection with nanowires

$$\delta m \approx 0.5 \ zg / \sqrt{Hz}$$

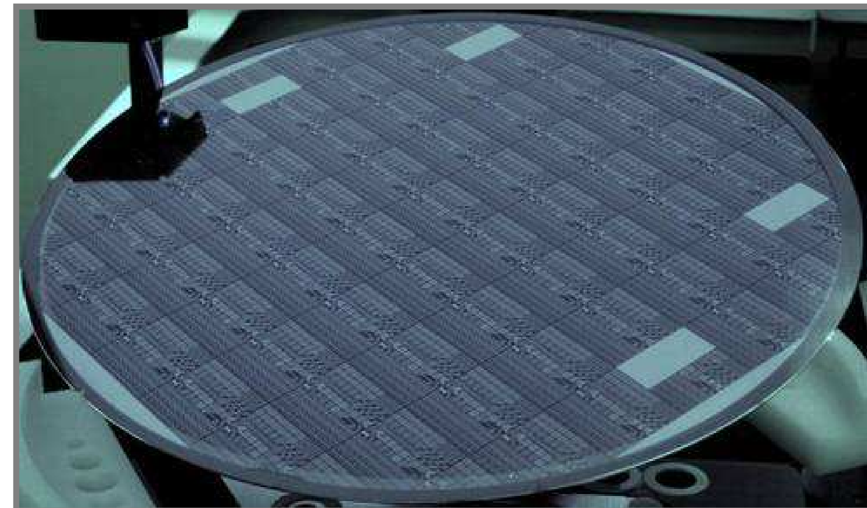




Thermo-elastic actuation & piezo-resistive detection.



NEMS array



leti

- First 200 mm wafers with 3.5 millions NEMS

- Same process as MultiNanowires CMOS NWFET

LETI: T.Ernst et al., IEDM 2008, Invited talk
L. Duraffourg et. al, APL 92, 174106 (2008)
E Mille et al, Nanotechnology, 165504, (2010)

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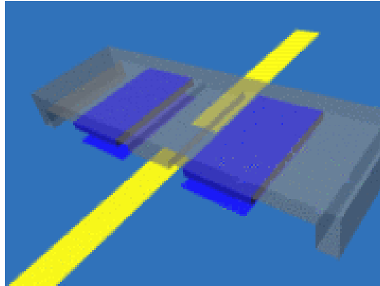
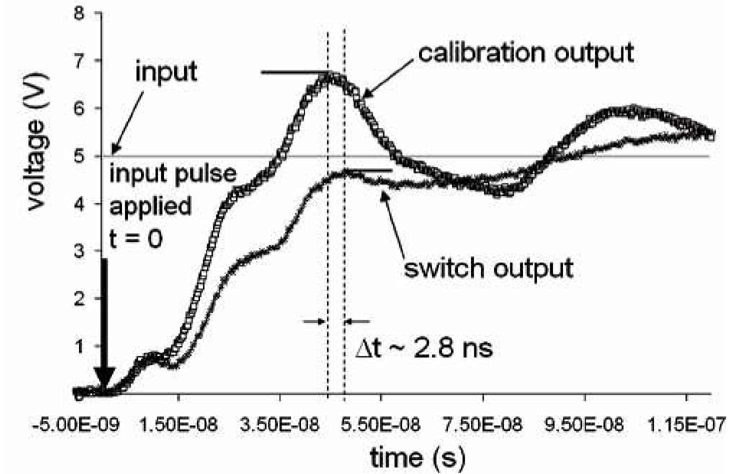
NEMS switch

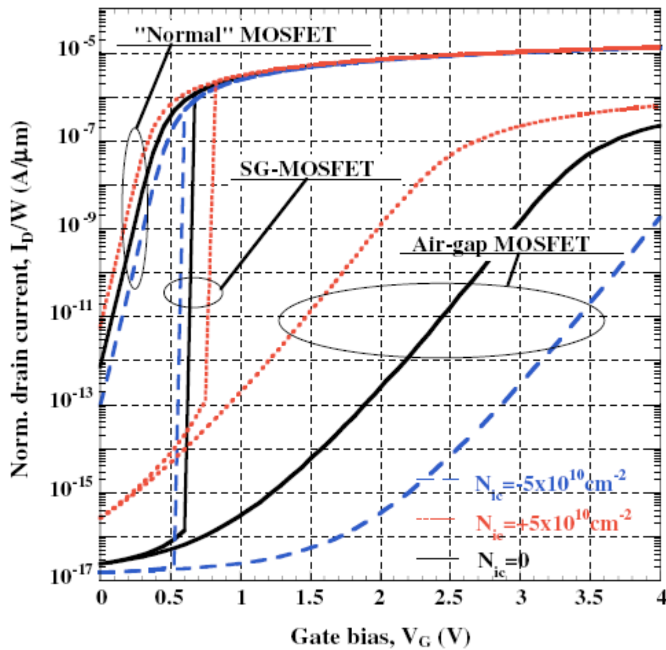


“high” speed

rf



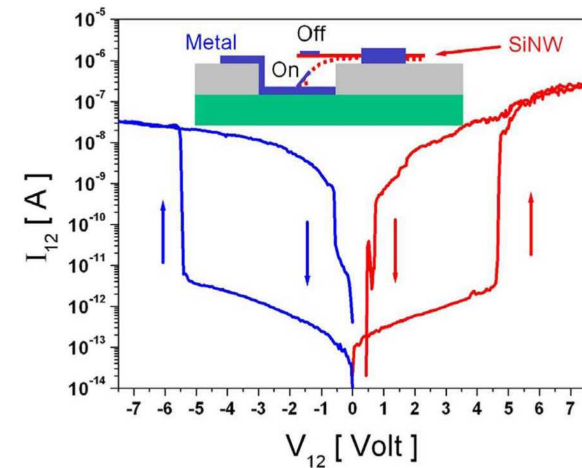
from AB. Kaul et al., Nano Letters 6(5) 942-947 (2006)



from D. Tsamados et al. Solid-State Elec. 52 1374 (2008)

bistable

memory



from Q.Li et al.,IEEE Nano 6(2) 256-262 (2007)

high on/off ➡ low power logic

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• Conclusions

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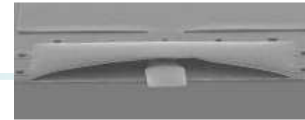
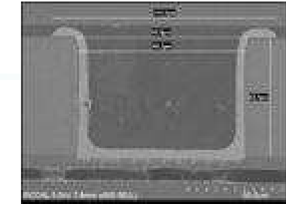
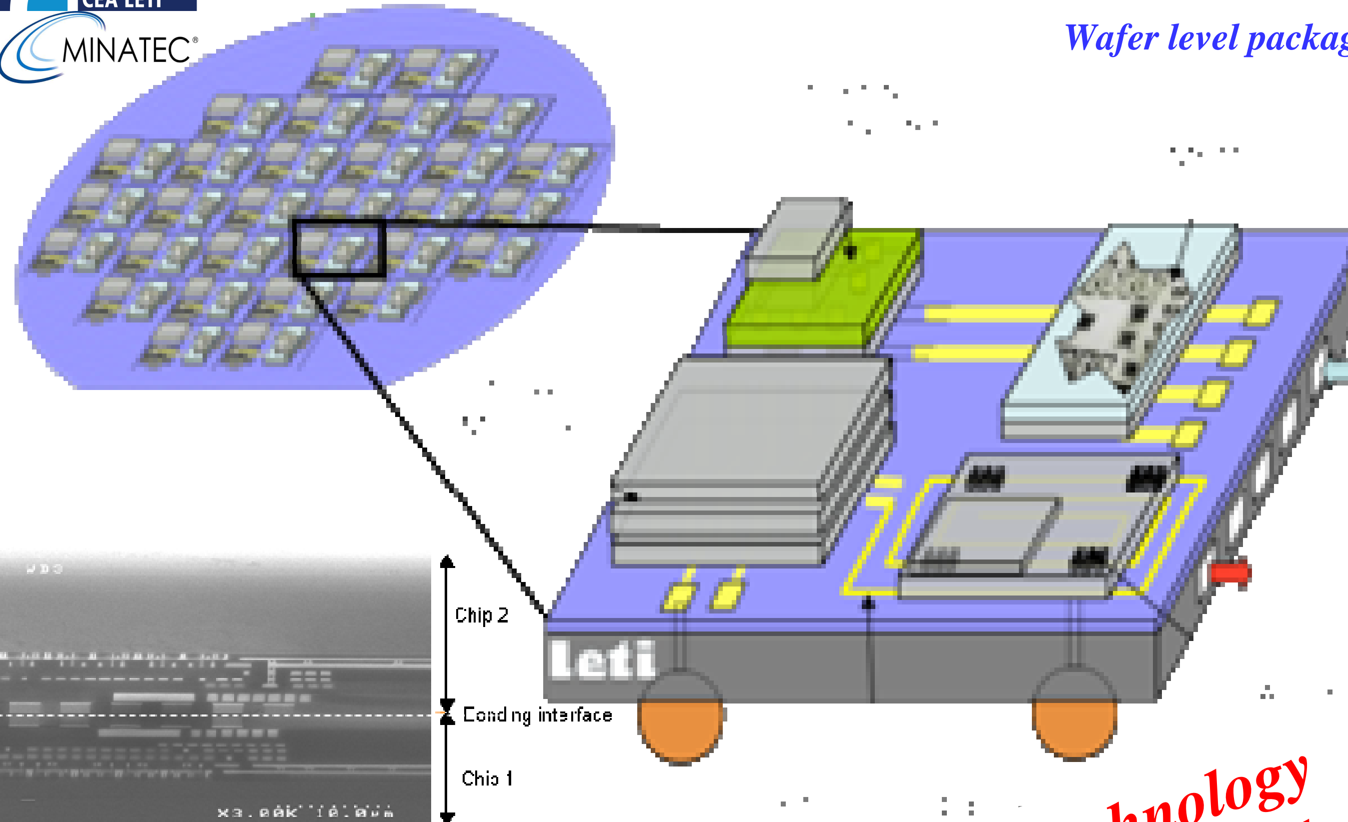
System On Wafer.

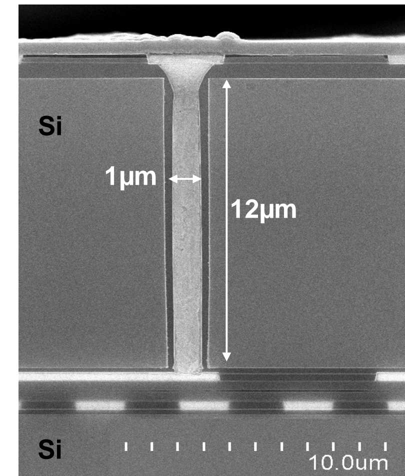


Wafer level packaged MEMS

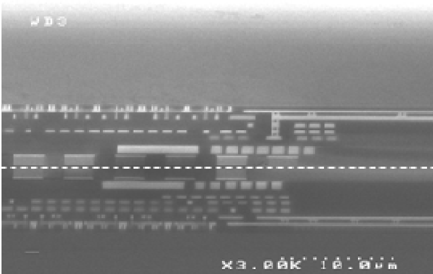


80 µm diameter TSV imagers packaging

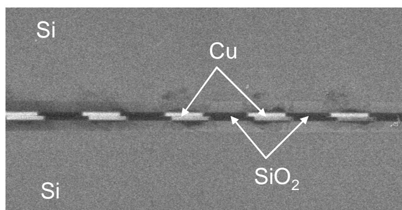




1 µm diameter
High AR TSV stacked ICs



Oxide/Oxide bonding



Copper/Copper bonding

Via belt technology
MEMS + IC stack
Ultra flat 3D
Chip stacking(TSV)
Active Silicon interposer

H... On Silicon
...ount
...level

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3D Integration: from imagers to advanced 3D ICs

ST – LETI collaboration

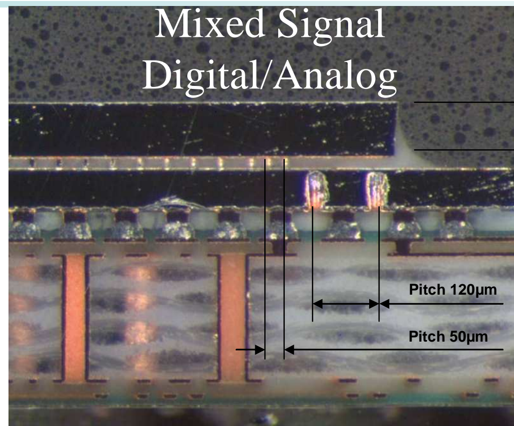
2001

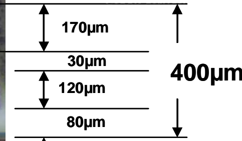
2008

with TSV

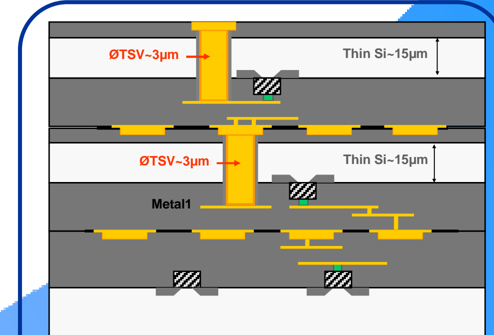
VGA cameras (300kpixels)

Image-on-Board





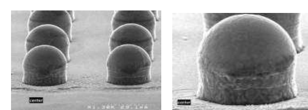
ST – LETI collaboration



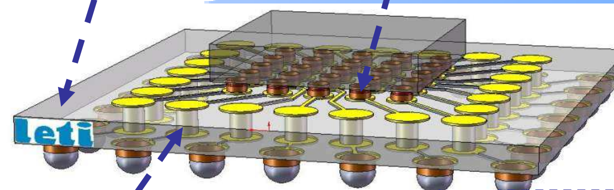
3D-IC

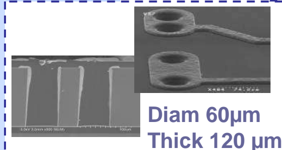
Memory, Processors, Imagers with high density TSV, NEMS…

Thinned wafer (~100 µm)



Die to Die Copper pillars





Diam 60µm
Thick 120 µm

Via Last TSV (Aspect Ratio 2-3)

Die to substrate copper pillars

Active Silicon interposer

3D high density

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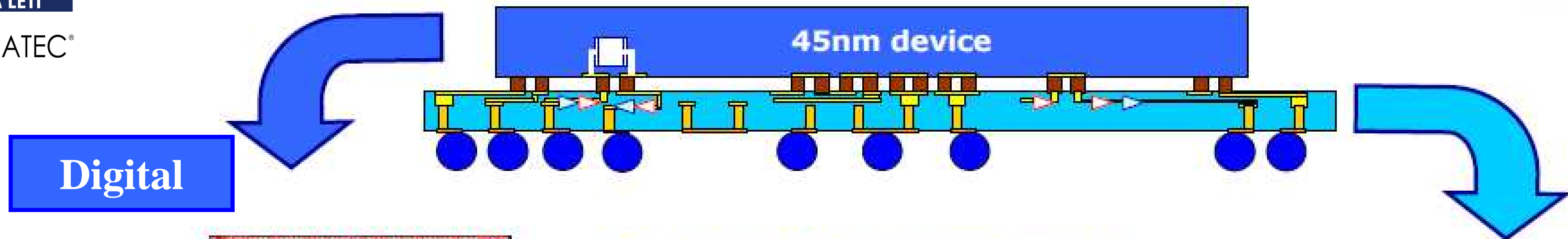
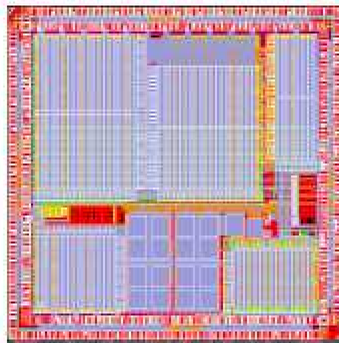
Digital on Analog: the first 3D demo

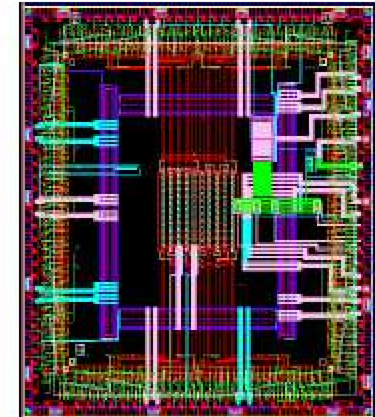


Digital



CMOS 45nm, 25 mm²

- TSV for top and bottom chips access
- Daisy chains & delay chains with F2F, TSV and RDL paths
- Voltage regulator driving a 45nm IP
- Mechanical stress sensors
- Thermal sensors
- IO boundary-scan

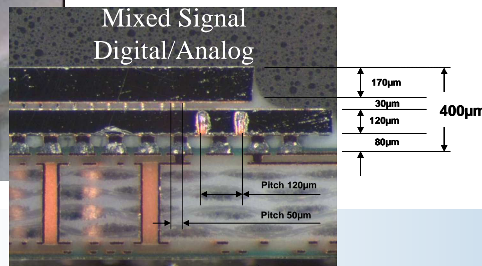


Active interposer, CMOS 0.13µm 32mm²

Analog

– Techno partitioning
– Best IP in best techno node
– Performance & Time to market
– Better scalability

•1056 inter-chip connections
•588 TSV's
•482 bumps
•In BGA 864 lead free balls, 1.0 mm pitch



By courtesy: D43D Workshop - 3D Integration program – P. Ancey Lausanne – 2010, May 27th-28th

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3D Roadmap: Overview of architectures

INSTITUT CARNOT CEA LETI

MINATEC

ITRS 65nm 45nm 32nm

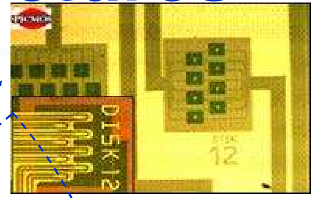
2007 2009 2012 >2014

Low density 3D via Chip-level bonding

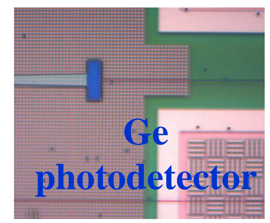
High density 3D via wafer-level bonding

Vertical device on CMOS (NTC, NW, NEMS)

Optical Interconnects

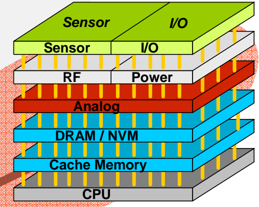


InP/SOI µ-laser 1.6µm 0.5mA



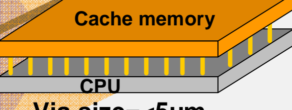
Ge photodetector

Cross talks:
-delay, matching,
-power dissipation
(global temp. increase,
hot spots, reliability, …)



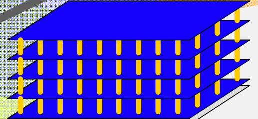
Via size=<2µm

Multi-level 3D IC (CPU + cache + DRAM + Analog + RF + sensor + IO)



Via size=<5µm

Logic (multicore processor with cache memory)

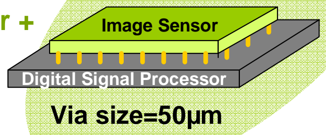


Via size=5-30µm

3D Stacked memory (NAND, DRAM, …)

100% filled via

CMOS Image sensor (Sensor + DSP + RAM)



Via size=50µm

Targets for MEDEA+ project

Vertical Interconnect Density (cm^{-2}): 1, 10, 1E2, 1E3, 1E4, 1E5, 1E6, 1E7, 1E8, 1E9

Vertical 3D via pitch (µm): 1000, 100, 10, 1, 0.1

Flip chip solder bump min pitch

ITRS C65nm min Global metal pitch

ITRS C65nm M1 min pitch

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Conclusion :Nanoelectronics CMOS from Devices to Systems Perspectives

- Si CMOS: Nanoelectronics Base platform beyond ITRS
- Durable Low Power solutions:
  health, environment, quality of life, energy, IST,…
- Low Power consumption: major challenge (sub 1V VDD CMOS).
  => Device/ system architecture optimization:
  Thin Films Gate All Around nanowires, low slopes,layout, 3D
  => Opportunities for new materials on Silicon
  (Ge, revised low BG III-V, Carbon,…)
- Heterogeneous 3D co-Integration on Si, Low Power:
  Monolithic/Sequential 3rd dimension in device. New active materials
  Reconfigurabilty with NVM ; NV Logic
  System On Wafer: 2 to 3D heterogeneity functions & chips

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Acknowledgements

Professors H.Iwai(TokyoTech) and WIMNACT 26 organizers

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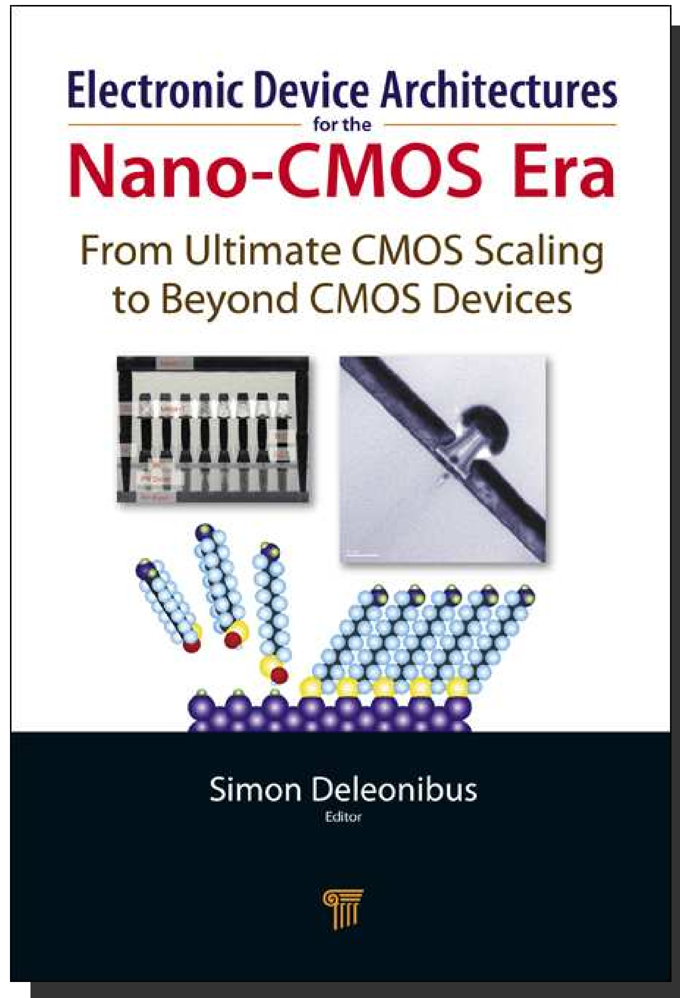

Electronic Device Architectures for the Nano-CMOS Era

From Ultimate CMOS Scaling to Beyond CMOS Devices

edited by **Simon Deleonibus** (*CEA-LETI, France*)

Cloth July 2008 978-981-4241-28-1

★ Discusses the scaling limits of CMOS, the leverage brought by new materials, processes and device architectures (HiK and metal gate, SOI, GeOI, Multigate transistors, and others), the fundamental physical limits of switching based on electronic devices and new applications based on few electrons operation

★ Weighs the limits of copper interconnects against the challenges of implementation of optical interconnects

★ Reviews different memory architecture opportunities through the strong low-power requirement of mobile nomadic systems, due to the increasing role of these devices in future circuits

★ Discusses new paths added to CMOS architectures based on single-electron transistors, molecular devices, carbon nanotubes, and spin electronic FETs

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