IEEE EDS Mini-colloquium on NAnometer CMOS Technology: (WIMNACT 26)

Sponsored by IEEE EDS Japan Chapter
Co-sponsored by Global COE Photonics Integration-Core Electronics (PICE), Tokyo Institute of Technology, Tokyo Institute of Technology
Co-sponsored by Frontier Research Center

Organization:
General Chair:　Shin-ichiro Kimura, Chair, IEEE EDS Japan Chapter
Program Chair: Hiroshi Iwai, Tokyo Institute of Technology
Publicity Chair: Kazuo Tsutsui, Tokyo Institute of Technology
Publication Chair: Kuniyuki Kakushima , Tokyo Institute of Technology
Local Arrangement Chair, Parhat Ahmet, , Tokyo Institute of Technology

Place: Meeting room, 2nd floor, Frontier Research Center, Tokyo Institute of Technology, Yokohama, Japan

Date: February 9, 2011
12:20-12:25 Opening
12:25-12:35 Introduction of IEEE EDS,
　　Sinichiro Kimura, Chair, EDS Japan Chapter
12:35-12:50 Introductory talk, Future of Nano CMOS Technology:
　　Hiroshi Iwai, Tokyo Institute of Technology
12:50-13:35 The future of Nanoelectronics by Scaling of CMOS and Functional Diversification:
　　Simon Delelonibus, Leti
13:35-14:20 SOI opportunities to speed up, save energy and memorize:
　　Sorin Cristoloveanu, IMEP, Grenoble Polytechnic Institute
14:20-15:05 The Case for Modeling and Simulation:
　　Claudio Fiegna,　University of Bologna
15:05-15:30 Coffee Break
15:30-16:15 Advanced simulation of nanotransistors:
　　Francisco Gamiz,　University of Granada
16:15-17:00 Methods for Improving Electrical Properties of La2O3-based Gate Dielectric Films:
　　Hei Wong, City University of Hong Kong
17:00-17:45 Memory Effects in SOI-FinFET with ONO Buried Insulator:
　　Jong-Hyun Lee, Kyungpook National University
17:45-18:00 Closing Talk, Nano-Electronic Devices based on Silicon MOS Structure:
　　Chandan Sarkar, Jadavpur University