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Effects of $In_{0.53}Ga_{0.47}As$ Surface Preparation on Electrical Characteristics of MOS Devices

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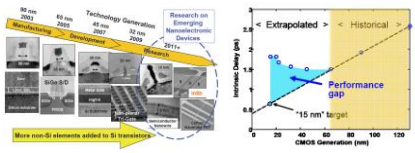
Background

Limits of Si



Points of Improvement:

1 Switching speed 2 Density 3 Power

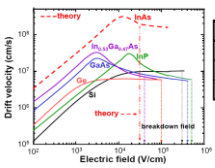
22nm node and below

Parasitic charge interference with channel charge → **Gate delay increases** $C_{ox} \cdot V_{CC}/I_{ON}$

Increasing carrier mobility can increase the drive current at low bias voltage to reduce the gate delay

Si replacements are considered for 15nm node and beyond

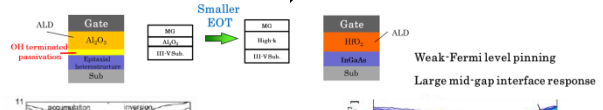
High Mobility Material

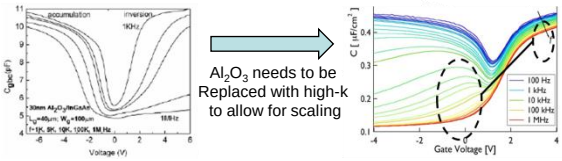


Parameter	Units	Material				
		Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
μ_e at n_i=1E12 cm^{-2}	$cm^2/V.s$	300	7,000	10,000	15,000	30,000
bulk μ_n	$cm^2/V.s$	450	400	200	460	1,250
E_g	eV	1.11	1.43	0.7	0.36	0.17

In-rich content reduces the band-gap thus carriers can accumulate in the channel at lower voltages

→ **Less power consumption**





Al_2O_3 needs to be Replaced with high-k to allow for scaling

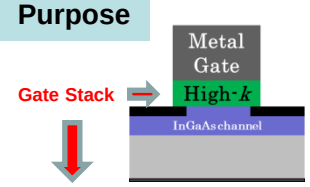
gate stack high-k requirements

- Thermal stability
- Sufficient band offset with semiconductor conduction band
- Low interface trap density

■ Extremely challenging to reduce D_{it}

Low fermi-level response
Frequency dispersion, high SS, Low drive current

Purpose



Optimizing high-k/$In_{0.53}Ga_{0.47}As$ interface for improved electrical properties

Surface treatment prior to high-k deposition

- S passivation
- Monolayer Si coating

Deposition and annealing condition investigation

Experimental Method

W
High-k Oxide
Sub.

← Various surface treatments

InGaAs / InP Substrate

- HF cleaning (Surface Treatment)
- High-k e-beam deposition

in situ

- Tungsten (W) deposition by sputtering
- Reactive ion etching (RIE) of W gate
- Backside Al contact
- Annealing in F.G

XPS analysis

Electrical characterization

Results

Optimizing Surface

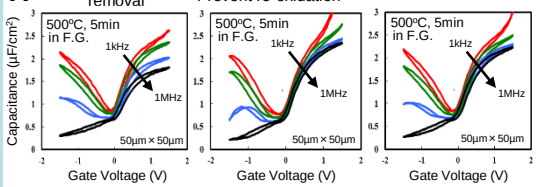
Surface wet-treatment

(I)

1-Concentrated HF treatment — Native oxide removal

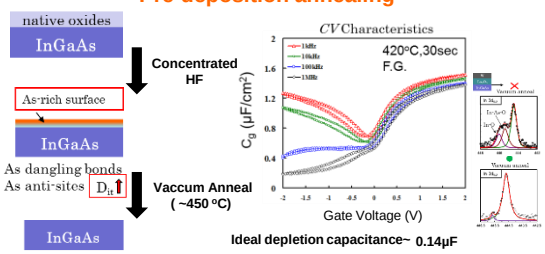
2-$(NH_4)_2S$ treatment — S-terminated Prevent re-oxidation

3-HMDS vapor coating — Mono-layer Si coating



(II)

Pre-deposition annealing



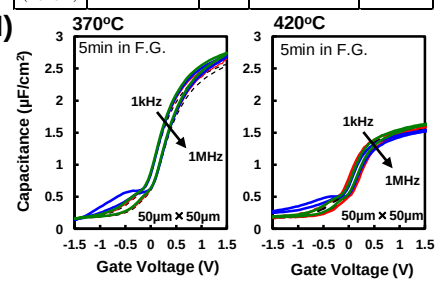
Ideal depletion capacitance~ 0.14μF

(doping level: 9×10^{16})

Deposition conditions

sample condition	pre-depo	depo		
	V.A. at 450°C for 30min	100°C	100°C in oxygen ambient (10^{-4} Pa)	300°C
Sample I (La_2O_3~16 nm)		✔		
Sample II (HfO_2~16 nm)	✔	✔		
Sample III (HfO_2~8 nm)	✔		✔ (>0.5 nm)	✔ (<0.5 nm)

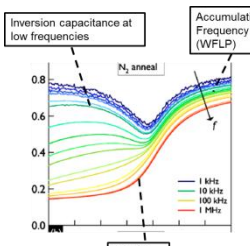
(II)



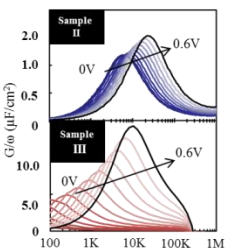
Accumulation and inversion frequency dispersion reduction

Discussion

Interface States Issues

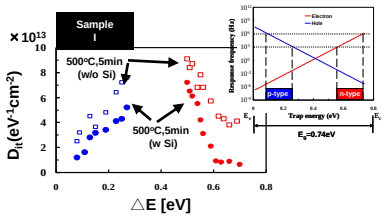


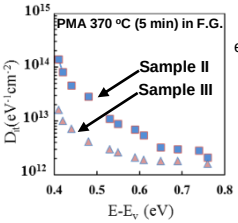
Effective when $C_{ox} > qD_{it}$



C_{ox} needs to increase

Balance between leakage current and C_{ox}





Peak movement is more efficient in sample III at the same voltage range within depletion region.

Effective Mid-gap states reduction

Conclusion

III-V Semiconductor strong candidate for high performance devices

- -high electron mobility (injection velocity)
- -low power dissipation

Major Challenges

- -stable gate stack with unpinned Fermi level interface
- -Modeling interface states for better understanding of their origins
- -low resistance source and drain formation for MOSFET structure

Progress

- -improvement of high-k/semiconductor Interface has been achieved by surface treatment and altering deposition and annealing conditions