Effects of corners of channel cross-section on electrical performance of silicon nanowire field-effect transistors

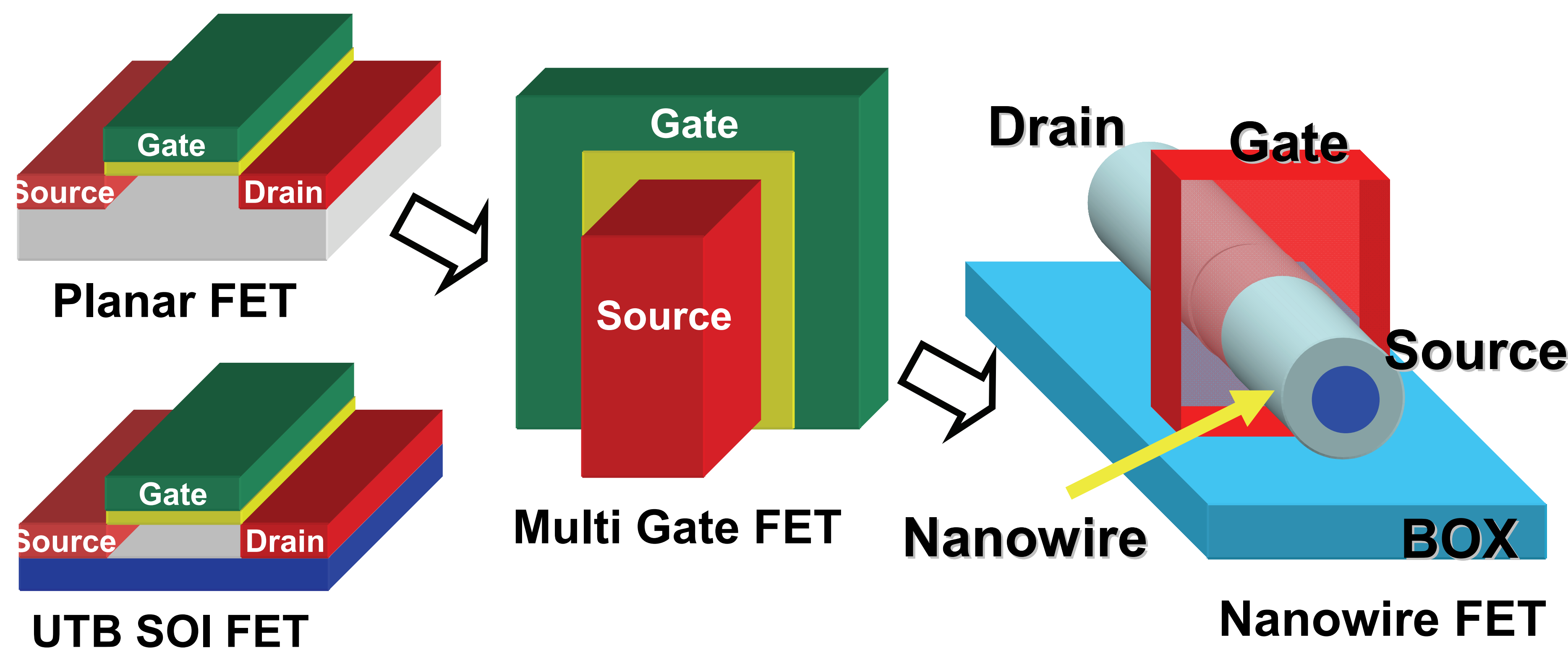
[1] Frontier Research Center, Tokyo Tech.
[2] Interdisciplinary Graduate School of Science and Technology, Tokyo Tech.
[3] Graduate School of Pure and Applied Sciences, University of Tsukuba

*S. Sato[1], K. Kakushima[2], P. Ahmet[1],
K. Ohmori[3], K. Natori[1], K. Yamada[3], and H. Iwai[1]

Outline

- Introduction
- Purpose of this work
- Fabrication process
- Electrical characteristics
  - Transfer and output characteristics
  - Evaluation and analysis of on-current
  - Evaluation of transconductance and $v_{\rm sat}$
- Conclusion

Introduction



- ✓ Immunity against the short channel effect is necessary as the gate length shrinks.
- ✓ Effective electrostatic control of 1-D like narrow channel with the gate all-around structure.
- ✓ Low I_{off} can be achieved with the nanowire structure.
- ✓ A concern of silicon nanowire FET is on-current.

Comparison of channel cross-sectional shapes

Cross-sectional shape	10 nm	10 nm	10 nm	10 nm
Size (h_{NW} x w_{NW}) (nm)	12 x 19	12 x 21	20 x 12	27 x 16
On-Current (μA/μm)	1277	893	861	780
On-Current w/o R_{SD} (μA/μm)	1361	1073	1051	834
R_{SD} (kΩ)	~1.3	~8.2	~7.4	~2.2

*normalized by peripheral length of silicon nanowire channel ** L_g~190 nm

- ✓SiNW nFET with rectangular cross-section had the largest normalized on-current.
- ✓Analysis of on-current of SiNW FET with rectangular cross-section is necessary.

Purpose of this study

- Characterization of SiNW FET with rectangular cross-sections focusing the on-current.

- Analysis of on-current of SiNW FET with rectangular cross-sections.

Fabrication flow based on bulk CMOS process

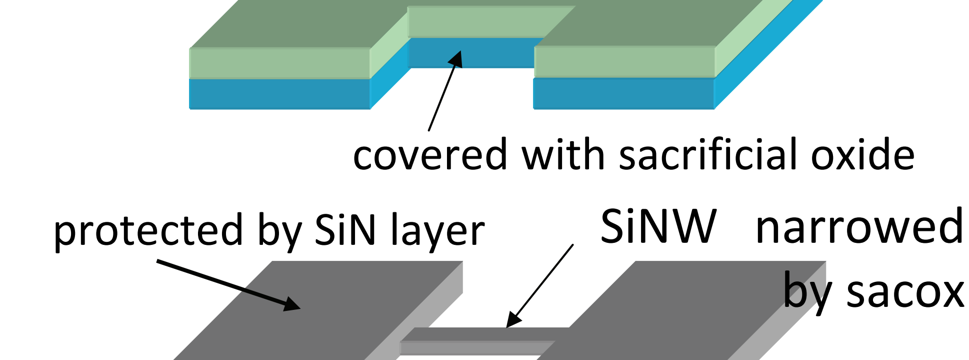
Starting wafer: Silicon-on-insulator (SOI layer 28 nm; BOX layer 50 nm)

✓Fin structure formation
with SiN HM

SiN

SOI

✓Sacrificial oxidation
(in dry oxygen, 1000°C for 1hour)



✓SiN and sacrificial oxide removal

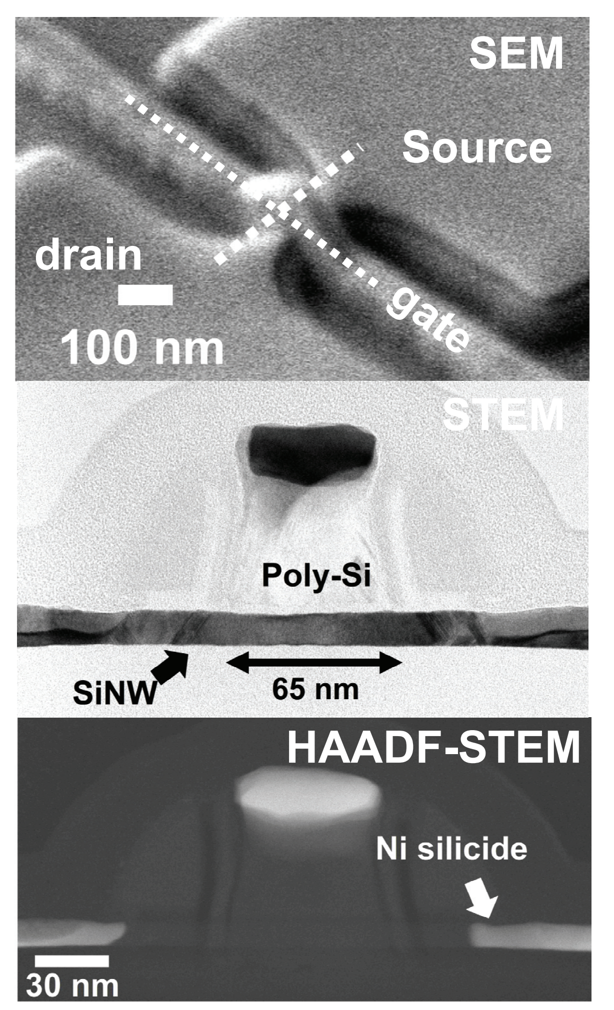
✓Gate oxide (3 nm) and poly-Si (75 nm) depo.

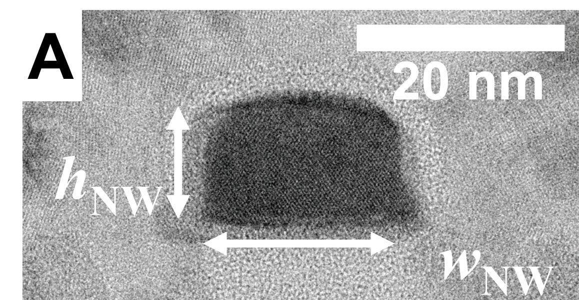
covered by gate oxide and poly-Si

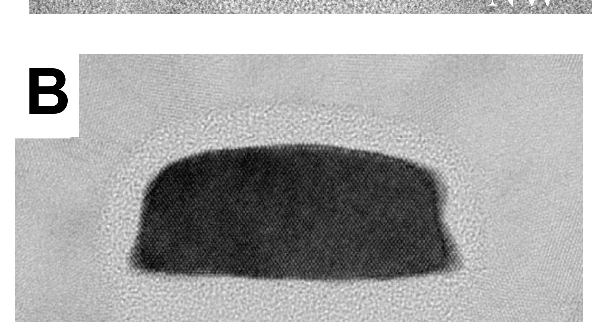
✓Gate pattering
✓Spacer formation & I/I (Phosphorus)
✓Activation annealing
✓Ni SALICIDE process

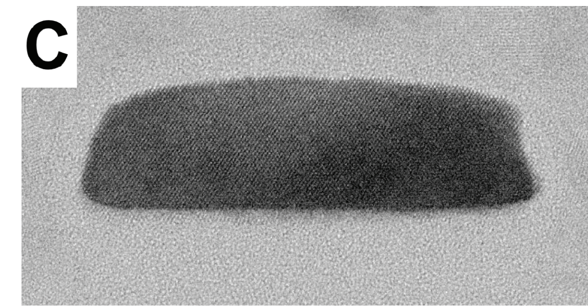
gate electrode
spacer
source
drain

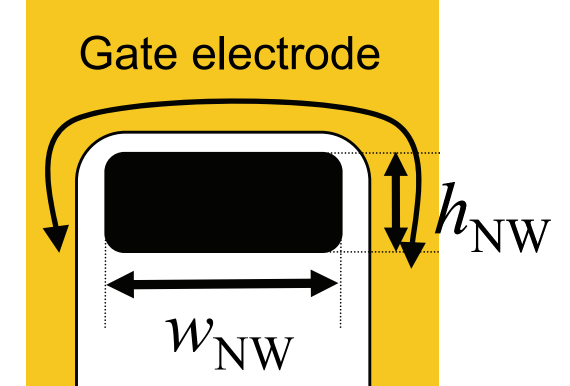
TEM and SEM images of SiNW FET with rectangular cross-sections

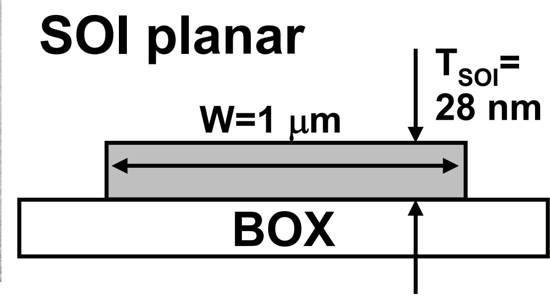






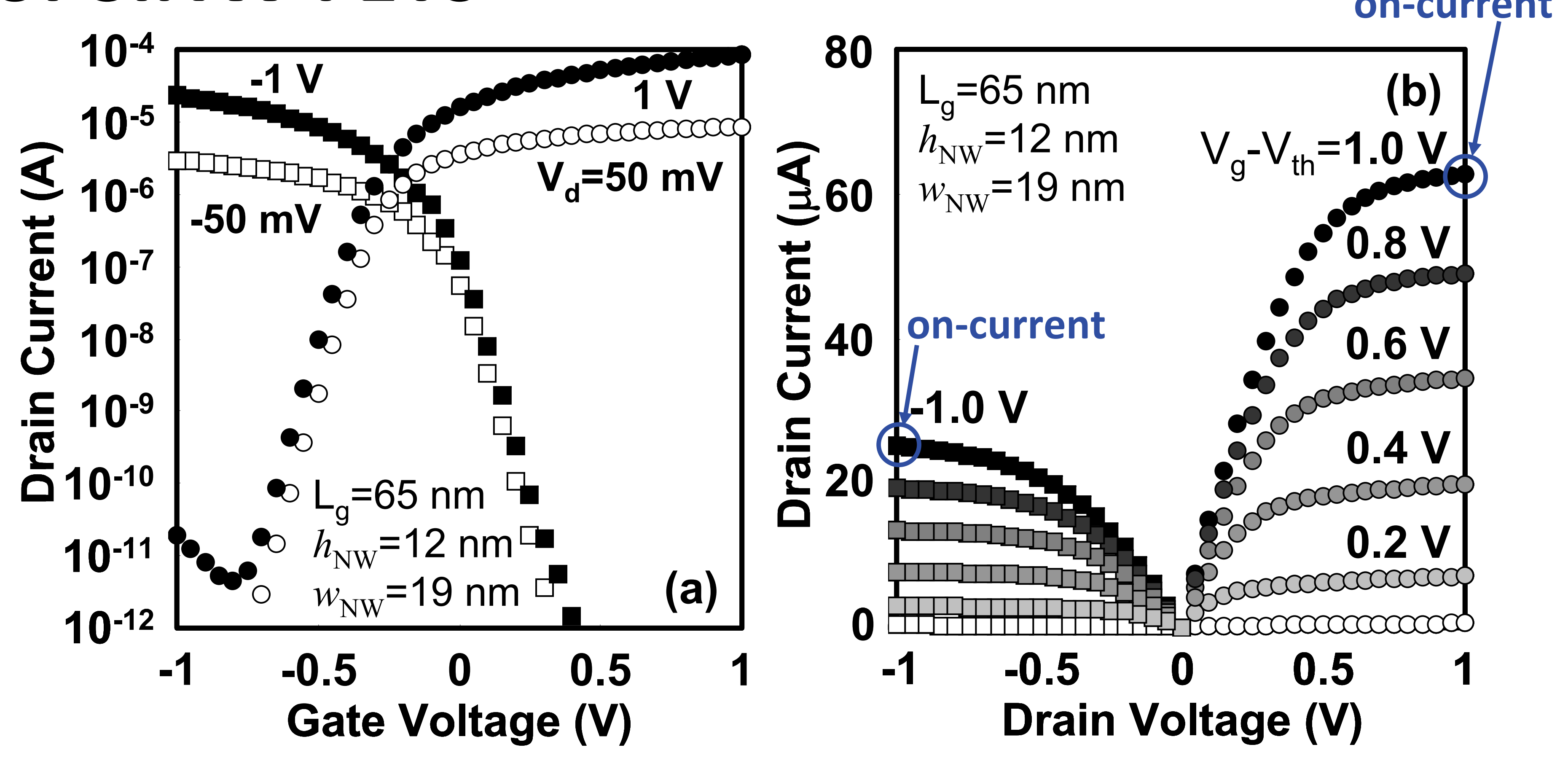






A: h_{NW} 12 nm w_{NW} 19 nm
B: h_{NW} 12 nm w_{NW} 28 nm
C: h_{NW} 12 nm w_{NW} 39 nm

Typical transfer and output characteristics of SiNW FETs

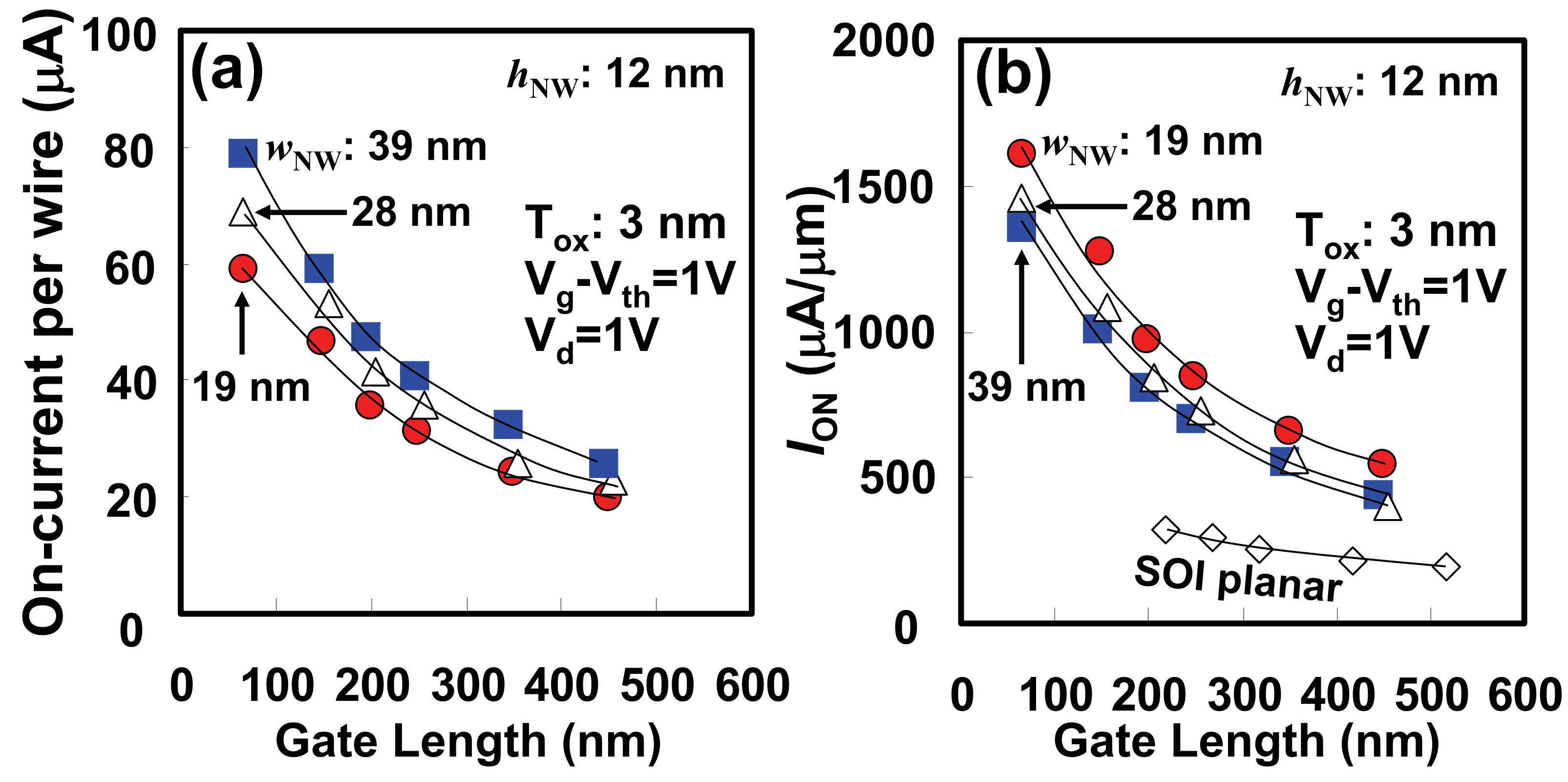


✓High on-current per wire was obtained for nFETs.

✓Good off characteristics were achieved.

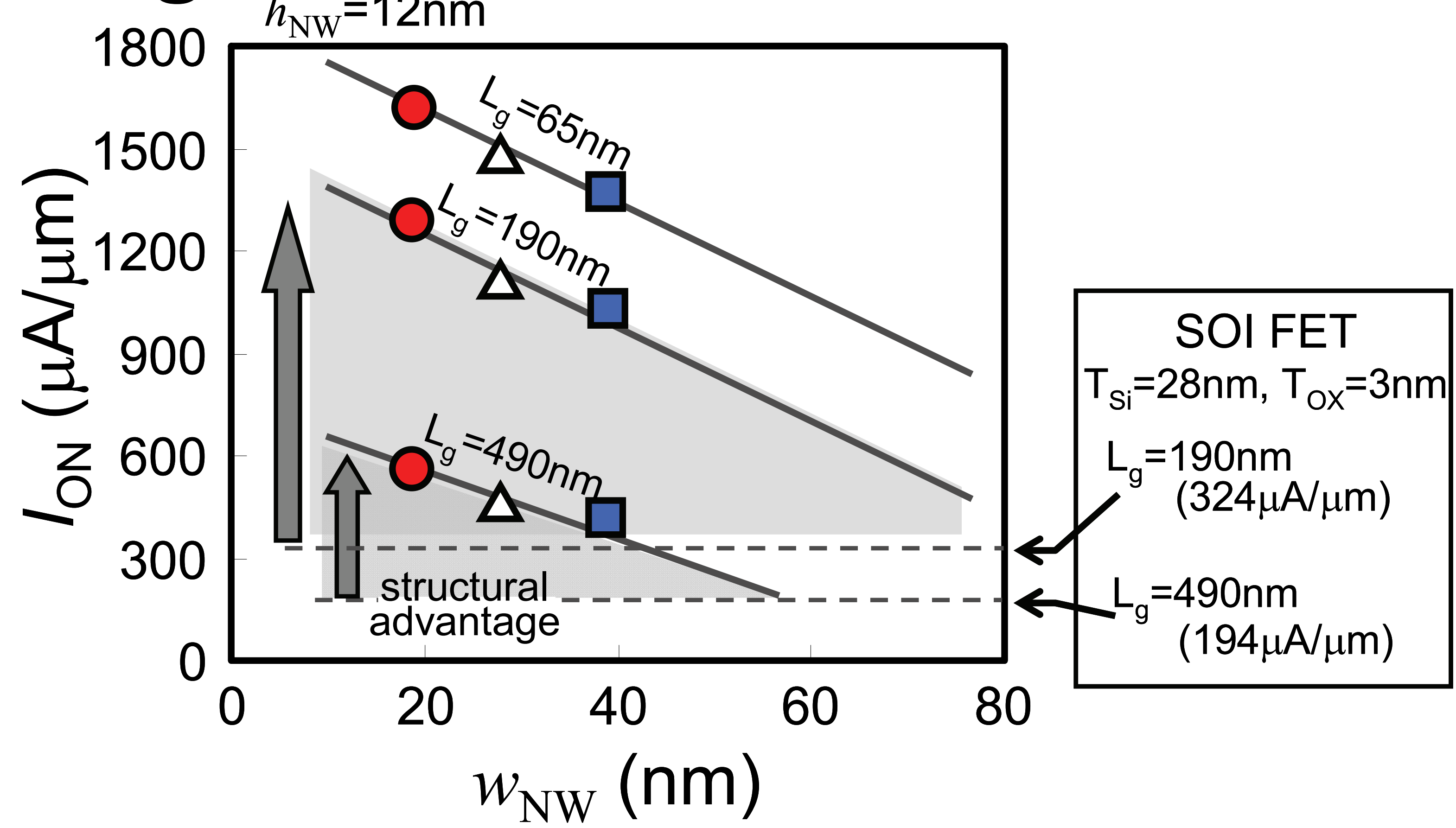
(DIBL:62 mV/V and SS:70 mV/dec. for nFETs)

Normalize on-current of SiNW nFETs



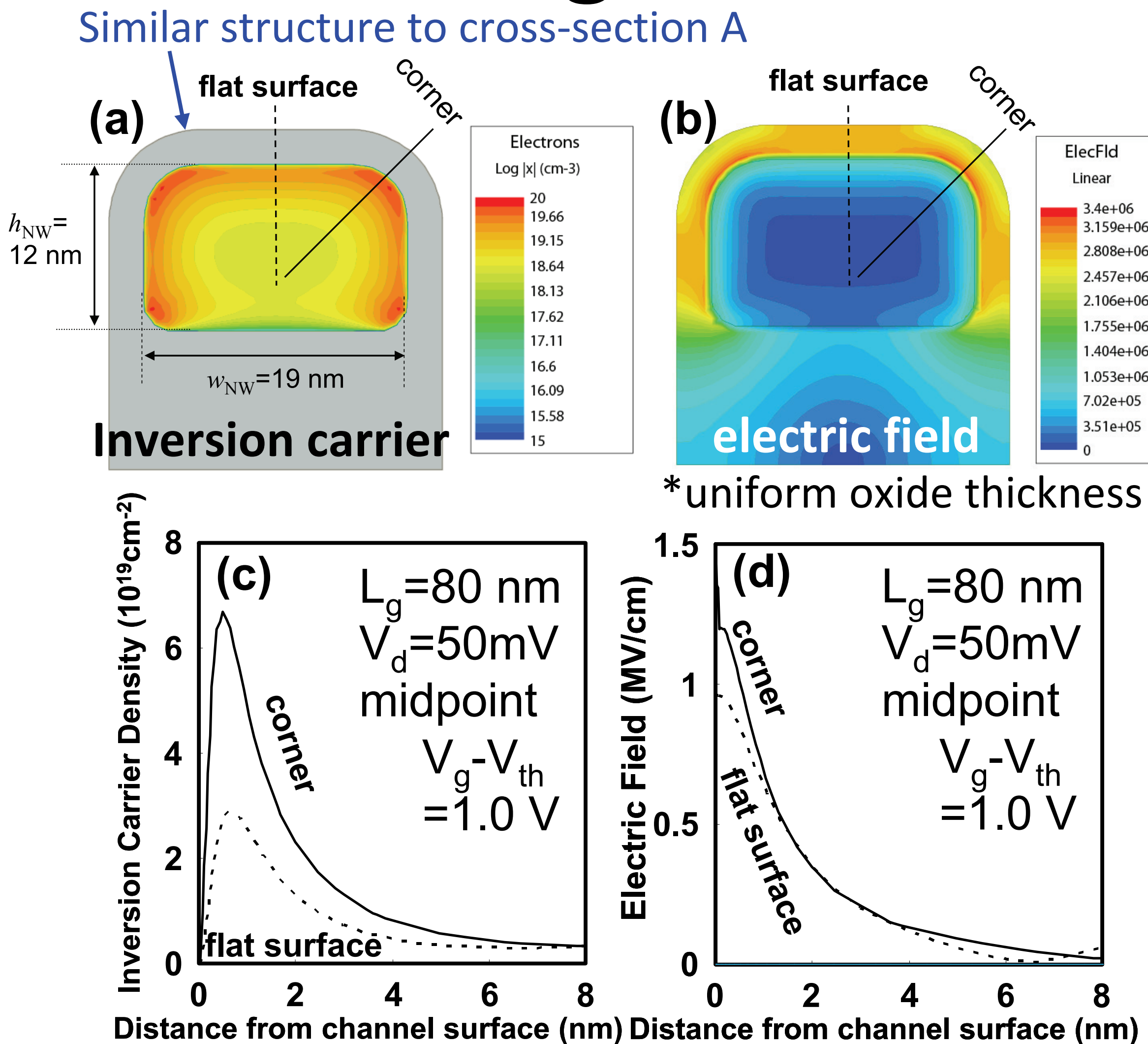
- ✓ As the w_{NW} increases on-current per wire also increased.
- ✓ Larger normalized on-current (I_{ON}) was obtained with smaller w_{NW}.
- ✓ Much larger I_{ON} of the SiNW nFETs than those of planar SOI nFETs on the same wafer.

Structural advantage of SiNW nFETs with rectangular cross-sections



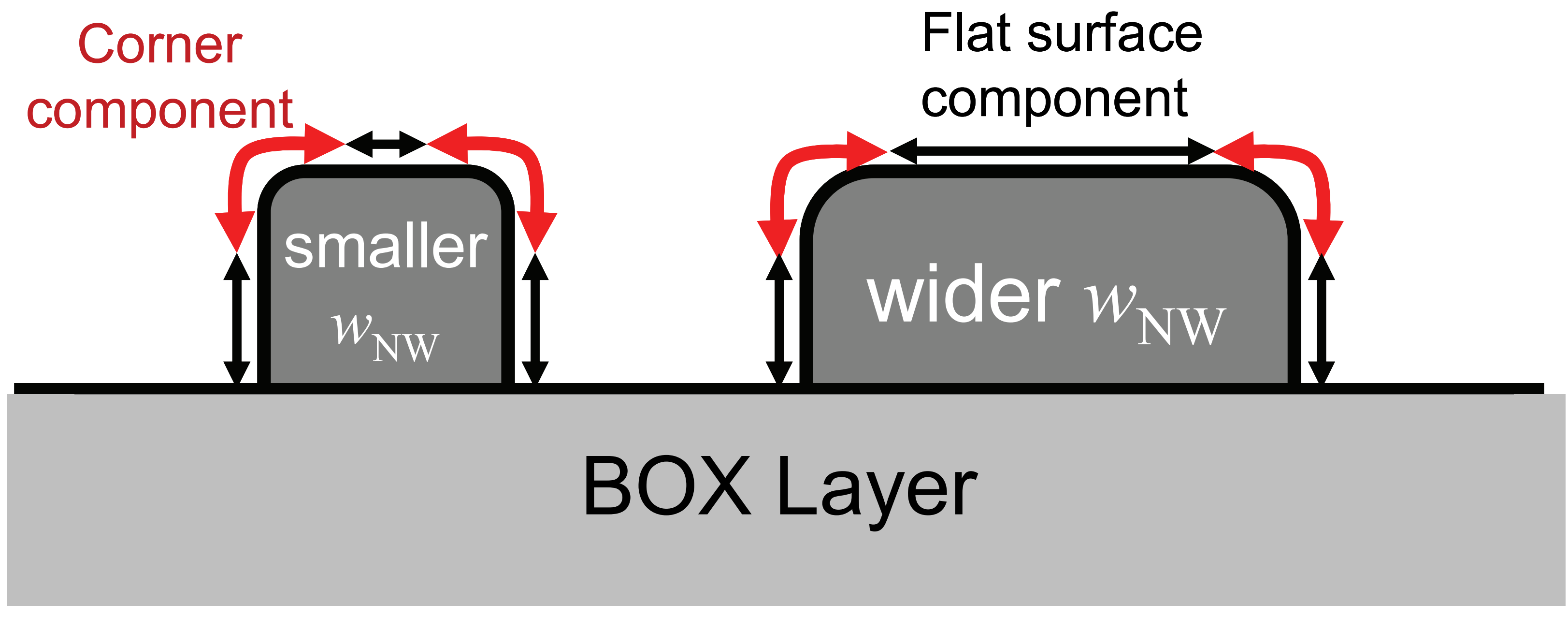
✓ As the channel width w_{NW} decreased, normalized on-current increased because of the structural advantage of SiNW FET.

Inversion carrier distribution across SiNW channel using TCAD



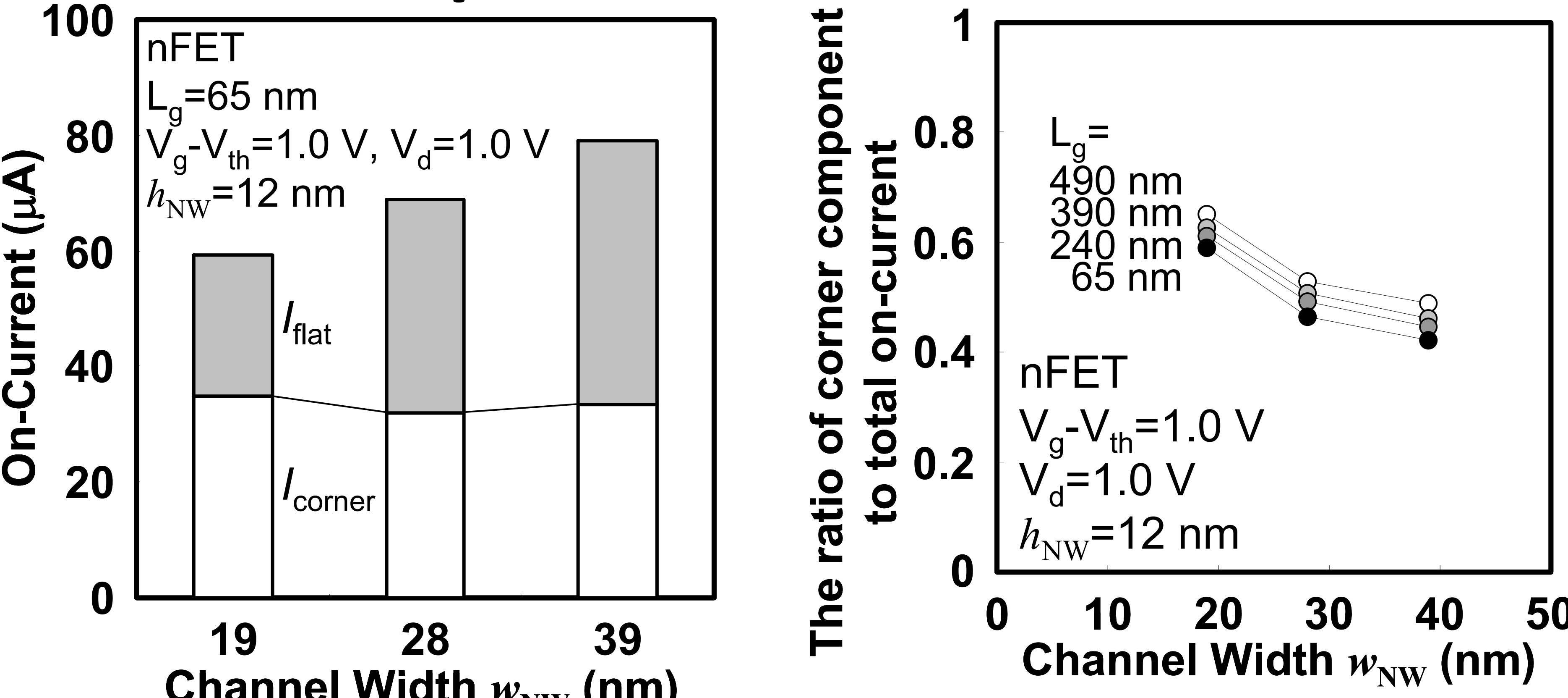
- ✓Higher inversion charge density near corners of SiNW channel because of higher electric field.
- ✓The peak inversion carrier density of corner is more than twice as that of the center of the SiNW channel.

How to separate on-current of corner component and flat-surface



- ✓ Assumed that on-current was composed of corner component and flat-surface component.
- ✓ On-current of flat-surface was calculated with difference of on-current per wire of the SiNW FET with larger w_{NW} and smaller w_{NW}.

On-current of corner component and flat-surface component

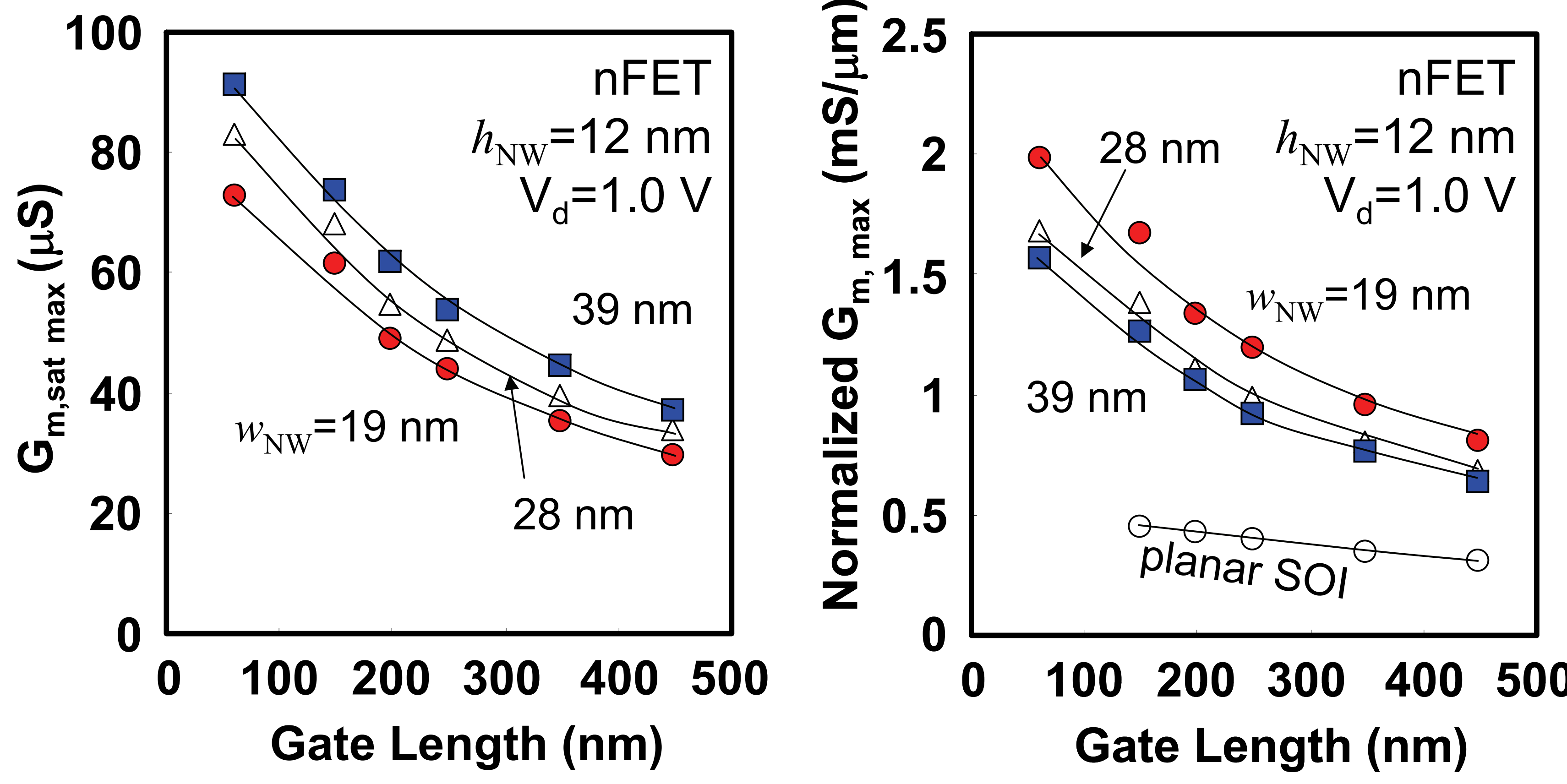


✓ I_{corner} is almost consistent with different w_{NW}.

✓ As the w_{NW} decrease I_{corner} becomes dominant.

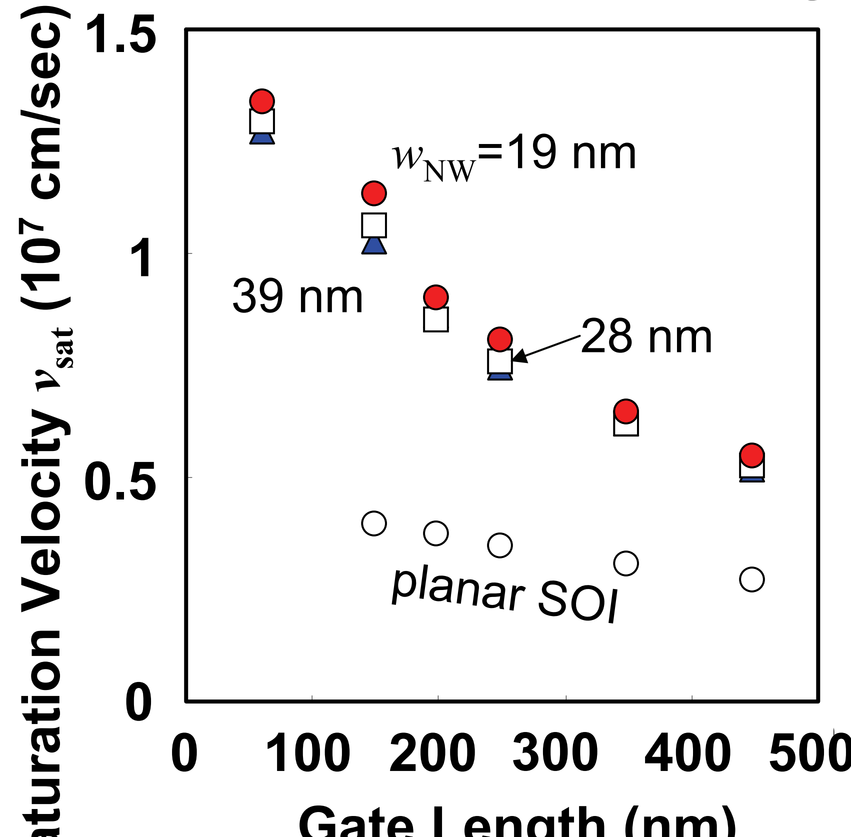
✓ As the L_g decrease, the ratio of corner component decreased.
→ suggests different carrier transports.

Transcontuctance at high drain voltage for evaluation of v_{sat}



✓Normalized $G_{m,\ max}$ at high drain voltage of narrower SiNW nFETs were higher.

Saturation velocity of SiNW FET



✓ v_{sat} of SiNW FET with the smallest w_{NW} was the largest.

✓ v_{sat} of SiNW FET was larger than v_{sat} planar SOI FETs on the same wafer.

✓ This result suggests high v_{sat} around the corners of rectangular cross-sections.

$$g_{m,sat} = C_{ox} W v_{sat}$$

$$v_{sat} = \frac{g_{m,sat}}{C_{ox} W}$$

EOT : 2.3 nm (h_{NW}=12 nm, w_{NW}=19 nm)
: 2.7 nm (h_{NW}=12 nm, w_{NW}= 28 nm)
: 2.8 nm (h_{NW}=12 nm, w_{NW}=39 nm)
: 3.0 nm (planar SOI nFET) (estimated)

Conclusions

✓On-Current of SiNW FET with rectangular cross-section was divided to the corner component and flat-surface component.

✓As the channel width decrease, the corner component increased up to 60 % with the channel width (w_{NW}) of 19 nm.

✓Saturation carrier velocity of SiNW nFET with the narrowest channel was the largest.

✓The corner plays an important role for carrier transport of SiNW nFET with rectangular cross-sections.

Acknowledgement

We thank all members of ASKA II line and the researchers in the front-end program in the R&D department 1, Selete, Tsukuba for device fabrication and fruitful discussions. This work was supported by the program ‘Development of Nanoelectronic Device Technology’ of the New Energy and Industrial Technology Development Organization (NEDO).