Experimental study on carrier transport limiting phenomena in 10 nm width nanowire CMOS transistors

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Abstract

For the first time, we experimentally analyze the limiting scattering phenomena in gate-all-around nanowire CMOS transistors with aggressive dimensions (L_{eff} of 32 nm for NMOS and 42 nm for PMOS with 15 nm nanowire width) and with high-k/metal gate stacks. One-level and multiple-level stacked nanowire structures are measured and compared. The apparent carrier mobility is degraded in short channel devices. Moreover, we show that the interface quality has a major impact on nanowire transport properties. In rounded nanowires (thanks to H_2 anneal), the extracted coulomb-limited mobility decreases whereas the surface roughness-limited mobility increases. Additionally, stacked nanowires suffer from additional coulomb scattering which is attributed to a degraded interface with high-k.

Introduction

Gate-all-around (GAA) silicon nanowire transistors (SNWTs) are one of the best structures to suppress short channel effects (SCEs) [1]. Recently, many GAA SNWTs have successfully been fabricated with very short channel lengths and small diameters by several top-down CMOS compatible processes [2-5]. Transport property degradations in nanowires with sub-10 nm diameter were reported by several groups [6-8]. However, it is possible to combine high performances and SCE immunity in sub-15nm gate length NWs with diameter varying from 20 nm down to 10 nm [5, 8]. Transport limiting phenomena have recently been studied in n-type SiO_2/Poly-Si SNWTs with diameters in the 15 to 50 nm range and long gate lengths [9]. Hole behaviour and the high-k impact on NW transistor are however still unknown. Moreover, in the quasi-ballistic transport regime, carrier mobility is still an important parameter [10]. Mobility limiting components, such as coulomb scattering, phonon scattering, and surface-roughness scattering, have hardly been investigated experimentally. To evidence those phenomena, we have thus studied the ballistic transport properties and the mobility limiting factors in SNWTs by low temperature measurements down to 5 K.

Device Structure

Multiple -stacked SNWTs were fabricated on (100) SOI wafers by top-down CMOS process with epitaxially-grown Si/SiGe layers. Superior on-state currents per surface unit have been achieved in those devices, whose cross-sectional TEM and SEM images can be found in Fig. 1. Fabrication details were provided in [8, 11]. The width (W_{NW}) of rectangular shape nanowire ranges from 10 nm up to 30 nm and the height (H_{NW}) is 15 nm. We also fabricated 1-level SNWTs by thermal oxidation and removal of its oxide (i.e. without SiGe epitaxy and selective etching) as shown in Fig.1 (a). H_2 annealing enabled us to obtain 1-level SNWTs with a circular cross-section [8, 12]. The resulting equivalent oxide thickness (EOT) is ~1.7 nm (3nm-thick-HfO_2 and 10nm-thick-TiN gate stack). All measured NWs are [110]-oriented

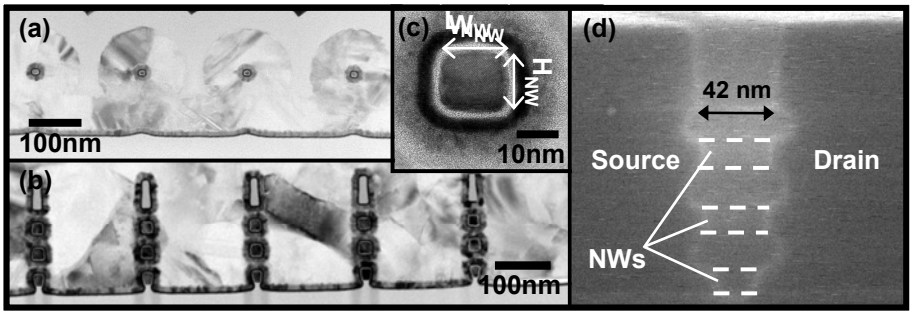

Figure 1: Cross-sectional Transmission Electron Microscopy and Scanning Electron Microscopy images of our SNWTs; (a) cross-section along the nanowire width for one-level SNWTs, (b) cross-section along the nanowire width for multiple-stacked SNWTs, (c) the enlarged image of a rectangular nanowire with a high-*k*/metal gate stacks, and (d) cross-section along the nanowire for multiple-stacked nanowire with 42 nm length before conformal gate stack deposition.

and horizontally arrayed with 50 parallel wires. The physical wire lengths (L_{NW}) are in the 42 – 607 nm range. Effective gate length (L_{eff}) and source/drain resistance (R_{SD}) were extracted thanks to the Y-function-based technique [13, 14]. Differences between L_{NW} and L_{eff} were less than 10 nm. This means that the source/drain implantation and activation annealing are well-controlled. Resulting R_{SD} are 159 Ω.µm for NMOS and 161 Ω.µm for PMOS.

Basic Characteristics and Ballistic Transport Properties

The measured I_{DS}-V_{DS} (Fig.2) and I_{DS}-V_{GS} (Fig.3) characteristics for multiple-stacked 15 nm width SNWTs with 32 nm effective gate length (L_{eff}) for NMOS and 42 nm for PMOS show well-behaved characteristics. I_{DS}-V_{GS} curves exhibit an excellent subthreshold slope (64 mV/dec for NMOS and 74 mV/dec for PMOS) and very low Drain Induced Barrier Lowering (32mV/V for NMOS and 62 mV/V for PMOS). On-currents I_{ON} (normalized by total circumference) of 840 µA/µm and 540 µA/µm with I_{OFF} of 4 nA/µm and 96 nA/µm are obtained for NMOS and PMOS, respectively. Comparable results were obtained in fully-depleted SOI and 1-level-SNWTs [2, 15]. When the currents are normalized by top-view width, the I_{ON} for NMOS is 7.2 mA/µm for 3D-stacked nanowires and 2.6 mA/µm for one-level, showing the interest of 3D devices to increase current density for a given layout. These extremely high currents are due to the vertically stacked structure. Fig. 4 shows I_{ON} as a function of L_{eff}. Gate length scaling is still effective down to sub-50nm L_{eff}. Meanwhile, low field mobility (μ_0) is degraded with decreasing L_{eff} as shown in Fig. 5. One of the possible reasons is the ballistic motion of carriers. The mobility experimentally extracted can be limited by ballistic transport. Indeed, mobility is defined as the ratio between the drift velocity and the electric field [16]. Thanks to the temperature dependence of both saturation velocity (v_{sat}) and injection velocity (v_{inj}), the nature of the transport can be evidenced by plotting the temperature dependence of the limiting velocity defined by v_{lim} = min (v_{sat}, v_{inj}) [17]. The temperature dependence of I_{DS}-V_{GS} curves for the SNWT with L_{eff} of 32 nm is shown in Fig. 6. The temperature range is from 5 to 300 K. The threshold voltage (V_T) decreases with temperature, while the sub-threshold slope (SS) increases. These changes in V_T and SS with temperature are mainly due to band gap changes and are consistent with the theory. Fig. 7 shows temperature dependence of v_{lim} for NMOS. It is clear that long SNWTs are almost exclusively v_{sat} limited. Meanwhile, v_{inj} slightly affects v_{lim} in short channel (L_{eff} = 32 nm) SNWTs.

Mobility Lowering Components

Since the backscattering rate is directly related to the mobility, it is important to examine the temperature dependence of mobility to quantify the contribution of each scattering mechanism. In order to accurately evaluate the transport properties, the effective mobility (μ_{eff}) was extracted by split C-V technique with parasitic capacitance and R_{SD} corrections [18]. Fig. 8 shows the validity of the extraction. A good agreement when compared to other techniques was achieved [19].

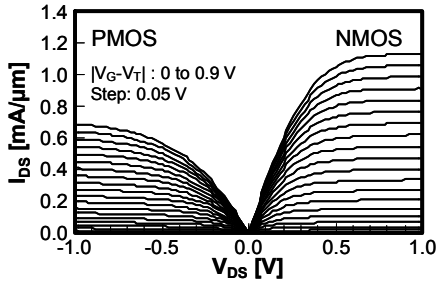

Figure 2: I_D-V_D characteristics of multiple-stacked L_{eff} = 32 nm NMOS and L_{eff} = 42 nm PMOS SNWTs. The W_{NW} and H_{NW} are 15nm. Currents are normalized by the circumference (W_{tot}).

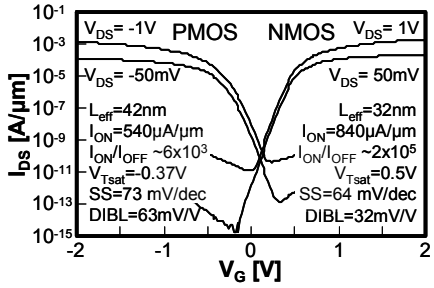

Figure 3: I_D-V_G characteristics of multiple-stacked L_{eff} = 32 nm NMOS and L_{eff} = 42 nm PMOS SNWTs. The W_{NW} and H_{NW} are 15nm. Currents are normalized by the circumference (W_{tot}).

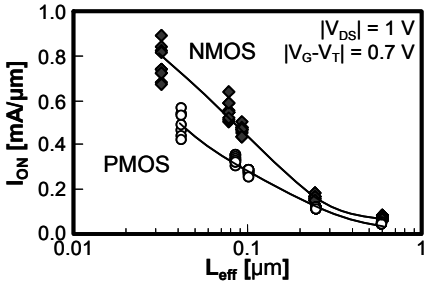

Figure 4: On-currents I_{ON} for NMOS and PMOS as a function of L_{eff}.

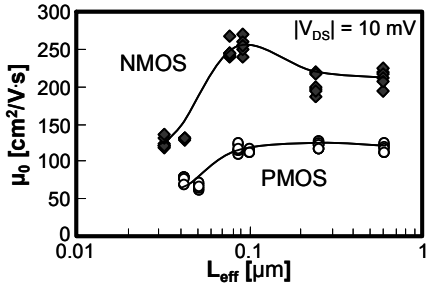

Figure 5: Low field mobility μ_0 for NMOS and PMOS as a function of L_{eff}. The mobility was extracted with the Y-function-based technique.

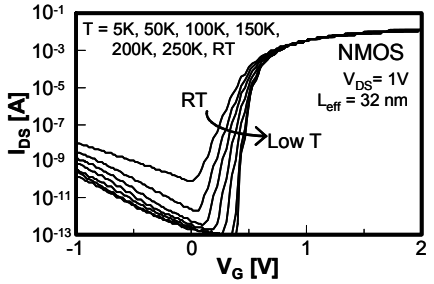

Figure 6: Temperature dependence of I_D-V_G characteristics for multiple-stacked SNWTs.

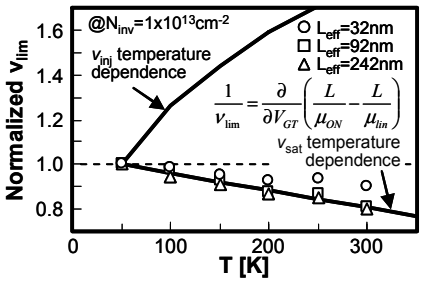

Figure 7: Temperature dependence of v_{lim} extracted with the equation provided in the insert [17].

Fig. 9 and 10 show effective mobility for electrons and holes in vertically stacked SNWTs as a function of inversion charge density (N_{inv}) at different temperatures. It is clear that the electron mobility dependence on temperature is much lower than for hole. In general, mobility in MOSFETs is limited by three scattering components; coulomb, phonon, and surface roughness as shown in Fig. 11. The coulomb-(μ_{cb}) and phonon-(μ_{ph}) limited mobilities have negative and positive contribution at low temperature, respectively. Meanwhile, the surface roughness-limited mobility (μ_{sr}) does not depend on temperature. At low temperature, mobility is limited by only the coulomb scattering only at low N_{inv} and only by the surface-roughness scattering only at high N_{inv}. Figs. 12 and 13 show effective mobility for electron and hole at high N_{inv} as a function of temperature for different W_{NW}, respectively. Electron and hole surface roughness-limited mobility μ_{sr} is degraded when W_{NW} decreases, while the temperature dependence of μ_{ph} does not depend on W_{NW} as shown in Fig. 14 and 15. On the other hand, in Fig. 16, electron mobility at low N_{inv} is degraded at lower temperatures. This indicates that the electron mobility in vertically stacked SNWTs is strongly limited by coulomb scattering, while the hole mobility is mainly limited by surface roughness scattering as shown in Fig. 17. Moreover, coulomb scattering is more dominant in wider nanowires for electrons than for holes. Fig. 18 shows a mobility comparison between multiple-stacked and 1-level SNWTs with 15 nm of W_{NW}. In the case of 1-level SNWTs, coulomb scattering is less dominant. The effective mobility temperature dependence for 1-level SNWTs is consistent with the reported μ_{eff} behavior in SNWTs [8]. The reason why stronger coulomb scattering is higher in stacked SNWTs may be the degraded interface quality with high-k because of the use of SiGe sacrificial layers. Additional surface treatments may thus be needed.

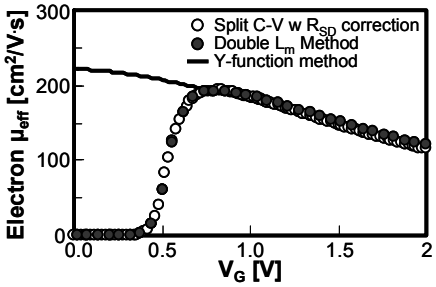

Figure 8: Comparison of effective mobility extracted by split C-V, double L_m method, and from parameters extracted by Y-function method. The measured device is the stacked SNWTs with W_{NW}=15 nm and L_{eff}=242 nm. The device with L_{eff}=592 nm was also used for double L_m method.

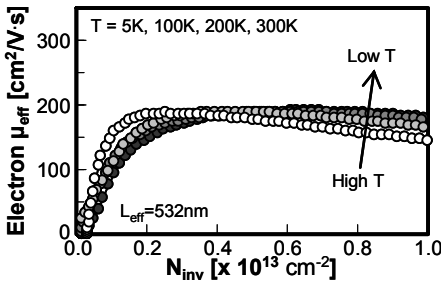

Figure 9: Effective electron mobility as a function of inversion charge density for multiple-stacked SNWTs with W_{NW}=15 nm and L_{eff}=532 nm for different temperatures from 300 K down to 5 K.

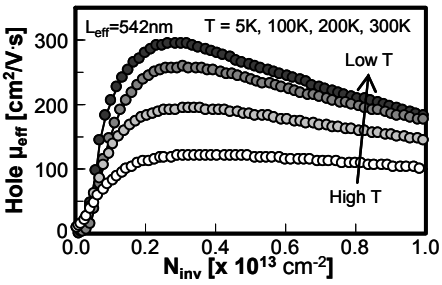

Figure 10: Effective hole mobility as a function of inversion charge density for multiple-stacked SNWTs with W_{NW}=15 nm and L_{eff}=542 nm for different temperatures from 300 K down to 5 K.

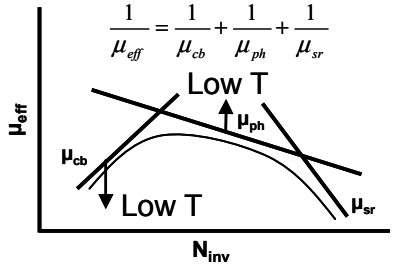

Figure 11: Schematic illustration of mobility limiting factors with temperature. As temperature decreases, μ_{ph} increases while μ_{cb} decreases.

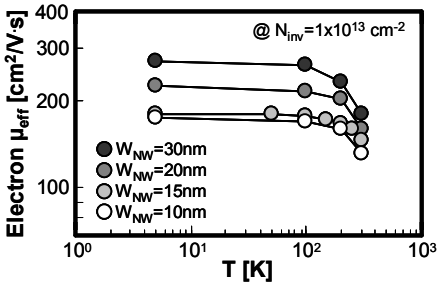

Figure 12: Effective electron mobility at high N_{inv} as a function of temperature for different W_{NW}. The μ_{eff} at 5 K can be regarded as the μ_{sr}.

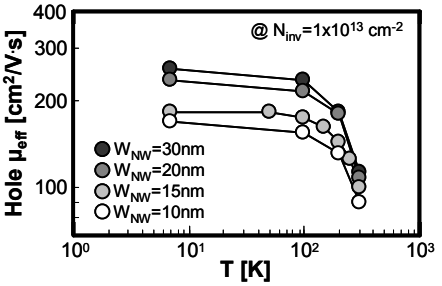

Figure 13: Effective hole mobility at high N_{inv} as a function of temperature for different W_{NW}

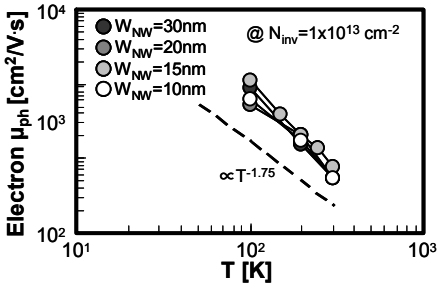

Figure 14: Phonon-limited electron mobility at high N_{inv} as a function of temperature for different W_{NW}.

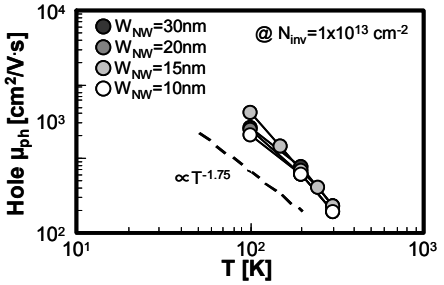

Figure 15: Phonon-limited hole mobility at high N_{inv} as a function of temperature for different W_{NW}.

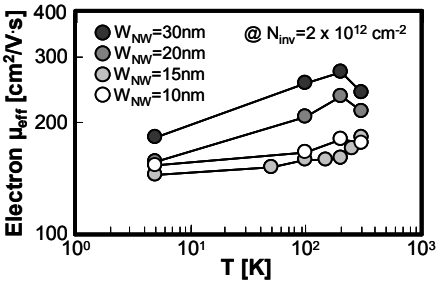

Figure 16: Effective electron mobility at low N_{inv} as a function of temperature for different W_{NW}.

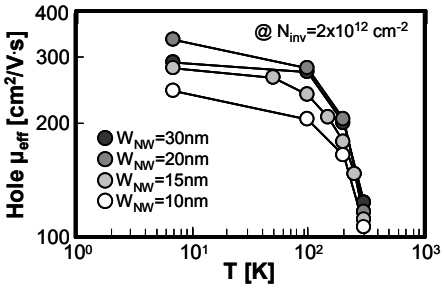

Figure 17: Effective hole mobility at low N_{inv} as a function of temperature for different W_{NW}.

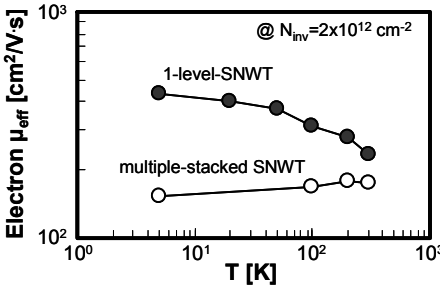

Figure 18: Effective electron mobility at low N_{inv} as a function of temperature for 1-level-SNWT and multiple-stacked SNWT.

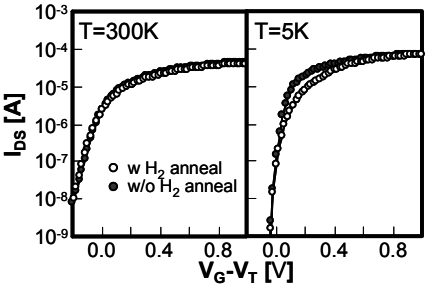

Figure 19: I_D-V_G curves for 1-level-SNWTs with and without H_2 annealing at 300 K and 5 K.

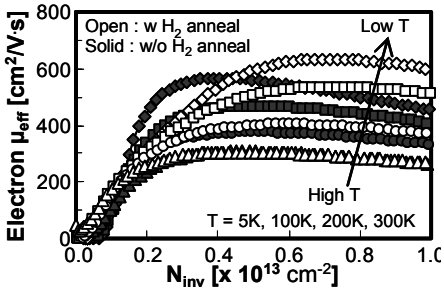

Figure 20: Effective electron mobility as a function of inversion charge density for 1-level-SNWTs with and without H_2 annealing for different temperatures.

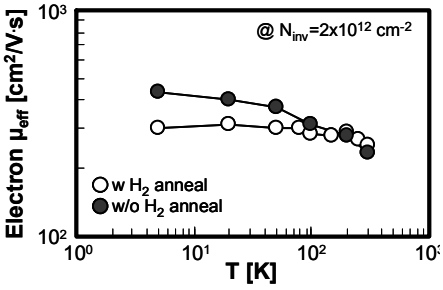

Figure 21: Effective electron mobility at low N_{inv} as a function of temperature for 1-level-SNWTs with and without H_2 annealing.

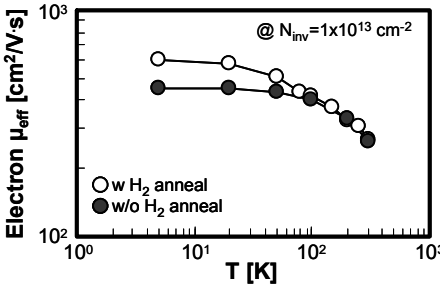

Figure 22: Effective electron mobility at high N_{inv} as a function of temperature for 1-level-SNWTs with and without H_2 annealing.

The impact of H_2 annealing on NW surface quality was investigated. Fig. 19 shows that I_{DS}-V_{GS} curves of 1-level SNWTs with and without H_2 annealing at 300 K and 5 K. The same curve is obtained at 300 K, while, at 5 K, degradation in the threshold region is observed in the H_2-annealed SNWTs. Figs. 20-22 show the comparison of effective electron mobility. It is clear that effective mobility in H_2-annealed SNWTs is more degraded by coulomb scattering, while surface roughness is improved. This coulomb scattering degradation is consistent with our previous work, which evidenced the increase of interface trap density on rounded nanowires [20].

Conclusion

The optimisation of short-channel CMOS nanowire drive current will have to take into account specific effects. In particular, additional scattering observed in rounded wires can limit ballisicity and thus the I_{ON} current. Additional work on interface optimization and passivation is thus needed on NW structures.

Acknowledgement

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