第一回複合創造領域シンポジウム

Vertically-Stacked Nanowire Transistors for future CMOS

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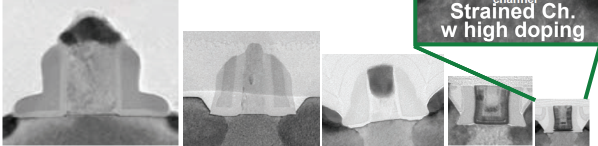
Introduction

CMOS scaling



Tech. node:	130nm	90nm	65nm	45nm	32nm
Gate length:	60nm	45nm	35nm	35nm	30nm

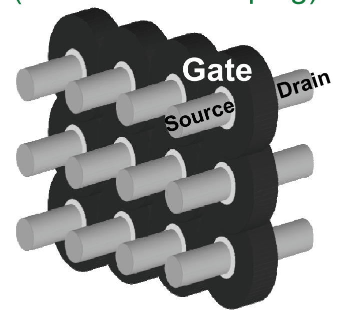
K. Kuhn (Intel), SSDM 2009 P. Packan (Intel), IEDM'09

Problems

- ☐ Gate leakage (Thin gate oxide)
  → **High-k/Metal gate**
- ☐ Mobility degradation (high-channel doping)
  → **Strained Channel**
- ☐ Short-channel effects (V_{TH} roll-off, SS and DIBL degradation)
  → **Multi-gate structure**

Nanowire FETs

- ✓ Good SCEs immunity
- ✓ High current density per layout surface (Vertically-stacking NWs)
- ✓ High mobility? (Low-channel doping)

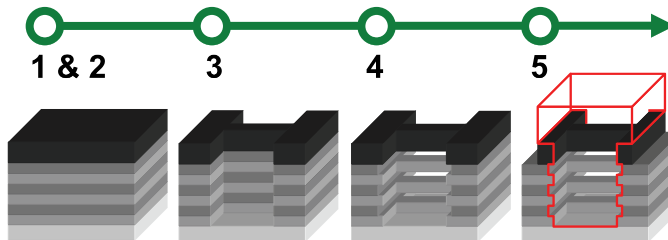


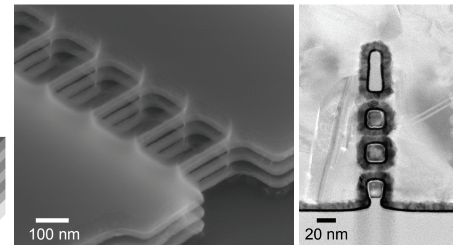
Purpose

To understand transport properties in vertically-stacked Silicon Nanowire Transistors (SNWTs)

Device fabrication

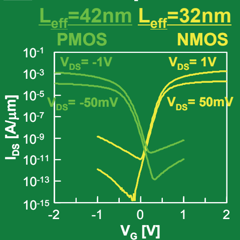
1. Si/SiGe superlattice selective epitaxy
2. Hard mask SiN deposition
3. Anisotropic etching of Si/SiGe layers
4. Isotropic etching of SiGe
5. Gate stack deposition
6. Gate patterning
7. Implantation
8. Nitride spacers





Results

☐ Device performance



	NMOS	PMOS
NW cross-section	2 square NWs + 1 Tri-gate	
NW dimensions	15 nm x 15 nm	
L_{eff} [nm]	32	42
EOT [nm]	1.7	1.7
V_{DD} [V]	1	1
I_{ON} by cir.	840 μA/μm	540 μA/μm
I_{ON} by top-view	7.2 mA/μm	4.7 mA/μm
I_{ON}/I_{OFF}	~2x10^5	~6x10^3
DIBL [mV/V]	32	63
SS [mV/dec]	64	73

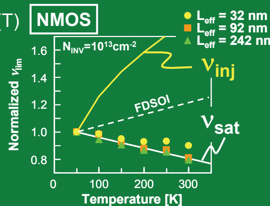
High on-current density
Excellent electrostatic control

☐ Transport mechanisms

Saturation velocity, v_{sat} (T)
Injection velocity, v_{inj} (T)
→ Opposite T-dependence

Limiting velocity
$v_{lim} = \min(v_{sat}, v_{inj})$
$$\frac{1}{v_{lim}} = \frac{d}{dV_{GT}}\left(\frac{L}{\mu_{ON}} - \frac{L}{\mu_{lin}}\right)$$

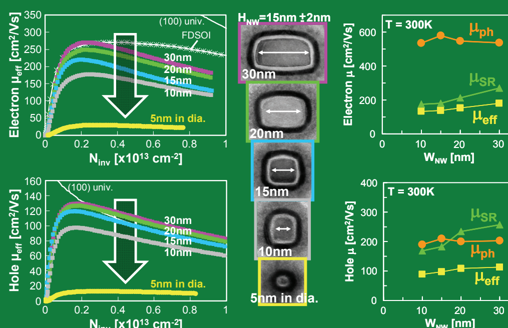
D. Fleury, VLSI'09



Strong scattering events are still occurring.

☐ Carrier mobility

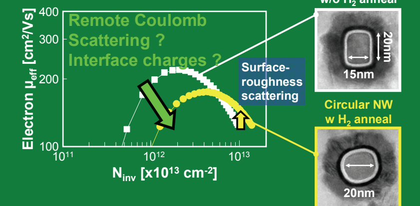
1. Size effects



Both electron and hole meff have the same degradation tendency with decreasing W_{NW}.

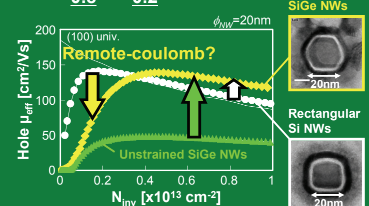
Electron μ_{eff} is strongly limited by μ_{sr}.
Hole μ_{eff} is limited by both μ_{sr} and μ_{ph}.

2. Shape effects



H_2 anneal can improve surface roughness, while coulomb scattering increases.

3. $Si_{0.8}Ge_{0.2}$ NWs



Summary

- ✓We have experimentally investigated the carrier transport limiting factors in vertically-stacked SNWTs.
- ✓High I_{ON} currents with excellent electrostatic control have been achieved.
- ✓μ_{sr} decreases with W_{NW} for both elec and hole.
- ✓Additional surface treatments are needed to cure the damaged Si surface.

References

K. Tachi et al., IEDM'09
K. Tachi et al., IEDM'10