第一回複合創造領域シンポジウム

Effect of Rare Earth Oxide Capping for La-based Gate Oxides

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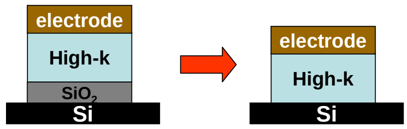
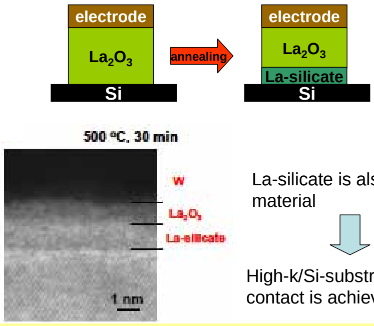
Back ground

To achieve an EOT below 1 nm, high-k gate insulators should be directly in contact with the Si substrate.



No SiO_2 interfacial layer



La-silicate is also high-k material

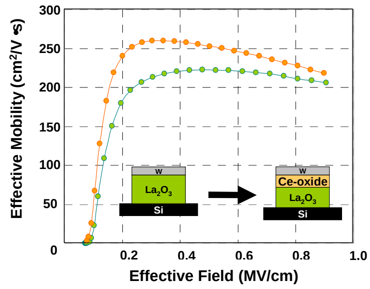
High-k/Si-substrate direct contact is achieved

La-silicate : dielectric constant = 9~12

➡ EOT~0.5nm ➞ physical thickness is so thin

➡ Electrical properties were degraded

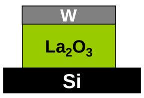
Capping a thin Ce-oxide layer on a La_2O_3 gate dielectric



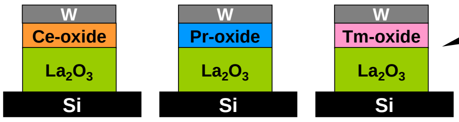
Electrical characteristics were improved

Purpose of this work

Examined the effects of rare-earth oxide as a capping material to further scale La_2O_3 dielectrics toward 0.5 nm in EOT.



La_2O_3 material is base layer
CeO_X, PrO_X, TmO_X capped on La_2O_3 gate dielectric



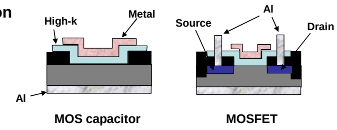
Rare- earth material capping

Fabrication of device

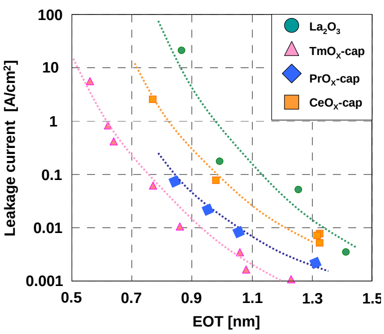
- n-type Si substrate (MOS capacitor)
  p-type Si substrate (MOSFET)
- SPM, HF last tretment
- High-k materials deposition (La_2O_3, Ce-oxide, Pr-oxide, Tm-oxide)
- Tungsten (W) metal gate electrode deposition by RF sputtering

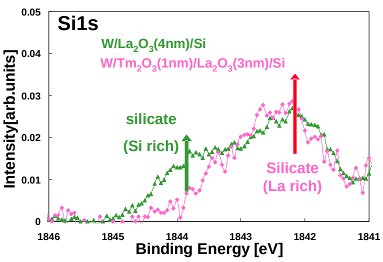
In situ

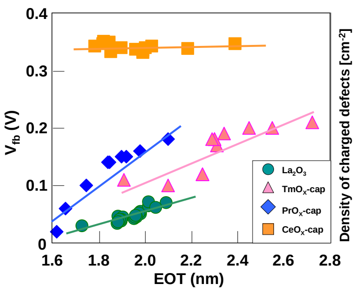
- PMA (Post Metallization Annealing) 500℃ 30min (FG:3%H_2)
- Source, Drain Al interconnection
- Bottom electrode Al deposition

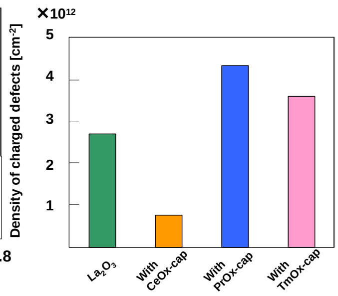


Result and discussion









Leakage current can be suppressed with rare-earth oxide capping, especially, with Tm-oxide

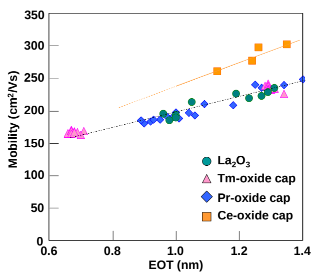
The density of charged defects in the film was reduced only with Ce-oxide capping

Formation of the silicate layer can be suppressed by XPS Si1s spectrum

Achieving a higher overall dielectric constant after annealing

Further device-scaling was achieved

Conclusion



Ce-oxide cap

charged defects reduction

⇨ Improvement of mobility

Tm-oxide cap

Higher dielectric constant

⇨ Small EOT was achieved