第一回複合創造領域シンポジウム

Feasibility study of Ce oxide for resistive RAM application

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Background and Motivation 1

- RRAM: Resistance Switching Random Access Memory

High resistance — Off state; Write voltage; Erase voltage; Low resistance — On state

- ➢nonvolatile
- ➢High speed
- ➢Compatibility with CMOS
- ➢Simple MIM structure
- ➢Low consumption
- ➢Great potential of scaling

Promising candidate for next-generation memory

- CeO_2: potential for high-performance RRAM device
  - ➢ Changeable valence number (Ce^{3+} and Ce^{4+})
  - ➢ Fluorite structure ⟹ high conductivity of oxygen ions [1]
  - ➢ Reactivity with Si to form amorphous Ce-silicate [2]

Ce, O

High performance RRAM based on Cerium oxide and Si buffer layer

Model for switching mechanism 4

W electrode; CeO_2; Oxygen ions at grain boundary; TiN electrode

Initial state → Forming process (+V): Formation of oxygen vacancies:

$2CeO_2 \xrightarrow{-2e^-} Ce_2O_3 + ½ O_2 + Vo^{--}$

oxygen vacancies drift under electric field

off state (HRS) (−V): elimination of oxygen vacancies

$Ce_2O_3 + ½ O_2 + Vo^{--} \xrightarrow{+2e} 2CeO_2$

on state (LRS) (+V)

Device design 2

n⁺-Si wafer (0.02 < Ω cm)

- Cleaning (SPM + DHF)
- Growth of SiO2 insulator (thermal oxidation)
- Patterning contact window
- Deposition of TiN bottom electrode (RF sputter)
- Deposition of Si buffer layer (RF sputter)
- Deposition of CeO2 switching layer (electron beam)
- Deposition of W top electrode (RF sputter)
- Electrode patterning process
- Evaporation of Al back contact
- Annealing 400°C, 30s, N_2

Layers: W 50 nm; CeO_2 20 nm; Si 0/1 nm; TiN 15 nm; SiO_2 200 nm; n⁺-Si wafer; Al. (50 µm, 20 µm, 10 µm)

Materials and structure are suitable for practical application

Results of W/CeO$_2$/Si/TiN structure 5

I–V: C.C = 1mA; LRS; HRS; Forming process; CeO_2 20nm, Si 1nm; 20um*20um. Resistance vs. Switching Cycle: Read@0.5V, R.T.; HRS; LRS; Window~10; 20um*20um.

Formation of Ce-silicate ⟹ Introduce oxygen vacancies

$CeO_2 + Si \rightarrow CeSiO_4 + 2Vo^{--}$

$Ce_2O_3 + Si \rightarrow Ce_2SiO_5 + 2Vo^{--}$

Initial state

By inserting Si buffer layer:

1. Forming process can be finished at lower voltage, results in protect devices from break down
2. A stable window (AVG=18) in 50times switching is achieved

Results of W/CeO$_2$/TiN structure 3

I–V: C.C = 1mA; ① Forming process; LRS; HRS; CeO_2 20nm; 20um*20um. Resistance vs. Switching Cycle: Read@0.5V, R.T.; HRS1/LRS1 = 9.5; HRS20/LRS20 = 1.5; 20um*20um. Resistance vs. Electrode Area: HRS, LRS; 10um*10um, 20um*20um, 50um*50um.

For resistance change of W/CeO$_2$/TiN:

1. Forming process is necessary
2. Bipolar switching behaviors
3. As electrode areas scales, window gets large
4. Endurance characteristics is worse

Summary 6

- W/CeO$_2$/TiN shows a bipolar resistance switching behavior, large forming voltage is necessary and endurance characteristics is worse.
- Its switching behavior can be explained by the formation and rapture of the filament composed by oxygen vacancies.
- By formation of silicate, Si buffer layer can introduce additional oxygen vacancies into the materials, which helps devices switch under lower voltage, enlarges its window and improves endurance characteristics.

Reference:

[1] P. Gao et al., Micron, 41, p.301-305(2010)
[2] K. Kakushima et al., VLSI Tech. Dig. p.69-70(2010).