第一回複合創造領域シンポジウム

Towards High Performance III-V MOSFET, A Study on high-*k* Gate Stacks on $In_{0.53}Ga_{0.47}As$

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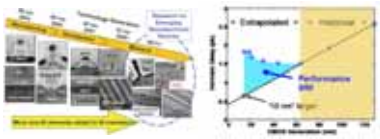
Background

limits of Si



Points of Improvement:
- Switching speed
- Density
- Power

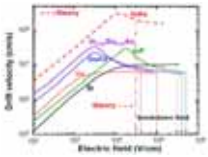
↓ 22nm node and below

Parasitic charge interference with channel charge

Gate delay ~ $C_{ox} \cdot V_{CC}/I_{ON}$ ↑

Si replacements are considered for 15nm node and beyond

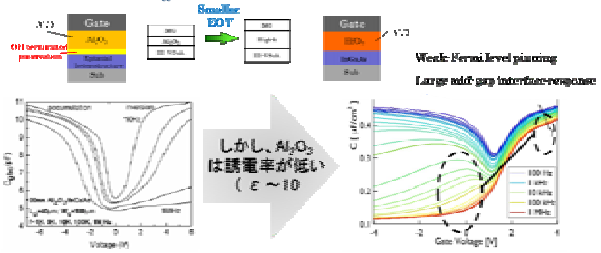
High Mobility Material



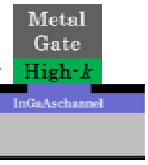
Parameter	Units	Material: Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
μ_n at n_s=1E12 cm^{-2}	$cm^2/V.s$	300	7,000	10,000	15,000	30,000
bulk μ_n	$cm^2/V.s$	450	400	200	460	1,250
E_g	eV	1.11	1.43	0.7	0.36	0.17

High mobility channel material (Indium contentを増やすことで移動度は増加)
Increasing carrier mobility can increase the drive current at
($In_{0.53}GaAs$ ~ 10,000 cm^2/Vs, $In_{0.7}GaAs$~ 11,000 cm^2/Vs)
low bias voltage to reduce the gate delay time
Superior intrinsic speed

低 supply voltage (V_{cc}= 0.5V) ⇒ low power consumption



Purpose

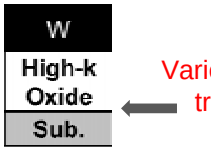


Important Transistor Factors

- ON current (I_{ON})
- OFF current (I_{OFF})
- V_T (Threshold Voltage)
- Subthreshold Swing (SS)
- Gate Capacitance
- Operating voltage (V_{DD})

Achieving High Performance III-V MOSFET

Experimental Method



Various surface treatments

InGaAs / InP Substrate
- HF cleaning (Surface Treatment)
- High-k e-beam deposition

in situ
- Tungsten (W) deposition by sputtering
- Reactive ion etching (RIE) of W gate
- Backside *Al* contact
- Annealing in F.G

XPS analysis

Electrical characterization

Results

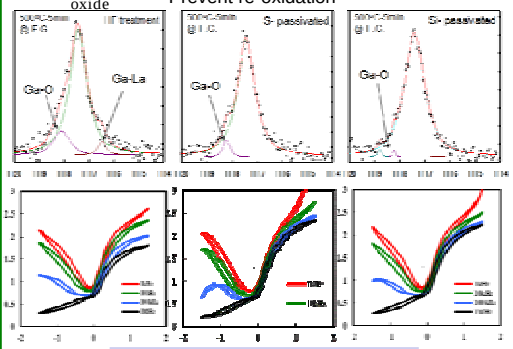
Optimizing Surface

Surface wet-treatment

1-Concentrated HF treatment: Native oxide

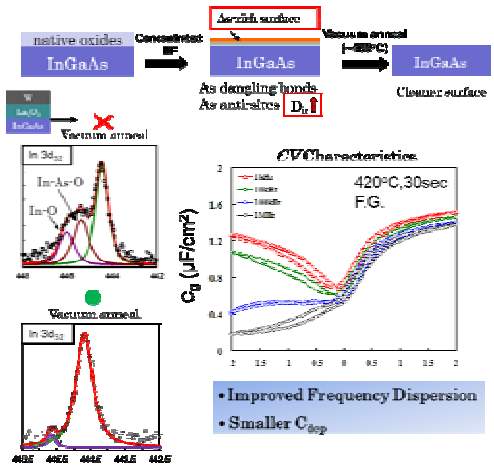
2-$(NH_4)_2S$ treatment: S-terminate, Prevent re-oxidation

3-HMDS vapor coating: Mono-layer Si coating



Native oxide & Frequency Dispersion Reduction

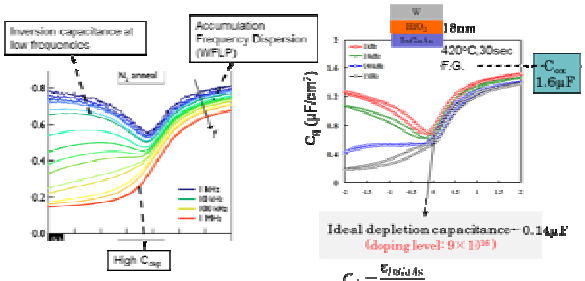
Pre-deposition annealing



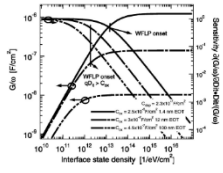
- Improved Frequency Dispersion
- Smaller C_{dep}

Discussion

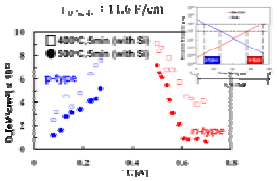
Interface States Issues



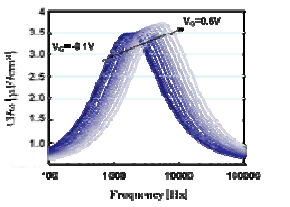
$$C_d = \frac{\varepsilon_{InGaAs}}{W_d}$$



Effective when $C_{ox} > qD_{it}$



High interface states at mid-gap



- Moderate G_p/ω peak response
- Peak D_{it}=4.3×10^{13}[$cm^{-2}eV^{-1}$] (> C_{ox}/q)

0.1 [eV] from mid-gap

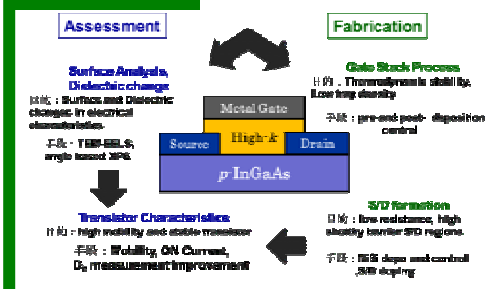
C_{ox} needs to increase

Balance between leakage current and C_{ox}

High bandgap-lower k material might be necessary for surface passivation

Conclusion

Towards III-V MOSFET



III-V Semiconductor strong candidate for high performance devices
-high electron mobility (injection velocity)

Major Challenges
- stable gate stack with unpinned Fermi level interface
-Modeling interface states for better understanding
-low resistance source and drain formation

Progress
-much improvement with pre- and post-deposition control
-much more work remains for improvement