# A Compact Modeling of Si Nanowire MOSFETs

Kenji Natori \*

Frontier Research Center, Tokyo Institute of Technology, J2-68 4259 Nagatsuta, Modori-ku, Yokohama 226-8502, Japan \* Email: natori.k.aa@m.titech.ac.jp

#### Abstract

Compact modeling of a Si nanowire MOSFET is discussed. Framework and detailed expression of the compact model for a ballistic Si nanowire MOSFET are provided. The device characteristics of a thin Si nanowire MOSFET is shown as a model calculation, and some characteristic features of the device are explained. Then a new scattering model for a quasi- ballistic Si nanowire MOSFET is introduced, and the basic concept of the model is explained. The elastic backscattering and the energy relaxation are separately considered. The result of model calculation of a quasi-ballistic Si nanowire MOSFET is shown.

# 1. Introduction

According to ITRS[1], 3-dimensional MOSFET structures are inevitable to replace planar structures in future LSI devices. Especially, the nanowire MOSFET attracts wide attention, for its promising performance as well as for its excellent short-channel-effect immunity. Investigation of the device is greatly facilitated by development of a handy analysis tool, giving a rough estimation of the device characteristics and also insight into the operational mechanism. Here we present a compact model of the Si nanowire MOSFET to meet the demand, and discuss some preliminary characteristics of the device.

# 2. Ballistic Si Nanowire MOSFETs

A compact model of the ballistic Si nanowire MOSFET is described[2] and representative characteristics of the device are discussed. Electric current of the device is derived by Landuer's formalism similarly as in other ballistic devices,

$$I_D = \frac{q}{\pi\hbar} \sum_i g_i \int \left[ f(E,\mu_S) - f(E,\mu_D) \right] T_i(E) dE \quad (1)$$

Here, *q* is elementary charge,  $\mu_{\rm S}$  and  $\mu_{\rm D}$  are Fermi levels of the source and the drain electrode, respectively. These two quantities are related to each other as  $\mu_D = \mu_S - qV_D$ where  $V_{\rm D}$  is the drain bias.  $f(E, \mu)$  is the Fermi distribution function. As is well known, the electronic state within a wire is described by 1-Dimensional subband structures. Here, summation over *i* denotes the summation over subbands,  $g_i$  stands for degeneracy of the subband, and  $T_i(E)$  represents the transmission probability of carriers from source to drain. In ballistic transport where  $T_i(E)=1$ , the integration in (1) is performed to yield,

$$I_{D} = G_{0} \left( \frac{k_{B}T}{q} \right) \sum_{i} g_{i} \ln \left\{ \frac{1 + \exp\left[ (\mu_{S} - E_{i0}) / k_{B}T \right]}{1 + \exp\left[ (\mu_{D} - E_{i0}) / k_{B}T \right]} \right\}.$$
 (2)

Here,  $G_0 \equiv 2q^2 / h = 77.8$  µS is the quantum conductance,

 $k_{\rm B}T$  is the thermal energy, and  $E_{i0}$  is the energy level of the *i*-th subband-bottom evaluated at the potential maximum point located close to the source edge. This point is known to act as the electric current bottleneck, and the conduction of the device is caused by carriers with a larger energy than the potential value, in the absence of quantum mechanical tunneling.

The other important relationship controlling the current is obtained by electrostatic consideration around the current bottleneck point, that is

$$(V_G - V_t) - \alpha \frac{\mu_S - E_{00}}{q} = \frac{|Q|}{C_G}$$
 (3)

Here  $V_{\rm G}$  is the gate bias,  $V_{\rm t}$  is the threshold voltage of the device,  $E_{00}$  is the subband-bottom energy of the lowest subband, and Q is the carrier charge at the current bottleneck.  $C_{\rm G}$  is the gate capacitance. It is preferable to constitute the capacitance value by a series connection of the electrostatic capacitance  $C_{\rm ox}$  in insulator region, and the capacitance due to quantum-mechanical charge separation from the interface,  $C_{\rm Q}$  (similar to the inversion capacitance).  $\alpha$  is defined by

$$\alpha = 1 + \frac{C_p}{C_c}.$$
 (4)

where  $C_p$  is the parasitic capacitance of the channel at the bottleneck point.  $C_{ox}$  is derived by simple electrostatics. The capacitance value for GAA (Gate-All-Around) structure are given by



Figure. 1.  $I-V_D$  characteristics of ballistic Si nanowire MOSFET, evaluated by the compact model.

$$C_{ox} = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r}\right)}$$
(5)

There is no parasitic capacitance in the structure. Electric current is basically controlled by the charge and the velocity of carriers, and both of these are closely related to the electronic states within the wire. An important aspect of electronic states in ballistic transport is represented by the carrier distribution within subbands,

$$|Q| = \frac{q}{\pi} \sum_{i} g_{i} \left[ \int_{k_{i\min}}^{\infty} \frac{dk}{1 + \exp\left\{\frac{E_{i}(k) - \mu_{s}}{k_{B}T}\right\}} + \int_{-\infty}^{k_{i\min}} \frac{dk}{1 + \exp\left\{\frac{E_{i}(k) - \mu_{D}}{k_{B}T}\right\}} \right].$$
 (6)

Here,  $E_i(k)$  is the *E*-*k* relation in the *i*-th subband,  $k_{imin}$  is the value of *k* for the lowest value of energy in the subband (i.e.  $E_{i_o} = E_i(k_{imin})$ ). Specific expression of  $E_i(k)$ is derived when the material and the structure of nanowire is given. It can be extracted from the band structure of bulk material using the effective mass approximation, or directly computed from the crystal structure of nanowire by e.g. first principles calculation.



Figure 2. I- $V_G$  characteristics of ballistic Si nanowire MOSFET. The subthreshold slope reproduces the ideal value of 58 meV/dec.

First we fix material and structure of the nanowire FET. then the subband structure as well as capacitances  $C_{ox}$ ,  $C_{\rm Q}$ ,  $C_{\rm G}$  and  $C_{\rm p}$  are evaluated. If bias voltage  $V_{\rm G}$  and  $V_{\rm D}$ are given, the simultaneous equations (3) and (6) yield the value of unknown parameters  $\mu_{\rm S}$  and Q. Substituting the value of  $\mu_{\rm S}$  into Eq. (2), we obtain the device current  $I_{\rm D}$ . The procedure combining Eqs. (2) through (6) constitutes a compact model for electric current of the ballistic nanowire MOSFET. Notice that no channel-length dependence is included in these formulae. The ballistic characteristics do not depend on channel length, because the whole injected flux constitutes the drain current regardless of the channel length.

Now we derive the *I-V* characteristics of a representative Si nanowire MOSFET. We tentatively use the subband structure reported by Gnani et al.[3] They derived the subband structure for a 1.34 nm width rectangular Si nanowire directed in <001> direction and surrounded by (110) surfaces by the first principles calculation. Actual expression of subbands are provided as

$$E_{0}(k) = \left(\frac{\gamma_{0}}{0.31}\right) - 0.3 \left(\frac{\gamma_{0}}{0.31}\right)^{2} + 0.0375 \left(\frac{\gamma_{0}}{0.31}\right)^{3}, (7)$$

$$E_{1}(k) = 0.0327 + \left(\frac{\gamma_{0}}{0.36}\right)$$

$$- 0.258 \left(\frac{\gamma_{0}}{0.36}\right)^{2} + 0.025 \left(\frac{\gamma_{0}}{0.36}\right)^{3}. (8)$$

**Potential Profile** 



Figure 3. The carrier scattering model for the quasiballistic Si nanowire MOSFET. Elastic scattering and the optical phonon emission are considered.

 $E_0(k)$  is the lowest single subband, and  $E_1(k)$  is the upper three-fold degenerate subbands. Electronic energy is in eV, and  $\gamma_0$  stands for  $(\hbar k)^2 / 2m$  where *m* is electron mass. The effective mass is around 0.3*m*, and is considerably larger than the bulk value. We assume a GAA MOSFET structure with the cylindrical channel of 1.51 nm diameter covered by the gate oxide of  $t_{ox}=1$  nm. The cylindrical channel is inconsistent with the rectangular wire subband, but one can assume that the effect of shape of the cross section is minor compared with the effect of size of the nanowire. And the cylindrical diameter is adjusted so that the area of cross section is the same for both structures. Then  $C_G=2.57$ pF/cm and  $C_p=0$ , neglecting the inversion capacitance.

The  $I_{\rm D}$ - $V_{\rm D}$  characteristics evaluated with use of the above compact model is shown in Fig. 1, and the ID-Gate overdrive (i.e.  $(V_G - V_I)$ ) characteristics are shown in Fig. 2. Figure 1 implies that the device current amounts to a few tens of micro-ampere in the absence of carrier scattering. In actuality, however, carrier scattering greatly decreases the value. The linear region and the saturated current region are clearly distinguished, and the current saturation seems complete. With scattering, however, the saturation is destroyed and the current continues to increase as we see later. The boundary between the two regions is located around  $V_{\rm D} \sim 0.15$  V. This value represents the Fermi energy of carriers around the current bottleneck in the channel, and the Fermi energy much larger than  $k_{\rm B}T$  (around 25 meV) indicates that the injected carriers are in strong degeneracy. The difference between two curves for 300 K and 4 K is small and the temperature effect is small. This is also due to the large value of Fermi energy compared to thermal energy. The  $I_{\rm D}$ - $V_{\rm G}$  characteristics in Fig. 2 clearly show two regions; the weak inversion region exponentially dependent on  $V_{\rm G}$  and the strong inversion region linearly dependent on  $V_{\rm G}$ . The subthreshold slope (SS coefficient) has an ideal value of 58 meV/dec without  $V_{\rm D}$ dependence. This is because our simple model has no consideration of the short channel effect, and the channel



Figure 4. I- $V_D$  characteristics of the quasi-ballistic Si nanowire MOSFET evaluated with the scattering model in Fig. 3.

in a GAA structure includes no parasitic capacitance.

#### 3. Quasi-Ballistic Si Nanowire MOSFET Model

Analysis of ballistic nanowire MOSFET provides lots of information on the device characteristics. But the consideration of the carrier scattering is inevitable for understanding actual device characteristics. Carrier scattering affects the transport in two ways. One is the carrier backscattering which yields the negative velocity component directly decreasing the device current. The other is the energy relaxation that encourages the drain current. The energy-relaxed carriers that lost a large amount of kinetic energy are unable to return to source and are eventually absorbed in the drain contributing the device current. These two functions are basically independent to each other, but the ordinary relaxation time approximation (RTA) describes the carrier scattering with a single parameter  $\tau$ . RTA is very convenient, but is too much simplified. Here we employ the carrier scattering model[4][5][6] illustrated in Fig. 3, where the two aspects of scattering are separately considered. The model employs the 1-dimensional motion with a linear potential profile along the channel. Two types of scattering mechanism, the general elastic scattering and the energy relaxation due to optical phonon emission, are considered. A large part of carriers are injected into channel with the kinetic energy comparable to  $k_{\rm B}T$ . The optical phonon energy in Si, around 60 meV, is much larger than  $k_{\rm B}T$  and the injected carriers run free of optical phonon emission in the region where the kinetic energy is still less than the optical phonon energy. We call this region the Initial Elastic Zone. Beyond, in the region denoted by Energy Relax Zone, carriers are subject to the both scattering processes, the elastic scattering and the optical phonon emission. A part of carriers injected from source are backscattered within the initial elastic zone and return to source. Others, which go through the initial elastic zone, have two choices; a small probability of returning to the initial elastic zone again by the elastic backscattering within the energy relax zone, and a large probability of energy relaxation and being absorbed in the drain as a part of drain current. The scattering model is described by Boltzmann transport equation, which is transformed into a flux equation. The solution yields the transmission coefficient  $T_i(E)$  from source to drain, and allows evaluation of the drain current in Eq. (1). Similarly as in Sec. 2, a compact model of quasi-ballistic Si nanowire MOSFET is constituted based on the scattering model just introduced. A result of model calculation is compared with that of a ballistic Si nanowire MOSFET in Fig. 4 assuming an identical device structure. Parameters representing the scattering amplitudes are chosen as is consistent with the 2-dimensional MOS mobility. The ballistic current of 38 µA is diminished to less than 30 µA due to the carrier scattering.

## 4. Summary

Specific expressions in a compact model of ballistic Si nanowire MOSFET are derived and described.  $I_D$ - $V_D$  and  $I_D$ - $V_G$  characteristics are shown and discussed. A new carrier scattering model for a quasi-ballistic Si nanowire MOSFET is introduced and explained. The  $I_D$ - $V_D$  characteristics of a quasi-ballistic Si nanowire MOSFET evaluated by the compact model with the proposed scattering model is shown and discussed.

# Acknowledgments

This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

## References

- [1] http://www.itrs.net/.
- [2] K. Natori, IEEE Trans. Electron Devices, 55, p.2877 (2008).
- [3] E. Gnani, S. Reggiani, A. Gnudi, P. Parruccini, R. Colle, M. Rudan, and G. Baccarani, IEEE Trans. Electron Devices, 54, p.2243 (2007).
- [4] K. Natori, Jpn. J. Appl. Phys., 48, p.034503, (2009).
- [5] K. Natori, Jpn. J. Appl. Phys., 48, p.034504, (2009).
- [6] K. Natori, 2009 Solid State Device and Materials (SSDM 2009), p.1058 (2009).