Observation of tunneling FET operation in MOSFET with NiSi/Si Schottky source/channel interface

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Introduction

As the MOSFET scaling goes down to 10nm region the supply voltage (V_{dd}) should be decreased accordingly. However, Subthreshold (S) slope cannot be scaled down below 60mV/decade at Room temperature (RT) and this fact hinders the V_{dd} scaling. The tunnel FET is one of the promising candidates to decrease S [1]. Schottky barrier tunneling FET (SBTT) has many advantages to ordinary PN junction tunnel FETs: low parasitic resistance, better short channel effect immunity and high controllability of output characteristics by the silicide material selection [2]. We fabricated tunnel MOSFETs with NiSi/Si Schottky barrier at the source/channel interface. This work is to find the tunneling emission, S slope dependence on temperature revealed that thermionic emission over the Schottky barrier dominated at temperatures higher than 150K. However, tunneling through the Schottky barrier became dominant at lower temperatures.

Experiments

Figure 1 shows the Schottky MOSFET structure fabricated on SOI substrate with Si thickness of ~55nm. The Si layer is p-type ($1x10^{16}cm^{-2}$). The BOX-layer thickness was about 125nm. The source/drain region was fully silicided by 12-nm thick Ni deposition followed by 400°C 30 sec silicidation annealing, and the excess Ni layer was chemically etched. The overlap of NiSi/Si interface under the gate electrode, which is indispensable for the tunnel FET operation, was formed by the encroachment phenomenon of NiSi during the silicidation [3]. The gate insulator was SiO_2 with the thickness of 60 nm.

Results

Fig.2 shows temperature dependence of S for the pMOS operation at the drain voltage of -3 V. The value at RT is very large (~2000 mV/decade). It can be attributed to very thick gate oxide and large interface-states density D_{it}. S at high temperatures (>150K) showed T^{+1} dependence which is typical for the thermionic emission currents over the Schottky barrier. On the contrary, below 100 K, S was almost independent on T. It indicates that the tunnel currents between the source and channel regions are dominant at these temperatures. Therefore, it is confirmed that this device operates as SBTT below 100 K. It should be noted that this device shows ambipolar characteristics and similar T dependence of S was observed for nMOSFET mode operation.

Conclusion

We fabricated tunnel MOSFETs with NiSi/Si Schottky barrier at the source/channel interface. Although the S slope showed T^{+1} dependence at high temperatures, the tunnel FET characteristics were confirmed by the smaller dependence of S slope on temperatures lower than 100K. RT tunnel FET operation might be possible by the tuning of the Schottky barrier height.

References

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[3] H.Arai, et al., Proc. ECS 2009

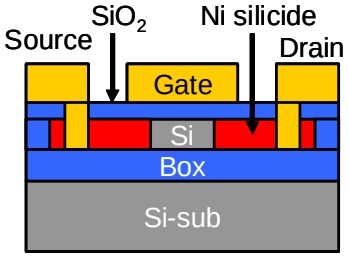

Fig. 1: Device structure of the fabricated SOI Schottky MOSFET

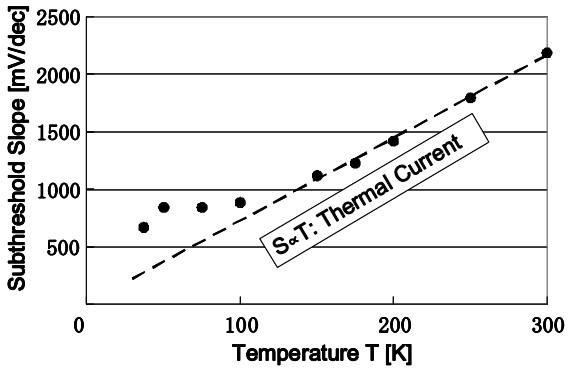

Fig. 2: Dependence of subthreshold-slope on temperature for pMOS mode operation at drain voltage of -3 V.