TiN Capping Effect on High Temperature Annealed RE-Oxide Devices for Scaled EOT

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Abstract

The effect of TiN capping on high temperature annealed W gated rare-earth oxide (RE-oxide) capacitors has been characterized. The increase in EOT has been well suppressed with TiN capping and a 0.55-nm EOT has been achieved even after an 900 ^{o}C annealing. The electrical characterization has revealed a significant reduction in the capacitance-voltage (*C*-*V*) hysteresis when the annealing temperature is 900 ^{o}C or higher.

Introduction

A direct contact of high-k/Si substrate (without a SiO_2 interfacial layer) is required for EOT as thin as 0.5 nm [1]. La_2O_3 can achieve a direct contact of high-k/Si by forming a silicate layer [2, 3]. However, the excess oxygen supplied from the gate electrode to the La_2O_3 dielectric increases the EOT especially with high-temperature processes. Therefore, a process to suppress the EOT growth is necessary. Selecting a proper gate electrode can be a solution. In this paper, TiN capping is investigated.

Experiment

La_2O_3 dielectric films were deposited by e-beam evaporation on a HF-last *n*-Si(100) substrates. A W film was in situ deposited by RF magnetron sputtering to avoid any moisture or carbon related contamination. A TiN film was subsequently deposited by the same method. The W and TiN films were patterned by reactive-ion etching (RIE) using SF_6 chemistry to form gate electrodes. The wafers were then post-metallization annealed (PMA) in a rapid thermal-annealing (RTA) furnace in forming gas (F.G.) (N_2:H_2= 97:3%) ambient at various temperatures for 2 s. An Al contact layer on backside of the substrate was deposited by thermal evaporation. The schematic illustration of the as-deposited gate stack structure is shown in fig. 1.

Results

Fig. 2 shows the annealing temperature dependence of EOT for TiN(40 nm)/W(6 nm) /La_2O_3(3.5 nm)/*n*-Si capacitors. It was confirmed that the EOT was maintained after annealing with the TiN capping. Compared to as-deposited condition, the amount of EOT increase after annealing at 1000 ^{o}C was less than 0.1 nm. Hysteresis of *C*-*V* curves versus annealing temperature is shown in fig. 3. Hysteresis can be suppressed down to 10 mV when the annealing temperature is 900 ^{o}C or higher.

Conclusion

The effect of TiN capping on high-temperature annealed W gated La_2O_3 capacitors has been characterized. The increase in EOT has been well suppressed with the TiN capping and a 0.55-nm EOT has been achieved with 900 ^{o}C annealing. Relatively large hysteresis in *C*-*V* curve in the as deposited condition has been extremely decreased to less than 10 mV by annealing at 900 ^{o}C or higher.

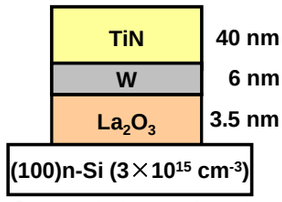

Fig.1. Schematic illustration of the MOS structure in as-deposited condition.

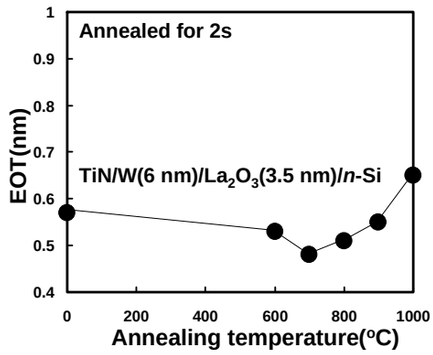

Fig. 2 Annealing temperature dependence of EOT for TiN(40 nm)/W(6 nm) /La_2O_3(3.5 nm)/*n*-Si capacitors.

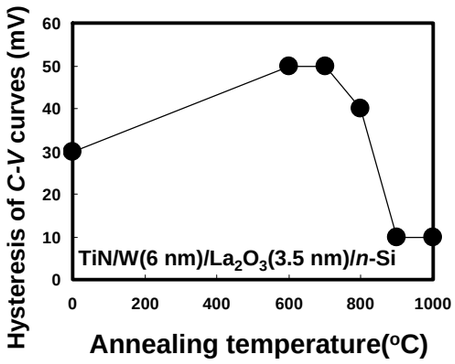

Fig.3 Hysteresis of C-V curves vs. annealing temperature for TiN(40 nm)/W(6 nm) /La_2O_3(3.5 nm)/*n*-Si capacitors.

Acknowledgment

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References

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