Electrical Properties of Yttrium-Titanium Oxide High- κ Gate Dielectric on Ge

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The feasibility of $YTiO_x$ as a high-k gate dielectric for germanium-metal-oxide-semiconductor (MOS) devices has been investigated. The effects of different concentration of TiO_x on electrical properties of $YTiO_x$-based MOS capacitors are reported. It has been demonstrated that higher TiO_x concentration in $YTiO_x$ may help to boost up dielectric constant while it causes serious damage to the interfacial properties. It has been observed that $YTiO_x$ film can effectively prevent re-growth of GeO_x-based interfacial layer likely due to formation of stable Y-Ti-germanate at the interface in consequence of strong interaction of $YTiO_x$ with underlying Ge substrate. Indeed, $YTiO_x$ with 22% TiO_x exhibits fairly good electrical characteristics with high dielectric constant value of $\kappa \sim 21 \pm 1$. The potentiality of $YTiO_x$ has further been examined with gate oxide downscaling and the results are compared with that of regularly used high-κ dielectrics promising for Ge MOSFETs.

Introduction

Aggressive dimensional scaling of field-effect-transistors (FETs) beyond 16 nm technology node has prompted interest in high mobility channel materials like germanium as an alternative to conventional Si based complementary-metal-oxide-semiconductor (MOS) devices. For Ge CMOS technology development, selection of an appropriate high-κ material and control of interfacial layer at the dielectric/Ge interface has been the most critical issue to date. However, to meet the requirement for the ultimate equivalent oxide thickness (EOT) down-scaling, direct deposition of high-κ dielectrics on Ge without interfacial layers is imperative while maintaining a high permittivity and decent interface quality between high- κ dielectrics and Ge.

Recently, it has been suggested that rare-earth oxides such as La_2O_3, Y_2O_3, Gd_2O_3, Lu_2O_3 etc. not only offers a good passivation but also exhibits fair insulating properties on Ge (1-2). Among them, Y_2O_3 has been found to be a promising candidate since it can efficiently restrict the diffusion of Ge into dielectric, inhibits the growth of Ge sub-oxide based interfacial layer as well as demonstrates fairly good electrical performances.

However, the effective dielectric constant has been the main concerning issue with Y_2O_3 on Ge. Meanwhile, Ti-incorporation has been reported to increase the permittivity of Hf-based oxides because of the extremely high relative permittivity of Ti-based oxides (κ ~80) (3). Hence, this paper reports the experimental results on the electrical characteristics of Yttrium-Titanium oxide based high-κ gate dielectric with various TiO_x concentrations directly deposited on Ge.

Experimental Details

The (100) oriented n-type bulk Ge wafers from Umicore with a resistivity of 0.1-1.0 Ω-cm were used as the starting substrate in this experiment. Preparation of a clean surface of a Ge substrate is a very critical issue especially for direct deposition of dielectrics without any incorporation of remaining native oxide. It has been found that conventional wet cleaning process e.g. (H_2O_2+HF), cyclic dilute HF dip with DI water rinsing, ammonium hydroxide solution etc. cannot completely remove the native GeO_2, but oxygen and carbon contaminations still remain (4-10). These signals may originate from a combination of adventitious carbon, hydrocarbon and water absorbed onto the surfaces during exposure to ambient atmosphere after the wet treatment. Therefore, thermal desorption of native oxides is being employed in this study to obtain a clean Ge surface.

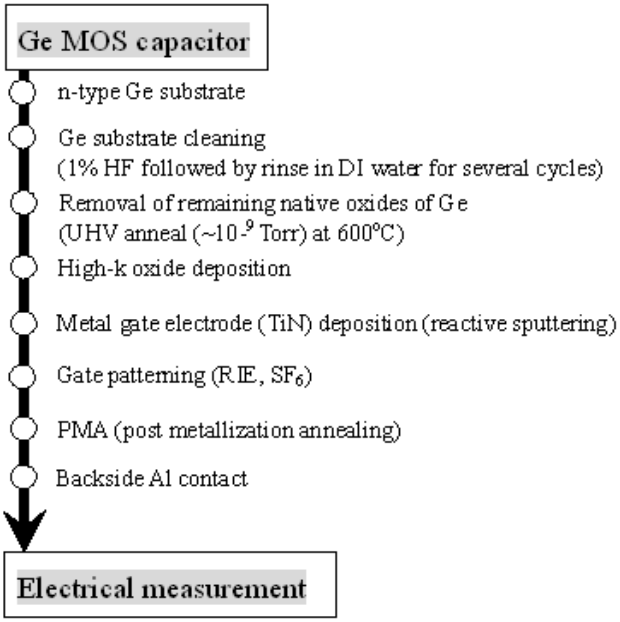

Figure 1. Fabrication process flow of Ge MOS capacitors.

After the chemical treatment with dilute HF (1%) followed by rinsing in de-ionized water for several cycle, *i.e.* leaving a H-terminated surface, the Ge wafers were then transferred into the MBE chamber to perform *in-situ* high-vacuum (~10^{-9} Torr) anneal at 600°C for 10 min in order do thermal desorption of the remaining native oxides of Ge. Thereafter, ultrathin $YTiO_x$ films having various thicknesses ranging between ~4-17 nm (measured using spectroscopic ellipsometer, Photal, FE 5000) were deposited on Ge by

electron beam (e-beam) evaporation under the pressure of ~$2x10^{-8}$ Torr at room temperature. The various TiO_x concentrations between 10-33% in $YTiO_x$ films have been fabricated while the TiO_x concentration was controlled by the calibrated thickness rate during $YTiO_x$ deposition. No additional substrate temperature was applied during the deposition while the deposition rate of both oxides was controlled to be 0.1 nm/min. Subsequently, a 50 nm-thick TiN layer was deposited using reactive sputtering. TiN gate-electrode was then patterned by conventional lithography and reactive ion etching (RIE) using SF_6 chemistry. Post deposition annealing was carried out at 450°C in FG (2.981% H_2) ambient for 1 min whereas post-metallization annealing, PMA was performed either in FG (2.981% H_2) or N_2 ambient at 500°C for 5 min using a rapid thermal annealing (RTA) furnace. Al was then deposited by thermal evaporation onto the backside to serve as a bottom electrode. In electrical characterization, the capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured using an Agilent E-4980A precision LCR meter and 4156C, respectively. The detail of the device fabrication process flow is summarized in Fig. 1.

Results and Discussion

Effect of TiO_x concentration on Electrical Properties of $YTiO_x$ Directly Deposited on Ge

The robustness of the $YTiO_x$ bulk oxide as well as $YTiO_x$/Ge interface is evidenced by the capacitance-voltage (C-V) and gate leakage measurements for the annealed MOS capacitors. The high-frequency (1 MHz) C-V characteristics of $YTiO_x$ having three different TiO_x concentrations in the range from 10-33 % are shown in Fig. 2.

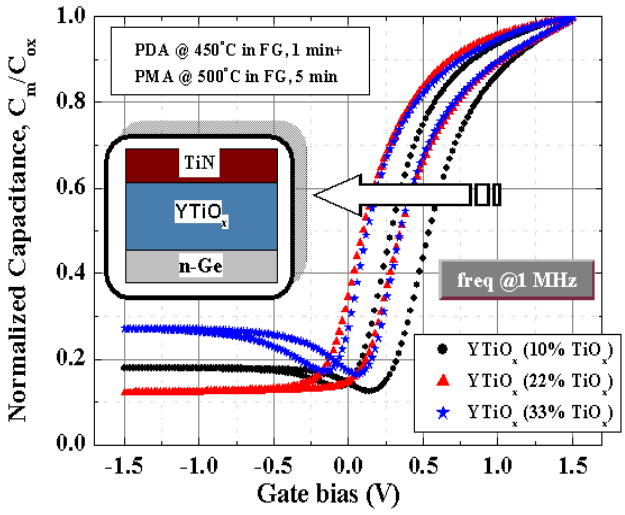

Figure 2. Effects of TiO_x concentration on high frequency (1 MHz) C-V characteristics of TiN/$YTiO_x$/n-Ge MOS capacitors with same physical oxide thickness have been compared.

The impact of TiO_x concentration in $YTiO_x$ films on flat band voltage shift even though considering hysteresis can be observed from the high-frequency (1 MHz) C-V characteristics for $YTiO_x$ samples with three different TiO_x concentrations in the range from 10-33% as shown in Fig. 2. A drastic change in flat band voltage shift towards even

less positive values with increasing TiO_x concentration from 10% to 22% has been observed while there is no further significant shifting in V_{fb} has been noticed even though considering hysteresis. Moreover, it has been noticed further that inversion capacitance generally increases with increasing TiO_x concentration demonstrating degradation of interfacial properties. It is worthwhile here that the dielectric constant increases with increasing TiO_x concentration in $YTiO_x$; e.g. it is $\kappa \sim 15 \pm 1$ for 10% TiO_x while it increases up to 25.4 for 33 % TiO_x concentrated $YTiO_x$. Apart from the advantage of κ value boost up by increasing the TiO_x concentration in $YTiO_x$, the leakage current is expected to rise further since higher concentration of TiO_x might cause to enhance the crystalline percentage in the film depending upon the annealing treatments. In fact, it has been observed that leakage current actually rises dramatically with increasing TiO_x concentration in $YTiO_x$ film as can be evidenced from Fig. 3.

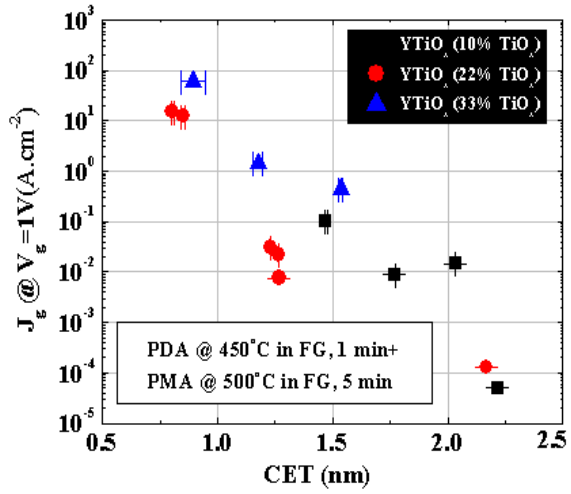

Figure 3. Gate leakage current density as a function of CET for $TiN/YTiO_x/n$-Ge MOS capacitors with several concentration of TiO_x. The error bars address uncertainty of CET extraction as well as statistical spread of gate leakage measurements.

The common approaches towards extracting the value of interface state density, D_{it} for Si MOS devices, namely the Terman, high-low frequency capacitance methods etc. cannot be fully applied to Ge MOS devices partly because carrier exchange between the interface states and the minority-carrier bondage influences the D_{it} extraction in the weak inversion regime (11-12). That is why; here conductance model has been utilized to extract the energy distribution of D_{it} only within the limited gate biases (12). Figure 4 shows the energy distribution of D_{it} for $YTiO_x$-based Ge MOS capacitors with different TiO_x concentration. Indeed, a moderate D_{it} values usually observed for Ge devices (CET:1.6-1.7 nm) are being obtained while D_{it} slightly increases with increase in TiO_x concentration. However, an average midgap D_{it} value of $\sim 5 \times 10^{12}$ $eV^{-1}cm^{-2}$ have been achieved for 22% TiO_x concentrated sample.

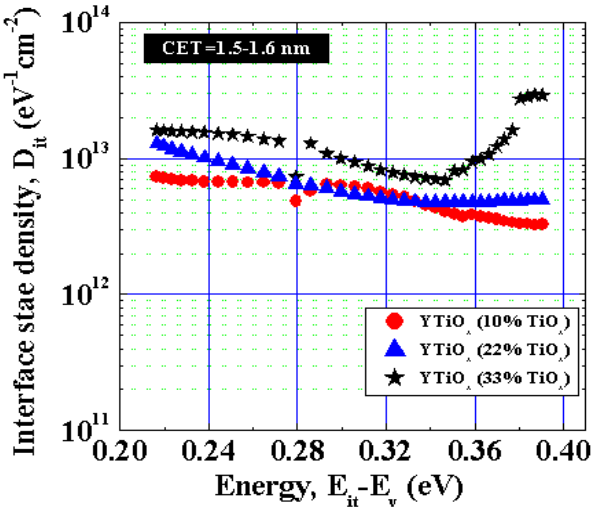

Figure 4. A comparison for energy distribution of interface state density for different TiO_x concentrated $YTiO_x$.

Moreover, we further examined that the level of D_{it} was quite high and still remained in the order of 5-9x10^{12} $eV^{-1}cm^{-2}$ even after receiving PDA and PMA treatment in N_2. Since a high Ti content in Ti-based oxide films may results in serious thermal-stability problems for gate dielectric application, hence, one needs to figure out the appropriate concentration of TiO_x such that a trade-off between leakage current and κ value boost-up can be maintained properly. Therefore, in this work we choose 22% TiO_x concentration to evaluate device performances in further detail.

Electrical characteristics of $YTiO_x$ (22% TiO_x) for scaled Ge MOS devices

The frequency dispersion in C-V characteristics of $YTiO_x$ having 22% TiO_x concentration is shown in Figs. 5(a)-5(c).

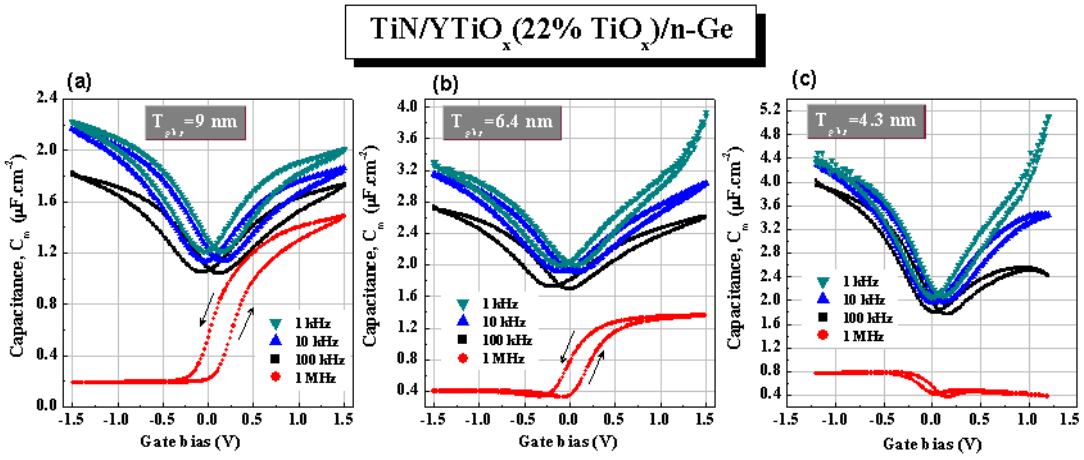

Figure 5. [(a)-(c)] Measured frequency dispersion in bi-directional C-V characteristics of TiN/$YTiO_x$/n-Ge MOS capacitors with different thickness of $YTiO_x$ having 22% TiO_x concentration.

In fact, a well behaved C-V stretch-out behavior with small hysteresis has been observed in general. Indeed, significant frequency dispersion in the strong inversion region is being observed for all kinds of oxide thickness, which is attributed to an increase in minority carrier generation due to diffusion of impurities from the dielectric into the substrate, or likely due to the interaction of interface slow states. Besides, a frequency dependent flatband voltage shift even taking into account hysteresis has been noticed which originates from the interface traps and may be a consequence of a week Fermi level pinning (13). Apart from that another noteworthy feature has been observed for the thinner oxides. In fact, the C-V measurements in the depletion as well as accumulation region additionally show a vertical shift with change in frequency towards its lower value, thus illustrating the growing influence of the interface trap density on the C-V behavior.

On the other hand, in order to examine the scalability with $YTiO_x$, the CET dependence electrical properties are investigated. First of all, the dielectric properties are being evaluated by considering various oxide thicknesses (T_{hk}) ranging from ~4-17 nm as shown in Fig. 6.

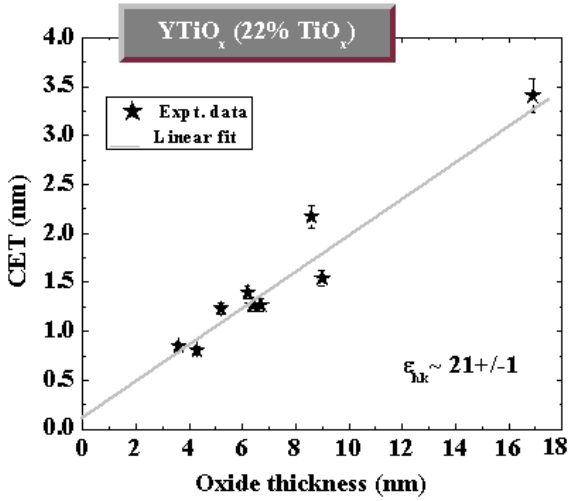

Figure 6. CET as a function of oxide thickness, T_{hk} for TiN/$YTiO_x$ (22% TiO_x)/n-Ge MOS capacitors. From the linear fit, the k value of the oxide is found to be ~21±1 with practically no interfacial layer, IL (IL equivalent thickness $T_{IL,eq}$=0.11±0.1 nm). The error bars address thickness measurement uncertainty as well as uncertainty of CET extraction.

In fact, a moderate dielectric constant of κ~21±1 has been extracted from the slope of capacitance equivalent thickness, CET vs. T_{hk} curve as is shown in Fig. 6 whereas the IL equivalent thickness, $T_{IL,eq}$ is found out to be 0.11±0.1 nm. Nonetheless, this result confirms that there is no re-growth of a GeO_x-based interfacial layer which may cause serious deterioration in electrical performance of the device. It is likely to some extent that Y-Ti-germanate may form spontaneously at the interface as a consequence of strong reaction of $YTiO_x$ with underlying Ge substrate as has also been observed in our earlier experiment with $YScO_x$ (14). Therefore, on the basis of these results, we may conclude that $YTiO_x$ provides a certain advantage in controlling the high-κ/Ge interface quality likely through forming stable Y-Ti-germanate which can act as a good surface

passivation layer as well as prevents to form Ge sub-oxide based interfacial layer during annealing treatment.

Meanwhile, a low gate leakage current density, J_g of ~2 x10^{-2} A.cm^{-2} (CET:~1.3 nm) has been achieved at a gate bias of +1V, which is in fact much lower than the ITRS requirements as well as it is also comparable with the regular promising dielectrics, such as GeO_xN_y, HfO_2, Al_2O_3 etc [15-17] (see Fig. 7).

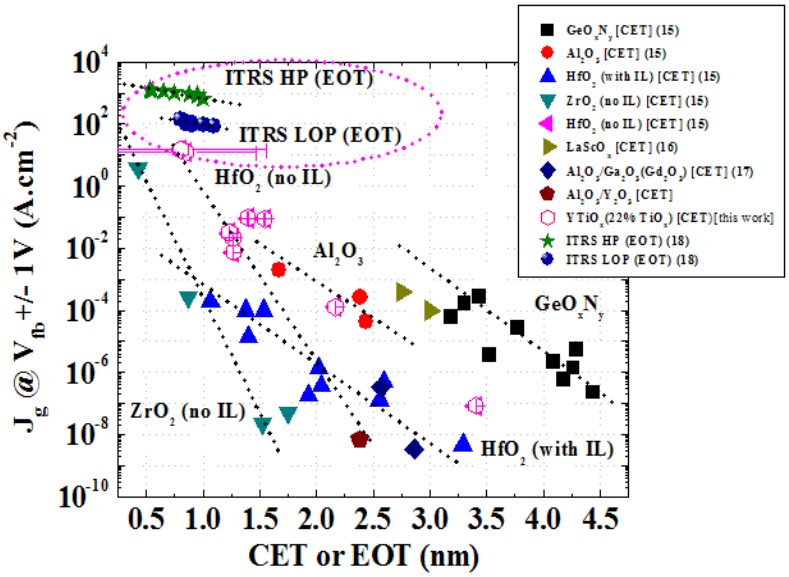

Figure 7. Gate leakage current density as a function of CET/EOT for TiN/$YTiO_x$ (22% TiO_x)/n-Ge MOS capacitors. The error bars address uncertainty of CET extraction as well as statistical spread of gate leakage measurements. CET data from this work is compared to the data taken from literature (Refs. 15-17) as well as with the leakage current density-EOT target values for HP and LOP applications taken from the ITRS 2009 update (18).

We performed room temperature conductance measurements to extract the interface state density. Figure 8(a) shows the typical interface trap conductance G_p/ω, as a function of the angular frequency ω, in the depletion-to-weak inversion surface potential regime for the as-deposited and post-FG annealed samples for 22% TiO_x concentrated $YTiO_x$. Particularly, two interesting features appeared upon decreasing the gate bias towards its negative value: (i) the G_p/ω peak increased in intensity gradually and moved towards lower frequency and (ii) the plateau in the ω range of ~700-10^3 s^{-1}had a higher magnitude. This phenomenon turns out to be dominated by the two main physical mechanisms that are responsible for the onset of the ac conductance loss peak: firstly, the carrier transition between the interface states near the Fermi level and the majority-carrier band edge, which predominantly governs at gate bias in depletion, and secondly, due to the contribution of dark current of the minority carriers that charge the inversion layer; they arise not only from the bulk traps within the depletion layer but also from the diffusion current from the bulk Ge. Nevertheless, based on the well observation that the generation and recombination of the bulk traps over the diffusion mechanism mainly contributes to the minority-carrier current at room temperature (19), however, we anticipate further that

in the weak inversion region the competition between bulk trap loss and interface state loss is intensified in some way.

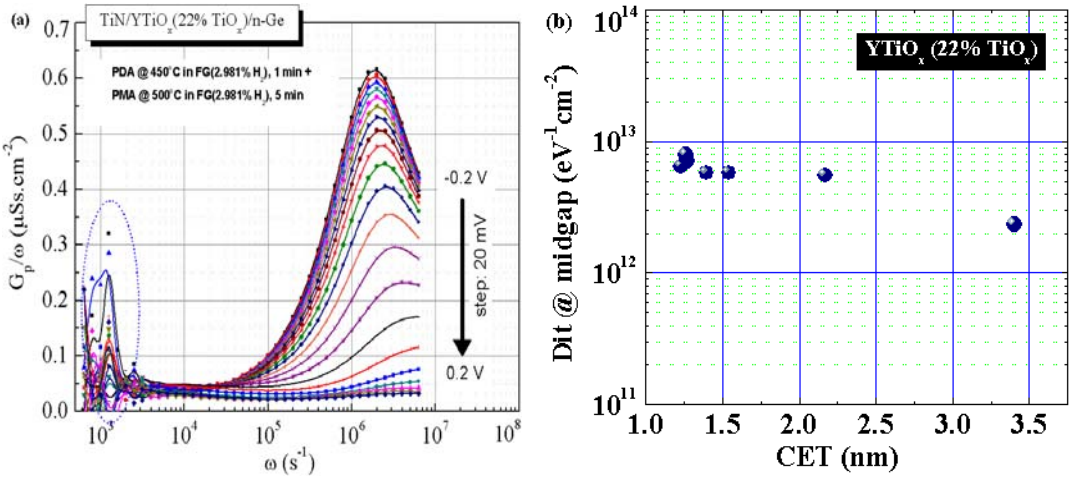

Figure 8. (a) Typical parallel conductance loss peaks in the frequency domain and (b) CET dependence of midgap D_{it} value for TiN/YTiO$_x$ (22% TiO$_x$)/n-Ge MOS capacitors. D_{it} extraction was done by conductance measurements at room temperature.

The observed resultant shift of the gate bias dependent G_p/ω reflects the fact that charging and discharging of the interface traps might dominate these energy losses. We anticipate that this insensitive conductance loss should be strongly related to the intrinsic properties of Ge; hence studies of temperature dependencies are required further which is currently under investigation. The CET dependence of D_{it} is summarized in Fig. 8(b). Apparently, the D_{it} value increases along with the reduction of CET. A value of $2x10^{12}$ $eV^{-1}cm^{-2}$ was obtained for relatively larger devices (CET: 3.4 nm), however, it continues to increase rapidly for scaled devices. Since the annealing condition (PDA at 450°C in FG for 1 min along with PMA at 500°C for 5 min) was identical for all scaled samples, the increase in D_{it} at smaller CET region is expected to be originated by diffusion of metal atoms or defects located at Ge substrate surface induced by TiN metal gate or perhaps due to increase in amount of crystallization in YTiO$_x$ film with downscaling. Nevertheless, the overall D_{it} values are still high enough to concern about reasonable FET performance including concerns with reliability issues and hence need to be improved further for the scaled Ge channel MOSFET devices.

Conclusion

In summary, the electrical properties of YTiO$_x$ directly deposited on Ge have been investigated. It has been demonstrated that higher TiO$_x$ concentration in YTiO$_x$ film may lead to substantial increase in dielectric constant values, however, at the same time trade-offs between dielectric constant and gate leakage as well as other interfacial parameters have been observed for which a suitable TiO$_x$ concentration needs to be selected since higher TiO$_x$ concentration might enhance the crystalinity of the deposited gate dielectric

as well as may cause serious concerns over thermal stability and reliability issues. Therefore, 22% TiO_x-concentrated $YTiO_x$ films were chosen to explore device performances with gate oxide downscaling since it can provide high enough dielectric constant (κ ~21±1). We were able to restrict the growth of GeO_x-based interfacial layer presumably by forming stable Y-Ti-germanate at the interface in consequence of spontaneous strong reaction between $YTiO_x$ and Ge substrate. It has also been demonstrated that $YTiO_x$ (22% TiO_x) can favorable compete with other regular promising dielectric for Ge devices in terms of meeting the requirement of gate oxide downscaling challenges. Nevertheless, the observed increase in interface state density with device downscaling reflects the influence of metal induced defects generated by TiN gate electrode itself or likely due to increase in crystallinity of $YTiO_x$ gate dielectric with downscaling. However, further improvements in interfacial properties can be possible through process optimization. Therefore, these studies recommend that $YTiO_x$ gate dielectric can be a promising high-κ candidate for future Ge MOSFETs.

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