Er Inserted Ni Silicide Metal Source/Drain for Schottky MOSFETs

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Abstract

A Schottky barrier height modulation technique for achieving a low Schottky barrier height in Ni silicide metal source/drain by Er layer insertion was reviewed. The effectiveness and possibility of the technique was demonstrated by fabricating Schottky barrier source/drain MOSFETs onto both bulk and SOI substrates.

1. Introduction

Schottky barrier source/drain MOSFET (SB-MOSFETs) is one of the most promising candidates for highly miniaturized CMOS devices, thanks to its shallow junction depth with low sheet resistance [1-5]. But, one the major obstacle for realizing high performance SB-MOSFETs was the presence of a relatively large Schottky barrier height at the junction. Larger Schottky barrier height makes it difficult to obtain higher drive current with SB-MOSFETs. Developing a method to reduce the Schottky barier hight is essential for realizing SB-MOSFETs. In this paper, we review our approach [6-7] on modulation of Schottky barrier of Si and Ni silicide contact by inserting Er thin layer at the interface.

2. Experimental

Figure 1 shows the fabrication process of Schottky diode structured samples. Both n- and p-type bulk (100) Si wafers were used as substrate. After cleaned in a mixed solution of H_2SO_4 and H_2O_2, the substrates were merged into a diluted HF and then inserted into a high vacuum sputter chamber. Er and Ni thin films were deposited subsequently onto the substrates by DC sputtering. Silicidation process was carried out at various temperatures ranging from 400°C to 700°C for 1 min. After the removal of un-reacted metals by chemical etching, Al back contacts were formed by thermal evaporation. The Schottky barrier heights were extracted form current-voltage (I-V) characteristics of the fabricated Schottky diodes.

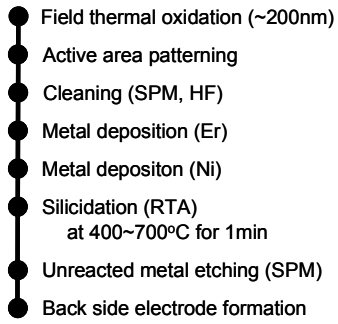

Figure 1. Fabrication process of Schottky barrier diode structured samples.

The fabrication process of n-channel SB-MOSFET is shown in Figure 2. Source/drain pre-formed p-Si(100) wafers with a SiO_2 top layer were used as starting substrates. After forming W/SiO_2 gate stack, Ni(12nm)/Er(7.2nm) layers were deposited. Pure Ni(12nm) layer samples were also fabricated. Silicidation process was carried out by annealing the samples at 600°C for 1 min. After the un-reacted metals were etched, an Al back contact was formed. All samples were annealed in a forming gas ambient (97%N_2 and 3% H_2) at 420°C for 30 minutes was carried out before the electrical measurement.

The fabrication process of SOI SB-nMOSFET was shown in Figure 3. The MOSFET was formed on the SOI wafers with a 100-nm-thick p-type SOI layer and a 200-nm-thick BOX layer. After patterning the SOI layer a SiO_2 layer was formed on the SOI layer by sputtering. The SiO_2 layer on the source/drain region was removed before depositing 55nm thick Ni layer with and without 7.2nm thick Er interlayer. The silicidation was performed at 600°C for 1 minute. The un-reacted metal was removed and then a backside Al gate electrode was formed.

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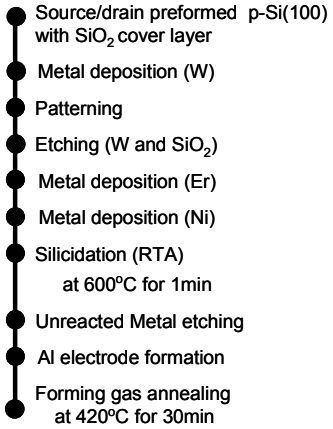

Figure 2. Fabrication process of n-channel SB-MOSFETs.

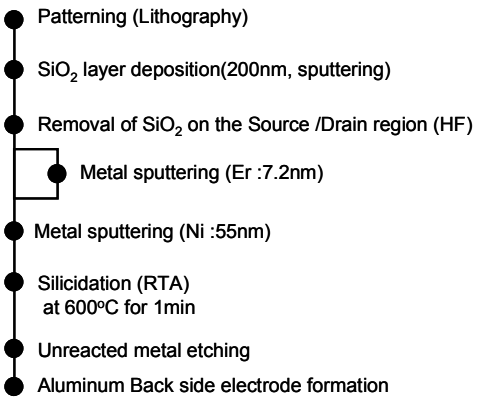

Figure 3. Fabrication process of SOI-SB-MOSFETs.

3. Results and Discussions

Schottky barrier height values for electrons were extracted from the obtained current-voltage (I-V) characteristics of the fabricated Schottky barrier diode structured samples and the results are plotted as a function of the annealing temperature in Figure 4. No significant change was observed in the Schottky barrier height with pure Ni slicide samples, while a significant decrease of Schottky barrier height with the increasing of annealing temperatures were observed for the Er layer inserted samples. A lowest Schottky barrier height of 0.42 eV was observed in a sample with 12nm thick Er interlayer after annealed at 700°C, a result is corresponding to a Schottky barrier height modulation of 0.22eV by Er layer insertion compare to the Schottky barrier height observed at the Ni silicide and Si contact. Obtained results indicating that, the Er insertion method is an effective method for Schottky barrier height modulation.

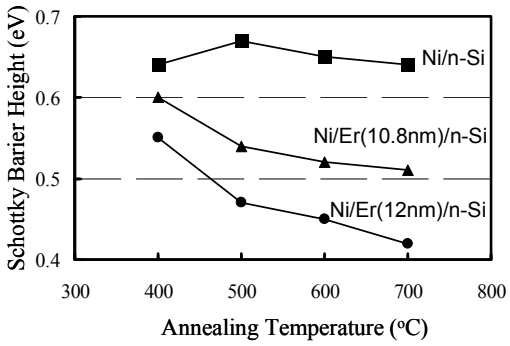

Figure 4. A plot of obtained Schottky barrier heights from the Schottky barrier diode structured samples as a function of thicknesses of the inserted Er interlayer and the annealing temperatures.

Employing the obtained results on the Schottky barrier height modulation method described above, planar type SB-MOSFETs were fabricated on to the source/drain pre-formed p-Si(100) substrates. Schematic of the fabricated SB-MOSFET is shown in Figure 5. MOSFET operation was confirmed and more than 25% increase in drain current was observed for the samples with 7.2nm Er inserted layer at Vg-Vth=3V as shown in Figure 6.

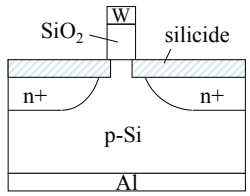

Figure 5. Schematic of the fabricated SB-MOSFETs.

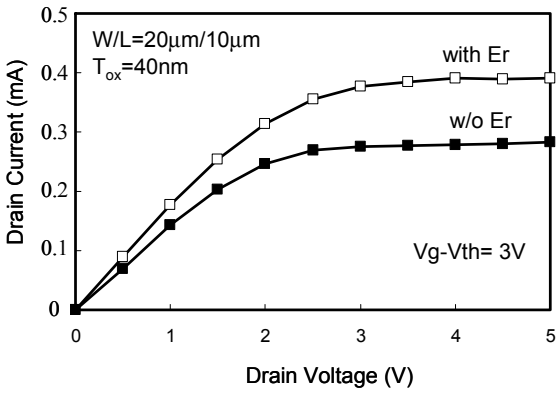

Figure 6. Drain current-Drain voltage charecteristcs of the fabricated SB-MOSFETs with and without Er layer insertion.

SB-nMOSFETs on SOI were also fabricated using Er

layer insertion method. An SEM image from Source/Drain and Channel junction region of one of the fabricated SOI SB-MOSFETs is shown in Figure 7. Drain current- Gate voltage characteristics of the fabricated SOI SB-MOSFETs with 7.2nm thick Er interlayer and without an Er layer are shown in Figure 8. Although the fabricated MOSFETs were back-gated and the gate oxide was very thick, a significant increase in Drain currents in the SOI SB-MOSFETs with Er interlayer were observed compare to those fabricated as references without Er interlayer insertion. The increase of the drain current can be understood as the result of the Schottky barier lowering by the insertion of Er interlayer. Obtained results from the SB-nMOSFETs fabricated on SOI show that the Er interlayer insertion method also effective for SOI SB-MOSFETs.

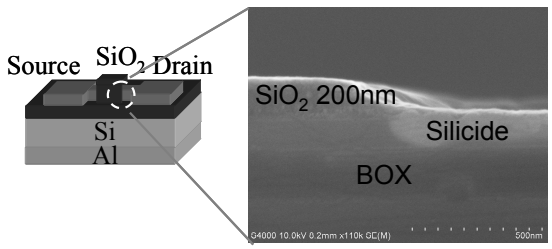

Figure 7. SEM image from Source/Drain and Channel junction region of the fabricated SOI SB-MOSFETs.

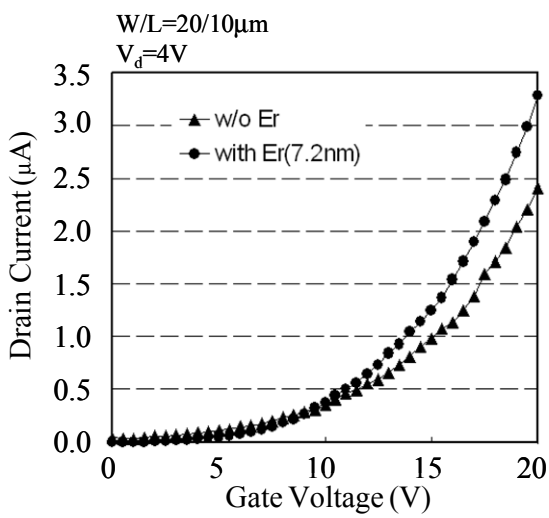

Figure 8. Drain current- Gate voltage charecteristcs of the fabricated SOI SB-MOSFETs with and without Er layer insertion.

4. Conclusions

A Schottky barrier height modulation technique, in which an Er layer was inserted between Ni layer and Si substrate before silicidation process, was proposed demonstrated and reviewed. Ni silicide metal source/drain SB-MOSFETs were fabricated onto both bulk and SOI substrates. It was observed that drain currents increase significantly in both bulk and SOI SB-nMOSFETs when Er interlayer inserted. Obtained results showed that the Schottky barrier height modulation technique by Er layer was inserted between Ni layer and Si substrate before silicidation process is one of the effective and promising method for Schottky barrier height modulation.

Acknowledgments

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