Towards the Ultimate Scaling of MOSFET Gate Dielectrics
- Direct Contact of High-k and Silicon-

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In this paper, we report our approaches in realizing high-k/Si interface without SiOx based interfacial layer by introducing Lanthanum silicates as interfacial layer at the interface of high-k dielectric and Si substrate. We also demonstrated the usefulness of 'Direct Contact' of high-k with Si through a lanthanum silicate interlayer in the scaling of EOT beyond 0.5nm.

Introduction

As a result of aggressive scaling of gate dielectrics in metal-oxide field effect transistors (MOSFET), SiO_2 based gate insulator thicknesses was already approached its limits of physical thickness as an insulator and replaced by Hf-based high-k dielectrics in some of the most advanced CMOS products with insertion of a thin SiOx based interfacial layer inserted at the interface between high-k dielectric and Si substrate to maintain device quality.

Figure 1 shows a schematic scaling tendency of equivalent oxide thickness (EOT) and its relation with power consumption in MOSFETs. Not only lower power consumption, there are also many other valuable benefits be obtained by the continuous scaling of MOSFETs. These benefits are continuously acting as the driving force from the beginning of MOSFET's history, pushing the technology to its ultimate scaling limit. With the scaling going on, elimination of the thin SiOx based interfacial layer inserted at the interface of high-k dielectric and Si substrate already become a problem only of time because of the SiO_x based interfacial layer limits further reduction EOT obtainable with high-k gate dielectric materials. However, eliminating the thin SiOx based interfacial between high-k dielectric and Si substrate bring about a great challenge to the CMOS technology since the interface between gate dielectric and Si substrate has always been SiO2/Si or SiON/Si in the past, no other interface than SiO_2/Si or SiON/Si was realized in Si CMOS technology. For eliminating the SiOx based interfacial layer, a direct contact of high-k material and Si which have a minimum thermal stability required by device fabrication processing should be realized. Realizing a device quality interface between high-k materials and Si substrate without a SiOx or SiON interfacial layer at the interface is also another great challenge. Although intensive researches were carried out on oxide thin films deposition onto Si (including epitaxial growth of oxides on Si), however, due to the poor thermal stability of most of the oxides with contact of Si (1), realizing a thermally stable direct contact of high-k material with Si is still a major obstacle in high-k gate stack technology.

In this paper, we report our approaches in realizing high-k/Si interface without SiOx based interfacial layer by introducing Lanthanum silicates as interfacial layer at the

interface of high-k dielectric and Si substrate. We also demonstrate the usefulness of our method in scaling of EOT beyond 0.5nm.

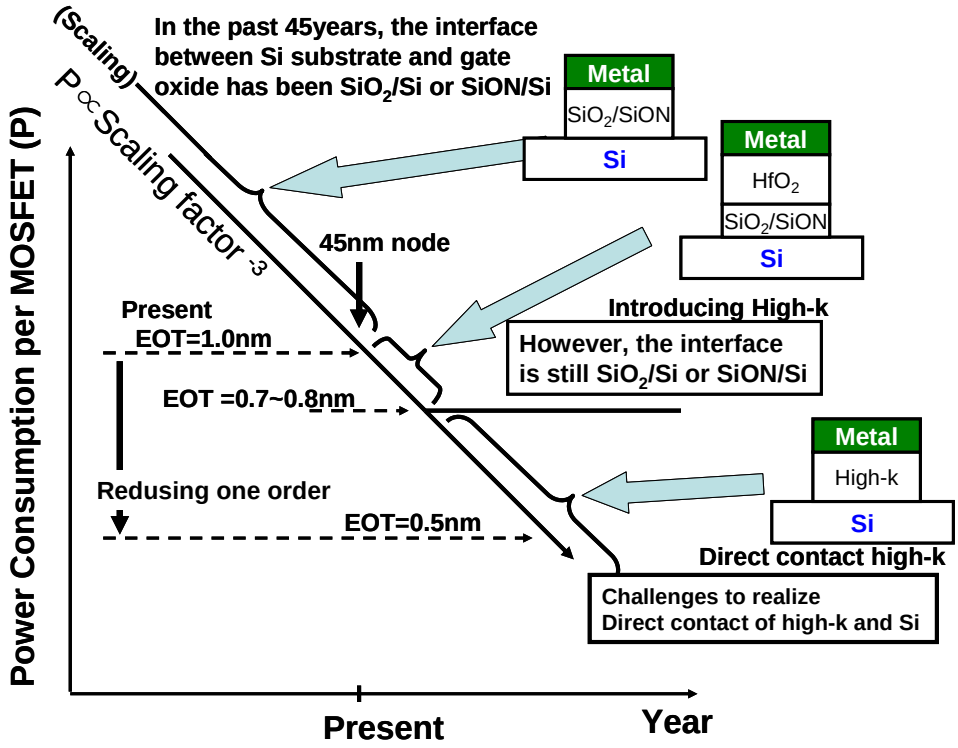

Figure 1. Scaling of EOT and its relation with power consumption.

Experimental

La_2O_3 thin film was deposited by e-beam evaporation in an ultra-high vacuum chamber on HF-last p-Si substrates. Tungsten (W) gate electrode was formed by RF sputtering without breaking ultra-high vacuum. After patterned by lithography and reactive ion etching (RIE), post-metallization annealing were carried out for the fabricated samples in a forming gas ambient (H2:N2 = 3:97%) at 300^{o}C and 500 ^{o}C for 30 min. Al was deposited on the source/drain region and back side of the substrate as contacts. Physical and electrical measurements were carried out for the necessary characterizations. A schematic diagram of fabrication process of La_2O_3 gated MOSFET is shown in Figure 2. Typical gate length and gate width of the measured devices were 2.5 micrometer and 50 micrometer, respectively.

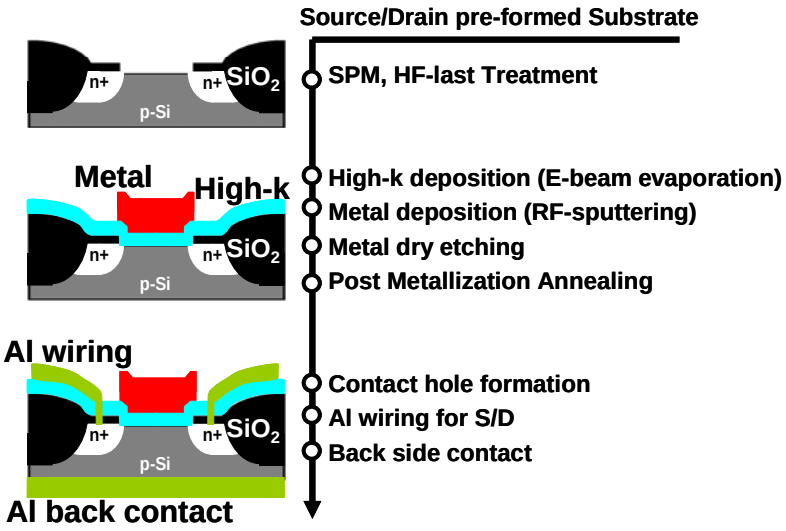

Figure 2. A Schematic diagram of La_2O_3 gated MOSFET fabrication process.

Results and Discussions

A typical La_2O_3/Si interface structure after proper annealing process is shown in Figure 3. Formation of La-silicate layer at the interface was confirmed by chemical analysis (2). From electrical characterizations of the fabricated samples, k-values of formed La-silicate layers were estimated to be in the range of from 8 to 12, a very high k value compare to that of SiOx based interfacial layers. By using such an interfacial layer which having higher-k value than that of SiOx layers at the interface of high-k dielectrics with silicon, it is expected to achieve the scaling EOT down to beyond 0.5nm, a value which is difficult to realize with SiOx based interfacial layers in high-k gate stack technology. Indeed, MOSFET with EOT as low as 0.37 nm has been demonstrated with La_2O_3 gate dielectric (3). Obtained Id-Vd characteristics of a W/La_2O_3 MOSFET with EOT 0.48 nm shown in Figure 4 indicating that the promising gate dielectric properties as well as the thermal stability in the scaling of the EOT down to below 0.5nm. It was also observed that, drain current increases with the scaling the EOT from 0.48 nm to 0.37 nm (not shown).

So far, the thermal stability of oxides on Si has always been one of the principal problems in high-k research because of a proper heat treatment is essential in the device fabrication process. Except a few known thermally stable oxides on Si, such as SiOx and SiON which cannot be used in the future scaling of EOT because of their relatively low k value, most of the oxides do not have the thermal stability when it is directly contacted to Si. This thermal instability of the interface between high-k and Si causes EOT increment during the needed thermal process for device fabrication. Our results show that forming an optimized Lanthanum silicate layer or other proper silicate layers at the interface is one of a promising way to overcome the thermal stability problems of high-k materials contacting with Si.

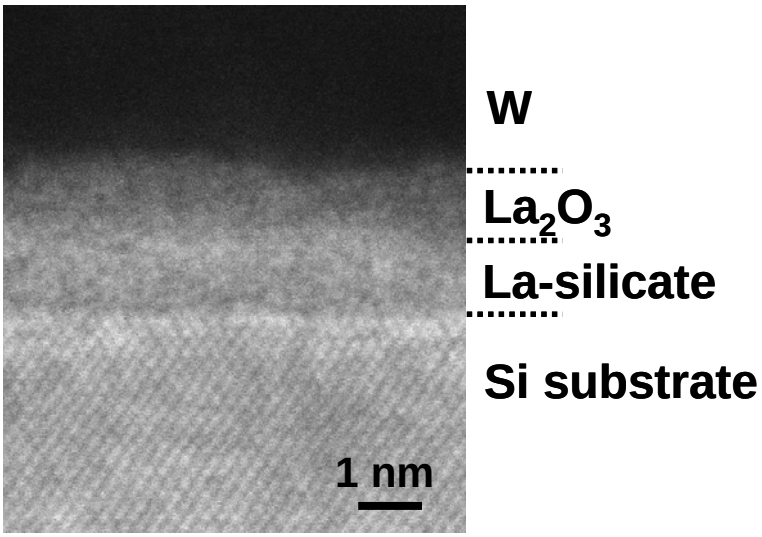

Figure 3. Cross sectional TEM image of La_2O_3/Si after annealing at 500^{o}C for 30 min.

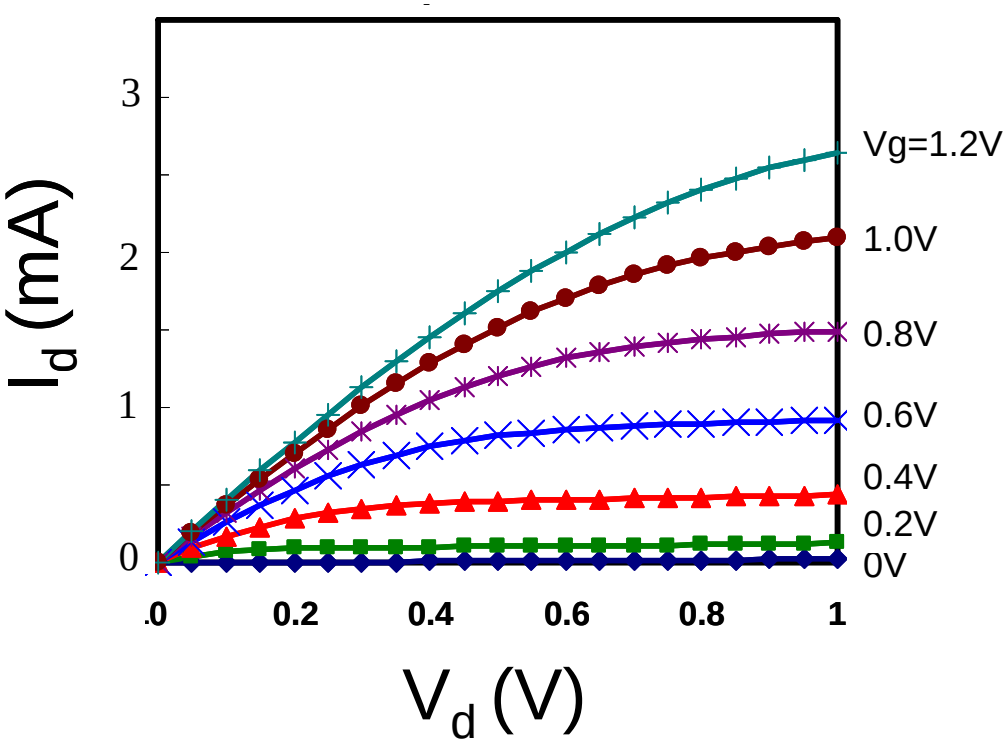

Figure 4. Id-Vd characteristics of a W/La_2O_3 MOSFET with EOT 0.48 nm.

Conclusions

The usefulness of Lanthanum silicate layer formed at the interface of high-k dielectric and Si in realizing 'Direct Contact' of high-k with Si was demonstrated. Using this method, MOSFET with EOT below 0.37 nm has been fabricated. With scaling the EOT from 0.48 to 0.37 nm, a sufficient increase in drain current was also observed.

Our results show that the 'Direct contact' using silicate layer would be one the most promising method for ultimate scaling of MOSFET Gate Dielectrics beyond 0.5nm.

Acknowledgments

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References

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