

Doctorial Thesis

**A Study on Gate-stack Process
for Ge MOS Devices
with La₂O₃ Gate Dielectric**

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Abstract

In order to achieve further device improvement beyond the limit of planar SiO₂/Si MOS devices, researches for high-mobility channel materials and high dielectric constant (high-k) materials for gate insulator have been necessary. Ge-channel has attracted much of attention due to the highest hole mobility in semiconductor and twice higher electron mobility than Si. In many high-k dielectric materials, La₂O₃, is more attractive than other high-k materials in terms of high dielectric constant (~27) and large band-gap (5.7eV) in the bulk state. In this study, therefore, gate-stack process of Ge-MOS structure with La₂O₃ high-k gate dielectric has been investigated for future Ge-channel MOSFET.

From the results for the samples after post-deposition annealing (PDA) treatment in inert N₂ ambient, it has been found that interfacial reaction between La₂O₃ and Ge is less than that between La₂O₃ and Si, which indicates the formation energy of La-germanate is larger than that of La-silicate. Despite the less reaction with La₂O₃ film, thermodynamic diffusion of Ge atoms by PDA is larger than that of Si atoms. Interface trap density (D_{it}) in La₂O₃/Ge structure can hardly be reduced by hydrogen annealing as opposed to the La₂O₃/Si structure. D_{it} reduction can be achieved by a growth of Ge-oxide and/or La-germanate interfacial-layer. In this case, simultaneously grown Ge sub-oxide causes to generate large amount of oxide trap density, which can be observed in large hysteresis characteristic on C-V curves.

The diffusion of Ge atoms and the growth of Ge sub-oxide can be completely suppressed by introduction of Si-passivation layer over 1nm on Ge substrate before La₂O₃ deposition. La-silicate formation by reaction between the La₂O₃ and Si layer during annealing also helps to decrease the oxide trap density caused by oxygen vacancy of La₂O₃. In addition, Lower D_{it} can be obtained with amorphous-phase Si layer as compared to the crystallized Si layer. Drain current increment in La₂O₃/Ge p-MOSFET has been also observed by using of Si-passivation layer. Especially, larger hole-mobility and better subthreshold slope characteristic in p-MOSFET can be achieved with amorphous-phase Si layer as compared with crystallized Si layer. On the other hand, critical degradation in electron-mobility for La₂O₃/Ge n-MOSFET with Si layer has been found. This degradation is considered to originate in band structure of Si and Ge which has similar electron affinity, causing the electron transport in channel region to take place in Si layer. Superior La₂O₃/Ge p-MOSFET characteristics with Si-passivation layer is expected for appliance of p-MOSFET in CMOS technology with n-MOSFET using Si-channel or compound semiconductor channel.

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Chapter 1.

Introduction

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- 1.2 Ge-based MOS Devices
- 1.3 Search for Next Generation high-k Gate Dielectric
- 1.4 Purpose and Organization of this Study

1.1 Limits of Planar Si MOS Devices Scaling

Since the invention of Si-based metal-oxide-silicon field effect transistor (MOSFET) [1-1, 1-2], there has been an unprecedented evolution in semiconductor industry. Nowadays large-scale-integrated circuits (LSIs) using complementary-MOS (CMOS) technology have been widely used as a main controlling unit everywhere in our life such as manufacturing, communication, healthcare, etc., which has become inevitable tools for living. The progress of LSIs has been accomplished by enormous increase in the number of transistors in accordance with Moore's Law proposed in the 1970s [1-3, 1-4]. Figure 1-1 shows the number of bits in DRAM [1-5] and that of transistors in a chip of intel's CPU [1-6]. The solid line called Moore line corresponds to Moore's Law, which fits well the number of bits or transistors at each year. As shown the Fig. 1-1, thousands of transistors in a chip in 1970s come to reach billions in 2000s.

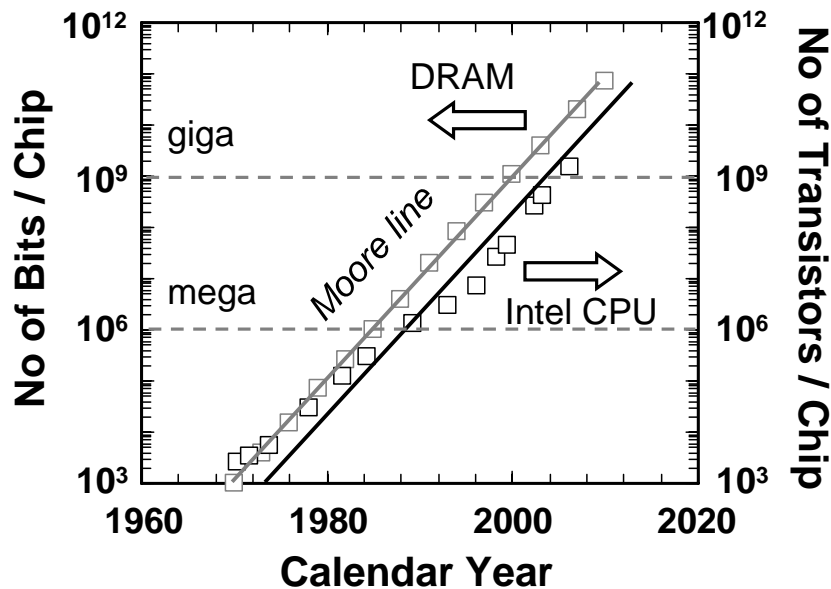


Figure 1-1. Scaling down of the number of bit in DRAM and the number of transistors in intel's CPU.

The tremendous increase in the numbers of transistors could be realized thanks to downsizing of MOSFET based on scaling rules proposed by R. Dennard [1-7, 1-8]. Scaling down of MOSFETs brings not only integration of transistors but also improvement of device performance. Figure 1-2 illustrates the concept of the scaling rule. Various dimensional parameters and supply voltage of MOSFETs should be scaled down by the same factor of k and substrate (and channel) doping concentration should be increased by the same factor k in order to shrink the depletion layer thickness by the same factor k . In consequence, the internal electric field of MOSFETs remains constant (called constant-field scaling) regardless of device size [1-9].

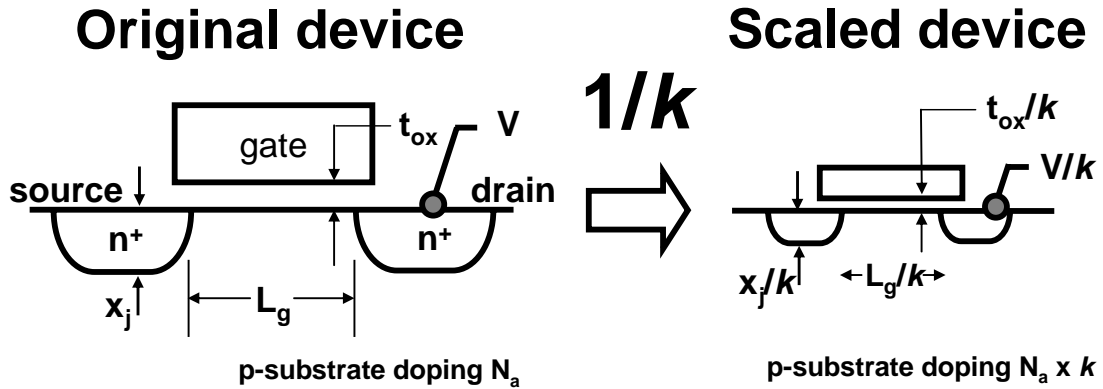


Figure 1-2. Downsizing of MOSFET and the concept of scaling rule.

In ideal scaling, the drain current (I_d) in MOSFETs downsized by the factor k can be written as

$$I_d = \frac{W}{L} \mu_{eff} \frac{\epsilon_{ox}}{T_{ox}} (V_g - V_t) V_d \propto \frac{1/k}{1/k} \cdot k \cdot \frac{1}{k} \cdot \frac{1}{k} \propto \frac{1}{k}, \quad (1-1)$$

where W and L are the gate width and length, T_{ox} is the gate oxide thickness, V_g , V_t , and V_d are gate voltage, threshold voltage and drain voltage, respectively. m_{eff} and e_{ox} are

effective mobility and permittivity of gate oxide, respectively, which are constant in SiO₂/Si structure. Also, signal-propagation delay time, t_d , can be written as

$$\tau_d = C_g \cdot R = \varepsilon_{ox} \frac{W \cdot L}{T_{ox}} \cdot \frac{V_d}{I_d} \propto \frac{1/k \cdot 1/k}{1/k} \cdot \frac{1/k}{1/k} \propto \frac{1}{k} \quad (1-2)$$

where C_g is the gate capacitance. Therefore, it is obvious that the downsizing of MOSFETs can decrease the switching time of the transistors. In addition, in the case of the ideal scaling rule, power dissipation (P) can be also reduced by k square, which can be expressed by Eq. (1-3),

$$P = V \cdot I \propto \frac{1}{k} \cdot \frac{1}{k} \propto \frac{1}{k^2}. \quad (1-3)$$

As the device area decreases by k square, circuit density can be increased by k square without increasing active power consumption per chip area.

Although the scaling rules have been brought the tremendous improvement in Si-MOS devices, downsizing of Si-MOS devices has been faced its fundamental limits recently. One is the limitation of gate-oxide thickness because the direct-tunneling occurs when the oxide is thinner than 3 nm [1-10]. The gate leakage current (I_g) occurred by direct-tunneling in MOS structure can be written as

$$I_g = \exp\left(-\frac{2\sqrt{2m_{SiO_2}}\Phi_B}{\hbar} T_{SiO_2-phys}\right) \cdot \exp\left(\frac{q}{\hbar} \sqrt{\frac{m_{SiO_2}}{2\Phi_B}} \cdot T_{SiO_2-phys} \cdot V_{SiO_2}\right) \quad (1-4)$$

where T_{SiO_2-phys} is physical thickness of SiO₂ gate insulator, m_{SiO_2} is tunneling mass of electron in the insulator, Φ_B is barrier height between Si and insulator and V_{SiO_2} is potential difference of oxide film [1-11]. Accordingly, it is thought that ultra-thin oxide does not act as an insulator because of significant leakage current. As shown in Fig. 1-3, equivalent oxide thickness (EOT) under 1 nm will be demanded after 2010. It is very hard to obtain normal MOSFET operation by using 1 nm SiO₂ due to the gate leakage

current. Thus, state-of-the-art technology focuses on the alternative gate dielectric with high dielectric constant (high- k) compared to silicon dioxide. As can be seen in Eq. (1-1), increase of permittivity (ϵ_{ox}) leads same effect of scale down of oxide thickness (T_{ox}). Therefore, scale-down of physical thickness in gate dielectric is not necessary with high- k gate dielectric for decreasing of EOT. This point is written as

$$EOT = \frac{\epsilon_{SiO_2}}{\epsilon_{high-k}} T_{high-k} \quad (1-5)$$

where T_{high-k} is physical thickness of high- k gate dielectric. Figure 1-4 also illustrates maintenance of same charge density with lower leakage current by using of high- k gate dielectric.

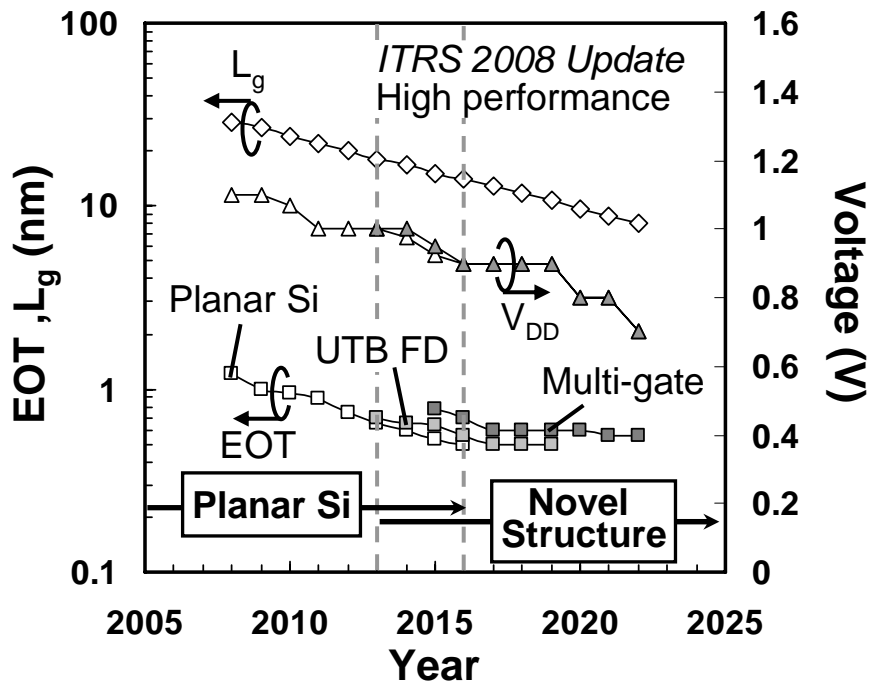


Figure 1-3. Demanded physical gate length, equivalent oxide thickness (EOT) and supply voltage for the next 15 years reported on ITRS 2008 update.

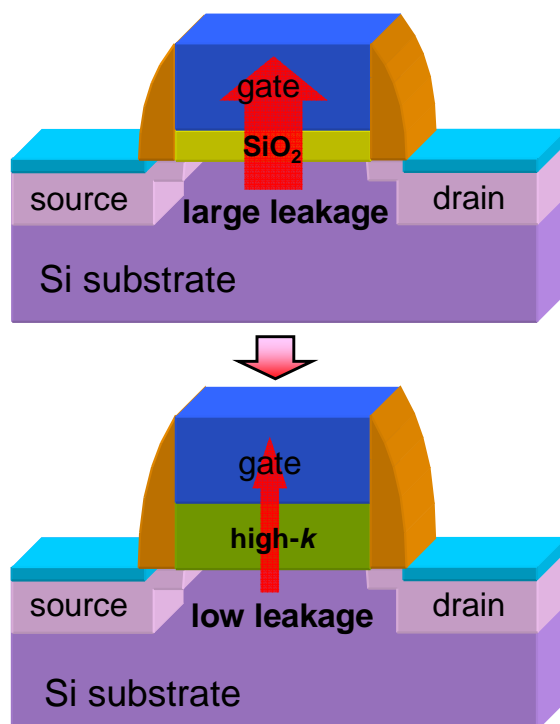


Figure 1-4. Illustration of high-k gate dielectric keeping the same charge density with lower leakage current.

In addition to the gate oxide limitation, it has been increasingly difficult to improve transistor performance with the downsizing of gate length due to the problem such as short-channel effect, velocity saturation of channel carrier, large series resistance of source/drain layers, increase of source/drain leakage current [1-12]. Thus, planar Si MOS devices is thought to be faced its scaling limit under gate length of 15~20 nm and the novel structure device such as ultra thin body fully-depleted (UTB-FD) silicon on insulator (SOI) MOSFETs and three-dimensional MOSFETs with double or surrounded gate has been proposed under gate length of 15~20 nm as shown in Fig. 1-3.

Considering the drain current equation (Eq. 1-1), increase of effective carrier mobility can be also alternative method to advance the performance without scaling. In fact, enhancement of carrier mobility is already realized by means of strained channel or change in channel direction [1-13 ~ 1-15]. To enhance the carrier mobility further, recently, high carrier mobility materials attract lots of attention. Especially, Ge has been extensively studied due to the highest hole mobility and twice higher electron mobility as compared with the case of Si as can be seen in table 1-1. Generally, high-k gate dielectrics are formed by deposition method on channel region, while SiO₂ gate dielectric is formed by thermal or radical oxidation of Si substrate. Insofar as using high-k gate dielectric, there is no need to use Si as a channel material by all means. Actually, there is also mobility degradation of Si MOSFET with high-k dielectric and that becomes worse with decreasing the EOT [1-16]. Therefore, achievement of performance improvement with high carrier-mobility channel will be expected.

Table 1-1. Electron and hole mobility in various semiconductors at 300k

	μ_e [cm ² /Vs]	μ_h [cm ² /Vs]
Si	1400	450
Ge	3900	1900
GaAs	8500	400
InP	4600	650

1.2 Ge-based MOS Devices

Historically, Ge was one of the most important semiconductors in the past and the first MOSFET was fabricated on Ge substrate. However, some inferior properties of Ge as compared to Si make Ge extinguish in semiconductor industry. Inferior properties in Ge are classified into two parts; one is Ge itself to use as a substrate and another is its oxide as a gate dielectric and field isolator.

Table 1-2 shows the inferior factors of Ge itself as compared to Si. First is hardness, second is thermal conductivity and finally deposit. As the hardness of Ge is smaller than that of Si, Ge substrate is more fragile. When a chip operates with a billion of transistors, a large amount of heat is generated and it must be emitted. As thermal conductivity of Ge is smaller than that of Si, heat in a chip with Ge substrate is hardly emitted and the chip is easy to overheat. Fundamental problem is that Ge exists very little even less than gold [1-17], while Si is one of the largest materials on earth. It goes without saying that the production cost using Ge substrate is higher than that using Si substrate. In order to resolve these problems about Ge substrate, some researches on the epitaxial growth of Ge on the Si substrate and strained germanium-on-insulator (s-GOI) wafer have been proceeded recently, which suggest that Ge is used as only channel region on Si substrate as shown in Fig. 1-5 and 1-6 [1-18,1-19]. Especially, it was proved that p-MOS transistor with s-GOI wafer had 4 to 5 times higher hole mobility rather than universal hole mobility of Si [1-19].

Table 1-2. The inferior properties of Ge substrate compared to Si substrate.

	Ge	Si
Mohs Hardness	6.0	6.5
Thermal Conductivity at 300 K (W/cm-°C)	0.6	1.5
Deposit (1000ton)	>0.5	large

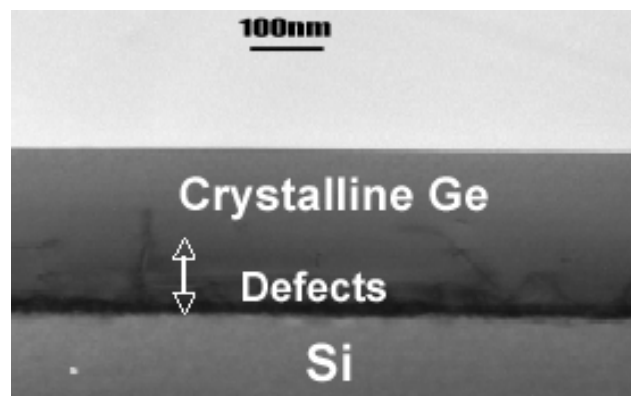


Figure 1-5. Epitaxial growth of Ge on Si substrate [1-18]

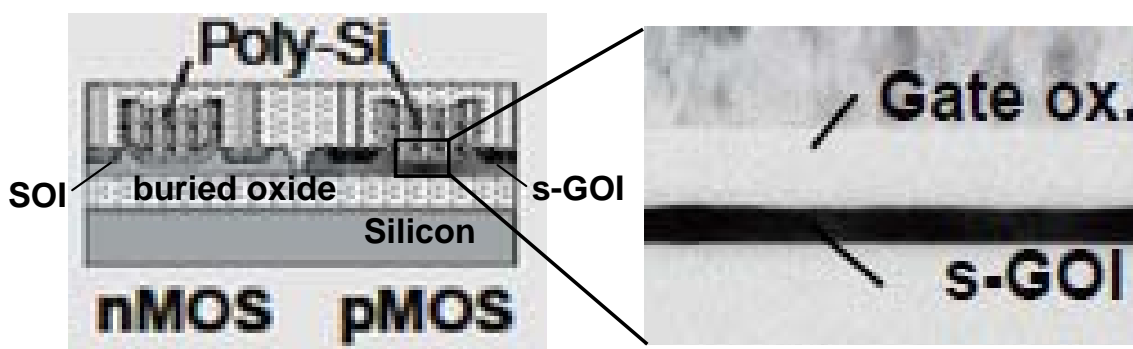


Figure 1-6. Strained germanium-on-insulator (s-GOI) structure fabricated by Ge condensation method [1-19].

Although the problems of using Ge as a substrate have been resolved, another big issue on Ge oxide is still remained. Ge dioxide (GeO₂) can be formed lower temperature than that of SiO₂; however, GeO₂ component decays and Ge sub-oxides are formed by annealing above 450 °C [1-20]. Though the electric properties of GeO₂ are not poor, the sub-oxides enlarge the hysteresis of Ge MOS capacitors [1-21]. Moreover, it is well known that Ge oxide is dissolved by dipping in water, which means that Ge oxide is inappropriate in wet processes. Considering that the wet processes are inevitable for reduction in cost, water solubility of Ge oxide is fatal for adopting Ge in semiconductor industry. For these reasons SiO₂, GeO_xN_y, Ge₃N₄, high-*k* materials such as Al₂O₃, ZrO₂, HfO₂, HfO_xN_y and Y₂O₃ have been studied as gate dielectric for Ge-based devices [1-22 ~ 1-40]. Especially, studies on Ge-MOS devices using high-*k* dielectric have increased recently in order to achieve smaller EOT without increasing the leakage current.

1.3 Search for Next Generation High-*k* Gate Dielectric

In making a choice among so many high-*k* materials, a sufficiently high dielectric constant, large band-gap and both conduction and valence band offset from substrate and thermodynamic stability are the key requirements for gate insulator application. Band-gap of several candidate oxides for gate dielectric is shown in Fig. 1-7, as a function of the relative dielectric constant. Figures 1-7 (a) shows data summarized from various international journals and conference [1-41] whereas Fig. 1-7 (b) is measurement results obtained from X-ray photoelectron spectroscopic (XPS) [1-42]. One can find the most promising dielectric in terms of the figure of merit given

by the product of the band gap and the relative dielectric constant. They are Al₂O₃, ZrO₂, HfO₂, La₂O₃, TiO₂, and etc.

Compared to other high-k materials, Lanthanum oxide (La₂O₃) is electrically hopeful for the gate insulator of the future MOSFET. La₂O₃ possesses high dielectric constant (~27) and large band-gap, especially higher band offset to silicon conduction band as shown in Fig. 1-7-(b). In addition, it has achieved smaller EOT with low leakage current, which seems better than Hf-based materials as shown in Fig. 1-8. In fact, La₂O₃ has been mentioned and reported in various versions of ITRS as the potential gate insulator for post-Hf generation, which is shown in Fig. 1-9.

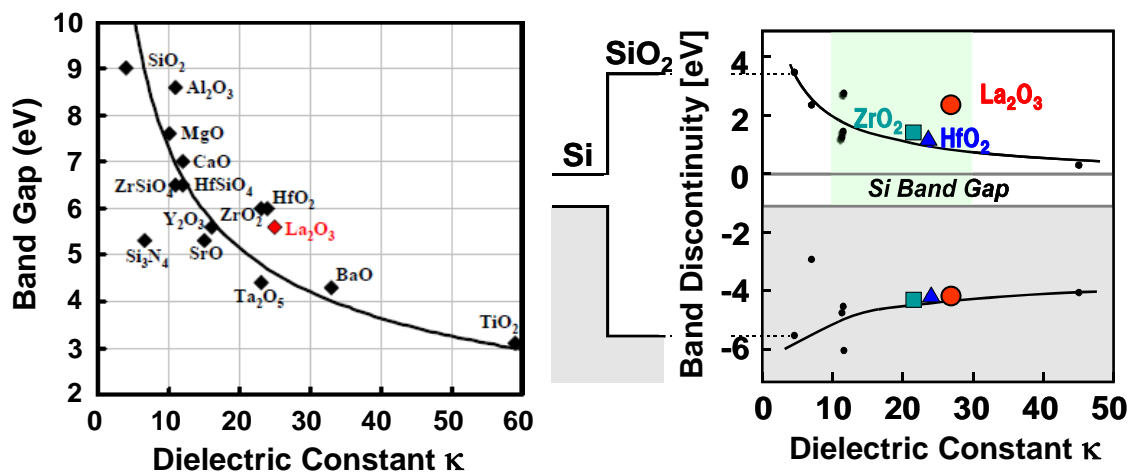


Figure 1-7. Band gap versus dielectric constant plots from (a) published data from journals and conference [1-41] and (b) experimental results from XPS [1-42].

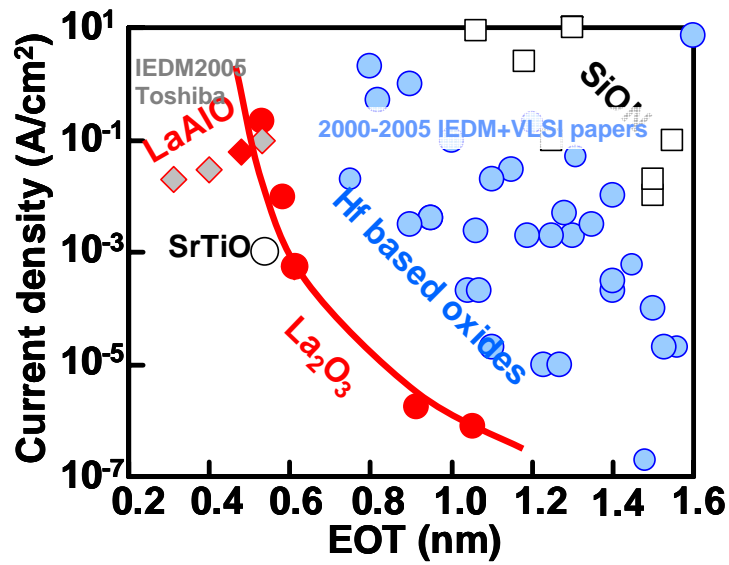


Figure 1-8. Leakage current density versus EOT plot for La_2O_3 and Hf-based high-k gate dielectric on Si substrate.

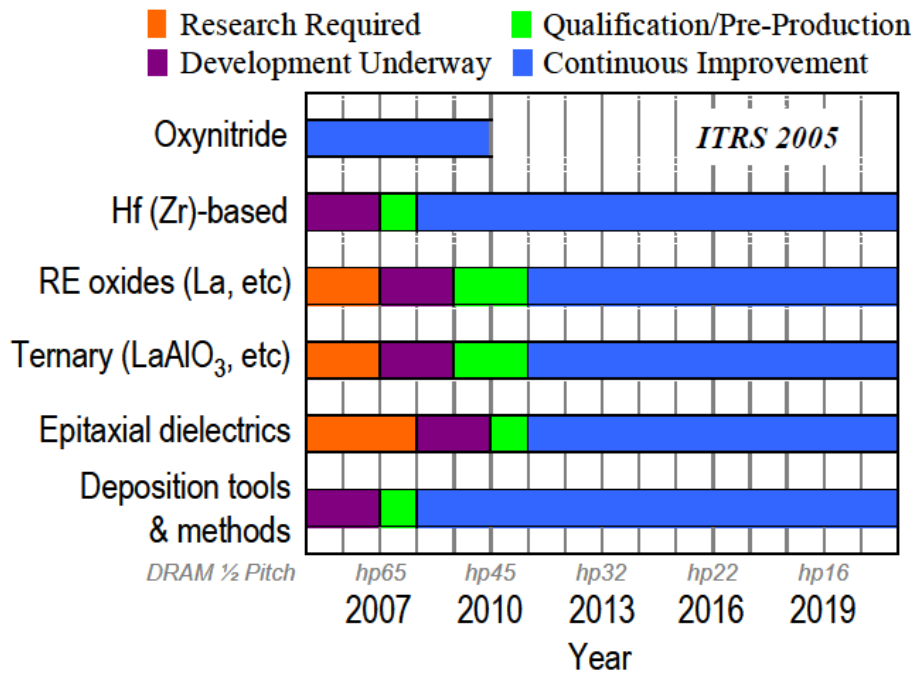


Figure 1-9. Roadmap of gate dielectric according to ITRS 2005.

1.4 Purpose and Organization of this Study

So far, motivation for alternative channel materials and gate dielectrics, and general properties of high-k materials has been discussed. It seems that Ge with high mobility is appropriate as an alternative channel material and La₂O₃ is good for the next-generation gate dielectric due to the high dielectric constant and large band-gap. Therefore, the objective of this study is to introduce the La₂O₃ as a gate dielectric of Ge MOS devices and examine the interfacial property and thermodynamic stability in La₂O₃/Ge MOS structure with various gate-stack processes, and also to fabricate and characterize the Ge MOSFETs with the proper process. To suggest the guidelines for getting high-performanced La₂O₃/Ge MOSFET based on whole study is set up as final goal.

The thesis consists of eight chapters, as illustrated in Fig. 1-10. Following this chapter, chapter 2 describes the fabrication and characterization methods used throughout this study. Specific fabrication flows of MOS capacitors and MOSFET and the basic principles behind all fabrication equipments are discussed. The measurement setups and characterization methods used in this study are also shown.

Chapter 3 is devoted to investigate the interfacial properties and reaction in directly contacted La₂O₃/Ge structure comparing with La₂O₃/Si structure. In this chapter, post deposition annealing (PDA) and post metallization annealing (PMA) was conducted in inert nitrogen (N₂) ambient with inert Platinum electrode to control needless reaction in MOS gate stack. Less reaction of La₂O₃ with Ge substrate compared with Si substrate by N₂ PDA has been observed, while diffusion of Ge atoms in La₂O₃ film is larger than that of Si atoms. Chapter 4 describes the effect of interfacial layer thermally grown by oxygen PDA after the deposition of La₂O₃ film and

chemically formed GeO₂ layer before La₂O₃ deposition. It has been found that thermally grown interfacial layer is Ge oxide layer and chemical GeO₂ layer react with La₂O₃ film by proper annealing resulting in formation of La-germanate layer. Interface trap density is well reduced by interfacial Ge oxide layer or La-germanate layer, while simultaneously grown Ge sub-oxide degrades the electric characteristic. In chapter 5, thermodynamic stability in leakage current density and interface property have been investigated with various metal gate electrode. *In situ* gate metallization process without air exposure after La₂O₃ deposition to suppress the moisture absorption of La₂O₃ film has been also studied. Very small EOT of 0.55 nm with leakage current density of 2.7×10^{-1} A/cm² can be achieved for W/La₂O₃/Ge structure prepared by *in situ* gate metallization process. In addition, hydrogen annealing effect is examined by introducing atomic hydrogen with Aluminum-capping layer on tungsten electrode.

Chapter 6 describes the effect of ultrathin Si passivation layer on Ge substrate in order to suppress the Ge diffusion and growth of Ge sub-oxide based on the result observed chapter 3, 4 and 5. Si passivation layer effectively improves the electric characteristics by preventing Ge from diffusing into La₂O₃ and restraining the growth of Ge sub-oxide layer. Three different phases of Si layer has been also investigated to achieve further improvement in interface properties between Si layer and Ge substrate. Amorphous Si layer shows quiet good interface properties with low interface trap density and oxide trap density. In chapter 7, Ge MOSFET has been demonstrated for the W/La₂O₃/Ge structure with or without Si passivation layer prepared by *in situ* gate metallization process. Finally, chapter 8 summarizes the findings in this study and suggests possible areas for further investigation.

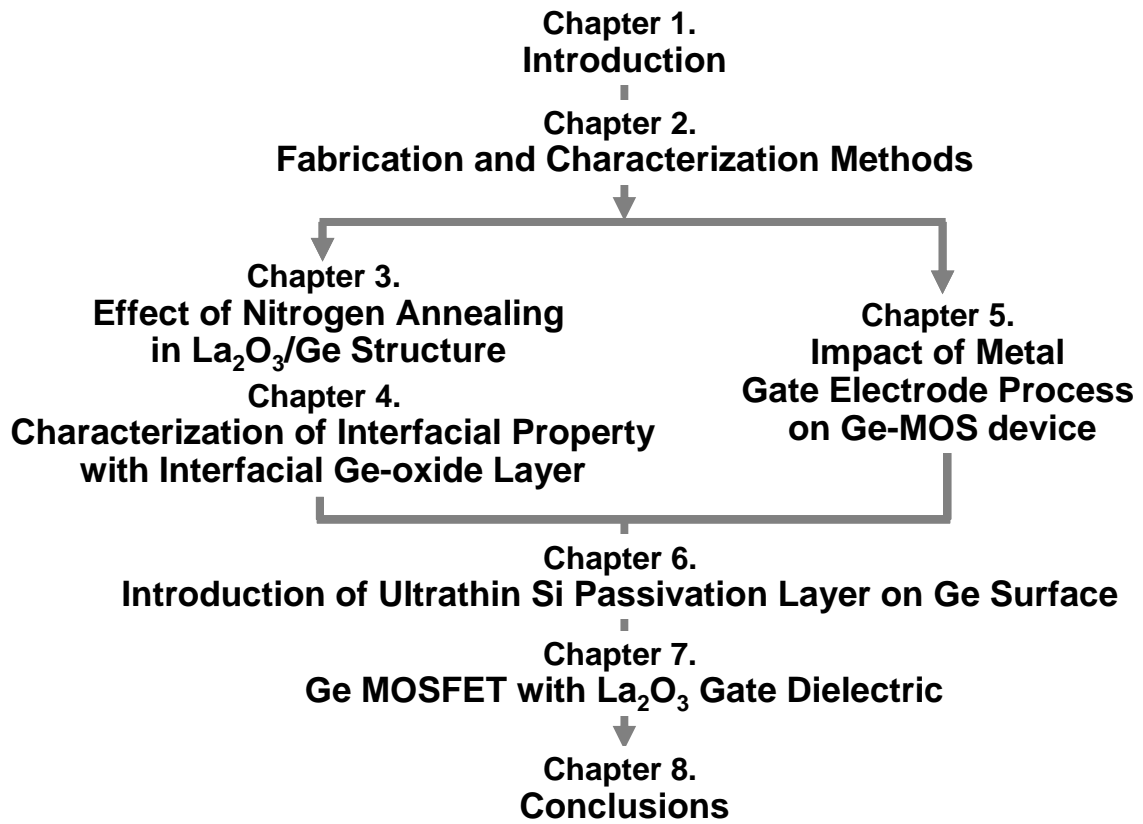


Figure 1-10. Outline and organization of this thesis

References

- [1-1] D. Kahng and M. Atalla, "Silicon-silicon dioxide field induced surface devices," IRE Solid-State Device Research Conference, 1960.
- [1-2] D. Kahng, "A historical perspective on the development of MOS transistors and related devices," IEEE Trans. Elec. Dev., vol. 23, pp. 655-57 (1976).
- [1-3] G. E. Moore, "Progress in digital integrated circuit," IEDM Tech. Dig., pp. 11-13, 1975.
- [1-4] G. E. Moore, "Microprocessors and integrated electronic technology," Proceedings of the IEEE, vol. 64, no. 6, pp. 837-841, June 1976.
- [1-5] ESSDERC 2004 Tutorial: Nanotechnology and Emerging Devices.
- [1-6] <http://www.intel.com/technology/mooreslaw/index.htm>
- [1-7] R. H. Dennard, F. H. Gaensslen, K. Kuhn and H. N. Yu, "Design of micron MOS switching devices," *IEDM Tech. Dig.*, p. 24, 1972.
- [1-8] R. H. Dennard, F. H. Gaensslen, H-N, Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," IEEE J. Solid-State Circuits, vol. SC-9, pp. 256-268, 1974.
- [1-9] Y. Taur and T. Ning, *Fundamentals of Modern VLSI devices*, Cambridge, 1998. Chapter 4.
- [1-10] Y. Taur and T. Ning, *Fundamentals of Modern VLSI devices*, Cambridge, 1998. p.97 and p.190.
- [1-11] H. S. Momose, "Study on Si transistors with high performance and high reliability for CMOS/BiCMOS integrated circuits", PhD thesis, Tokyo Institute of Technology (2006).

- [1-12] Y. Taur and T. Ning, *Fundamentals of Modern VLSI devices*, Cambridge, 1998. Chapter 3-2.
- [1-13] S. Tiwari et al., "Hole mobility improvement in silicon-on-insulator and bulk silicon transistors using local strain," *IEDM Tech. Dig.*, pp. 939-41, 1997.
- [1-14] A. Shimizu et al., "Local mechanical-stress control (LMC): a new technique for CMOS-performance enhancement," *IEDM Tech. Dig.*, pp. 433-436, 2001.
- [1-15] K. Ota et al., "Novel locally strained channel technique for high performance 55nm CMOS," *IEDM Tech. Dig.*, pp. 27-30, 2002.
- [1-16] M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta, Y. Watanabe, K. Iwamoto, S. Migita, N. Yasuda, H. Ota, T. Nabatame and A. Toriumi, "Gate-First Processed FUSI/HfO₂/HfSiO_x/Si MOSFETs with EOT=0.5 nm," *IEDM Tech. Dig.*, pp. 523-526, 2007.
- [1-17] http://home.hiroshima-u.ac.jp/er/A_Japan_Sea/A3.PDF
- [1-18] K. C. Saraswat, C. O. Chui, T. Krishnamohan, A. Nayfeh, and P. C. McIntyre, "Ge based high performance nanoscale MOSFETs," *Microelectronic Engineering*, vol. 80, pp. 15-21 (2005).
- [1-19] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Hirashita, E. Toyoda, N. Sugiyama, T. Mizuno, and S. Takagi, "A new strained-SOI/GOI dual CMOS technology based on local condensation technique," *Symp. VLSI Tech. Dig.*, pp. 80-81 (2005).
- [1-20] A. Molle, M. N. K. Bhuiyan, G. Tallarida, and M. Fanciulli, "Chemical and structural investigation of the initial stages of germanium oxidation," *E-MRS spring meeting*, T9-02 (2006).
- [1-21] A. Toriumi, "Ge-MOSFET no kanouseito kadai," *Oyobuturi*, vol. 75(12), 2006, p. 1453-1460 [in Japanese].
- [1-22] L. L. chang and H. N. Yu, "The germanium insulated-gate field-effect transistor (FET)," *Proc. IEEE*, vol. 53, p. 316 (1965).

[1-23] S. V. Hattangady, M. J. Mantini, G. G. Fountain, R. A. Rudder, and R. J. Markunas, "The role of an ultrathin silicon interlayer at the SiO₂-Ge interface," *J. Appl. Phys.*, vol. 71, pp. 3842 (1992).

[1-24] D. ReinKing, M. Kammler, N. Hoffmann, M. Horm-von Hoegen, and K. R. Hofmann, "Germanium p-MOSFET's compatible with Si CMOS technology," in *Proc. ESSDERC*, pp. 300–303 (1999).

[1-25] R. S. Johnson, H. Niimi, and G. Lucovsky, "New approach for the fabrication of device-quality Ge/GeO₂/SiO₂ interfaces using low temperature remote plasma processing," *J. Vac. Sci. Technol. A*, vol. 18, pp. 1230–1233 (2000).

[1-26] J. J. Rosenberg and S.C. Martin, "Self-aligned germanium MOSFETs using a nitrated native oxide gate insulator," *IEEE Elec. Dev. Lett.*, vol. 9, pp. 639-640, (1988).

[1-27] T. N. Jackson, C. M. Ransom and J. F. DeGelormo, "Gate-self-aligned p-channel germanium MISFETs," *IEEE Elect. Dev. Lett.*, vol. 12, pp. 605 – 607, (1991).

[1-28] H. Shang, H. Okorn-Schmidt, J. Ott, P. Kozlowski, S. Steen, E. C. Jones, and H.-S. P. Wong, "High Mobility p-channel Germanium MOSFETs with a Thin Ge Oxynitride Gate Dielectric," *IEEE IEDM Tech. Dig.*, pp.441-444 (2002).

[1-29] T. Yashiro, "Determination of trap levels in Ge N and barrier energies at the Ge N-Ge interface by C-V characteristics," *Jpn. J. Appl. Phys.*, vol. 10, pp. 1691-1697 (1971).

[1-30] T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, and Y. Morita, "Ge metal-insulator-semiconductor structures with Ge₃N₄ dielectrics by direct nitridation of Ge substrates," *Appl. Phys. Lett.*, vol. 85, pp. 3181-3183 (2004).

[1-31] S. Iwauchi and T. Tanaka, "Interface properties of Al₂O₃-Ge structure and characteristics of Al₂O₃-Ge MOS transistors," *Jpn. J. Appl. Phys.*, vol. 10, pp. 260-265 (1971).

[1-32] Z. Benamara, S. Tizi, M. Chellali, and B. Gruzza, "Experiments in MIS structure based on germanium and improvements of the interfacial properties," *Materials*

Chemistry and Physics, vol. 62, Issue 3, pp.273-276 (2000).

[1-33] C. H. Huang, M. Y. Yang, Albert Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very Low Defects and High Performance Ge-On-Insulator p-MOSFETs with Al₂O₃ Gate Dielectrics," Symp. VLSI Tech. Dig., pp. 119-120 (2003).

[1-34] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A sub-400°C germanium MOSFET technology with high-k dielectric and metal gate," IEEE IEDM Tech. Dig., pp. 437-440 (2002).

[1-35] H. Kim, C. O. Chui, P. C. McIntyre, and K. C. Saraswat, "Local epitaxial growth of ZrO₂ on Ge (100) substrates by atomic layer epitaxy," Appl. Phys. Lett., vol. 83, pp. 2647-2649 (2003)

[1-36] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS Characteristics with CVD HfO₂ Gate Dielectrics and TaN Gate Electrode," VLSI Symp. Tech. Dig., pp. 121-122 (2003).

[1-37] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, and B. J. Cho., "Effect of surface NH₃ anneal on the physical and electrical properties of HfO₂ films on Ge substrate," App. Phys. Lett., vol. 84, pp. 3741-3743 (2004).

[1-38] Q. C. ZHANG, N. WU, C. X. ZHU, "The Electrical and Material Properties of HfO_xN_y Dielectric on Germanium Substrate," Jpn. J. Appl. Phys., vol. 43, pp. L1208-L1210 (2004).

[1-39] C. -C. Cheng, C. -H. Chien, C. -W. Chen, S. -L Hsu, M. -Y. Yang, C. -C. Huang, F. -L. Yang, and C. -Y. Chang, "Impact of post-deposition-annealing on the electrical characteristics of HfO_xN_y gate dielectric on Ge substrate," Microelectronic Engineering, vol. 80, pp. 30-33 (2005).

[1-40] H. Nomura, K. Kita, K. Kyuno, and A. Toriumi, "Thermally Robust Y₂O₃/Ge MOS Capacitors," Ext. Abstr. SSDM, pp. 858-859 (2005).

[1-41] J. Robertson "High dielectric constant gate oxides for metal oxide Si transistors," Rep. Prog. Phys., vol. 69, pp. 327 (2006).

[1-42] T. Hattori, T. Yoshida, T. Shiraishi, K. Takahashi, H. Nohira, S. Joumori, K. Nakajima, M. Suzuki, K. Kimura, I. Kashiwagi, C. Ohshima, S. Ohmi, and H. Iwai, "Composition, chemical structure, and electronic band structure of rare earth oxide/Si(100) interfacial transition layer," *Microelectronic Engineering*, vol. 72, pp. 283-287 (2004).

Chapter 2.

Fabrication and Characterization Method

- 2.1 Ge MOS Capacitors and MOSFET Fabrication
- 2.2 Fabrication Process
- 2.3 Characterization Method

2.1 Ge MOS Capacitors and MOSFET Fabrication

2.1.1 Ge MOS Capacitors Fabrication

Figure 2-1 shows the fabrication process of Ge MOS capacitors. Ge MOS capacitors were fabricated on n-type Ge (100) wafers with resistivity of 1.9~2.4 $\Omega\cdot\text{cm}$. Ge wafers were cleaned by chemical solution such as $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1/2/20) treatment or cyclic dipping of diluted-hydrofluoric acid (DHF) treatment and de-ionized (DI) water. After that, the wafers were transferred into ultra-high vacuum (UHV) chamber ($\sim 10^{-8}$ Pa) and annealed at 500-600 °C to remove the Ge oxide completely. La_2O_3 films were deposited by electron-beam evaporation using La_2O_3 tablet as a source under pressure of $\sim 1 \times 10^{-6}$ Pa at the substrate temperature of 250 °C. After the La_2O_3 deposition, post-deposition annealing (PDA) was carried out under various gas conditions such as nitrogen (N_2), oxygen (5% $\text{-O}_2 + \text{N}_2$), hydrogen forming gas (3% $\text{-H}_2 + \text{N}_2$) ambient at various temperatures. Gate electrodes such as Pt, Ta, W and Pt/Si, Al/W dual layer were formed by electron-beam evaporation or magnetron sputtering method. Some samples were subjected to post-metallization annealing (PMA) after gate electrode deposition. MOS capacitors were completed after deposition of backside Al layer for ohmic contact.

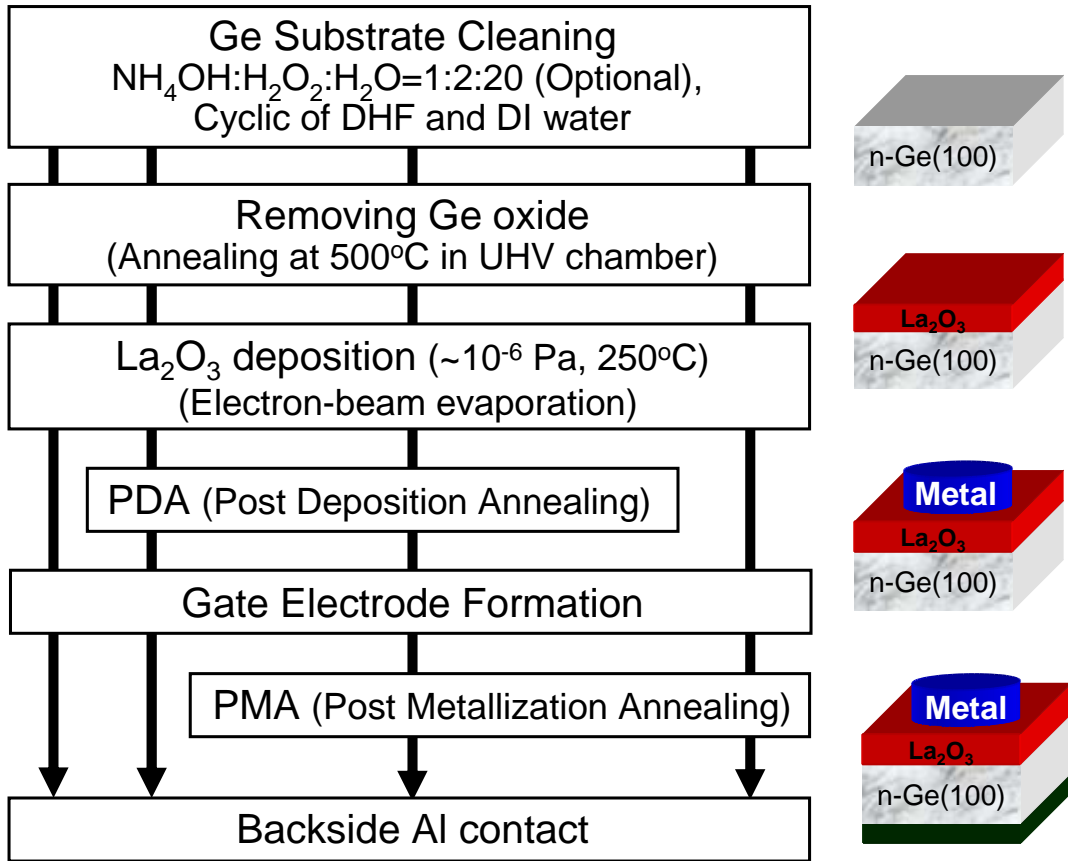


Figure 2-1. Fabrication process of Ge MOS capacitors.

2.1.2 Ge MOSFET Fabrication

Ge MOSFETs were fabricated with a conventional self-aligned process, which the process flow is shown in Fig 2-2. In this study, a ring-shaped gate electrode was used for simplicity, because the isolation process is not necessary. The MOSFETs and the MOS capacitors were fabricated using the same gate-stack fabrication processes on the same substrate. The p^+ and n^+ source and drain (S/D) were formed by BF_2^+ and P^+ implantation respectively, followed by activation annealing. Then PMA was conducted covering activation annealing of S/D. Next, contact hole of S/D and Al wiring was fabricated and finally backside Al layer was deposited for ohmic contact.

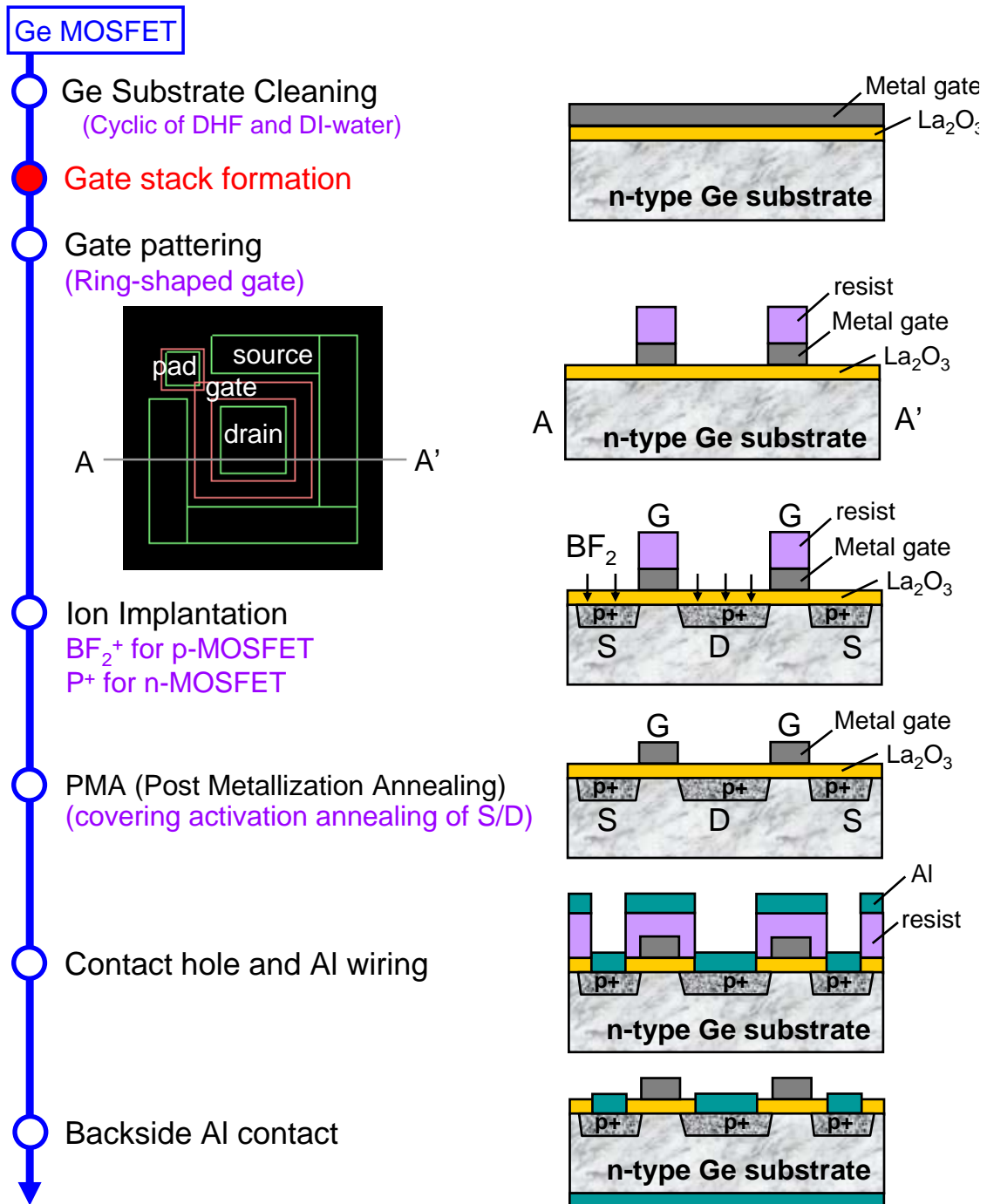


Figure 2-2. Fabrication flow of Ge MOSFET.

2.2 Fabrication Process

2.2.1 Ge Substrate Cleaning

For deposition of high quality thin film, ultra clean surface is required, without metallic, organic and ionic contaminations, particles, native oxide. It has been reported that surface region of Si wafers is contaminated with various matters when it is as-received. It being similar in case of Si substrate, C, O and Sn related XPS signals was detected on the surface of as-received Ge(100) wafers [2-1].

The Si substrate is cleaned by the RCA cleaning process, which was proposed by W. kern et al. [2-2]. In case of Si, The surface oxide was removed completely with HF treatment, and HF-last surface does not oxidize soon in air. On the other hand, chemical-cleaning method for Ge surface has not been established yet. XPS results show that Ge sub-oxide still remained after HF treatment (see Fig. 2-3), which means Ge-oxide can not be removed easily by HF treatment. In order to achieve the ultra-clean surface, alternative method forming GeO₂ as a passivation layer and performing annealing in ultra-high vacuum (UHV) chamber has been proposed [2-3, 2-4]. Figure 2-4 shows the XPS results for the samples with or without annealing in UHV chamber at 600 °C for 5 min. Ge sub-oxide was removed completely for the sample after annealing in UHV chamber. Moreover, H. Okumura et al. proposed more useful NH₄OH/H₂O₂/H₂O (1/2/20) treatment to form the protective Ge oxide layer. It is effective for removal of particles by NH₄OH treatment, moreover, organic and/or metallic contaminations was not detected by Auger electron spectroscopy measurement [2-1].

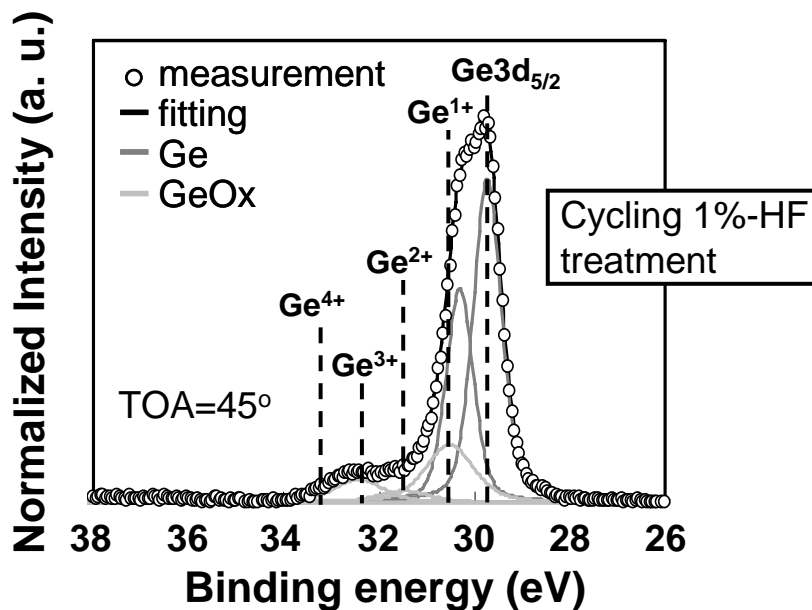


Figure 2-3. Deconvoluted XPS spectra of Ge3d from Ge substrate with cyclical treatment of dipping in 1%-HF solution and de-ionized (DI) water.

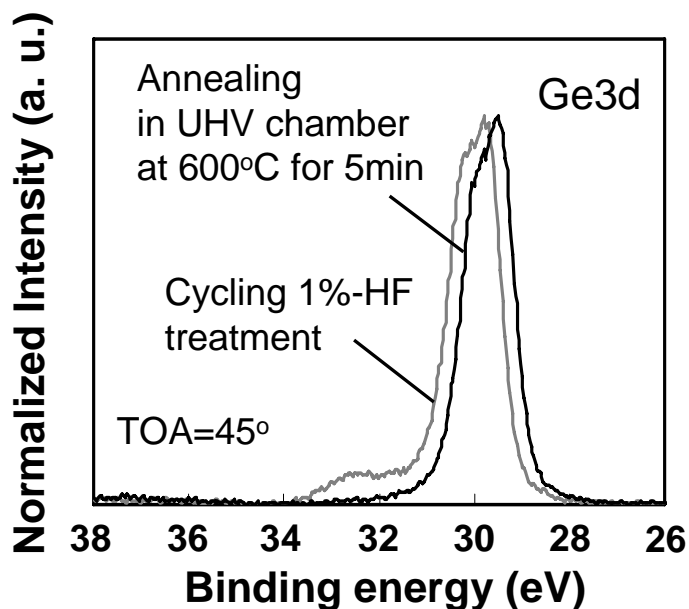


Figure 2-4. XPS spectra of Ge3d from Ge substrate with cyclical treatment of dipping in 1%-HF solution and DI water and with annealing in UHV chamber at 600°C.

2.2.2 Electron-beam Evaporation of La₂O₃

As discussed in various literatures and reports, the high-k gate dielectric film must be deposited on the substrate. Various deposition methods have been proposed such as ALCVD, LPCVD, MOCVD, sputtering and e-beam evaporation [2-5]. In this study, La₂O₃ film is deposited by e-beam evaporation method in the UHV chamber, which is shown in Fig. 2-5. La₂O₃ tablet is heated by the electron-beam (E-beam) near the source. Then, since the chamber is maintained at the ultra high vacuum state, the LaO_x molecule begins to evaporate when the temperature of the source is larger than the evaporation temperature. Evaporation temperature is reported as 3620°C [2-6]. Figure 2-6 shows the equilibrium vapor pressure of La and La₂O₃ with some materials as a function of temperature.

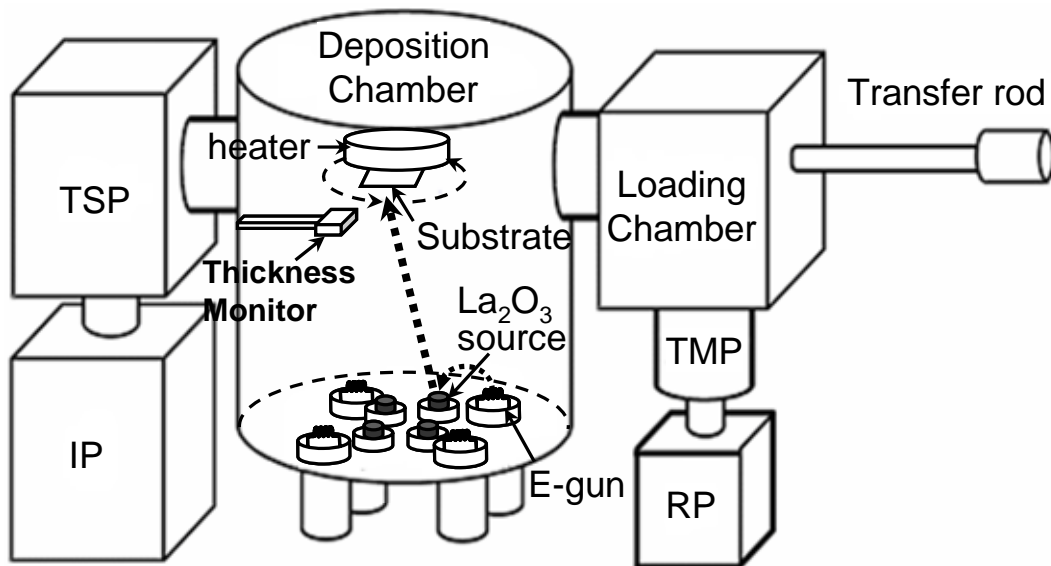


Figure 2-5. Schematic of the chamber for La₂O₃ film deposition.

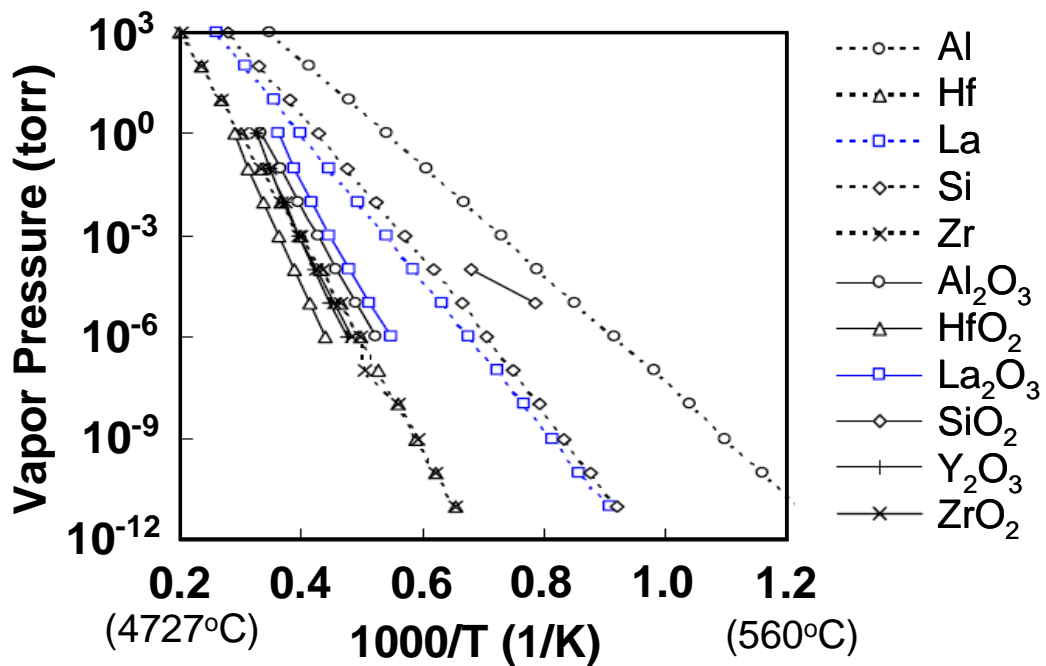


Figure 2-6. Equilibrium vapor pressure of La and La₂O₃ compared to some materials, as a function of temperature [2-7].

2.2.3 Electron-beam Evaporation for Gate Electrode

The schematic cross section of metal e-beam evaporation system used in this study for platinum (Pt), tantalum (Ta) and tungsten (W) gate evaporation is shown in Fig. 2-7. E-beams were accelerated by 4 KV before bombarded onto Pt source. Base pressure during metal evaporation is 10⁻⁴-10⁻⁵ Pa. Film thickness of metal electrode and evaporation rate are monitored by crystal oscillator throughout the whole evaporation process. Metal source used in this study has purity of 99.999 %.

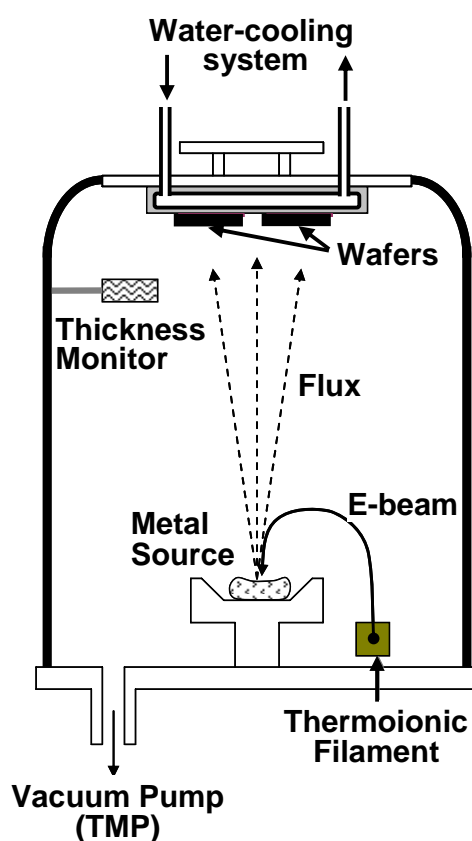


Figure 2-7. Schematic drawing of e-beam evaporation system for metal gate electrode deposition.

2.2.4 Thermal Evaporation for Al Layer

Aluminum (Al) evaporation in this study was formed by using bell-jar type thermal evaporation as illustrates in Fig. 2-8. This system utilized a turbo molecular pump (TMP) to achieve background pressure up to 1.0×10^{-5} Pa prior to Al evaporation. Filament which used to hold Al wires is made of tungsten (W). Purity of W filament and Al source is 99.999%. Methanol and acetone were used to clean the W filament and Al wires prior to every evaporation process. Chamber pressure during evaporation is 2×10^{-5} - 5×10^{-5} Pa.

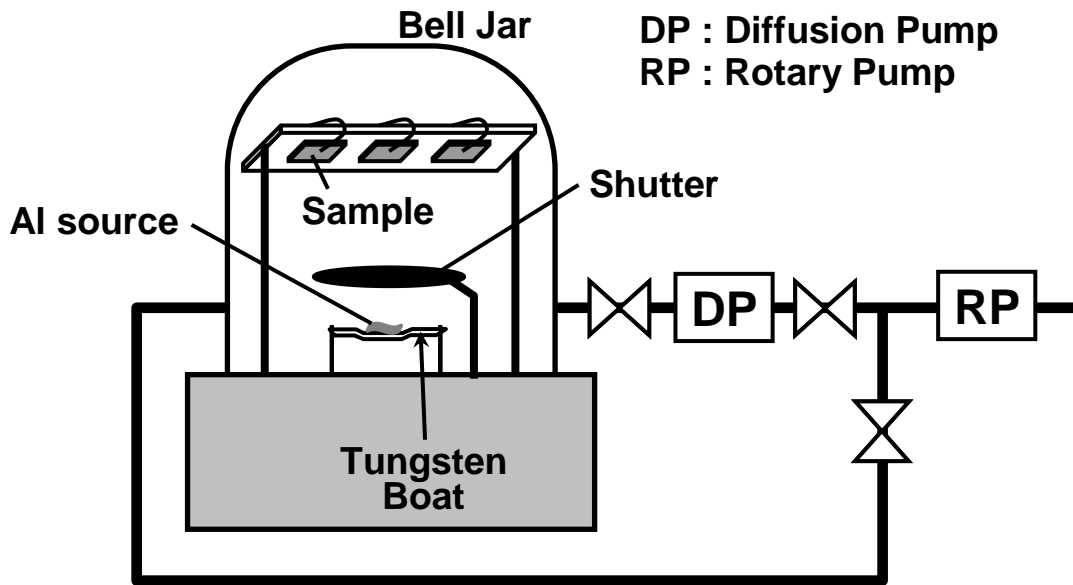


Figure 2-8. Schematic drawing of bell-jar type thermal evaporator.

2.2.5 Photolithography

The process flow of photolithography that used throughout this study is shown in Fig. 2-9. Electrical hotplate is used for baking purposes. Positive photoresist layer of S1805 (for dry etching) or S1818 (for wet etching) was coated on the sample by spin coater system followed by samples were baked (pre-baking) at 100 °C for 5 minutes. The spin-coated photoresist layer was aligned and exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. MJB3 of Karl-Suss contact-type mask aligner was used for aligning and exposition purposes. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.). Post-baking at 130 °C for 5 minutes is necessary to harden the developed photoresist pattern before metal gate etching.



Figure 2-9. Process flow of photolithography.

2.2.6 Metal Gate Etching

The etching process of Al, Pt, Ta and W metal gates were all different between each other. Basically, metal gate was etched by dry etching process for avoiding of La₂O₃ contacting with etchant and DI water due to the strong hygroscopic property of La₂O₃ except Al layer deposited on W electrode. Al layer on W electrode was etched by NMD-3 solution after development of gate pattern. Pt etching was carried out by physical Ar bombardment inside reactive ion etching (RIE) system. Ar flow rate and RF power is 30 sccm and 50 W, respectively. RIE was also performed to define Ta and W-based patterns with 50 sccm SF₆ gas at 30W. After the gate metal etching, photoresist layer on top of metal gate was removed by O₂-based ashing method inside the same RIE system.

2.2.7 Thermal Annealing Process

Thermal annealing processes are often used in modern semiconductor fabrication for defects recovery, lattice recovery or impurity electrical activation of doped or ion implanted wafers. In this study, low temperature (between 300°C–600°C) thermal treatments utilizing infrared lamp typed rapid thermal annealing (RTA) system were used. QHC-P610C RTA systems from ULVAC Co., were used for nitrogen (N₂), oxygen (5%-O₂+N₂) or forming gas (3%-H₂+N₂) annealing, either for post deposition annealing (PDA) or post metallization annealing (PMA). Figure 2-10 illustrates the schematic drawing for QHC-P610C RTA systems. Prior to every annealing cycle, existent gases inside the annealing chamber and gas lines were pumped by turbo molecular pump (TMP) to minimize any possibility of contamination of other residual gases or particles. This RTA system is heated-up by infrared lamp heating furnace and cooled-down by constant flowing of pipe water. Thus, it has an asymmetric profile of temperature ramping for heating up and cooling down. The ramp up rate of annealing temperature is set at 10 °C/sec. The gas flow rate is kept at 1.0 l/min for annealing cycles. All annealed samples were removed from the chamber under 100 °C.

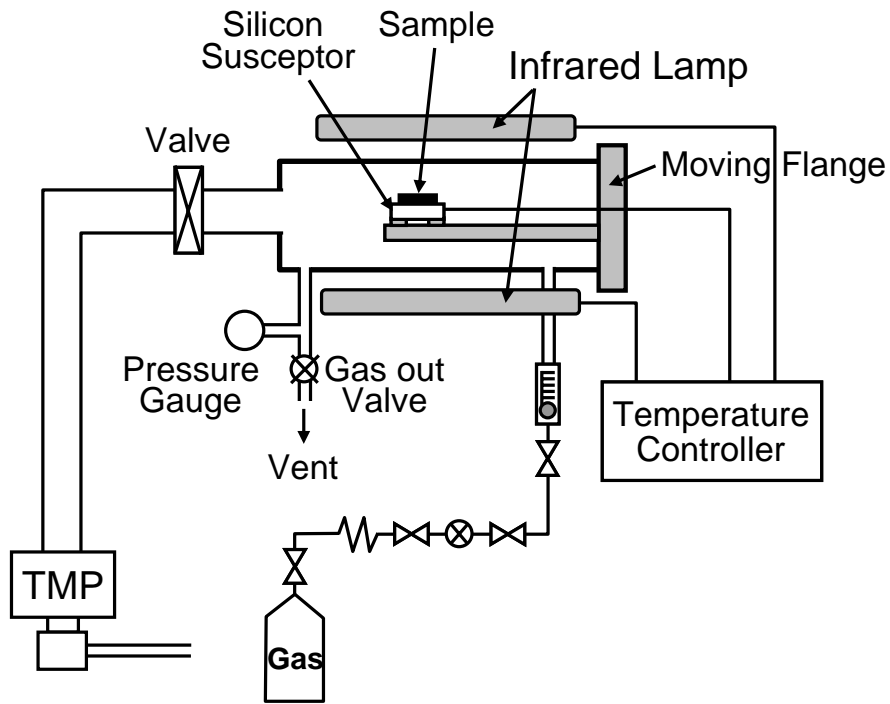


Figure 2-10. Schematic drawing for QHC-P610C RTA systems.

2.3 Characterization Method

In this sub-chapter, characterization method used throughout the analysis and evaluation of La₂O₃ MOS capacitors and MOSFET in this study will be discussed in details. Physical thickness of the deposited La₂O₃ films was analyzed optically by spectroscopic ellipsometry. Film thickness and structure of the interfacial layer was also confirmed physically by transmission electron microscope (TEM). The chemical bonding states of interfacial transition layer were analyzed by x-ray photoelectron spectroscopy (XPS). Electrical characterization of MOS capacitors was mainly performed by using capacitance-voltage ($C-V$) characteristics, gate leakage current density-voltage (J_g-V) characteristics and interface-trap density (D_{it}) calculated by conductance method. Drain current-gate voltage (I_d-V_g) characteristics for subthreshold slope (a.k.a. subthreshold swing) and threshold voltage (V_{th}) extraction, split $C-V$ method for effective mobility evaluation were used to examine the MOSFET characteristics.

2.3.1 Spectroscopic Ellipsometry

Spectroscopic ellipsometry is used predominantly to measure the thickness of thin dielectric films as a non destructive measurement technique.

The physical film thickness of La₂O₃ film was optically extracted by Otsuka FE-5000 ellipsometer using a Cauchy model and a single layer approximation [2-8]. Incident angle was fixed at 70°. Photon energy varied from 1.55 to 4.14 eV, which correspond to wavelength from 800 to 300 nm, was used for data fitting. Film thickness without PDA corresponds to the as-deposited film thickness.

The index increase with decreasing wavelength in the visible range, and this is referred to as normal dispersion [2-8]. One of the common empirical relations for this behavior is the Cauchy formula:

$$n = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \quad (2-1)$$

Here, n is refractive index of single wave length. A, B and C are all fitting constants. On the other hand, in the region of the natural frequency where resonance occurs, the index decrease with decreasing of wavelength and this is known as anomalous dispersion. Eq. (2-1) can be derived by the following way [2-8]. The square of the refractive index n , at frequencies far from the resonant frequency, is expressed by the relation:

$$n^2 = 1 + \frac{Ne^2/\pi m}{\nu_0 - \nu} \quad (2-2)$$

where N is the number of the atoms per unit volume, e is the electronic charge, m is the electronic mass, ν_0 is the natural frequency, and finally ν is the frequency of the incident radiation. If $\nu \gg \nu_0$, with the binomial series expansion, Eq. (2-2) becomes

$$n^2 = 1 + \frac{Ne^2}{\pi m} \frac{1}{\nu_0^2} \left[1 - \left(\frac{\nu}{\nu_0} \right)^2 \right]^{-1} = 1 + \frac{Ne^2}{\pi m} \frac{1}{\nu_0^2} - \frac{Ne^2}{\pi m} \frac{\nu^2}{\nu_0^4} \quad (2-3)$$

It is worth to introduce that densification of the films after PDA heat treatment can be evaluates by the film density obtained from the Lorentz-Lorenz relationship, in the similar fashion of SiO₂ thin film case [2-9]. From the refractive index n , the film density can be determined by the Clausius-Mossotti (CM) or Lorentz-Lorenz relationship [2-10].

$$\rho = K \frac{n^2 - 1}{n^2 + 2} \quad (2-4)$$

where K is a constant, which can be evaluated using the values of bulk La₂O₃.

2.3.2 Transmission Electron Microscopy (TEM)

Cross section of the fabricated samples was observed by transmission electron microscope (TEM). The principle of TEM is similar to that of optical microscope. In TEM, observation is made in ultrahigh vacuum, where an electron beam is focused onto the sample by electromagnetic lenses. Because the electron beam's wavelength is less than that of visible spectra, resolution of TEM is higher than the conventional optical type microscope. The thickness of the sample must not be greater than 0.1 μm in order for the electron beam to transit through the structure under study. Thus, special way of sample preparation has to be done prior to every cross section evaluation. In this study, Hitachi FB-2100 system which is a focus ion beam (FIB) system and equipped with micro-sampling module was used for sample preparation, which will be then transferred to Hitachi HD-2300 scanning transmission electron microscope (STEM) ultra-thin film evaluation system for observation and evaluation. Prior to transfer to HD-2300 system, TEM samples were treated and cleaned with ozone (O₃) plasma to reduce ion density on the sample's surface. Samples preparation and observation was done in Fujita laboratory of Tokyo University.

2.3.3 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as the Electron Spectroscopy for Chemical Analysis (ESCA), is one of the useful methods to detect chemical bondings in the oxide or at the interface. Figure 2-11 shows the Schematic of XPS equipment. Samples were irradiated with X-ray and the emitted photoelectrons with kinetic energy KE were detected. Measured KE was given by

$$KE = h\nu - BE - \phi_s \quad (2-5)$$

where $h\nu$ is the photon energy, BE is the binding energy of the atomic orbital from which the electron generates and ϕ_s is the spectrometer work function. Figure 2-12 explains the principle of XPS. The binding energy (BE) is the minimum energy which is necessary for breaking the chemical bond of molecule and is inherent in each bond of molecule. Thus, the binding states can be identified by the positions of the binding energy where the peak appears. In the case that the peak position is different from the expected one, the chemical bonding states would be discussed with considering the amount of shift toward higher or lower energy side [2-11].

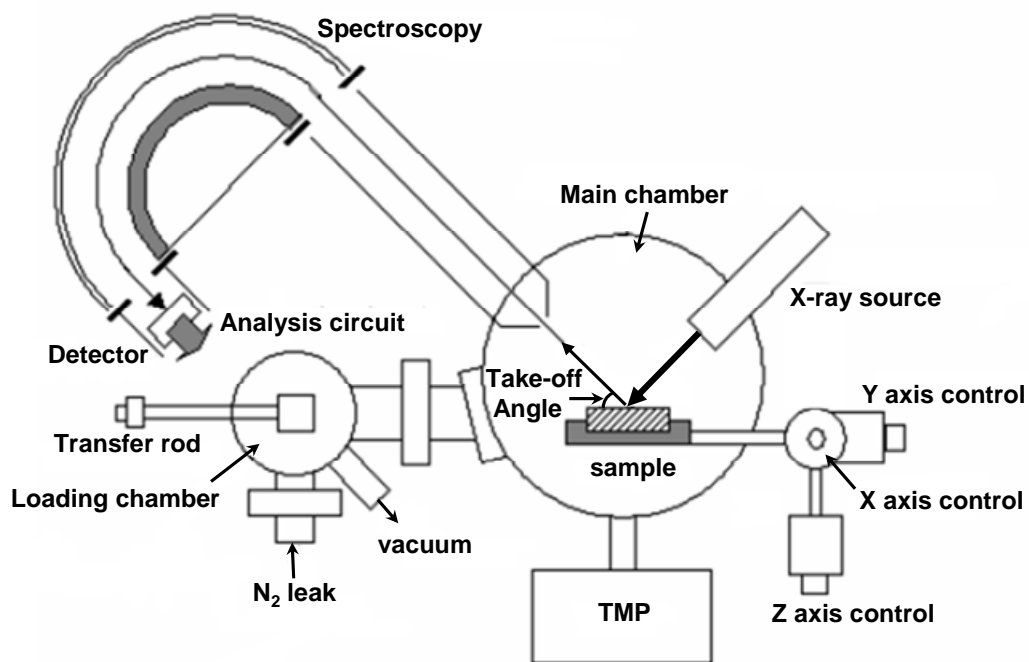


Figure 2-11. Schematic drawing of XPS equipment,

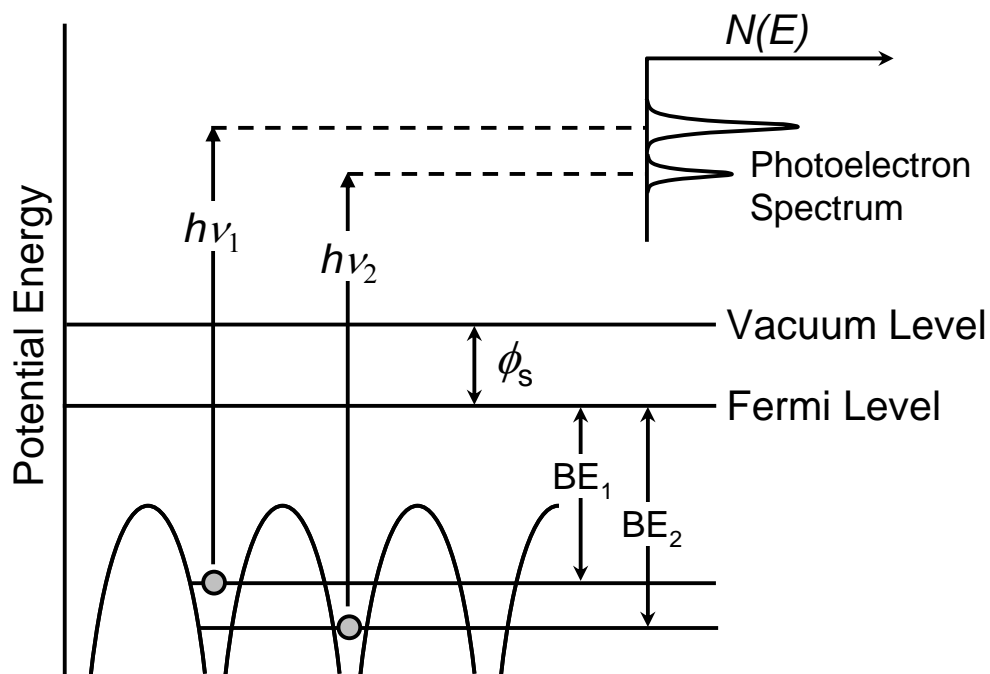


Figure 2-12. Principle of XPS measurement.

2.3.4 Capacitance-Voltage (*C-V*) Characteristics

C-V characteristic measurements were performed with various frequencies (1kHz~1MHz) by precision LCR Meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in Fig. 2-13. The intrinsic energy level E_i or potential ϕ in the neutral part of device is taken as the zero reference potential. The surface potential ϕ_s is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \quad (2-6)$$

where Q_G and V_G are the gate charge and the gate voltage, respectively. It is the change of charge due to a change of voltage and is most commonly given in units of farad/units area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitor from the gate, $C = dQ_G / dV_G$, where Q_G and V_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = - (Q_S + Q_{it})$, where Q_S is the semiconductor charge, Q_{it} the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \phi_s$, where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential, allowing Eq. (2-6) to be rewritten as

$$C = \frac{dQ_S + dQ_{it}}{dV_{ox} + d\phi_s} \quad (2-7)$$

The semiconductor charge density Q_S , consists of hole charge density Q_p , space-charge region bulk charge density Q_b , and electron charge density Q_n . With $Q_S = Q_p + Q_b + Q_n$, Eq. (2-7) becomes

$$C = -\frac{1}{\frac{dV_{ox}}{dQ_s + dQ_{it}} + \frac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \quad (2-8)$$

Utilizing the general capacitance definition of Eq. (2-6), Eq. (2-8) becomes

$$C = -\frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_p + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \quad (2-9)$$

The positive accumulation Q_p dominates for negative gate voltages for p -substrate devices. For positive V_G , the semiconductor charges are negative. The minus sign in Eq. (2-8) cancels in either case.

Equation (2-9) is represented by the equivalent circuit in Fig. 2-14-(a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in Fig. 2-14-(b) and the overall capacitance is C_{ox} . For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = -qN_A W$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in Fig. 2-14-(c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (Fig. 2-14-(d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in Fig. 2-14-(e) applies in inversion, with $C_b = K_s \epsilon_o / W_{inv}$ with W_{inv} the inversion space-charge region width.

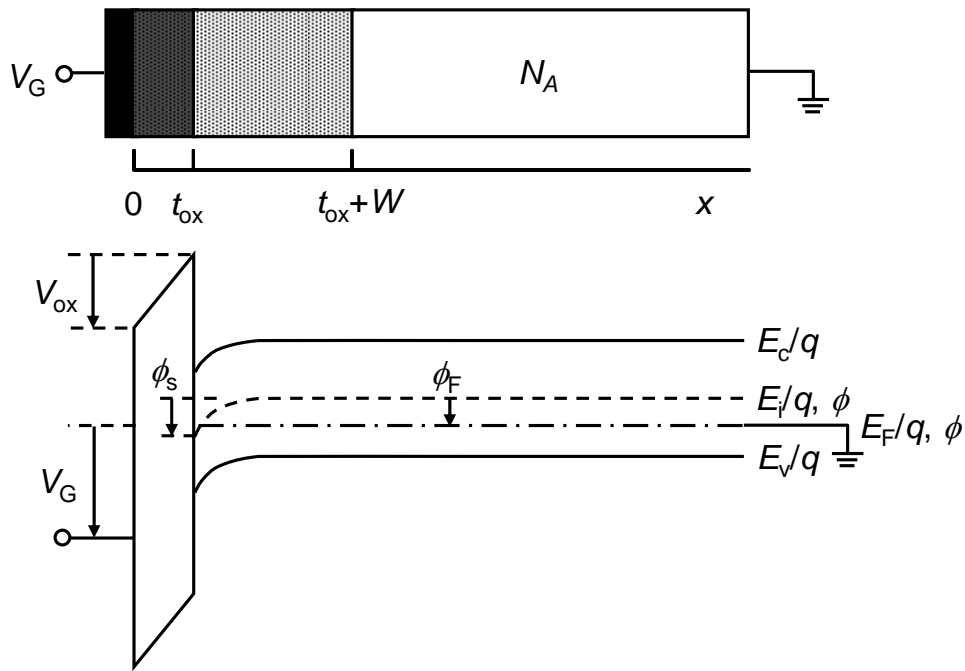


Figure 2-13. Cross section and potential band diagram of an MOS capacitor.

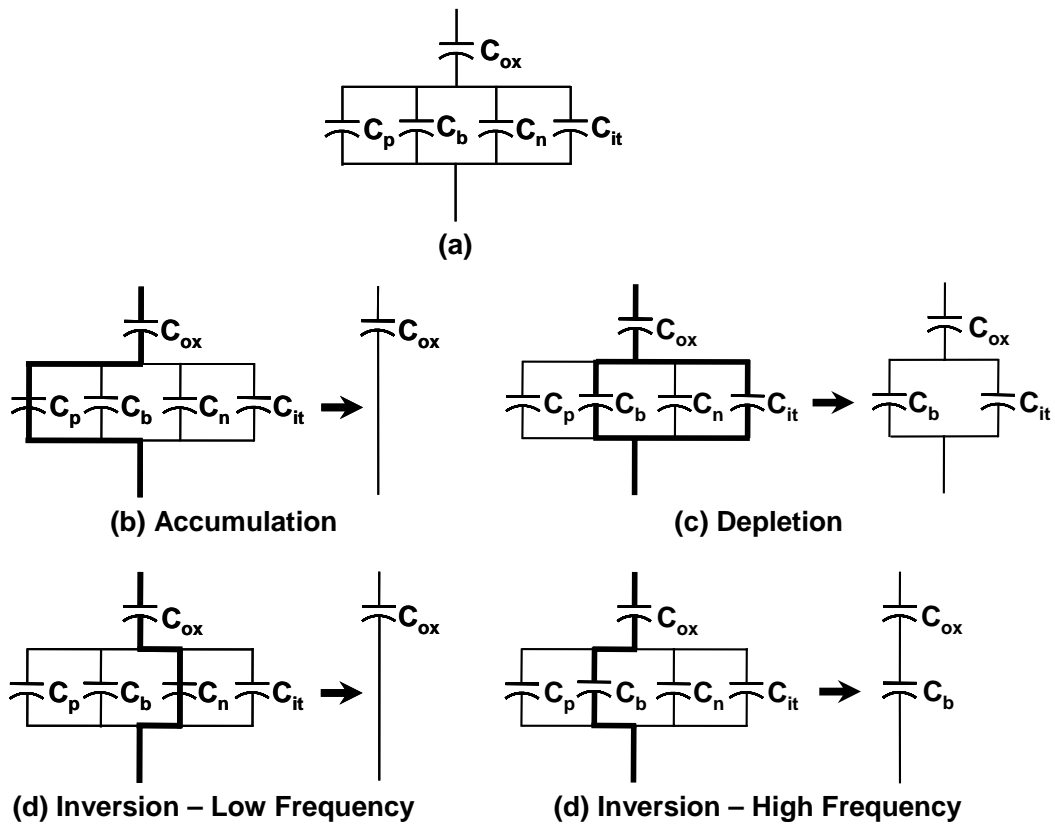


Figure 2-14. Capacitances of MOS capacitors for various bias conditions.

2.3.5 Leakage Current Density-Voltage (J - V) Characteristics

It is important to suppress the leakage current of the gate dielectric film as small as possible in order to lower the power consumption of LSI. To estimate the leakage current density, J - V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.). The measurement started at 0 V and sweep towards accumulation region until breakdown occurs. Detailed analyses on conduction mechanisms of La₂O₃ can be found on Kim [2-12].

2.3.6 Interface Trap Density by Conductance Method

The conductance method, proposed by Nicollian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it} [2-13]. The technique is based on measuring the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in Fig. 2-15-(a). It consists of the oxide capacitance C_{ox} , the semiconductor capacitance C_s , and the interface trap capacitance C_{it} . The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it} . It is convenient to replace the circuit of Fig. 2-15-(a) by that in Fig. 2-15-(b), where C_p and G_p are given by

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \quad (2-10)$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \quad (2-11)$$

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$, the interface trap time constant, given by $\tau_{it} = [\nu_{th}\sigma_p N_A \exp(-q\phi_s/kT)]^{-1}$. Dividing G_p by ω makes Eq. (2-11) symmetrical in $\omega\tau_{it}$. Equations (2-10) and (2-11) are for interface traps with a single energy level in the band gap. Interface traps at the insulator-semiconductor interface, however, are continuously distributed in energy throughout the semiconductor band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2]. \quad (2-12)$$

The conductance is measured as a function of frequency and plotted as G_p/ω versus ω . G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$. For Eq. (2-12) one can find $\omega \sim 2/\tau_{it}$ and $D_{it} = 2.5G_p/q\omega$ at the maximum. Hence one can determine D_{it} from the maximum G_p/ω and determine τ_{it} from ω at the peak conductance location on the ω -axis. G_p/ω versus ω plots measured for the sample of metal/La₂O₃/Ge structure is shown in Fig. 2-16.

An approximate expression giving the interface trap density in terms of the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{\max}. \quad (2-13)$$

Capacitance meters generally assumed the device to consist of the parallel C_m - G_m combination in Fig. 2-15-(c). A circuit comparison of Fig. 2-15-(b) to 2-15-(c) gives

G_p/ω in terms of the measured capacitance C_m , the oxide capacitance, and the measured conductance G_m as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (2-14)$$

assuming negligible series resistance. The conductance measurement must be carried out over wide frequency range. The portion of the band gap probed by conductance measurements is typically from flatband to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50mV or less to prevent harmonics of the signal frequency giving rise to spurious conductances.

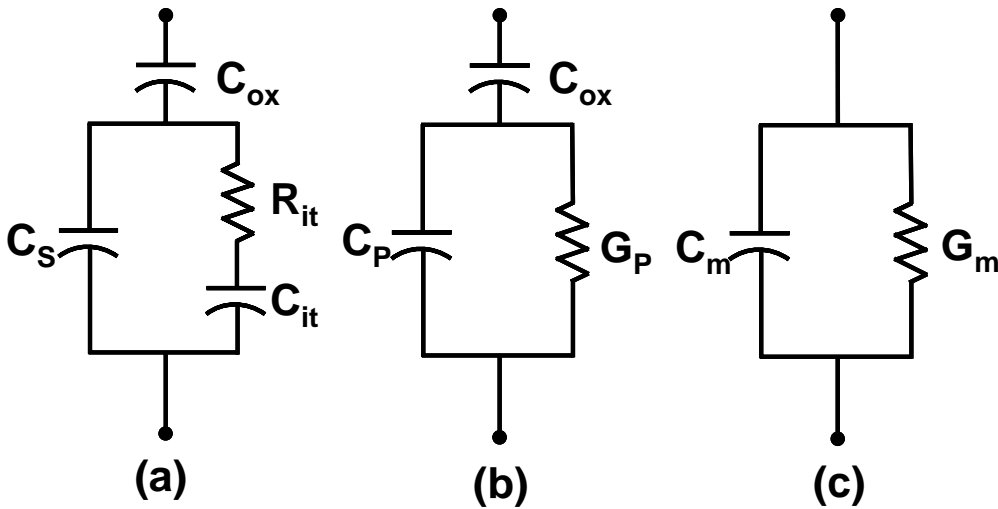


Figure 2-15. Equivalent circuit for conductance measurement; (a) MOS-C with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit.

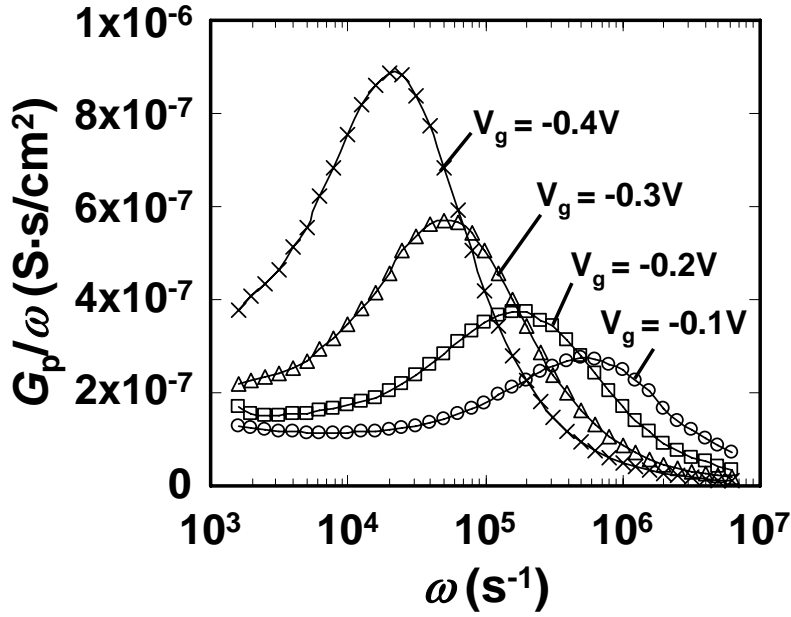


Figure 2-16. G_p/ω versus ω plots measured for the sample of metal/La₂O₃/Ge structure.

2.3.7 Threshold Voltage Extraction

Threshold voltage (V_{th}) is an important MOSFET parameter. However, V_{th} is a voltage that is not uniquely defined [2-14]. The existent of nonlinear curve at subthreshold region on the I_d - V_g plot make it difficult to have a universal definition. One of the most common threshold voltage measurement techniques is the “linear extrapolation method” with the drain current measured as a function of gate voltage at a low drain voltage of 50-100 mV to ensure operation in the linear MOSFET region [2-14]. The drain current is not zero below threshold and approaches zero only asymptotically. Hence the I_d versus V_g curve is extrapolated to $I_d = 0$, and the threshold voltage is determined from the extrapolation or intercept gate voltage V_g by

$$V_{th} = V_{Gs} - \frac{V_d}{2} \quad (2-15)$$

where V_{Gs} is the intercepted V_g value at $I_d = 0$ and V_d is the drain voltage used during the measurement.

The I_d-V_g curve deviates from the straight line at low gate voltage below threshold voltage due to subthreshold currents and above threshold voltage due to series resistance and mobility degradation effects. Thus, in order to determine the threshold voltage accurately, it is a common practice to find the point of maximum slope on the I_d-V_g curve by maximum in the transconductance, fit a straight line to the I_d-V_g curve at the point and extrapolate to $I_d = 0$, as illustrated in Fig. 2-17 [2-14].

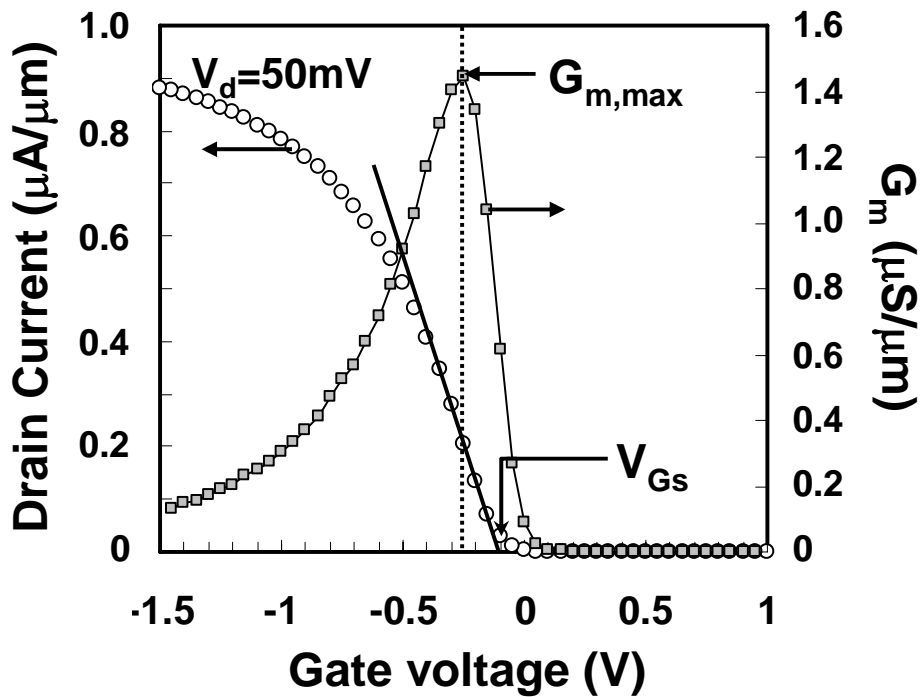


Figure 2-17. Threshold voltage determination by the linear extrapolation technique (for Ge p-MOSFET).

2.3.8 Subthreshold Slope Measurement

Depending on the gate and source-drain voltages, a MOSFET device can be biased in one of the three following regions; subthreshold, linear or saturation. In the subthreshold region where $V_g < V_{th}$, the drain on the linear scale appears to approach zero immediately below the threshold voltage. However, on a logarithmic scale, the descending drain current remains at nonnegligible levels for several tenths of a volt below threshold voltage [2-15]. This is because the inversion charge density does not drop to zero abruptly. Rather, it follows an exponential dependence on gate voltage. Subthreshold behavior is of particular important in modern ULSI application because it describes how a MOSFET device switches off (or turns on).

The subthreshold current is independent of the drain voltage once drain voltage is larger than a few kT/q , as would be expected for diffusion-dominated current transport. The dependence on gate voltage, on the other hand, is exponential with an inverse subthreshold slope (a.k.a. subthreshold swing) [2-15].

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \quad (2-16)$$

Subthreshold slope, which is that gate voltage necessary to change the drain current by one decade, is typically 70 – 100 mV/decade in modern MOSFET device [2-15].

In order to determine exact subthreshold slope, correct drain current excluded the leakage current should be extracted. Figure 2-18 illustrates the considerable leakage current in high-k/Ge MOSFET. Dot lines express the leakage current. With the ultrathin gate dielectric, one can think the leakage current between gate and source/drain, which is indicated as I_{GS} and I_{GD} in Fig. 2-18. In case of Ge-MOSFET, small band-gap of Ge induces non-negligible reverse-biased p-n junction leakage current. Therefore, measured

drain current (I_D) and source current (I_S) written as

$$I_D = I_{ds} - I_{GD} + I_{pn} \quad (2-17)$$

$$I_S = I_{ds} + I_{GS} \quad (2-18)$$

As I_{GS} and I_{GD} are almost same value, I_{ds} is given by

$$I_{ds} = 1/2(I_D + I_S - I_{pn}), \quad (2-19)$$

here, I_{pn} can be measured as I_B . Figure 2-19 shows the logarithm plots of I_D and I_{ds} against gate voltage. Drain leakage current increment due to large amounts of reverse-biased p-n junction leakage was appeared in I_D . Furthermore, the value of subthreshold slope extracted from I_D (106.5 mV/dec) became larger due to the leakage current compare with that from I_{ds} (78.8 mV/dec).

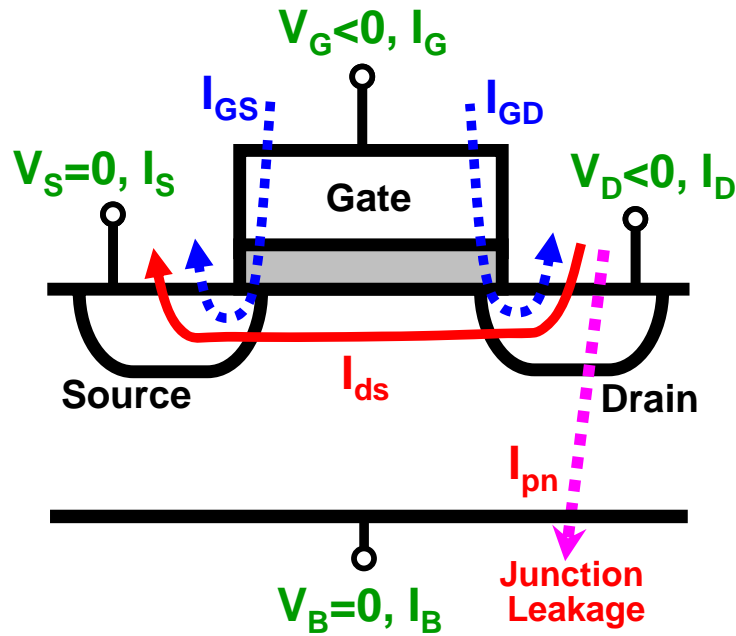


Figure 2-18. Considerable leakage current in high-k/Ge MOSFET.

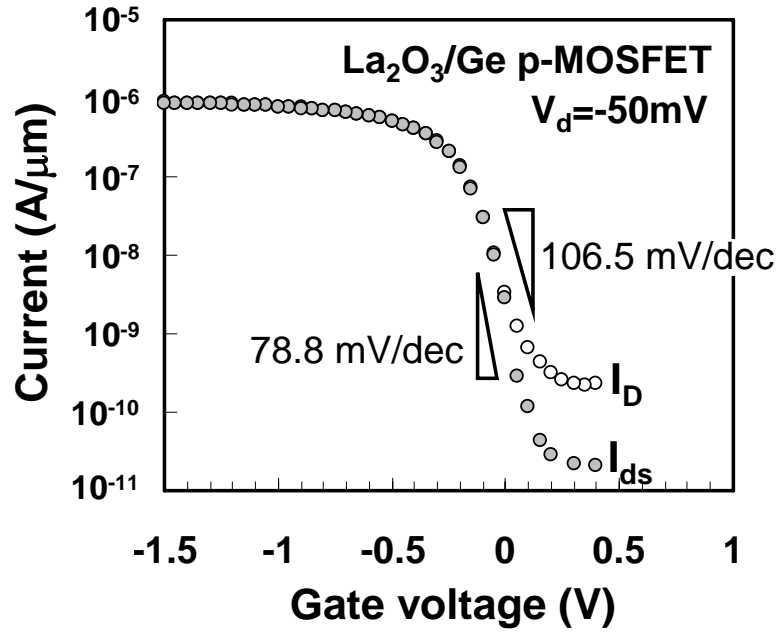


Figure 2-19. Logarithm plots of I_D and I_{ds} against gate voltage. Subthreshold slope was extracted as 78.8 mV/dec from I_{ds} and 106.5 mV/dec from I_D .

If the gate dielectric-semiconductor interface trap density is high, the subthreshold slope will be more degraded since the capacitance associated with the interface trap is in parallel with the depletion-layer capacitance C_{dm} . Hence, Eq. (2-19) can be rewrite as,

$$S = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm} + C_{it}}{C_{ox}} \right) \quad (2-20)$$

where C_{it} is the interface trap capacitance. The direct relationship between S and C_{it} , as shown in Eq. (2-20) can be used to obtain the interface trap density (D_{it}) with simple assumption of $C_{it} \sim qD_{it}$ [2-16].

$$D_{it} = \frac{1}{q} \left(\left(\frac{qS}{2.3kT} - 1 \right) C_{ox} - C_{dm} \right) \quad (2-21)$$

This technique required an accurate knowledge of C_{ox} and C_{dm} . However, interface trap density obtained from this technique is usually used as a comparative technique to other more accurate and sensitive measurement techniques, like conductance method on MOS capacitor or charge pumping on MOSFET.

2.3.9 Mobility Measurement Method based on Split $C-V$

The MOSFET drain current is due to drift and diffusion of the mobile carriers in the inverted Si channel. Let consider an n-channel device of gate length L and gate width W for the derivation. The derivation for p-channel device is similar to n-channel device with minor changes. The drain current I_d can be written as

$$I_d = \frac{W\mu_{eff}Q_nV_{ds}}{L} - W\mu_{eff} \frac{kT}{q} \frac{dQ_n}{dx} \quad (2-22)$$

where Q_n is the carrier channel charge density and μ_{eff} the effective mobility. The effective mobility is measured at low drain voltage under 100 mV. At low V_{ds} , one can assume that channel charge to be fairly distribute and uniform from the source to drain, allowing the diffusive second term in Eq. (2-22) to be dropped. Solving Eq. (2-22) then gaves,

$$\mu_{eff} = \frac{g_d L}{WQ_n} \quad (2-23)$$

where the drain conductance g_d is defines as

$$g_d = \left. \frac{\partial I_d}{\partial V_{ds}} \right|_{V_g = \text{constant}} \quad (2-24)$$

To accurately determine the Q_n , direct measurement of Q_n from 100 KHz high

frequency capacitance measurement, with mobile channel density or inverted charge density determined from the gate-to-channel capacitance/unit area (C_{gc}) according to the following equation

$$Q_n = \int_{V_{fb}}^{V_g} C_{gc} dV_g \quad (2-25)$$

where V_{fb} and V_g are the flatband voltage and gate voltage, respectively. The C_{gc} is measured by using the connection of Fig. 2-20 (a). The capacitance meter is connected between the gate and the source-drain connected together with substrate grounded. Setup in Fig. 2-20 (b) is used to measure the gate-to-substrate capacitance/unit area (C_{gb}). The connected source-drain is grounded during C_{gb} measurement. C_{gb} is used to calculate bulk charge density (Q_b) according to the following equation

$$Q_b = \int_{V_{fb}}^{V_g} C_{gs} dV_g \quad (2-26)$$

Both Q_n and Q_b are then used to calculate the effective vertical electric field (E_{eff}) according to

$$E_{eff} = \frac{Q_b + \eta Q_n}{\kappa_s \epsilon_o} \quad (2-27)$$

where Q_b and Q_n are the charge densities in the space-charge region and the inversion layer, respectively. The η is the inversion layer charge accounts for averaging of the electric field over the electron distribution in the inversion layer. The parameter $\eta = 1/2$ for the electron mobility and $\eta = 1/3$ for the hole mobility. κ_s and ϵ_o are the Si dielectric constant and permittivity of vacuum, respectively [2-17, 2-18, 2-19].

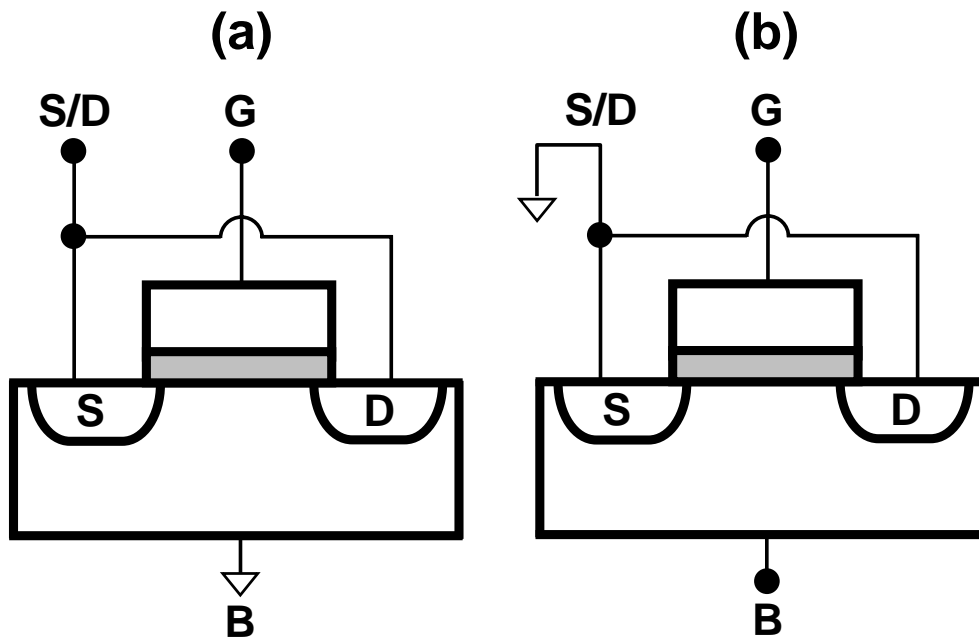


Figure 2-20. Configuration for (a) gate-to-channel, (b) gate-to-substrate capacitance measurement for split $C-V$ measurement [2-18].

Reference

- [2-1] H. Okumura, T. Akane, and S. Matsumoto, "Carbon contamination free Ge(100) surface cleaning for MBE", *Appl. Surf. Sci.*, vol. 125, pp. 125 (1998).
- [2-2] Kern, W. and Puotinen, D. A. "Cleaning Solutions Based Hydrogen on Peroxide for Use in Silicon Semiconductor Technology," *RCA Review*, vol. 31, pp.187 (1970).
- [2-3] K. Prabhakarana, T. Ogino, R. Hull, J. C. Bean, and L. J. Peticolas, "An efficient method for cleaning Ge(100) surface," *Surf. Sci.*, vol. 316, pp. L1031 (1994).
- [2-4] T. Akane, J. Tanaka, H. Okumura, and S. Matsumoto, "Preparation of high-quality Ge substrate for MBE," *Appl. Surf. Sci.*, vol. 108, pp. 303 (1997).
- [2-5] S.M. Sze, "VLSI technology," McGraw-Hill Book Co., (1983).
- [2-6] G. Adachi, *Kidorui no Kagaku (Science of Rare Earths)*, Kagakudojin Co., 1999, p.273 [in Japanese].
- [2-7] Japan Academic Promotion Thin Film 131st committee, *Thin film handbook*, 1983, pp.909-910 and p.917.
- [2-8] W. Kingery, H. Bowen, and D. Uhlmann, "Introduction to ceramics", John Willey & Son, 2nd Edition, pp.664 (1976).
- [2-9] A. Pecheur, J. Autran, J. Lazari, and P. Pinard, "Properties of SiO₂ film deposited on silicon at low temperatures by plasma enhanced decomposition of hexamethyldisilazane," *J. Non-Crystalline Solids*, vol.245, pp.20 (1999).
- [2-10] A. Hippel, "Dielectrics and waves", John Willey & Son, 1954.
- [2-11] K. Hirose, H. Nohira, K. Azuma, T. Hattori, "Photoelectron spectroscopy studies of SiO₂/Si interfaces," *Prog. Surf. Sci.*, vol.82, pp. 3 (2007).
- [2-12] Y. Kim, "Analysis of electrical conduction in rare earth gate dielectrics", PhD thesis, Tokyo Institute of Technology (2005).

- [2-13] E.H. Nicollian and A. Goetzberger, "The Si-SiO₂ Interface-Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique," *Bell Syst. Tech. J.*, vol.46, pp.1055 (1967).
- [2-14] D.K. Schroder, "Semiconductor material and device characterization", John Willey & Son, 3rd Edition, pp.222-230 (2006).
- [2-15] Y. Taur and T.H. Ning, "Fundamentals of modern VLSI devices", Cambridge Press, pp.125-129 (1998).
- [2-16] D.K. Schroder, "Semiconductor material and device characterization", John Willey & Son, 3rd Edition, pp.344 (2006).
- [2-17] C. G. Sodini, T. W. Ekstedt, and J. L. Moll, "Charge accumulation and mobility in thin dielectric MOS transistors", *Solid-State electron.*, vol.25, pp.833 (1982)
- [2-18] D.K. Schroder, "Semiconductor material and device characterization", John Willey & Son, 3rd Edition, pp.489-500 (2006).
- [2-19] S. Takagi, M. Iwase, and A. Toriumi, "On universality of inversion-layer mobility in n- and p-channel MOSFETs", *IEDM Tech. Digest*, pp.398 (1988).

Chapter 3.

Effect of Nitrogen Annealing in La₂O₃/Ge Structure

3.1 Introduction

3.2 Characterization of La₂O₃/Ge MOS Structure on PDA in Nitrogen
Ambient

3.3 Ge Diffusion into the La₂O₃ film by Annealing

3.4 Effect of PMA in N₂ on Pt/La₂O₃/Ge MOS Structure

3.5 Conclusion

3.1 Introduction

Interfacial properties such as interface trap density and interfacial layer growth are very important factor in introducing the high-k materials as gate dielectric. Interface trap density has to do with the effective mobility [3-1] and subthreshold swing (SS) [3-2] and the growth of low-permittivity interfacial-layer would increase the equivalent oxide thickness (EOT).

In this chapter, interfacial properties between La₂O₃ and Ge for directly contacted La₂O₃/Ge MOS structures were studied on the various annealing condition in inert nitrogen ambient (N₂). In the first sub-chapter, the characteristics of La₂O₃/Ge MOS structure with post deposition annealing (PDA) in nitrogen (N₂) ambient will be discussed comparing with Pt/La₂O₃/Si structure. Next, the effect of post metallization annealing (PMA) for the Pt/La₂O₃/Ge MOS structure will be reported.

3.2 Characterization of La₂O₃/Ge MOS Structure on PDA in Nitrogen Ambient

Figure 3-1 shows the 1kHz~1MHz $C-V$ characteristics and leakage current density of sample after PDA at 500 °C. The EOT of 1.45 nm with leakage current density of 3×10^{-7} A/cm² at 1V was achieved from Pt/La₂O₃/Ge structure after PDA at 500 °C, which is sufficiently high for activation of the source and drain region for Ge MOSFET [3-3, 3-4]. However, a large amount of frequency dependence and $C-V$ bump was observed and these were also observed for the samples with PDA at 300-800 °C. Capacitance decrease in 1MHz $C-V$ curve observed for the case of accumulation is attributed to series resistance effects [3-5]. Low-frequency behavior shown in 1kHz $C-V$ characteristic is explained by high intrinsic carrier concentration of Ge which is as thousand times large as that of Si [3-6]. Frequency dispersion nearby flat band voltage (V_{fb}) and bump shown in $C-V$ curves measured above 10kHz is caused by large amount of interface trap density (D_{it}) of 1.3×10^{13} cm⁻²eV⁻¹ [3-7]. This large amount of D_{it} was also observed for the samples with PDA at different temperature.

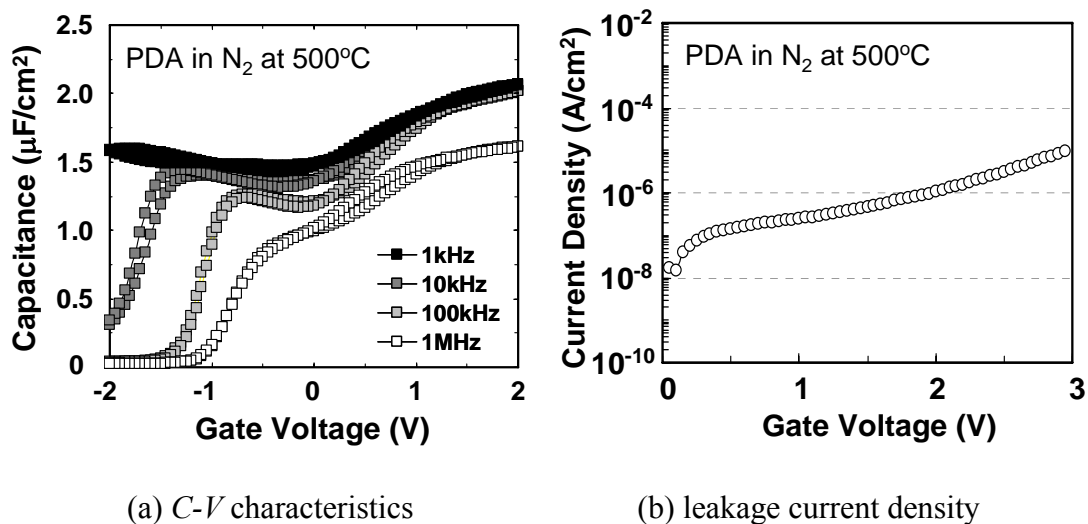


Figure 3-1. $C-V$ characteristics and leakage current density after PDA at 500 °C.

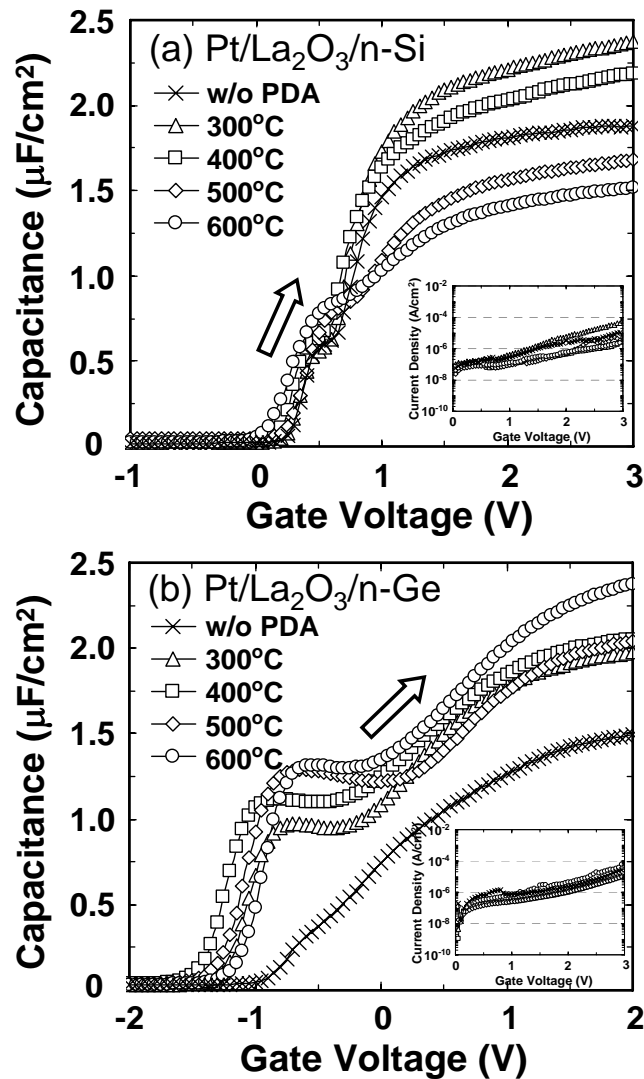


Figure 3-2. C - V characteristics of (a) Pt/La₂O₃/n-Si and (b) Pt/La₂O₃/n-Ge MOS structures after PDA at various temperatures. The inset shows leakage current of the MOS structures.

Figure 3-2 shows the C - V characteristics of (a) Pt/La₂O₃/n-Si and (b) Pt/La₂O₃/n-Ge MOS structures after PDA at various temperatures. The insets show the leakage current density of samples. As shown in Fig. 3-2 (a), capacitance of Si MOS structures once increased by PDA at 300 °C, while those soon decreased with the increase in PDA temperature. On the contrary, in case of Ge MOS structures, increased

capacitance after PDA did not change up to 500 °C and that increased after PDA at 600 °C as shown in Fig. 3-2 (b). Effective dielectric constant of La₂O₃ on Ge was about 14, whereas that of on Si was about 9 after high temperature PDA. Low dielectric constant on Si substrate can be explained by the reaction at the interface as shown below.

Figure 3-3 shows hysteresis of the *C-V* curves. A large amount of hysteresis was observed in samples with PDA up to 400 °C and as-deposited one in Pt/La₂O₃/Ge structures compared with those of Pt/La₂O₃/Si structures. The small hysteresis shown in case of Si substrate might be due to silicate reaction of Si with La₂O₃ even in as-deposited samples [3-8], in which silicon was caused to combine with dangling bonds at oxygen vacancy in La₂O₃. In case of Ge substrate, the hysteresis dramatically reduced at 500 °C PDA, which suggests that dangling bonds were reduced by reaction of Ge substrate with La₂O₃ at this temperature.

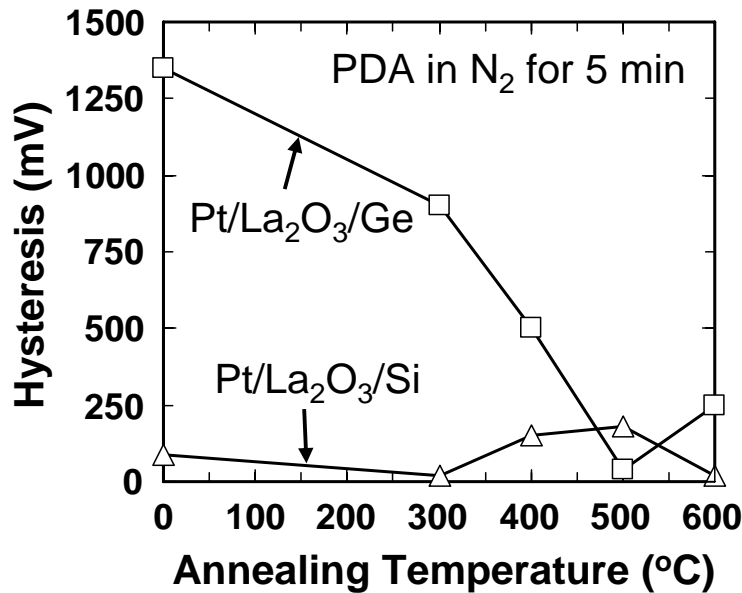


Figure 3-3. Hysteresis of Pt/La₂O₃/n-Si and Pt/La₂O₃/n-Ge MOS structures with PDA at various temperatures.

Figure 3-4 shows the physical-thickness change of La₂O₃ films normalized by the value of the as-deposited films, which were measured by spectroscopic ellipsometry. At the temperature of 300 °C, the film thickness decreased in both cases of Si and Ge substrate due to the densification of the deposited films and desorption of the some hydroxyl group which was absorbed into La₂O₃ from water component in air because of strong hygroscopic property of La₂O₃ [3-9~3-11]. By PDA at 400 °C and above, however, the thickness of La₂O₃ films on Si substrate increased, suggesting the growth of interfacial La-silicate and/or SiO₂ layer between the La₂O₃ film and the Si substrate [3-8, 3-11]. This growth of interfacial layer (IL) caused to decrease the capacitance with increasing the PDA temperature. On the contrary, film thickness on Ge substrate showed little change after PDA up to 500 °C, which suggests that either La-Germanate or GeO₂ layer is less formed by PDA in N₂. Moreover the film thickness of La₂O₃ on Ge substrate decreased by PDA at 600 °C, which eventually increased the capacitance. This decrease of thickness with PDA at 600 °C might be caused by sublimation of Ge oxide, which will be discussed specifically next sub-chapter.

The cross sectional images of the films after PDA at 600 °C were observed by HR-TEM (Fig. 3-5). It should be noted that the thickness of the interfacial layer is less than 0.3 nm on a Ge substrate, while more than 1.7 nm SiO₂ layer was grown on a Si substrate. Such an absence of interfacial layer formation in high-*k*/Ge system has been reported in other high-*k* materials [3-12~3-14].

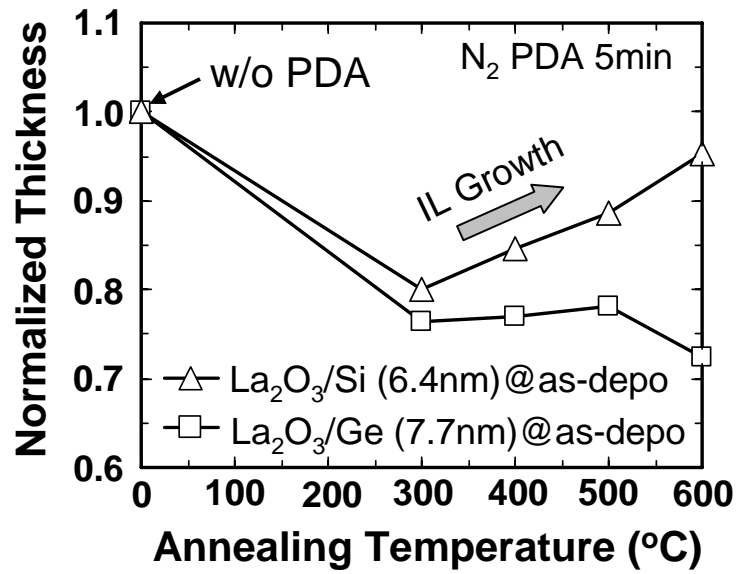


Figure 3-4. Physical thickness change of La_2O_3 films normalized by as-deposited thickness, which were measured by spectroscopy ellipsometry.

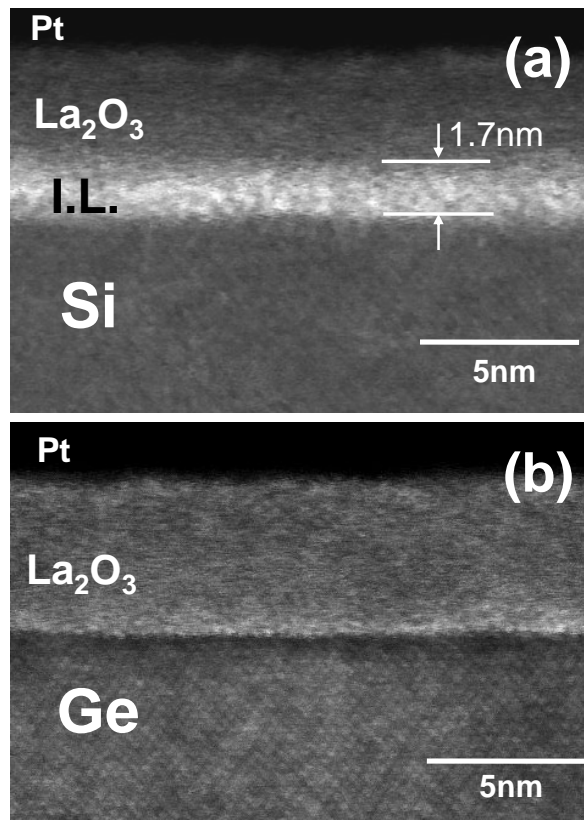


Figure 3-5. HR-TEM images of $\text{La}_2\text{O}_3/\text{Si}$ and $\text{La}_2\text{O}_3/\text{Ge}$ structures after PDA in N_2 at 600 °C.

The chemical bonding configuration in the La₂O₃/Ge interface was analyzed using XPS. The source x-ray was monochromatized Al *K*α radiation (1486.7 eV). Thicknesses of La₂O₃ films were chosen to be 1.8~2.0 nm in order to acquire the signals from the La₂O₃/Ge interface. Figure 3-6 shows Ge 3*d* spectra for the samples with and without PDA. PDA was carried out in N₂ ambient at 400 °C and 600 °C for 5 minutes. Ge-oxide (GeO_x) spectra, chemically shifted from Ge 3*d* peak, were deconvoluted using four GeO_x peaks (Ge¹⁺, Ge²⁺, Ge³⁺, Ge⁴⁺) with energy shifts of 0.8, 1.8, 2.6, and 3.4 eV relative to the binding energy of elemental Ge 3*d*_{5/2} [3-15]. As shown in Fig. 3-6, no GeO₂ (Ge⁴⁺) peak was observed for all samples. This is in contrast to the case using a Si substrate; SiO₂ was detected even for the as-deposited film at the La₂O₃/Si interface [3-8]. The sub-oxides (Ge¹⁺, Ge²⁺) detected from the La₂O₃/Ge structure might be formed because of the interfacial bonding configured at the interface between La₂O₃ and Ge, considering that similar sub-oxides were also observed at the interface with other high-*k* materials on Ge [3-16, 3-17]. Taking into account of smaller electronegativity of La ($\chi_{\text{La}}=1.1$) than Ge ($\chi_{\text{Ge}}=2.0$), the peaks of La-germanate (La-O-Ge bonding) formed by reaction between La₂O₃ and Ge might be also included in those sub-oxide spectra. In case of Si which has similar electronegativity ($\chi_{\text{Si}}=1.9$) to that of Ge, actually, La-silicate peaks appear at lower binding energy than that of SiO₂ [3-18]. In addition, focusing to La 5*s* spectra appearing around binding energy of 34 eV, certain shift in binding energy was observed for the sample after PDA at 600 °C, which suggests that the La-germanate had been formed as a result of reaction between La₂O₃ film and Ge substrate. The spectrum of La-germanate is thought to be contained in Ge sub-oxide spectra.

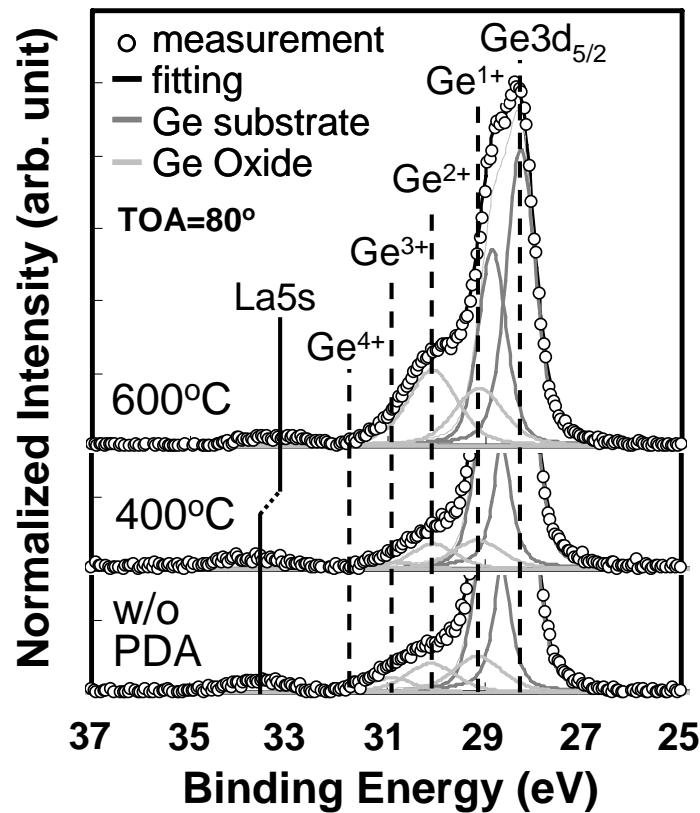


Figure 3-6. Deconvoluted XPS spectra of Ge 3d from La₂O₃(2nm)/Ge structure with different annealing temperature.

Figure 3-7 shows O 1s spectra for the samples with and without PDA. Peaks appearing at 528.2eV and 530.5eV correspond to the chemical bonding states of La-O-La and La-O-H, respectively [3-19]. Due to the strong hygroscopic property of La₂O₃, large amount of La-hydroxide was observed for the as-deposited film and the one with 400 °C PDA. The other peak between La-O-La and La-O-H whose intensity significantly increased by PDA at 600 °C originates in the bonding of La-O-Ge. The La-O-Ge bonding indicates the formation of La-germanate and the increase of La-O-Ge bonding intensity with PDA at 600 °C well supports the peak shift of La 5s as shown in Fig. 3-6. Although the thickness of interfacial layer attained from the TEM image was less than 0.3 nm as shown in Fig. 3-5, the intensities of La-O-Ge and Ge-O-Ge was

larger than those of La-O-La and La-O-H for the sample after PDA at 600 °C. This result is due to the diffusion of Ge during PDA, which will be discussed in next sub-chapter specifically. The formation of La-germanate was observed in even as-deposited film and showed almost same proportion up to PDA temperature of 400 °C. One can confirm that these La-germanate component is included in Ge sub-oxide peaks in case of Ge 3d spectra as shown in Fig. 3-6. The peak arising at 531.1eV correspond to the chemical bonding states of Ge-O-Ge, which is thought to originate mainly from Ge oxide. The Ge-O-Ge bonding state can be also detected from the some structure of La-germanate (e.g. La:Ge:O=2:2:7) corresponding to observation of Ge⁴⁺ spectrum in Ge core spectra, carefully applying the analogy between Si and Ge [3-20]. As no Ge⁴⁺ was observed from Ge 3d spectra in the PDA case, Ge-O-Ge bonding is thought to arise from Ge sub-oxide.

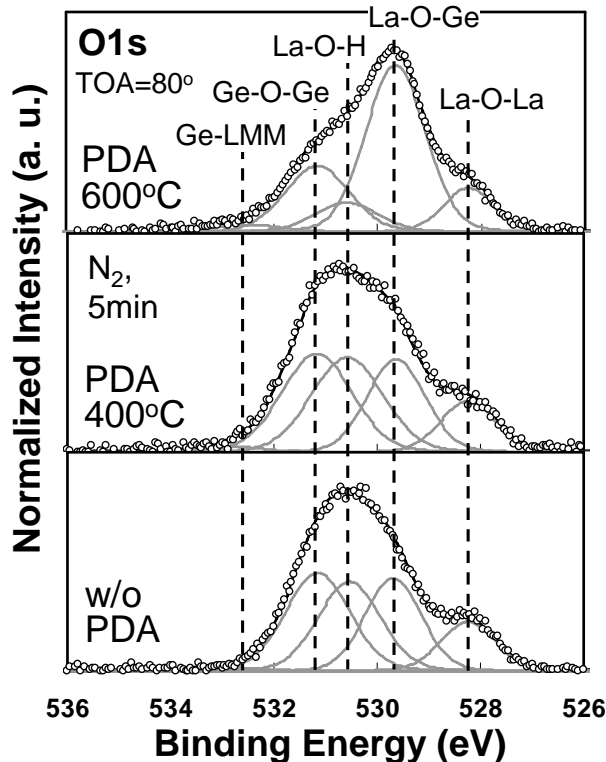


Figure 3-7. O 1s spectra for the samples with and without PDA.

3.3 Ge Diffusion into the La₂O₃ Film by Annealing

In the previous sub-chapter, the intensity of La-germanate spectra increased although there is little increase in film thickness measured by spectroscopic ellipsometry. In general, the intensity of spectra arising from upper layer becomes larger than that from under layer in the XPS measurement. Thus, in order to examine the distribution in the film, angle-resolved XPS (AR-XPS) analysis was performed. Figure 3-8 shows O 1s spectra measured at the take-off angle (TOA) from 15° to 80° for the sample with and without PDA, in which spectra was deconvoluted by each chemical bonding state. From the intensity (N_x) of deconvoluted spectra, the dependencies of intensity ratio on TOA for some compositions were calculated. Figure 3-9 shows the intensity ratio dependence of (a) $N_{\text{Ge-O-Ge}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ and (b) $N_{\text{La-O-Ge}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ on TOA. The $N_{\text{Ge-O-Ge}}$ and $N_{\text{La-O-Ge}}$ become smaller than sum of $N_{\text{La-O-La}}$ and $N_{\text{La-O-H}}$ with decreasing the TOA for the samples without PDA and with PDA at 400 °C. In contrast, that intensity ratio becomes larger for the sample with PDA at 600 °C. These results mean Ge sub-oxide (Ge-O-Ge bonding) and La-germanate (La-O-Ge bonding) are located under deposited La oxide for the samples without PDA and with PDA at 400 °C, while the Ge sub-oxide and La-germanate are located on the La oxide layer for the sample after PDA at 600 °C. These results suggest Ge significantly diffused into the La oxide film and finally reached the surface of La oxide in case of PDA at 600 °C. Actually, diffusion of Ge into La oxide film was also observed for the sample with PDA at 400°C basing on the comparison of $N_{\text{Ge-O-Ge}}$ and $N_{\text{La-O-Ge}}$ with only $N_{\text{La-O-La}}$ as shown in Fig. 3-10. On the other hand, in case of Si substrate, Si oxide (Si-O-Si bonding) and La-silicate (La-O-Si bonding) are located under the La oxide layer even for the sample with PDA at 600 °C, which is shown in Fig. 3-11.

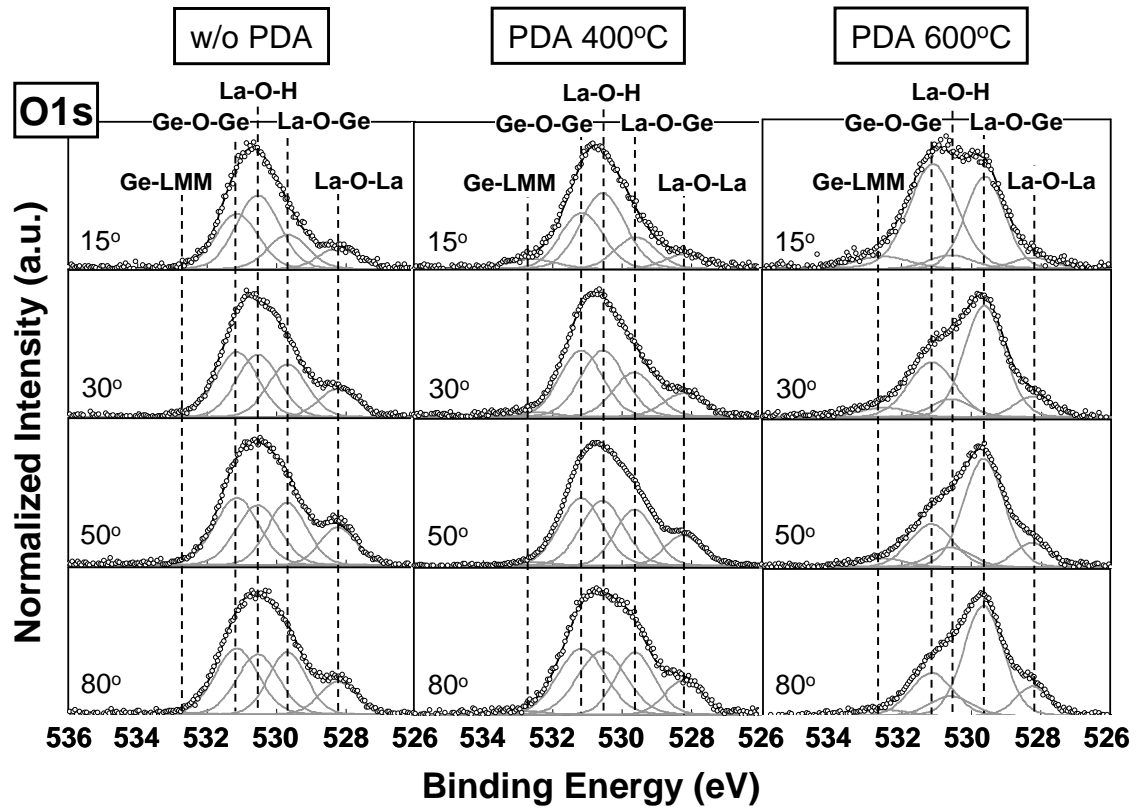


Figure 3-8. O *1s* spectra measured in the take-off angle (TOA) from 15° to 80° for the sample with and without PDA.

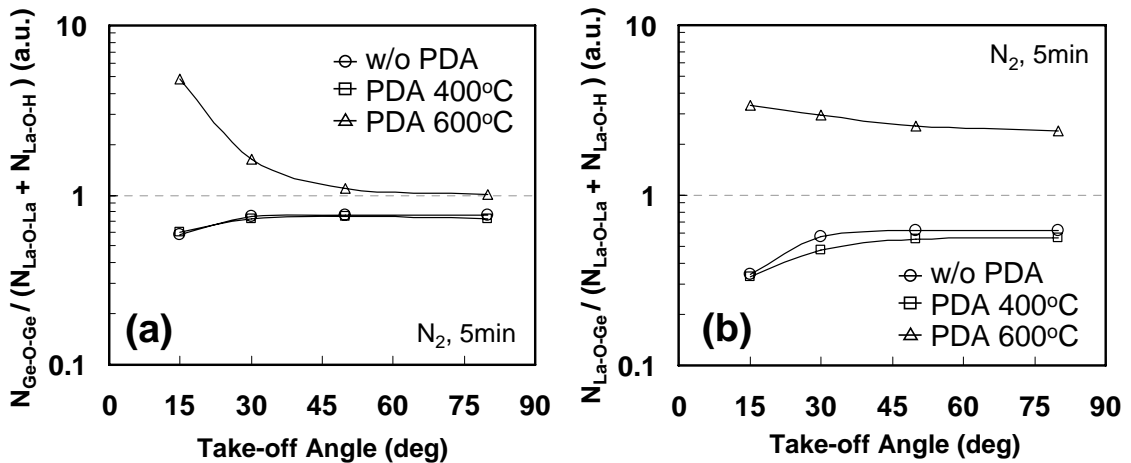


Figure 3-9. Dependence of (a) $N_{\text{Ge-O-Ge}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ and (b) $N_{\text{La-O-Ge}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ on TOA in La₂O₃/Ge structures.

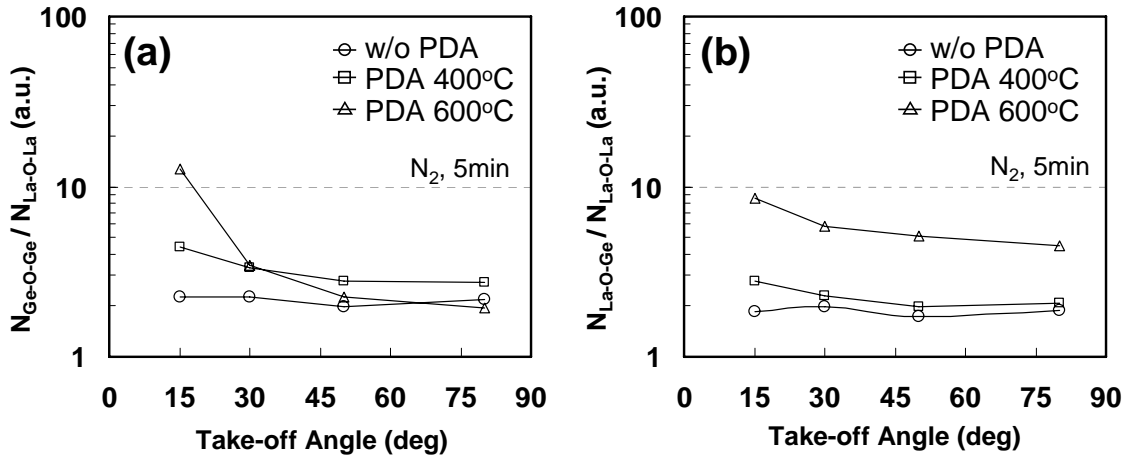


Figure 3-10. Dependence of (a) $N_{\text{Ge-O-Ge}} / N_{\text{La-O-La}}$ and (b) $N_{\text{La-O-Ge}} / N_{\text{La-O-La}}$ on TOA in La₂O₃/Ge structures.

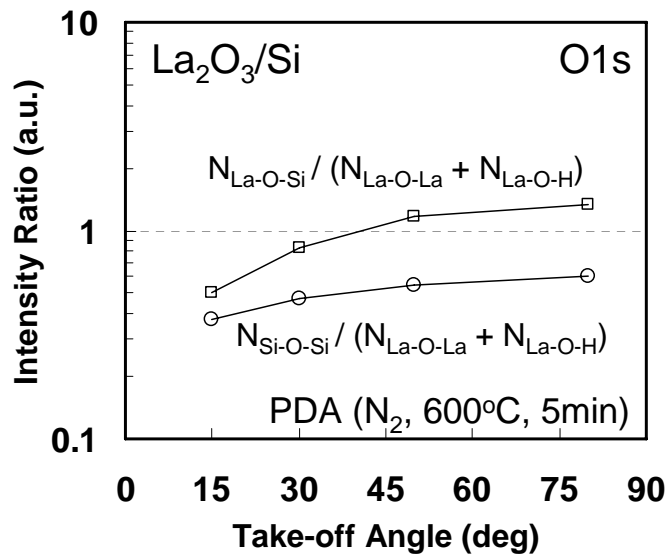


Figure 3-11. Dependence of (a) $N_{\text{Si-O-Si}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ and (b) $N_{\text{La-O-Si}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ on TOA in La₂O₃/Si structures.

The diffusion of Ge atoms induced by PDA was also investigated for the sample having thicker La₂O₃ films. Figure 3-12 shows La 5s and Ge 3d spectra measured at TOA of 80° for the La₂O₃/Ge structure after PDA at 400 °C and 600 °C. La₂O₃ film thicknesses were 8-8.5 nm and 21-22 nm, respectively. In the XPS measurement, detection depth of photoelectron is defined by inelastic mean free path (IMFP) in photoelectron of materials. The ratio of number of photoelectron arising from x to surface with respect to total intensity can be expressed as

$$I_o^x = \frac{\int_0^x e^{-\frac{z}{\lambda \sin \theta}} dz}{\int_0^\infty e^{-\frac{z}{\lambda \sin \theta}} dz} = 1 - e^{-\frac{x}{\lambda \sin \theta}}, \quad (3-1)$$

where λ and θ are IMFP and TOA, respectively. The IMFPs of Ge 3d photoelectron excited by x-ray source of Al $K\alpha$ radiation (1486.7 eV) are 2.80 nm and 2.92 nm in La₂O₃ and La(OH)₃, which are calculated by TPP-2M equation [3-21]. From the Eq. (3-1) and IMFP, one can see the intensity of 90% was obtained for 6.4nm-depth and 95% from 8.4nm-depth, i.e. only 10%-signal can be detected under the 6.4nm-La₂O₃. As shown in Fig. 3-12, very small intensity of Ge-oxide (GeO_x) and no signal of Ge element were observed for 8nm-La₂O₃ sample with PDA at 400 °C, which eventually vanished for 21nm-La₂O₃ sample with PDA at 400 °C because almost all signal from Ge 3d core levels attenuated in upper-existing La₂O₃ film. However, large amount of GeO_x was observed even for 21nm-La₂O₃ sample in the case of PDA at 600 °C, which suggest tremendous diffusivity of Ge into the La₂O₃ after PDA at 600 °C.

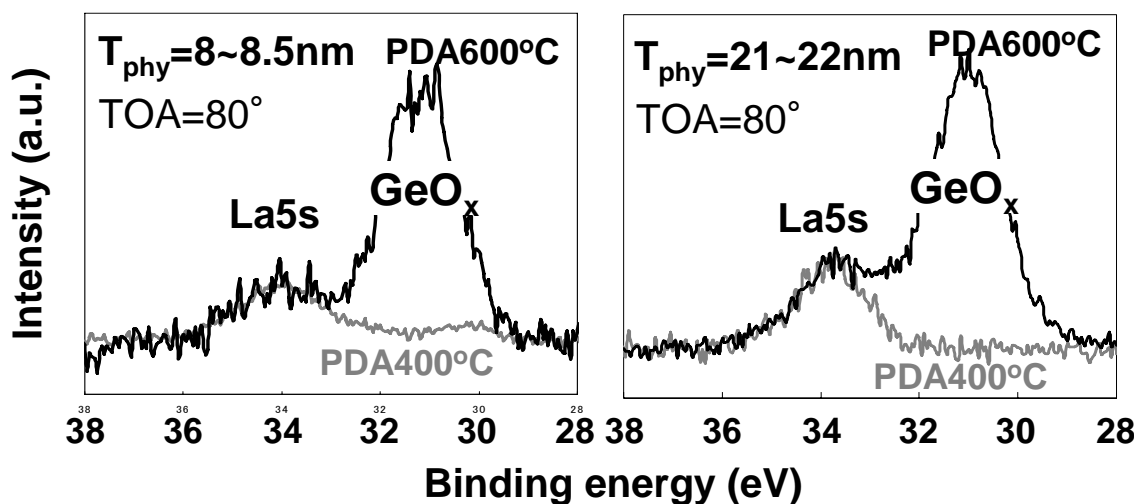


Figure 3-12. La 5s and Ge 3d spectra measured at TOA of 80° for the La₂O₃/Ge structure with PDA at 400 °C and 600 °C.

Figure 3-13 shows O 1s spectra measured at TOA from 15° to 80° for the sample having 21nm-thick La₂O₃. PDA was conducted in N₂ at 600 °C for 5 minutes. In contrast to the sample with 2nm-thick La₂O₃ in which little La oxide remained after the reaction with Ge to form La-germanate, a large intensity of La-O-La bonding was observed in the O 1s spectrum measured in 80° in case of 21nm-thick La₂O₃. However, the intensity of La-O-La spectrum noticeably decreased in comparison with that of other spectrum, which indicates La₂O₃ is located at the bottom within the range of photoelectron detection.

Figure 3-14 shows the dependence of intensity ratio of $N_{\text{GeO}_x}/N_{\text{LaO}_x}$ ($N_{\text{GeO}_x} = N_{\text{Ge-O-Ge}} + N_{\text{La-O-Ge}}$ and $N_{\text{LaO}_x} = N_{\text{La-O-La}} + N_{\text{La-O-H}}$) on TOA after PDA at 600 °C for the sample having different thickness of La₂O₃. The N_{GeO_x} become larger than the N_{LaO_x} with decreasing TOA for all La₂O₃ thickness, which means Ge oxide and La-germanate exists on the La oxide and Ge diffusion reached to the surface of La₂O₃. The GeO_x spectra in Ge 3d after PDA at 600 °C shown in Fig. 3-12 were mostly originated from

top-side Ge oxide and La-germanate. Furthermore, considering the existence of La-O-La and La-O-H bonding, Ge was thought to be diffused interstitially into the La₂O₃ and reached the top of La₂O₃. On the other hand, Ge oxide formed on the surface of the film was considered to be sublimated so that the film thickness measured by spectroscopic ellipsometry decreased after PDA at 600 °C as shown in Fig. 3-4. The sublimation of Ge oxide by annealing at 600 °C in N₂ ambient support this result and such decrease of film thickness was also reported for HfO₂/Ge structure [3-22].

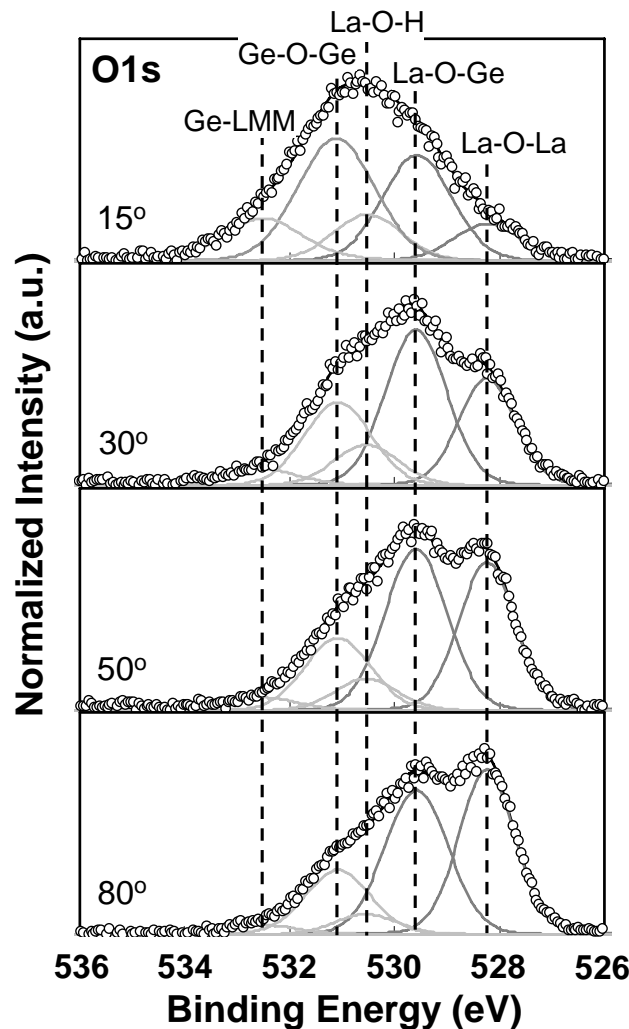


Figure 3-13. O 1s spectra measured in TOA from 15° to 80° for the sample with 21nm-thick La₂O₃.

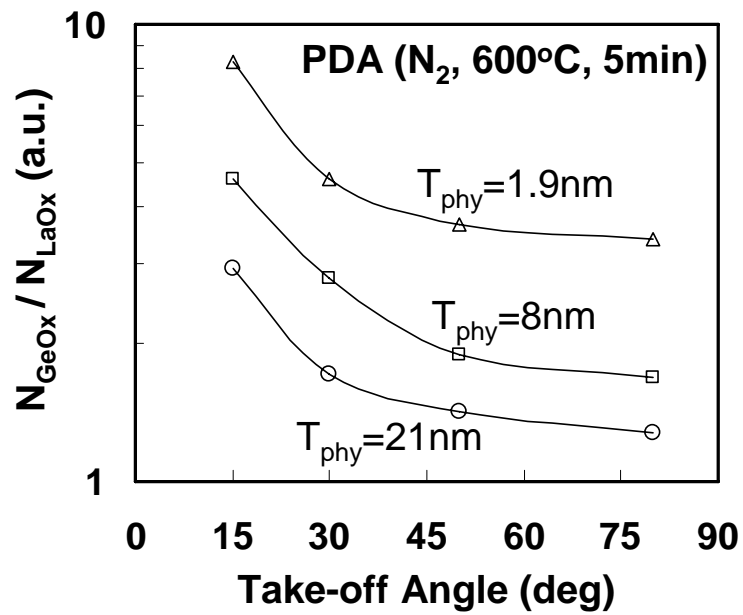


Figure 3-14. Dependence of intensity ratio of $N_{\text{GeOx}}/N_{\text{LaOx}}$ ($N_{\text{GeOx}} = N_{\text{Ge-O-Ge}} + N_{\text{La-O-Ge}}$ and $N_{\text{LaOx}} = N_{\text{La-O-La}} + N_{\text{La-O-H}}$) on TOA after PDA at 600 °C for the sample having different thickness of La₂O₃.

3.4 Effect of PMA on Pt/La₂O₃/Ge MOS Structure

Figure 3-15 shows 1kHz~1MHz $C-V$ characteristics of Pt/La₂O₃/Ge MOS structure after PMA at 500 °C. The thickness of as-deposited La₂O₃ film is 9.2nm. Frequency dispersion decreased dramatically as compared with the sample with PDA at 500 °C shown in Fig. 3-1, while $C-V$ hysteresis increased in comparison with that of PDA sample. Figure 3-16 shows 100kHz $C-V$ characteristics of samples with PDA, PMA and PDA+PMA at 300 °C. A large amount of $C-V$ bump shown in sample with PDA was significantly reduced by PMA treatment and very little $C-V$ bump was observed in sample with only PMA. This decrease of frequency dispersion shown in Fig. 3-15 and $C-V$ bump were caused by the reduction of D_{it} , which was shown in Fig. 3-17. As shown in Fig. 3-17, D_{it} can be much smaller with increasing of PMA temperature. However, there was capacitance decrement caused by PMA treatment, which indicates the increase of interfacial layer growth. These results suggest that the increase of interfacial layer would decrease the D_{it} .

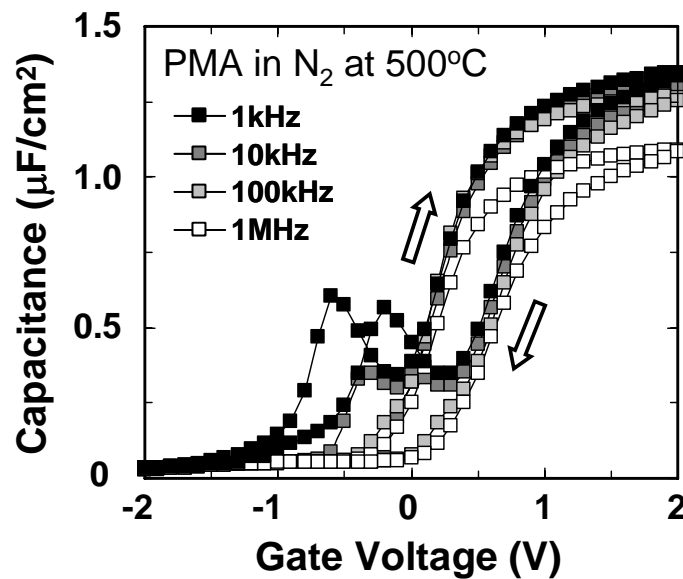


Figure 3-15. $C-V$ characteristics of Pt/La₂O₃/n-Ge MOS structures with PMA at 500 °C.

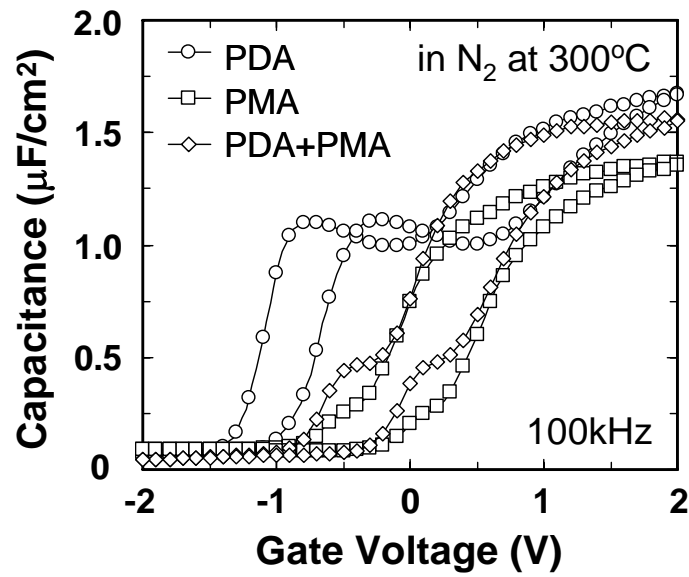


Figure 3-16. 100kHz $C-V$ characteristics of samples with PDA, PMA and PDA+PMA at 300 °C.

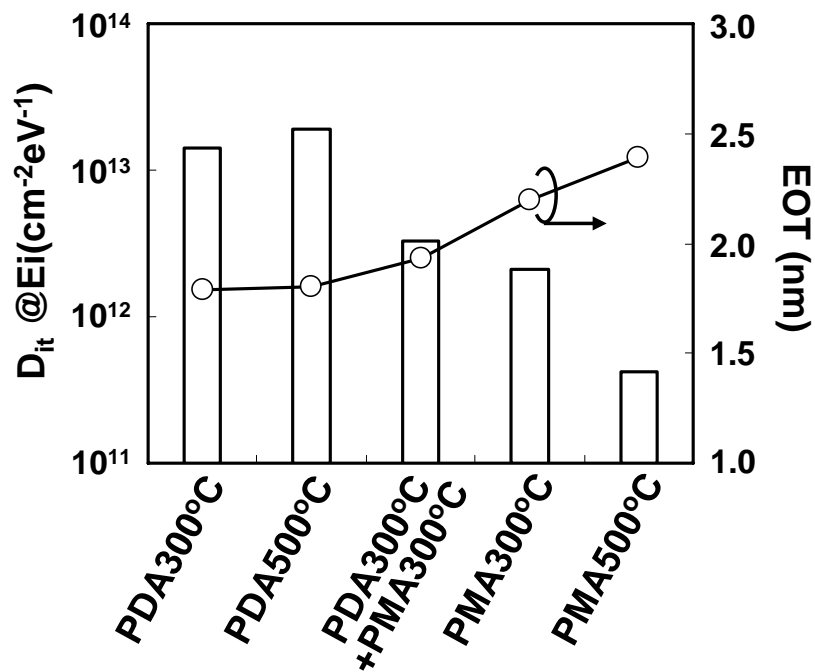


Figure 3-17. D_{it} and EOT of samples with PDA, PMA and PDA+PMA at 300 °C and sample with PMA at 500 °C.

In order to examine the formation of interfacial layer, XPS analysis was performed using samples annealed at 400 °C either with PDA or PMA treatment, which is shown in Fig. 3-18. The thicknesses of the Pt electrode and the La₂O₃ films were set to 1.5 nm and 2.0 nm, respectively. The spectra arising from Ge oxide (GeO_x), appearing at higher binding energy with respect to Ge 3*d* core spectrum, can be deconvoluted into four GeO_x peaks (Ge¹⁺, Ge²⁺, Ge³⁺ and Ge⁴⁺) with energy shifts of 0.8, 1.8, 2.6, and 3.4 eV, as described in chapter 3-2. Distinct Ge⁴⁺ as well as Ge³⁺ peaks was observed for the PMA sample, which is minor in the spectrum for the PDA one. The generation of Ge³⁺ and Ge⁴⁺ components might contribute in the improvement in D_{it} at the cost of increase in the capacitance. The source to oxidize the Ge substrate during PMA is considered to be the hydroxyl group absorbed near the surface of La₂O₃ from the ambient, as La₂O₃ has high hygroscopic property [3-9]. The hydroxyl group can be decomposed during PDA, whereas a capping with gate electrode prevents the hydroxyl from evaporation in the case of PMA. Since Pt is an inert material, the hydroxyl group in La₂O₃ is thought to be the source to oxidize Ge substrate.

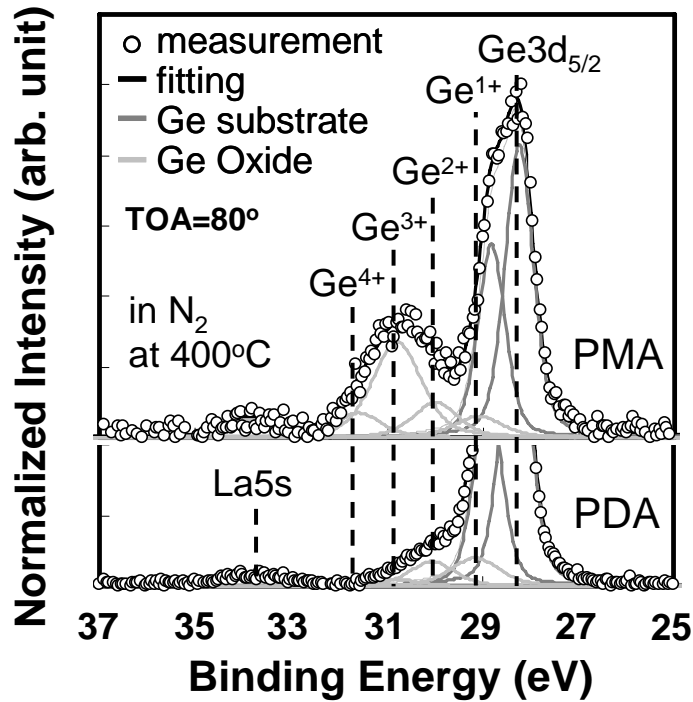


Figure 3-18. Spectra of Ge 3d measured by XPS using Pt(1.5nm)/La₂O₃(2.0nm)/Ge structure after PMA at 400 °C and La₂O₃(2.0nm)/Ge structure after PDA at 400 °C.

In order to confirm the effect of the absorbed hydroxyl group, vacuum annealing to remove the hydroxyl group was performed *in situ* prior to the Pt electrode deposition. Annealing temperature was set at 250 °C, which is the same as the substrate temperature during the La₂O₃ deposition. Figure 3-19 shows (a) *C-V* characteristics and (b) *D_{it}* in Pt/La₂O₃/Ge structure with and without the *in-situ* vacuum annealing before the Pt electrode deposition. PMA was conducted at 300 °C and 500 °C in N₂ for 5 minutes. Larger capacitance value was observed for the samples with the vacuum annealing. However, a bulky hump was observed in the *C-V* curve, which indicates the degradation in *D_{it}* as shown in Fig. 3-19-(b). These results suggest that the thickness of interfacial GeO_x layer for the sample with vacuum annealing is smaller than that without vacuum annealing.

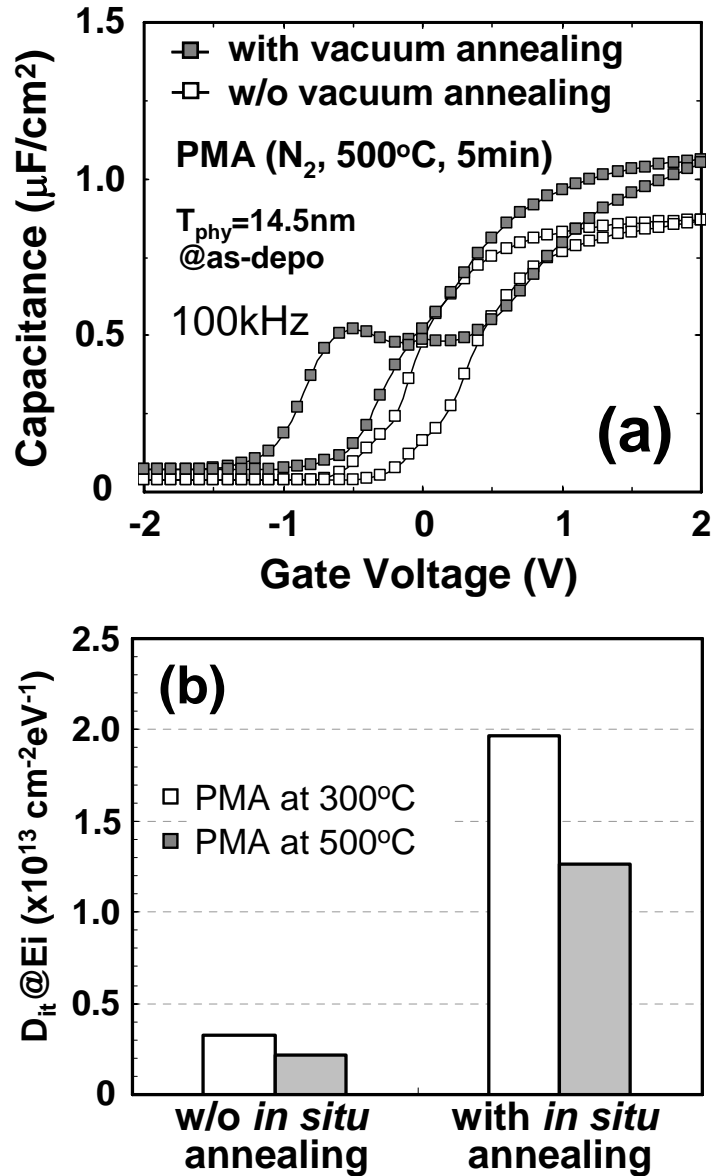


Figure 3-19. (a) C - V characteristic and (b) D_{it} in Pt/ La_2O_3 /Ge structure with and without *in situ* vacuum annealing before Pt electrode deposition.

The interfacial layer growth was further confirmed by XPS analyses as shown in Fig. 3-20 (Ge $3d$ spectra) and Fig. 3-21 (O $1s$ spectra). The thicknesses of Pt electrode and La_2O_3 film and were 1.5 nm and 4.5 nm, respectively. In the Ge $3d$ spectra as shown in Fig. 3-20, the spectra were normalized by La $5s$ peak intensity considering

that the photoelectrons arising from La₂O₃ should be the same with each other because it was deposited simultaneously. A large reduction in GeO_x intensity was observed with *in-situ* vacuum annealing in both cases of PMA at 300 °C and 500 °C. Moreover, decrement of intensities arising from Ge-O-Ge bonding and La-O-Ge bonding was observed from the O 1s spectra as can be seen in Fig. 3-21. These results confirm the suppression of the interfacial layer growth by reduction in density of the hydroxyl group in the La₂O₃ film during the vacuum annealing. On the other hand, a large amount of La-hydroxide still remained in La₂O₃ film after the *in situ* vacuum annealing at 250 °C and PMA. Further research should be needed to control the La-hydroxide to achieve the high dielectric constant of La₂O₃.

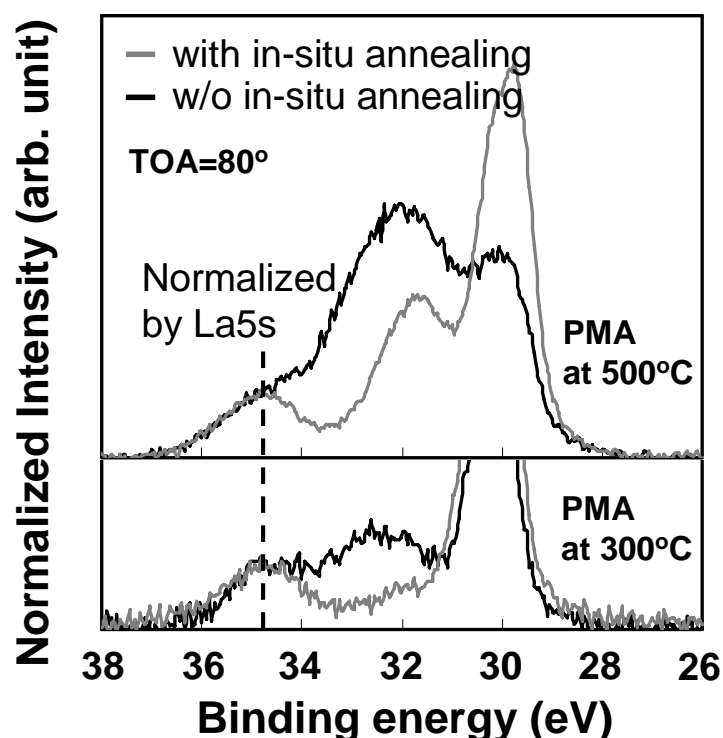


Figure 3-20. XPS spectra of Ge 3d in Pt/La₂O₃/Ge structure with and without *in situ* vacuum annealing before Pt electrode deposition.

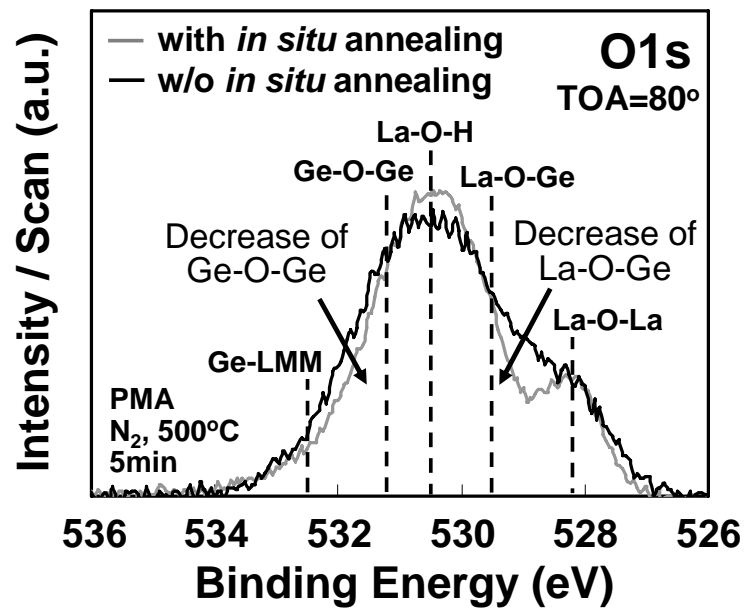


Figure 3-21. XPS spectra of O $1s$ in Pt/ La_2O_3 /Ge structure with and without *in situ* vacuum annealing before Pt electrode deposition.

3.5 Conclusion

Interfacial properties between La₂O₃ and Ge for directly contacted La₂O₃/Ge MOS structures were studied on the various annealing condition in inert N₂ ambient. Less growth of interfacial layer has been observed in La₂O₃/Ge structure compared with La₂O₃/Si system after PDA in N₂ ambient, which suggests formation energy of La-germanate is larger than that of La-silicate. In addition, Ge atoms could be easily diffused into La₂O₃ film as compared with Si, especially Ge oxide was observed on the surface of 21-nm-thick La₂O₃ film after PDA at 600 °C. If La oxide will be used as gate dielectric with EOT less than 1 nm, the thickness of La-oxide film would be necessary less than 7 nm, which means Ge diffused to the surface of La-oxide film by all means after PDA in N₂ at 600 °C. Furthermore, sublimation of Ge oxide diffused to the surface of gate oxide would make device characteristics and reliability be worse.

On the other hand, D_{it} dramatically decreased by PMA in N₂ ambient. This improvement in D_{it} is attributed to growth of interfacial layer caused by the hydroxyl group absorbed in La₂O₃ film. Further discussion about the relation between the interfacial layer and interfacial properties will be described next chapter.

Reference

- [3-1] J. A. Ng, N. Sugii, K. Kakushima, P. Ahmet, K. Tsutsui, T. Hattori, and H. Iwai, "Effective mobility and interface-state density of La₂O₃ nMISFETs after post deposition annealing," *IEICE ELEX*, vol. 3, pp. 316 (2006).
- [3-2] S. M. Sze and Kwok K. Ng, *Physics of Semiconductor* 3rd edition, Wiley, 2007, chapter 6, p. 316.
- [3-3] T. Nishimura, M. Toyama, K. Kita, K. Kyuno and A. Toriumi, "Ion-Implanted p/n Junction Characteristics p- and n-type Germanium," *Ext. Abst. of International Conference on Solid State Devices and Materials (SSDM)*, p.520 (2005)
- [3-4] T. Nishimura, S. Sakata, K. Nagashio, K. Kita, and A. Toriumi, "Low Temperature Phosphorus Activation in Germanium through Nickel Germanidation for Shallow n+/p Junction," *Appl. Phys. Express*, vol. 2, pp.021202 (2009).
- [3-5] A. Dimoulas, G. Vellianitis, G. Mavrou, E. K. Evangelou, K. Argyropoulos, and M. Houssa, "Short minority carrier response time in HfO₂/Ge metal-insulator-semiconductor capacitors," *Microelectronic Eng.*, vol. 80, pp. 34 (2005).
- [3-6] A. Dimoulas, G. Vellianitis, G. Mavrou, E. K. Evangelou, and A. Sotiropoulos, "Intrinsic carrier effects in HfO₂-Ge metal-insulator-semiconductor capacitors," *Appl. Phys. Lett.*, vol. 86, pp. 223507 (2005).
- [3-7] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS capacitors incorporating ultrathin high-k gate dielectric," *IEEE Elect. Dev. Lett.*, vol. 23, pp. 473 (2002).
- [3-8] H. Nohira, T. Yoshida, H. Okamoto, Ng Jin Aun, Y. Kobayashi, S. Ohmi, H. Iwai, E. Ikenaga, K. Kobayashi, Y. Takata, and T. Hattori, "Thermal stability of LaO_x/Si interfacial transition layer", *ECS Trans.* vol. 1 , pp. 87 (2005).
- [3-9] T. Gougousi, M. J. Kelly, D. B. Terry, and G. N. Parsons, "Properties of La-silicate high-K dielectric films formed by oxidation of La on silicon," *J. Appl. Phys.*, vol. 95, pp.

1691 (2004).

[3-10] G. Adachi, *Kidorui no Kagaku (Science of Rare Earths)*, Kagakudojin Co., 1999, p.304 [in Japanese].

[3-11] J.A. Ng, Y. Kuroki, N. Sugii, K. Kakushima, S.-I. Ohmi, K. Tsutsui, T. Hattori, H. Iwai and H. Wong, "Effects of low temperature annealing on the ultrathin La₂O₃ gate dielectric; comparison of post deposition annealing and post metallization annealing," *Microelectronic Engineering*, vol. 80, pp. 206-209, 2005

[3-12] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A sub-400°C germanium MOSFET technology with high-k dielectric and metal gate," *IEEE IEDM Tech. Dig.*, pp. 437 (2002).

[3-13] H. Kim, C. O. Chui, P. C. McIntyre, and K. C. Saraswat, "Local epitaxial growth of ZrO₂ on Ge (100) substrates by atomic layer epitaxy," *Appl. Phys. Lett.*, vol. 83, pp. 2647 (2003).

[3-14] H. Nomura, K. Kita, K. Kyuno, and A. Toriumi, "Thermally Robust Y₂O₃/Ge MOS Capacitors," *Ext. Abstr. SSDM*, pp. 858-859 (2005).

[3-15] D. Schmeisser, R.D. Schnell, A. Bogen, F.J. Himpsel, D. Rieger, G. Landgren, and J.F. Morar, "Surface oxidation states of germanium," *Surf. Sci.*, vol. 172, pp. 455 (1986).

[3-16] C. O. Chui, D-I. Lee, A. A. Singh, P. A. Pianetta, and K. C. Saraswat, "Zirconia-germanium interface photoemission spectroscopy using synchrotron radiation," *J. Appl. Phys.* vol. 97, pp. 113518 (2005).

[3-17] K-I. Seo, S. Sun, D-I. Lee, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Chemical states and electronic structure of a HfO₂/Ge(001) interface," *Appl. Phys. Lett.*, vol. 87, pp. 042902 (2005).

[3-18] K. Tachi, K. Kakushima, P. Ahemt, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "Effect of Oxygen for Ultra-Thin La₂O₃ Film Deposition," *ECS Trans.*, vol. 3, pp. 425 (2006).

[3-19] H. Yamada, T. Shimizu, A. Kurokawa, K. Ishii and E. Suzuki, "MOCVD of High-Dielectric-Constant Lanthanum Oxide Thin Films," J. ECS, vol. 150, pp. G429 (2003).

[3-20] K. Kakushima, K. Tachi, J. Song, S. Sato, H. Nohira, E. Ikenaga, P. Ahmet, K. Tsutusi, N. Sugii, T. Hattori, and H. Iwai, "Comprehensive x-ray photoelectron spectroscopy study on compositional gradient lanthanum silicate film," J. Appl. Phys., *Article in press*.

[3-21] S. Tanuma, C. J. Powell and D. R. Penn, "Calculations of electron inelastic mean free paths. V. Data for 14 organic compounds over the 50-2000 eV range," Surf. Interface Anal., vol. 21, pp. 165 (1994).

[3-22] K. Kita, M. Sasagawa, K. Tomida, M. Toyama, K. Kyuno and A. Toriumi, "Further EOT Scaling of Ge/HfO₂ over Si/HfO₂ MOS Systems," Ext. Abst. of International Workshop International Workshop on Gate Insulator (IWGI), p.186 (2003).

Chapter 4.

Characterization of Interfacial Property with Interfacial Ge-oxide Layer

- 4.1 Introduction
- 4.2 Growth of Interfacial Layer by PDA in Oxygen Ambient
- 4.3 Formation of Chemical GeO₂ Layer before La₂O₃ Deposition
- 4.4 Hysteresis on *C-V* Characteristic in La₂O₃/Ge Structure
- 4.5 Conclusion

4.1 Introduction

In the previous sub-chapter, interface trap density (D_{it}) of La₂O₃/Ge interface can be decrease significantly with the growth of interfacial layer by post metallization annealing. In this chapter, in order to examine the effect of interfacial layer, interfacial layer was introduced intentionally before and after La₂O₃ deposition.

In the first sub-chapter, electric characteristics and chemical composition for the La₂O₃/Ge structure with thermally grown interfacial layer by post-deposition annealing (PDA) in oxygen ambient after the La₂O₃ deposition will be reported. The thickness of interfacial layer was varied with various PDA temperatures and for various PDA durations. Next, chemically formed ultrathin GeO₂ layer was introduced before the La₂O₃ deposition and PDA was performed on various conditions. Finally, hysteresis on C - V characteristic for the La₂O₃/Ge system will be discussed.

4.2 Growth of Interfacial Layer by PDA in Oxygen Ambient

Figure 4-1 shows (a) 100kHz C - V characteristic and (b) interface trap density (D_{it}) of Pt/La₂O₃/Ge MOS structure after PDA in N₂, 3%-H₂+N₂ (FG) and 5%-O₂+N₂ ambient at 425 °C for 30 minutes. A huge bump was observed for the samples after PDA in N₂ and FG resulting in large amount of D_{it} as shown in Fig. 4-1-(b). In contrast, little bump appeared for the sample after PDA in 5%-O₂+N₂ and D_{it} was smaller about one order than those for the samples with PDA in N₂ or FG. It should be noted that D_{it} decreased by oxygen annealing in La₂O₃/Ge structure while the interface defects were not recovered by FG annealing. Moreover, annealing in oxygen ambient induced

increase in D_{it} in the case of HfO₂/Ge structure [4-1] and La₂O₃/Si system [4-2]. Capacitance decrement by PDA in oxygen ambient well indicates the growth of interfacial layer, which was confirmed by XPS measurement and will be described below. $C-V$ hysteresis was not improved by PDA in oxygen ambient. The origin of $C-V$ hysteresis in La₂O₃/Ge will be discussed later.

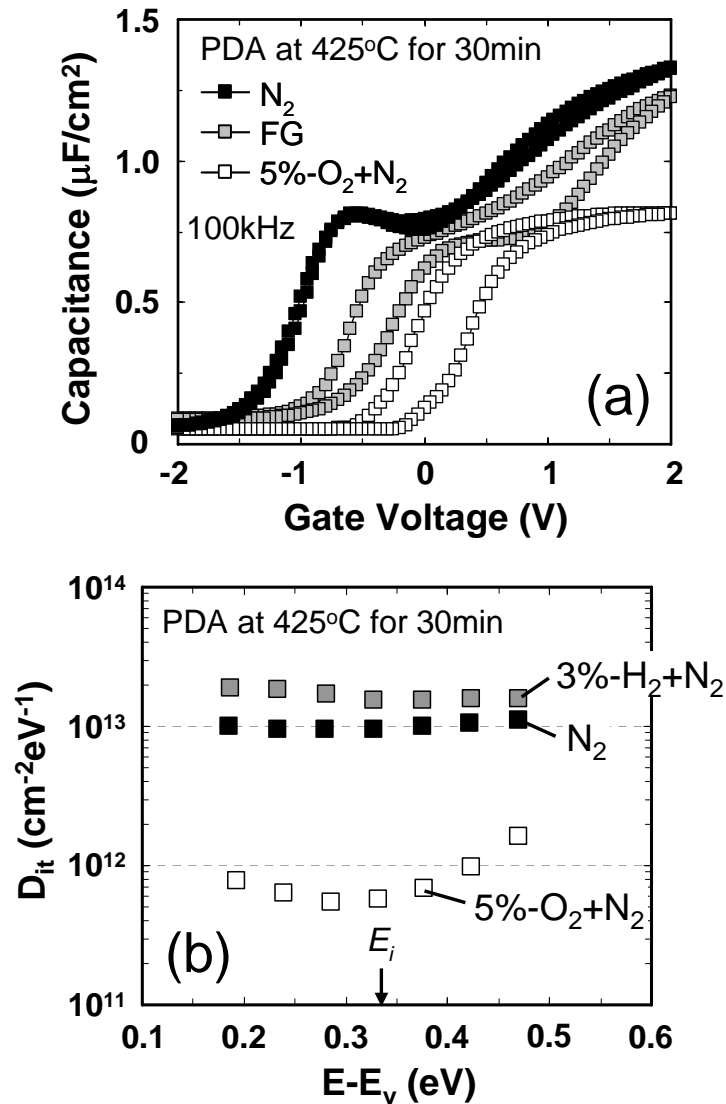


Figure 4-1. (a) 100kHz $C-V$ characteristics and (b) interface trap density of samples after PDA in N_2 , 3% $\text{H}_2 + \text{N}_2$ (FG) and 5% $\text{O}_2 + \text{N}_2$ ambient at 425 °C for 30 minutes.

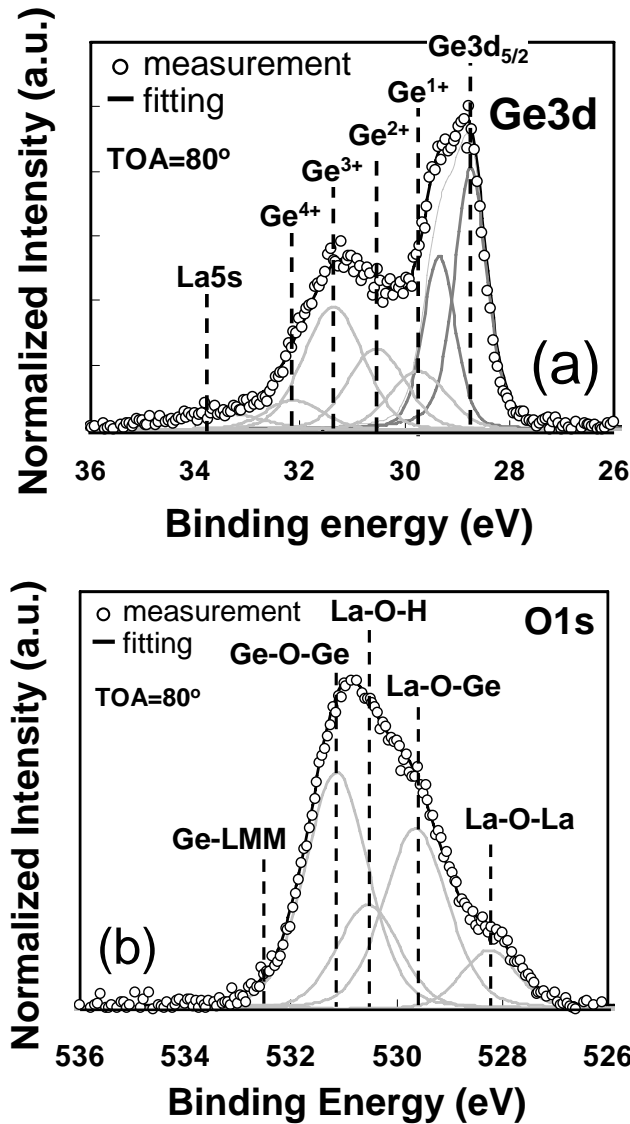


Figure 4-2. (a) Ge 3d and (b) O 1s spectra measured by XPS for the sample after PDA in 5%-O₂+N₂ ambient at 425 °C for 5 minutes.

Figure 4-2 shows (a) Ge 3d and (b) O 1s spectra measured by XPS for the sample after PDA in 5%-O₂+N₂ at 425°C for 5 minutes. In the Ge 3d spectra, the intensities of Ge³⁺ and Ge⁴⁺ spectra increased by PDA treatment in oxygen ambient such as those by PMA treatment as shown in chapter 3. Moreover, the intensity of Ge-O-Ge bonding also became larger than those arising from the sample after PDA in

N₂ ambient as shown in Fig. 3-7. These results suggest the grown layer would be Ge sub-oxide. The grown layer was confirmed to be surely located at the interface by the angle-resolved XPS analysis as can be seen in Fig. 4-3. The N_{Ge-O-Ge} and N_{La-O-Ge} become smaller than sum of N_{La-O-La} and N_{La-O-H} with decreasing TOA, which means Ge sub-oxide (Ge-O-Ge bonding) and La-germanate (La-O-Ge bonding) are grown under the deposited La oxide.

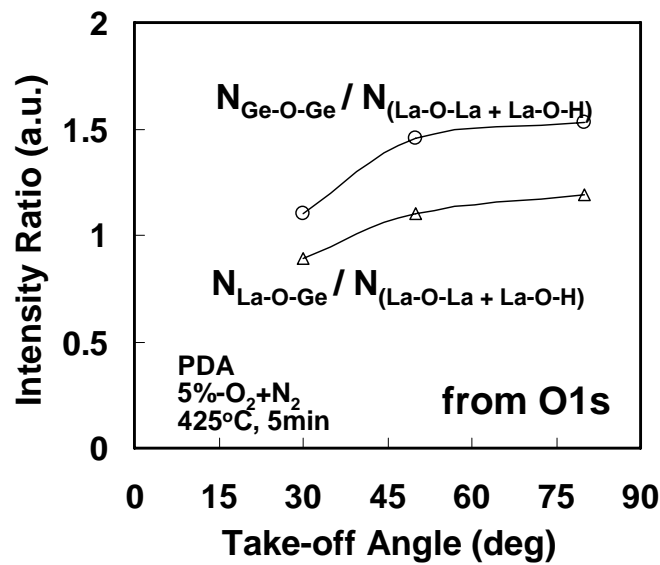


Figure 4-3. Dependence of intensity ratio of (a) $N_{\text{Ge-O-Ge}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ and (b) $N_{\text{La-O-Ge}} / (N_{\text{La-O-La}} + N_{\text{La-O-H}})$ on take-off angle.

Figure 4-4 shows 100kHz $C-V$ characteristics of samples after PDA in 5%-O₂+N₂ at 400-500 °C. Capacitance decreased with increasing annealing temperature, which suggests increase in growth of the interfacial layer. Moreover, the bump of $C-V$ curves decreased with increasing annealing temperature, there being no bump after PDA in 5%-O₂+N₂ at 500 °C. The decrease of $C-V$ bumps was in proportion to reduction of interface trap density as shown in Fig. 4-5. The amount of hysteresis was almost same at

all annealing temperature, in which the $C-V$ hysteresis in sample after PDA in 5%-O₂+N₂ at 500 °C was larger than that of sample after PDA in N₂ at 500 °C.

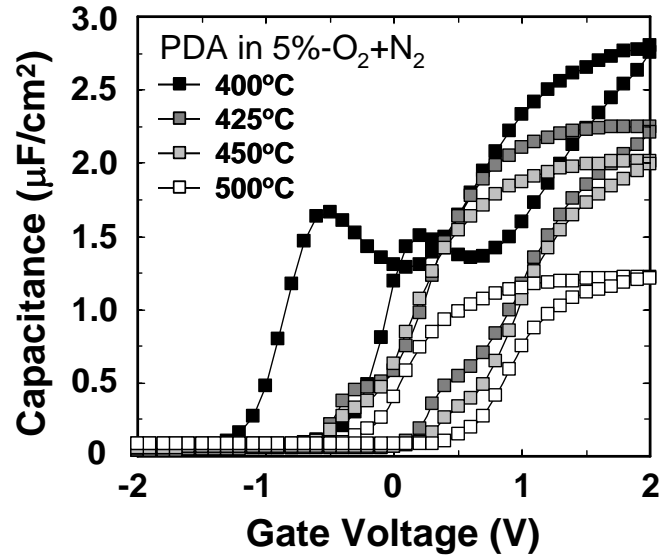


Figure 4-4. 100kHz $C-V$ characteristics of samples after PDA in 5%-O₂+N₂ at 400-500°C for 5 minutes.

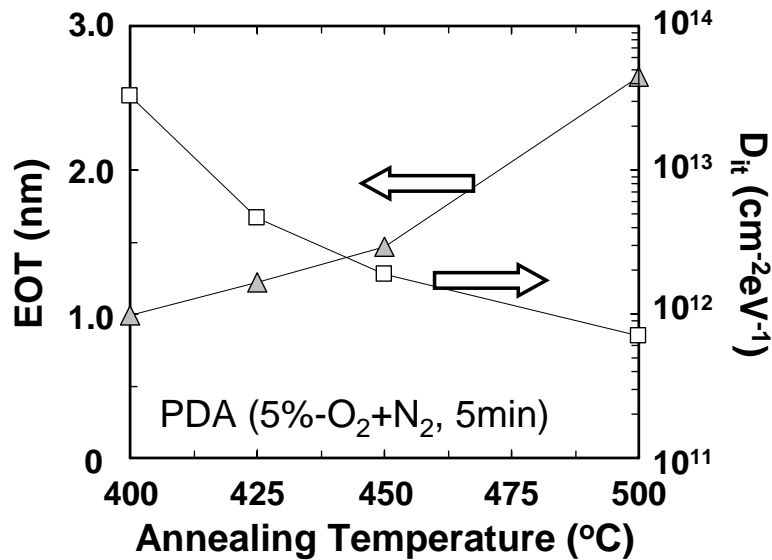


Figure 4-5. Dependence of interface trap density (D_{it}) and EOT on PDA temperature for the samples after PDA in 5%-O₂+N₂ for 5 minutes.

Figure 4-6 shows the physical-thickness change of La₂O₃ films for the samples after PDA in N₂ or 5%-O₂+N₂, which was measured by spectroscopic ellipsometry. At the annealing temperature of 400 °C, the film thickness decreased by PDA both in N₂ and 5%-O₂+N₂ ambient due to the densification and/or desorption of hydroxyl in the La₂O₃ films. However, the film thickness increased significantly with increasing annealing temperature above 425 °C in the case of PDA in 5%-O₂+N₂ ambient, suggesting the growth of interfacial layer, while film thickness was almost same for the samples with PDA in N₂ up to the annealing temperature of 600 °C.

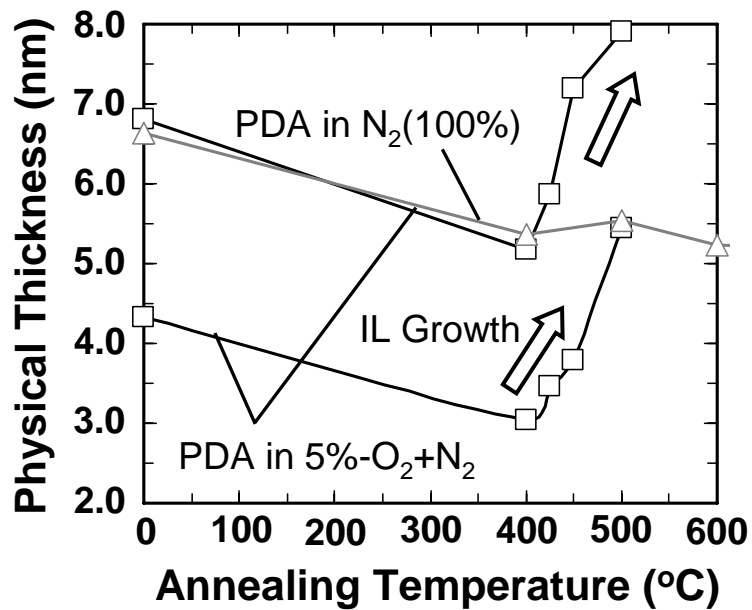


Figure 4-6. Dependence of physical thickness of La₂O₃ films on annealing temperature for the samples after PDA in N₂ or 5%-O₂+N₂, which was measured by spectroscopic ellipsometry.

Similar results of D_{it} decrease in accordance with growth of interfacial layer could be acquired for the samples after various durations of PDA in 5%-O₂+N₂ ambient. Figure 4-7 shows 100kHz $C-V$ characteristics of samples after PDA in 5%-O₂+N₂ for

various annealing time at 425 °C. Capacitance and C - V bump decreased with increasing annealing time, suggesting that increase in the thickness of interfacial layer. The film thicknesses and EOT increased in proportion to logarithmic order with respect to annealing time as shown in Fig. 4-8.

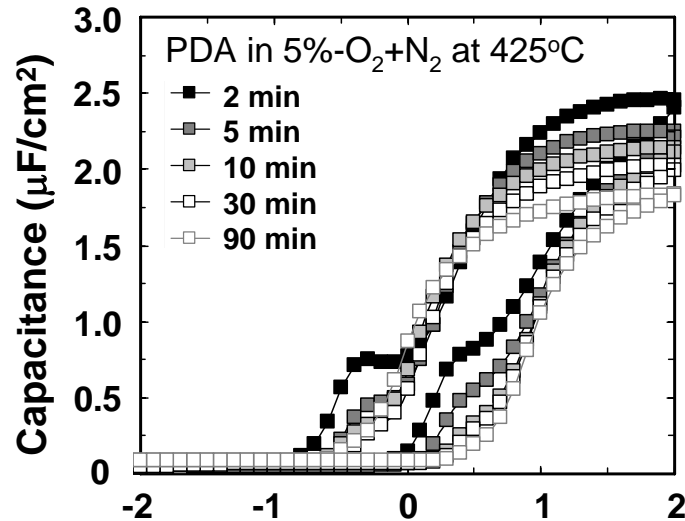


Figure 4-7. 100kHz C - V characteristics of samples after PDA in 5%-O₂+N₂ at 425 °C for various annealing time.

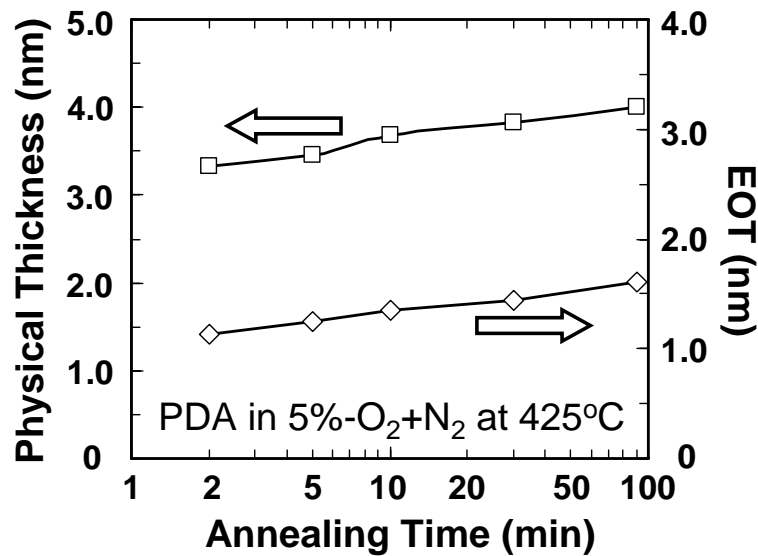


Figure 4-8. Dependence of physical thickness and EOT on annealing time.

Figure 4-9 shows changes in EOT as a function of physical thickness for the samples after PDA in 5%-O₂+N₂ ambient. EOT changes are dependant on annealing temperature or time. Considering that increase in physical thickness and EOT was caused by growth of the interfacial layer, dielectric constant of the interfacial layer was obtained from the slope in the Fig. 4-9 and an equation is expressed below.

$$\Delta EOT = \frac{\epsilon_{SiO_2}}{\epsilon_{IL}} \Delta T_{phy} . \quad (4-1)$$

Here, ϵ_{SiO_2} and ϵ_{IL} are dielectric constant of SiO₂ and the interfacial layer (IL) respectively. The calculated dielectric constant of the interfacial layer is 5.6~5.8, which is similar with that of GeO₂ [4-3, 4-4]. Considering the dielectric constant of La₂O₃ and Ge are 27 and 16, the dielectric constant of La-germanate would become much larger than the value of 5.8. Thus, the grown interfacial layer should be not La-germanate but Ge sub-oxide.

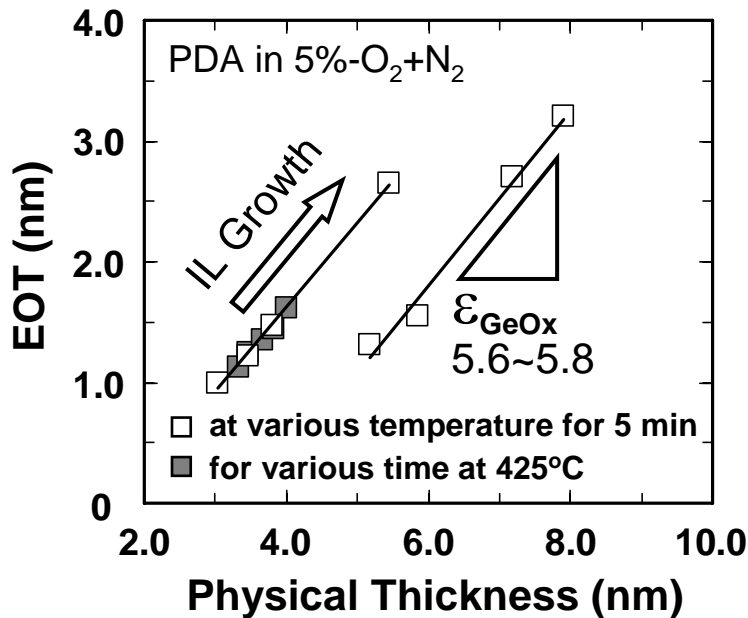


Figure 4-9. Changes in EOT as a function of physical thickness, which is dependant on annealing temperature or time.

The physical thickness (PT) measured by spectroscopic ellipsometry actually consist of the physical thickness of La₂O₃ ($PT_{La_2O_3}$) and the interfacial Ge-oxide layer (PT_{GeO_x}), i.e.

$$PT = PT_{La_2O_3} + PT_{GeO_x} . \quad (4-2)$$

By treating the bilayer structure as two capacitors in series, total EOT is showed by sum of $EOT_{La_2O_3}$ and EOT_{GeO_x} .

$$EOT = EOT_{La_2O_3} + EOT_{GeO_x} . \quad (4-3)$$

On the other hand

$$PT_{La_2O_3} = \frac{\epsilon_{La_2O_3}}{\epsilon_{SiO_2}} EOT_{La_2O_3} = \frac{\epsilon_{La_2O_3}}{\epsilon_{SiO_2}} (EOT - EOT_{GeO_x}) \quad (4-4)$$

and

$$PT_{GeO_x} = \frac{\epsilon_{GeO_x}}{\epsilon_{SiO_2}} EOT_{GeO_x} . \quad (4-5)$$

Inserting Eq. (4-4) and (4-5) into Eq. (4-2) and rearranging, one can obtain

$$EOT = \frac{\epsilon_{SiO_2}}{\epsilon_{La_2O_3}} PT + \left(1 - \frac{\epsilon_{GeO_x}}{\epsilon_{La_2O_3}}\right) EOT_{GeO_x} . \quad (4-6)$$

In the Eq. (4-6), EOT_{GeO_x} can be obtain easily by plotting EOT against the physical thickness with different La₂O₃ film thickness and physical thickness of the interfacial Ge-oxide layer can be calculated from Eq. (4-5).

Figure 4-10 shows EOT versus physical thickness plot for the samples with different La₂O₃ film thicknesses. PDA was performed in 5%-O₂+N₂ ambient at 425-500 °C. Dielectric constant of La₂O₃ films calculated from the slop of Fig. 4-10 on the basis of the Eq. (4-6) is 17~18, which did not change by annealing temperature. This value is

smaller than that of bulk La₂O₃ [4-5], which was considered to be due to the water absorption of La₂O₃ films in ambient before deposition of gate electrode [4-6]. The physical thickness of interfacial layer can be evaluated by the intercept of vertical axis at zero film thickness from Fig. 4-10 on the basis of the Eq. (4-5) and (4-6) as dielectric constant of La₂O₃ and GeO_x is already known. The physical thickness of interfacial layer was also confirmed by HR-TEM image for the sample after PDA in oxygen ambient at 425 °C, which can be seen in Fig. 4-11. From the thickness of interfacial layer of 1.1 nm in the case of 425 °C PDA and total film thicknesses measured by spectroscopic ellipsometry, thickness of interfacial layer for the samples with PDA at 400, 450 and 500 °C was also calculated. Figure 4-12 shows the thickness of interfacial layer extracted by EOT versus physical thickness plot or TEM image and spectroscopic ellipsometry measurement. IL thicknesses evaluated from electrical and physical method similarly increases exponentially with respect to PDA temperature.

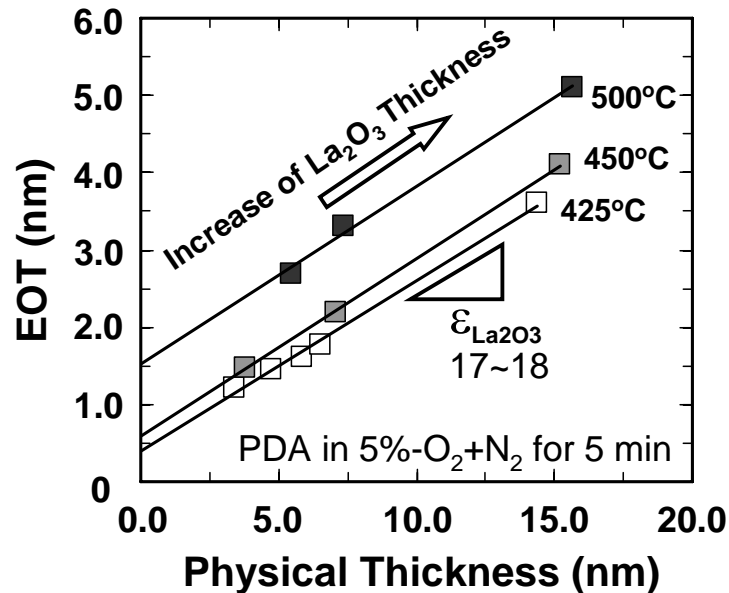


Figure 4-10. EOT versus physical thickness plot for the samples with different La₂O₃ film thicknesses, where PDA was performed in 5%-O₂+N₂ ambient at 425-500 °C.

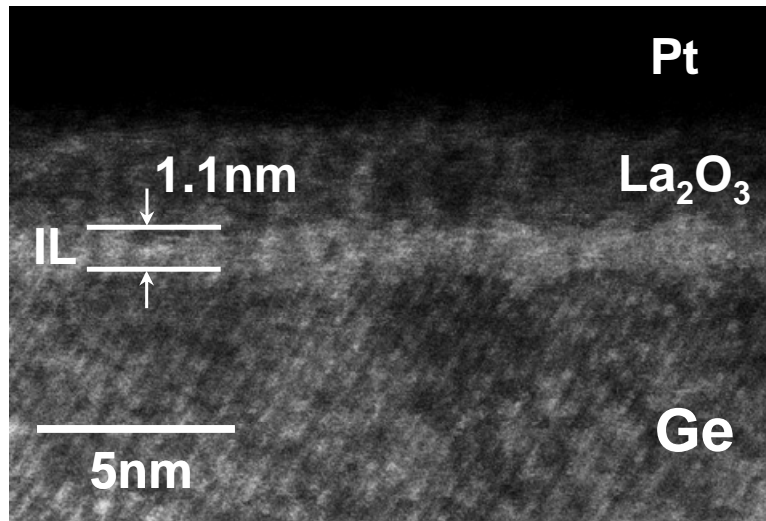


Figure 4-11. HR-TEM image of La₂O₃/Ge structure with PDA in 5%-O₂+N₂ at 425°C for 5 minutes. The total film thickness is 3.5 nm and the thickness of the interfacial layer is 1.1 nm.

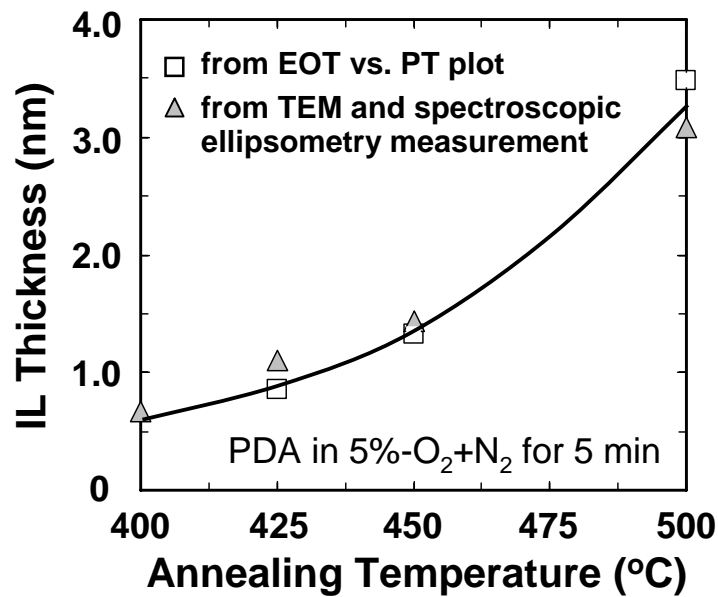


Figure 4-12. The thicknesses of interfacial layer calculated from EOT versus physical thickness (PT) plot and obtained from HR-TEM image and spectroscopic ellipsometry measurement.

Figure 4-13 shows EOT and interface trap density as a function of the estimated IL thickness. The interface trap density was reduced significantly with increasing the interfacial layer thickness up to 1.5 nm; however, the decrease in interface trap density weakened over 1.5 nm. On the other hand, EOT swelled with increasing the interfacial layer thickness relatively. Considering the both small EOT and little interface trap density, appropriate thickness of the interfacial layer is regarded as about 1.5 nm.

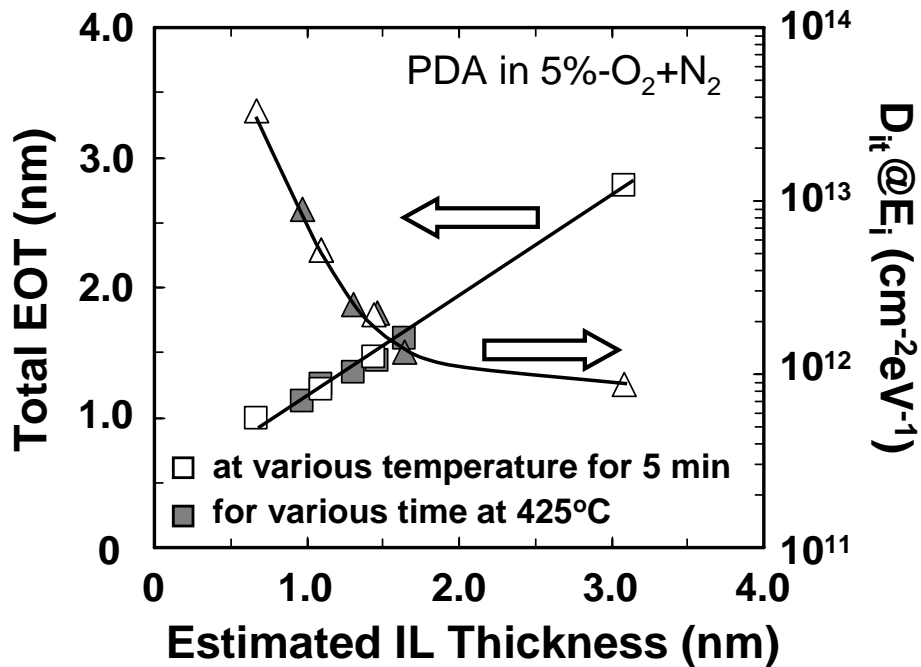


Figure 4-13. EOT and interface trap density as a function of the thickness change in interfacial Ge-oxide layer, where thickness of interfacial layer were estimated from HR-TEM images and spectroscopic ellipsometry measurement.

4.3 Formation of Chemical GeO₂ Layer before La₂O₃ Deposition

The large hysteresis on *C-V* characteristics was observed for the sample after PDA in 5%-O₂+N₂ as shown in Fig. 4-4 and 4-7. This *C-V* hysteresis might be generated by the growth of Ge sub-oxide [4-7]. In order to examine the effect on interfacial Ge oxide layer with little amount of sub-oxide, a GeO₂ layer was formed chemically by H₂O₂ solution before the La₂O₃ deposition. Figure 4-14 shows Ge 3*d* spectra measured by XPS for the sample with chemical oxide (CO) formed by dipping Ge substrate in H₂O₂ for 30 seconds. The thickness of chemical oxide layer was 1.3-1.5 nm, which was measured by spectroscopic ellipsometry. As shown in Fig. 4-14, the chemically formed Ge oxide showed almost single peak of Ge⁴⁺ (GeO₂) with little sub-oxide.

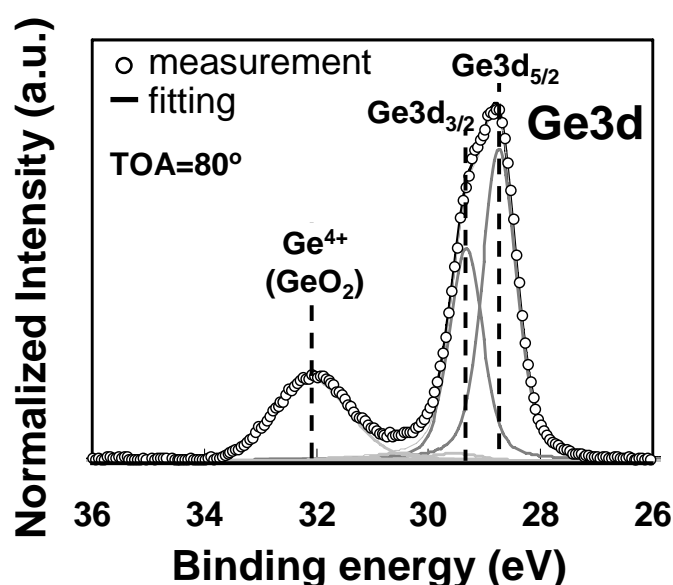


Figure 4-14. Ge 3*d* spectra measured by XPS for the sample with chemical oxide (CO) formed by dipping Ge substrate in H₂O₂ for 30 seconds.

For the Ge MOS capacitor fabrication, a La₂O₃ layer was deposited on CO layer at room temperature below the sublimation temperature of CO that is considered to be 150 °C in the UHV chamber. Figure 4-15 shows $C-V$ characteristics for the sample with the CO layer. PDA was carried out in N₂ ambient at 400-500 °C for 5 minutes. Although PDA was performed in N₂ ambient, $C-V$ bump was dramatically reduced with the CO layer as compared to that without the CO layer as shown in Fig. 3-1. Moreover, small $C-V$ hysteresis could be achieved after PDA at 500 °C for the sample with CO layer.

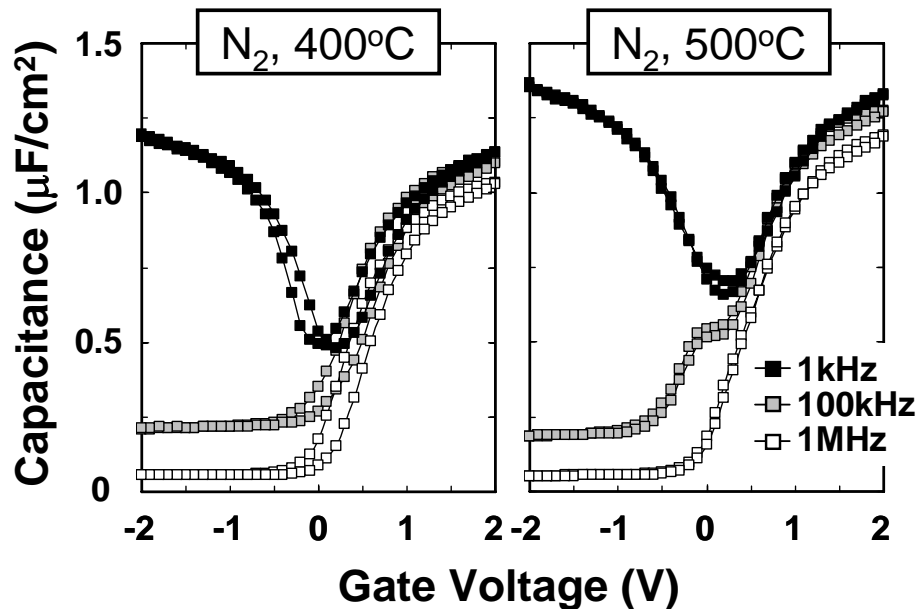


Figure 4-15. shows $C-V$ characteristics for the sample with the CO layer. PDA was carried out in N₂ ambient at 400-500 °C for 5 minutes.

Figure 4-16 shows EOT, $C-V$ hysteresis and D_{it} obtained by various annealing conditions with the CO layer. D_{it} for the samples without the CO layer was also plotted as reference. Although little improvement in D_{it} was observed at as-deposited state, samples with the CO layer showed significant improvement after PDA in N₂ and

5%-O₂+N₂ ambient. EOT increment by PDA in 5%-O₂+N₂ ambient at 425 °C indicated the additional growth of the interfacial layer, which shows smallest D_{it} value. Very large amount of $C-V$ hysteresis could be reduced after PDA, though it still remained quiet large except the case of PDA in N₂ at 500 °C.

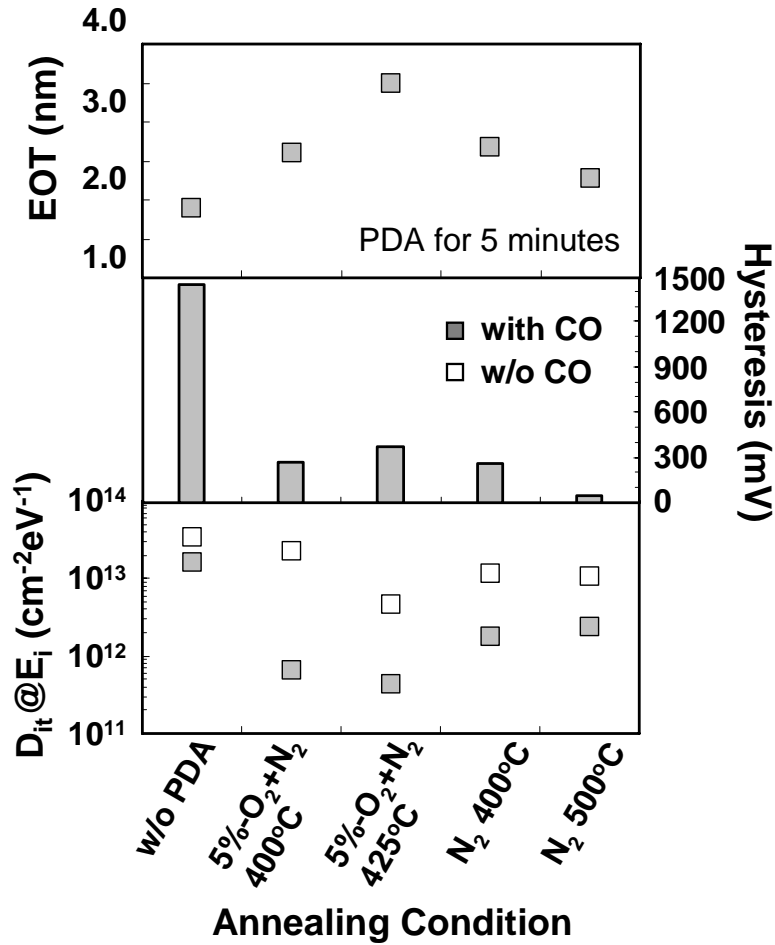


Figure 4-16. EOT, $C-V$ hysteresis and D_{it} obtained by various annealing conditions with the CO layer. D_{it} for the samples without the CO layer was also plotted as reference.

Figure 4-17 shows XPS spectra of Ge 3*d* and O 1*s* for the samples with and without the CO layer. The Ge 3*d* spectrum of CO on Ge substrate is also showed as reference. As shown in Ge 3*d* spectra, the chemically formed GeO₂ showed single peak of Ge⁴⁺, however, various sub-oxide signals were detected after La₂O₃ deposition in samples with the CO layer. Furthermore, PDA treatment eliminated the GeO₂ component completely so as to form Ge¹⁺ and Ge²⁺ components. In the spectra of O 1*s*, almost same intensity ratio was observed in deconvoluted each spectrum for the samples without PDA and with PDA at 400 °C. Only in case of the sample with the CO layer and PDA at 500 °C, La-O-H bonding decreased and La-O-Ge bonding increased, suggesting the formation of La-germanate which appeared as Ge¹⁺ and Ge²⁺ in Ge 3*d* spectra. Therefore, the formation of La-germanate is considered to effectively improve both the *D_{it}* and hysteresis.

On the other hand, in case of La-silicate, mainly two compositions of La₂Si₁O₅ and La₂Si₂O₇ can be formed by reaction between La₂O₃ and Si with oxygen supply [4-8], which is shown below.



By analogy with La-silicate case, La-germanate is also thought to be formed those of two compositions. In fact, the La-silicate of La₂Si₂O₇ and La₂Si₁O₅ can be also detected in Si spectra between Si³⁺ and Si⁴⁺ and between Si²⁺ and Si³⁺ respectively [4-9]. As very little amount of Ge³⁺ and Ge⁴⁺ was observed in Ge 3*d* spectra, grown La-germanate should be almost La₂Ge₁O₅. Moreover, the La-silicate of La₂Si₁O₅ contains four of La-O-Si bonding and one La-O-La, the intensity increment of La-O-La bonding for the

sample with CO after PDA at 500 °C was due to the formation of La-germanate.

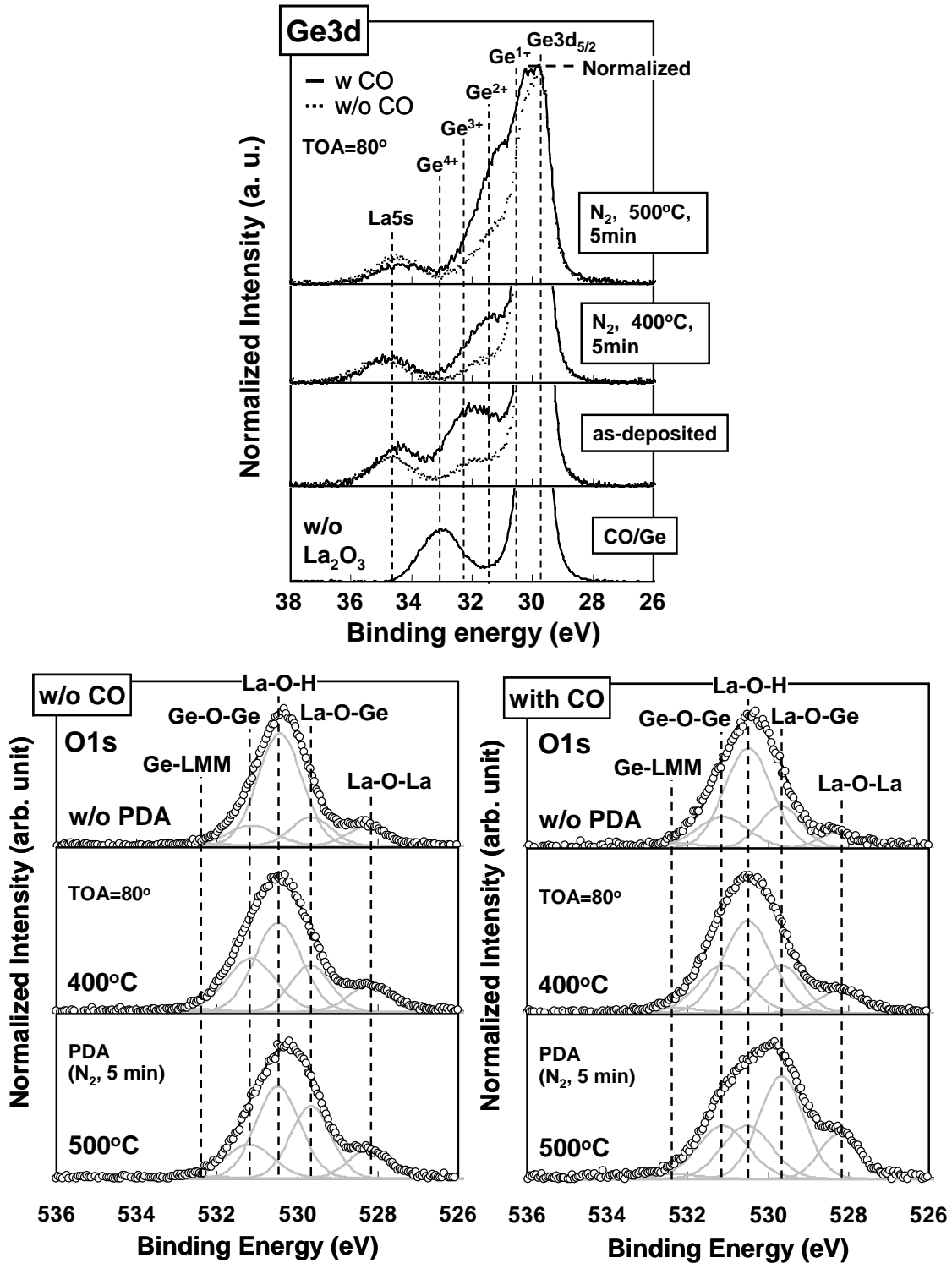


Figure 4-17. XPS spectra of Ge 3d and O 1s in samples with and without the CO layer.

The Ge 3d spectrum of CO on Ge substrate is also shown as reference.

In order to attain the small EOT, samples using thinner La₂O₃ films with same chemical GeO₂ layer. Figure 4-18 shows $C-V$ characteristics for the samples with various thickness of La₂O₃ film. PDA was performed in N₂ at 500 °C for 5 minutes. Very small $C-V$ hysteresis for the sample with EOT over 2 nm became larger with decreasing the EOT. The intensity of electric field comes to be strengthened with decreasing the EOT in same range of gate voltage. Thus, strengthened gate electric-field induced more charges in the density of oxide trap through the oxide (by tunneling effect) so that $C-V$ hysteresis increases with decreasing the EOT. D_{it} increment observed in Fig. 4-19 was negligible compared with increase in $C-V$ hysteresis. The origin of large $C-V$ hysteresis in La₂O₃/Ge structure will be discussed specifically in the next sub-chapter.

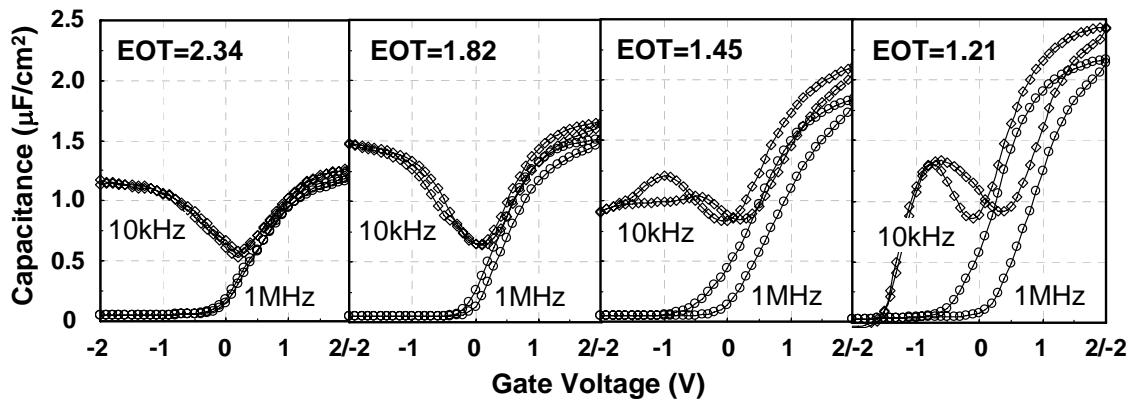


Figure 4-18. $C-V$ characteristics for the samples with various thickness of La₂O₃ film. PDA was performed in N₂ at 500 °C for 5 minutes.

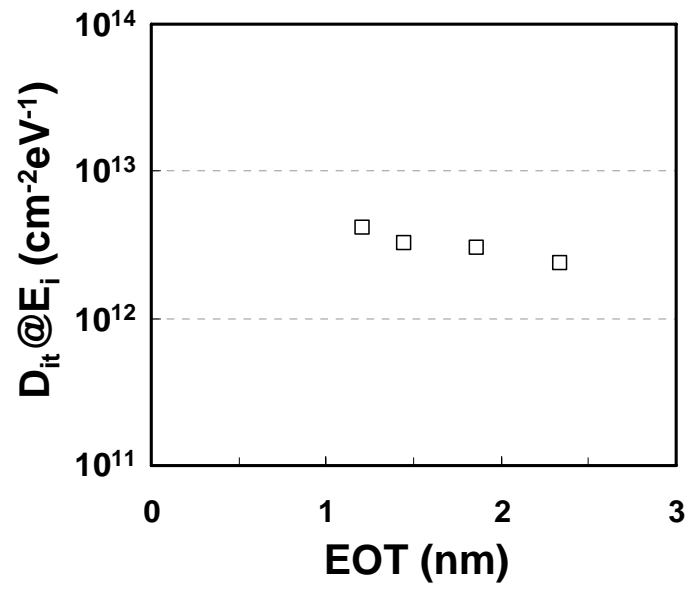


Figure 4-19. Dependence of D_{it} on EOT. D_{it} increment was negligible as compared with increase in $C-V$ hysteresis.

4.4 Hysteresis on $C-V$ Characteristic in La₂O₃/Ge Structure

Figure 4-20 shows the dependence of $C-V$ hysteresis on different EOT for the samples fabricated on three different conditions. A large amount of $C-V$ hysteresis was observed in both EOT for the samples after PDA in oxygen ambient due to the growth of Ge sub-oxide layer, which is discussed in previous chapter. As opposed to the sample with PDA in oxygen ambient, small $C-V$ hysteresis can be achieved by PDA in N₂ at 500 °C without interfacial layer growth as shown in chapter 3-2. On the other hand, $C-V$ hysteresis became larger with decreasing the EOT in case of interfacial La-germanate-layer formation by reaction between La₂O₃ and chemically formed GeO₂.

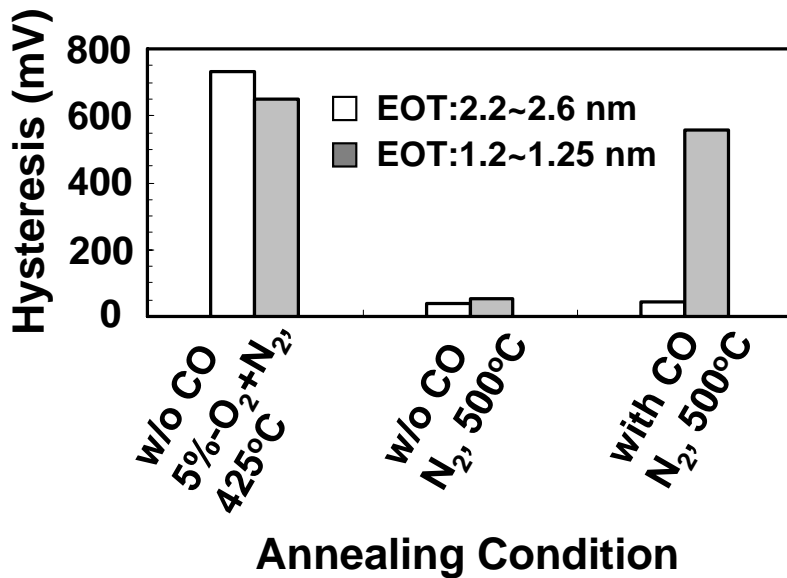


Figure 4-20. $C-V$ hysteresis on different EOT for the samples fabricated on three different conditions.

The reason of $C-V$ hysteresis in La₂O₃/Ge structure is roughly considered to be oxygen vacancy of deposited La₂O₃ film [4-10] and growth of the Ge sub-oxide layer [4-7]. Actually, a large amount of $C-V$ hysteresis has been also observed in as-deposited La₂O₃ film on Si substrate, which can be reduced by the formation of La-silicate by oxygen supply during the La₂O₃ deposition or annealing over 500 °C [4-10]. In case of La₂O₃/Ge structure, small $C-V$ hysteresis can be achieved after PDA at 500 °C in N₂. This result would be attributed to the formation of La-germanate through whole La₂O₃ film with less growth of Ge sub-oxide (see Fig. 4-21), though it showed large D_{it} due to little interfacial layer. The formation of La-germanate was also observed for the sample with PDA in oxygen ambient as shown in Fig. 4-21; however, large amounts of Ge sub-oxide induced a large amount of oxide-trap density. As most of Ge sub-oxide layer is located in the La₂O₃/Ge interface in case of PDA in oxygen ambient, moreover, large amounts of charges are easily drawn into the oxide traps from the substrate. Thus, large $C-V$ hysteresis is induced even in the case of large EOT (low gate electric field) as shown in Fig. 4-20. On the other hand, Ge sub-oxide is distributed throughout the La₂O₃ film for the samples after PDA in N₂ at 500 °C both with and without the CO layer. $C-V$ hysteresis increment with decreasing in EOT observed only for the sample with the CO layer is thought to be due to the larger amount of Ge sub-oxide which is the remainder of decomposed CO after the formation of La-germanate. Larger amount of Ge sub-oxide increases oxide-trap density in La₂O₃ film, causing strengthened gate electric-field to fill more charges into oxide traps with decreasing of EOT.

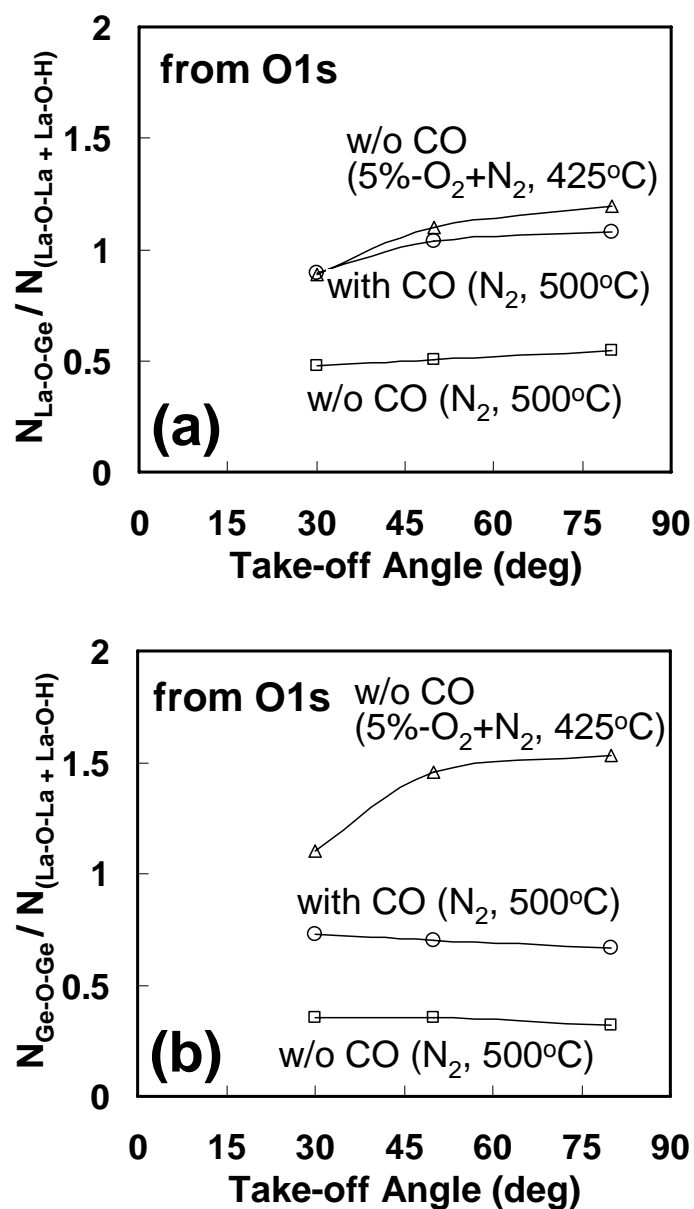


Figure 4-21. Angle-resolved XPS analyses of (a) La-O-Ge and (b) Ge-O-Ge intensities against the La oxide (La-O-La and La-O-H). Ge sub-oxide is distributed throughout the La₂O₃ film for the samples after PDA in N₂ at 500 °C both with and without the CO layer.

4.5 Conclusion

In this chapter, effect of interfacial Ge oxide layer has been examined for the improvement of interfacial properties in La₂O₃/Ge structure. D_{it} can be reduced by thermally grown interfacial layer with PDA in oxygen ambient. Grown interfacial layer is thought to be Ge sub-oxide according to the dielectric constant of 5.8 and the results of XPS measurement. Considering the both small EOT and low D_{it} , appropriate thickness of the interfacial layer is assumed to be about 1.5 nm.

Ge sub-oxide in the grown interfacial layer is considered to cause increase in $C-V$ hysteresis. By using the interfacial chemical oxide layer with little Ge sub-oxide, both hysteresis and D_{it} can be reduced after proper annealing. This would be attributed to the formation of La-germanate at the La₂O₃/Ge interface. However, Ge sub-oxide has been still remained in the film, resulting in increase of $C-V$ hysteresis with decreasing in EOT. In order to remove the $C-V$ hysteresis in La₂O₃/Ge structure, growth of Ge sub-oxide should be completely suppressed.

References

- [4-1] K. Kita, M. Sasagawa, K. Tomida, K. Kyuno, and A. Toriumi, "Oxidation-induced damages on germanium MIS capacitors with HfO₂ gate dielectric," Ext. Abstr. SSDM, pp. 292-293 (2003).
- [4-2] J. A. Ng, N. Sugii, K. Kakushima, P. Ahmet, K. Tsutsui, T. Hattori, and H. Iwai, "Effective mobility and interface-state density of La₂O₃ nMISFETs after post deposition annealing," IEICE ELEX, vol. 3, pp. 316-321 (2006).
- [4-3] E. B. Gorokhov, I. G. Kosulina, S. V. Pokrovskaya, and I. G. Neizvestny, "Mechanical and electrical properties of the double-layer film system GeO₂-Si₃N₄ on Ge," Phys. Stat. Sol. (a), vol. 101, pp. 451 (1987).
- [4-4] C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Ge/GeO₂ Interface Control with High-Pressure Oxidation for Improving Electrical Characteristics," Appl. Phys. Express, vol. 2, pp. 071404, (2009).
- [4-5] J. Robertson "High dielectric constant gate oxides for metal oxide Si transistors," Rep. Prog. Phys., vol. 69, pp. 327 (2006).
- [4-6] Y. Zhao, M. Toyama, K. Kita, K. Kyuno, and A. Toriumi "Moisture Absorption-Induced Permittivity Deterioration and Surface Roughness Enhancement of Lanthanum Oxide Films on Silicon," Ext. Abstr. SSDM, pp. 546-547 (2005).
- [4-7] H. Nomura, K. Kita, T. Nishimura, and A. Toriumi, "Oxidation and Reduction of GeO_x/Ge and GeO_x/ Si in O₂ and N₂ annealing," 2nd Int. Workshop on New Group IV Semiconductor Nanoelectronics, pp. 31 (2006).
- [4-8] L. Li, Z. Tang, W. Sun, and P. Wang, "Phase Diagram Prediction of the Al₂O₃-SiO₂-La₂O₃ System," J. Mat. Sci. and Tech. vol. 15, pp. 439 (1999).
- [4-9] K. Kakushima, K. Tachi, J. Song, S. Sato, H. Nohira, E. Ikenaga, P. Ahmet, K. Tsutusi, N. Sugii, T. Hattori, and H. Iwai, "Comprehensive x-ray photoelectron spectroscopy study on compositional gradient lanthanum silicate film," J. Appl. Phys.,

Article in press.

[4-10] K. Tachi, K. Kakushima, P. Ahemt, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "Effect of Oxygen for Ultra-Thin La₂O₃ Film Deposition," ECS Trans., vol. 3, pp. 425 (2006).

Chapter 5.

Impact of Metal Gate Electrode Process on Ge-MOS device

- 5.1 Introduction
- 5.2 Leakage Current in Pt/La₂O₃/Ge Structure with PMA
- 5.3 Characterization of Ge MOS Structure with Various Metal Gate Electrodes
- 5.4 *in situ* Metallization Process for Gate Electrode Formation
- 5.5 Introduction of Atomic-hydrogen with Al-capping Layer on Tungsten Electrode
- 5.6 Conclusion

5.1 Introduction

For self-align process and recrystallization after interconnection, post metallization annealing (PMA) is crucial for semiconductor process. In case of Ge MOSFET, source and drain (S/D) activation energy was quiet low compared to Si MOSFET. Boron implanted S/D for p-MOSFET and phosphorous implanted S/D for n-MOSFET can be activated by annealing at 400 °C and 500 °C, respectively [5-1]. Moreover, Ni-germanide with phosphorous implantation needs only 300 °C for making p/n junction [5-2]. In this chapter, thermodynamic stability of metal/La₂O₃/Ge structures with various metal electrodes after PMA at 300-500 °C will be described.

On the other hand, La₂O₃ has strong hygroscopic property so that it easily forms hydroxide by absorbing moisture from air [5-3]. Dielectric constant of La-hydroxide is lower than La₂O₃ and the more it exposed in air, the more degraded dielectric constant was [5-4]. In addition, the hydroxyl group absorbed in the La₂O₃ film enhances the chemical reaction at the La₂O₃/Ge interface during the PMA, which is shown in chapter 3. In order to avoid the formation of La-hydroxide, *in situ* gate metallization process, namely deposition of a gate electrode without exposing La₂O₃ to the air after deposition of the La₂O₃ film, has been proposed [5-5]. In this chapter, the *in situ* gate metallization process for La₂O₃/Ge MOS structures in terms of electrical characteristics and interfacial properties will be discussed. Furthermore, the effect of atomic hydrogen introduction generated by Al-capping on tungsten electrode will be also discussed.

5.2 Increase of Leakage Current in Pt/La₂O₃/Ge Structure with PMA

In the chapter 3, interface properties of Pt/La₂O₃/Ge structure after PMA was described. Interface trap density (D_{it}) can be reduced by growth of the interfacial Ge oxide layer after PMA due to absorbed hydroxyl group into the La₂O₃ film. On the other hand, increase of leakage current density was observed after PMA as can be seen in Fig. 5-1. Leakage current density increased sharply with increasing PMA temperature and showed almost dielectric breakdown characteristics at the temperature of 500 °C. Increase of leakage current was also getting larger with increasing PMA time (see Fig. 5-2). Moreover, leakage current density suddenly increased and dispersed with the thickness of La₂O₃ film under 7 nm, which is shown in Fig. 5-3.

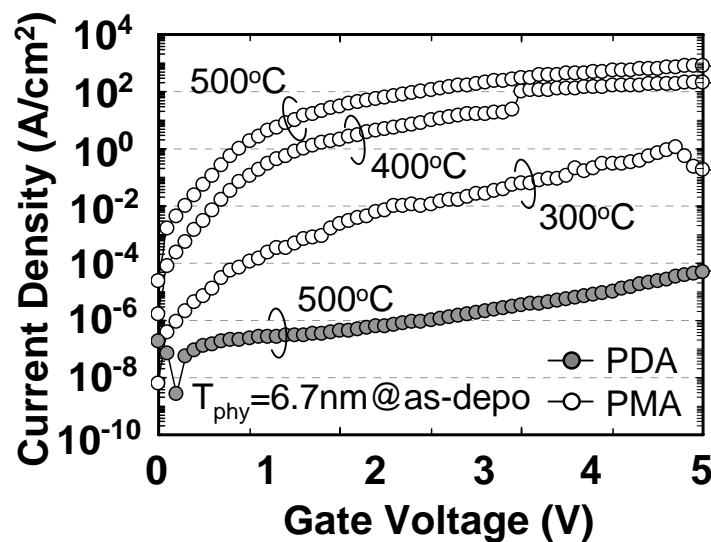


Figure 5-1. Leakage current density in samples with PMA or PDA at various temperatures. The film thickness of La₂O₃ is 6.7 nm at as-deposited condition.

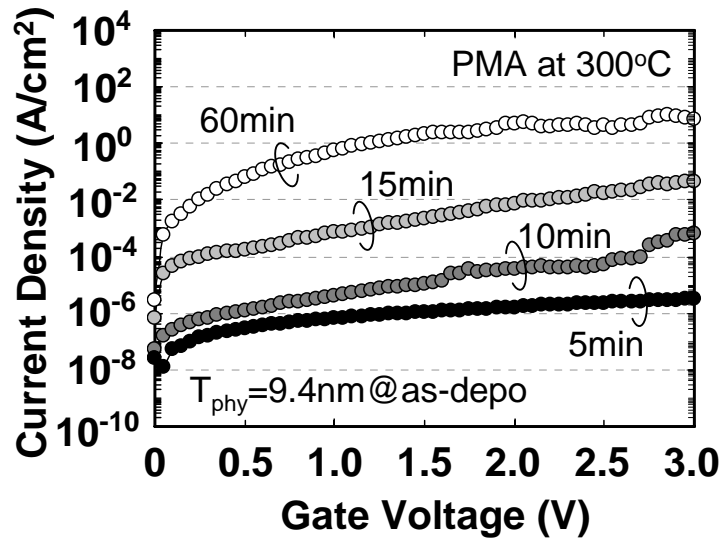


Figure 5-2. Dependence of leakage current density on PMA time for the samples with PMA at 300 °C. Leakage current density increased with increasing annealing time.

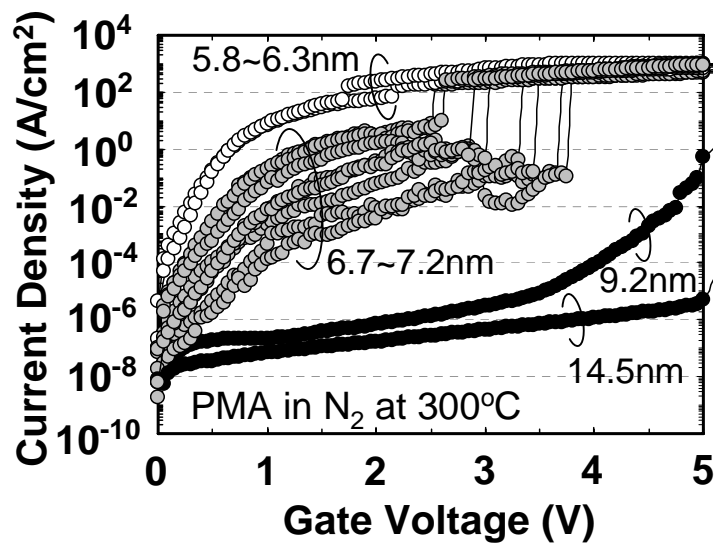


Figure 5-3. Dependence of leakage current density on La₂O₃ thickness for the samples after PMA at 300 °C. Leakage current came to increase and disperse with film thickness around 7nm and below.

Figure 5-4 shows optical microscopy images of Pt/La₂O₃/Ge samples after PMA at 300 °C and 600 °C. Large amount of stains were observed on Pt surface after PMA at 600 °C. This extraordinary change after PMA at 600 °C was attributed to diffusion of Ge atoms discussed in chapter 3-3. Large amount of diffused Ge atoms would react with Pt electrode so that Pt-Germanide has been formed.

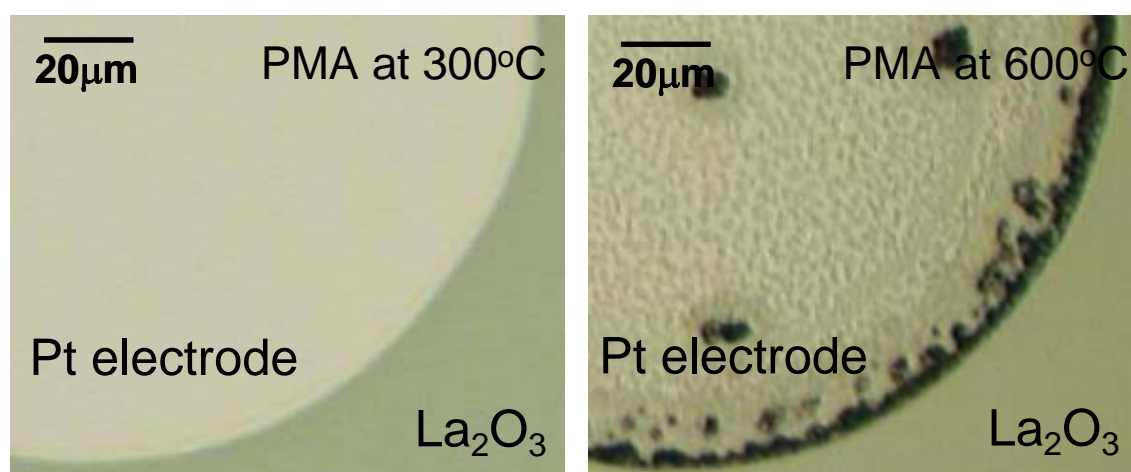


Figure 5-4. Optical microscopy images of Pt/La₂O₃/Ge samples after PMA at 300 °C and 600 °C. Large amounts of stains were observed on Pt surface for the sample with PMA at 600 °C.

Figure 5-5 shows results of angle-resolved XPS analyses for Pt(1.5nm)/La₂O₃(2.0nm)/Ge structure after PMA in N₂ at 500 °C and the La₂O₃(2.3nm)/Ge structure after PDA in N₂ at 500 °C, where those spectra were normalized by Ge 3d_{5/2} peak intensity. In case of PMA, the intensity of GeO_x (N_{GeO_x}) becomes smaller than that of Ge (N_{Ge}) while decreasing the take-off angle (TOA), which means unoxidized Ge is located on the interfacial GeO_x layer. As the La₂O₃ layer is located on the GeO_x layer from the N_{GeO_x} decreasing against the N_{La₂O₃} with decreasing the TOA, the unoxidized Ge

might exist in the La₂O₃ film. The diffused Ge atoms in the La₂O₃ film should take the form of GeO_x as excess oxygen is supplied from hydroxyl group in the La₂O₃ film. Therefore, it is reasonable that the unoxidized Ge on the GeO_x layer is Pt-germanide formed by diffused Pt and Ge atoms, which spectra have almost same binding energy with Ge 3d.

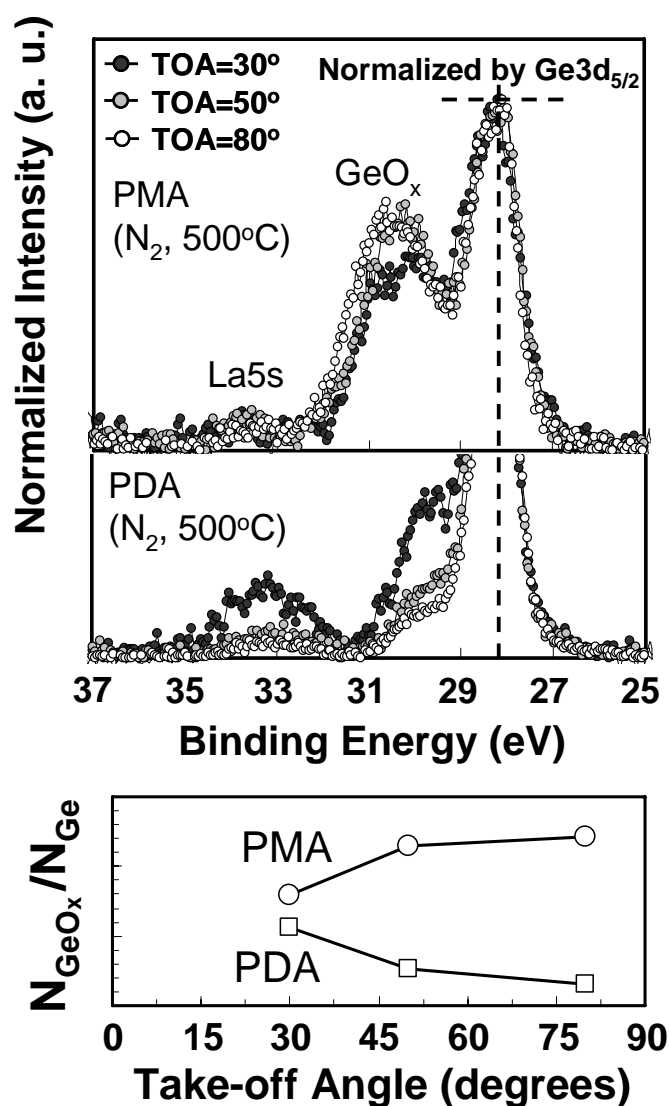


Figure 5-5. Results of angle-resolved XPS analyses for Pt(1.5nm)/La₂O₃(2.0nm)/Ge structure after PMA in N₂ at 500 °C and La₂O₃(2.3nm)/Ge structure after PDA in N₂ at 500 °C.

Figure 5-6 shows XPS Spectra of Pt 4f for Pt(0.5nm)/La₂O₃(3.5nm)/Ge structure with or without PMA. The spectra were gathered at the TOA of 90° and 15°. In case of the spectra gathered at the TOA of 15°, any difference was not observed between the samples with PMA and without PMA. However, extra peak considered to be arisen from Pt-Ge bonding appeared for the sample with PMA in case of the spectra measured at TOA of 90°. This result suggests Pt-germanide was formed in the La₂O₃ film not on the Pt surface or at the interface between the La₂O₃ film and Pt electrode, because Pt thickness of 0.5 nm is not enough to make a layer. In fact, Pt-germanide peak did not appear in Pt 4f spectra measured from Pt(1.5nm)/La₂O₃(2.0nm)/Ge structure because almost of Pt 4f spectra was arisen form the surface Pt electrode of 1.5 nm due to surface sensitivity of XPS measurement. Therefore, Pt-germanide formation is caused by not only Ge diffusion but also Pt diffusion, which schematic diagram can be seen in Fig. 5-7. Moreover, it seems very small amount of Pt-germanide was formed in the La₂O₃ film, which become a large amount of leakage spot.

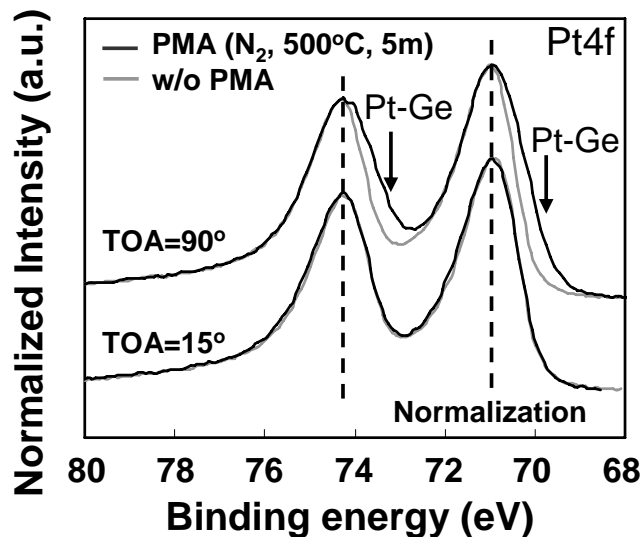


Figure 5-6. XPS Spectra of Pt 4f for Pt(0.5nm)/La₂O₃(3.5nm)/Ge structure with or without PMA. The measurement were performed at the TOA of 90° and 15°.

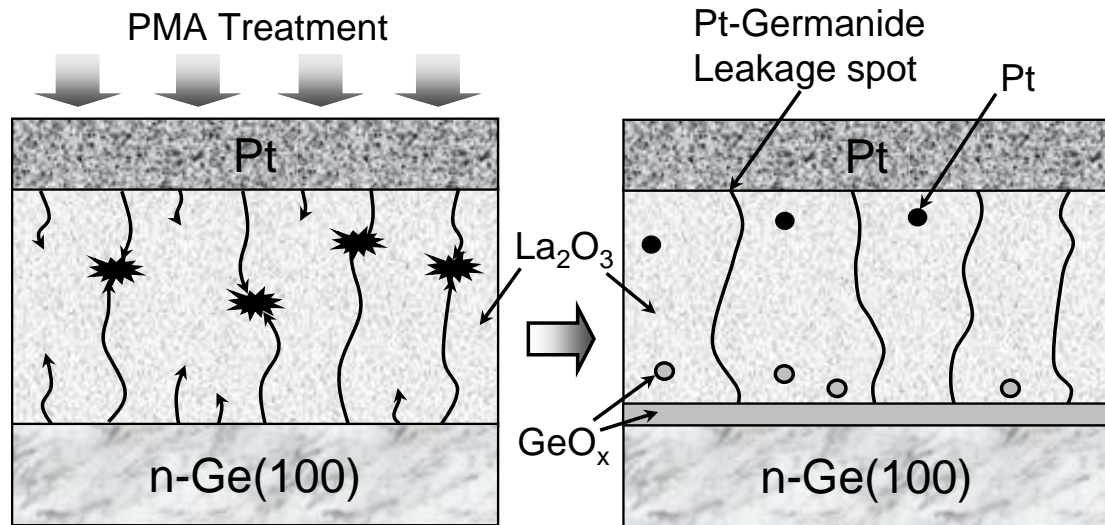


Figure 5-7. Schematic diagram about diffusion of Ge and Pt atoms and formation of Pt-germanide in the La₂O₃ film during PMA, which become a leakage spot.

5.3 Characterization of Ge MOS Structure with Various Metal Gate Electrodes

Platinum (Pt) has been often selected as a gate electrode for studies on MOS devices using high-k materials, since Pt does not take the oxygen from high-k materials. In this reason, Pt electrode was also used in chapter 3 and 4 to concentrate the reaction at the interface between La₂O₃ and Ge substrate. However, increase of leakage current density after PMA was observed in Pt/La₂O₃/Ge structure due to the Pt-germanide reaction in the La₂O₃ film as shown in previous sub-chapter. In order to suppress the increase of leakage current after PMA, restraint of Ge and gate metal diffusion or control of metal-germanide reaction should be effective. The diffusion of Ge atoms could be suppressed partially by Ge nitride or oxynitride layers; however this interfacial

layer reduced the gate capacitance. In this sub-chapter, some metal electrodes which are considered to have high reaction temperature against Ge and Pt-silicide (PtSi_x) electrode formed by thermal reaction between deposited Pt/Si on the La₂O₃ film during PMA were studied.

Figure 5-8 shows the (a) leakage current density and (b) 100kHz *C-V* characteristics in metal/La₂O₃/Ge structure using Pt, tungsten (W), tantalum (Ta) and PtSi_x gate electrode. All metals were deposited by electron-beam deposition and PtSi_x was formed by thermal reaction between deposited Pt/Si during PMA. W and Ta was selected due to the high-reaction temperature over 500 °C with Ge [5-6, 5-7] and PtSi_x was examined to the effect of prevention of Pt diffusion into La₂O₃ film by Si layer. PMA was performed in N₂ at 300 °C for 5 minutes for the samples with Pt, W, Ta electrode. For the case of sample using PtSi_x electrode, PMA was performed for 30 minutes to consume all Si reacting with Pt. The leakage current densities for the samples using alternative metals were reduced dramatically compared to those for the sample using Pt electrode as can be seen in Fig. 5-8-(a). A difference was also observed in *C-V* characteristics with various metal electrodes as shown in Fig. 5-8-(b). The largest capacitance was obtained for the sample with W electrode. *C-V* characteristic can not be measured for the sample with Pt electrode due to the large amount of leakage current density. The lower capacitance for the sample with PtSi_x electrode could be explained growth of La-silicate layer between La₂O₃ and deposited Si layer during PMA. Large *C-V* hysteresis could not be improved by changing gate metal electrode.

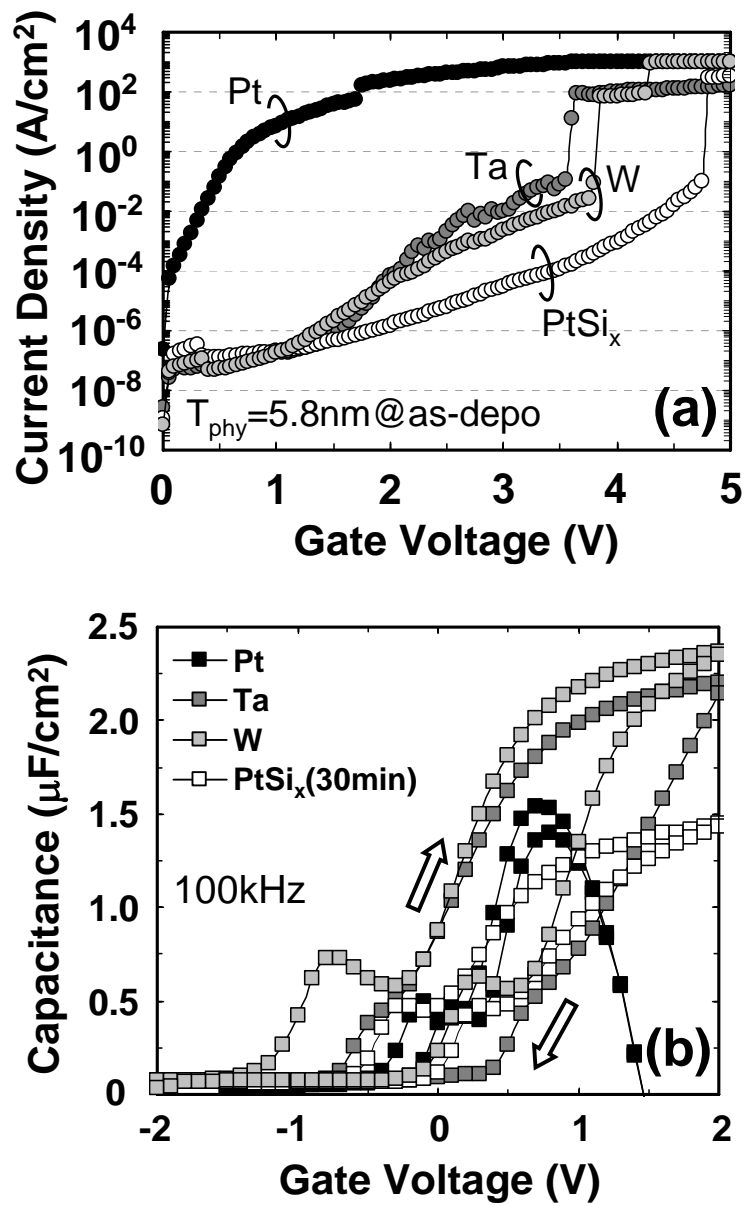


Figure 5-8. (a) leakage current density and (b) 100kHz C - V characteristics in metal/La₂O₃/Ge structure with PMA at 300 °C using Pt, W, Ta and PtSi_x as a gate electrode.

5.4 *in situ* Metallization Process for Gate Electrode Formation

First of all, suppression of moisture absorption by *in situ* metallization was confirmed by XPS spectra of O *1s*, which was shown in Fig. 5-9. Pt well known as inert metal was used as a gate electrode deposited *in situ* in order to prevent the oxidation of gate electrode. Pt/La₂O₃/Pt structure was also examined as a reference to exclude the spectra arising from chemical reaction between the Ge substrate and the La₂O₃ film. The film thicknesses of Pt capping layer and La₂O₃ layer were 6 nm and 4 nm, respectively. In order to detect the photoelectrons from the oxide layer through the metal layer, high-energy x-ray radiation source ($h\nu = 7940$ eV) was used at BL47XU of SPring-8 [5-8].

As shown in Fig. 5-9, two main spectra were detected at the binding energy around 529 eV and 531 eV in both Pt/La₂O₃/Ge and Pt/La₂O₃/Pt structure prepared by *in situ* metallization. The O *1s* spectrum at 529 eV originates from La-O-La bonding and the one at 531 eV is thought to arise from Pt-oxide since the spectrum was found to be located above the Pt film from angle-resolved analyses (not shown) and oxygen adsorption on the Pt surface has been already reported by other group [5-9]. Not only the formation of La-hydroxide but the oxidation of Ge (formation of Ge-oxide or germanate) could be well suppressed by *in situ* metallization while the spectra appeared at the binding energy of La-O-H, La-O-Ge and Ge-O-Ge bonding as a result of exposing La₂O₃ layer to the air. The Ge *3d* spectra also indicated that Ge could be oxidized by exposure La₂O₃ film to the air even without annealing as shown in chapter 3-2. This kind of oxidation was caused by the oxygen diffusion in ionic oxide even at room temperature, which was also reported for Pr₂O₃/Si structure [5-10]. Considering the sample had been exposed to the air in about an hour after La₂O₃ deposition to XPS

measurement, oxidation is considerably effective in La₂O₃/Ge structure. In other words, the hydroxyl group absorbed to the La₂O₃ film supplies the plenty of atomic oxygen in short time to enhance the oxidation of Ge. Therefore, *in situ* metallization would contribute to prevent the absorption of hydroxyl thereby suppressing the growth of interfacial layer.

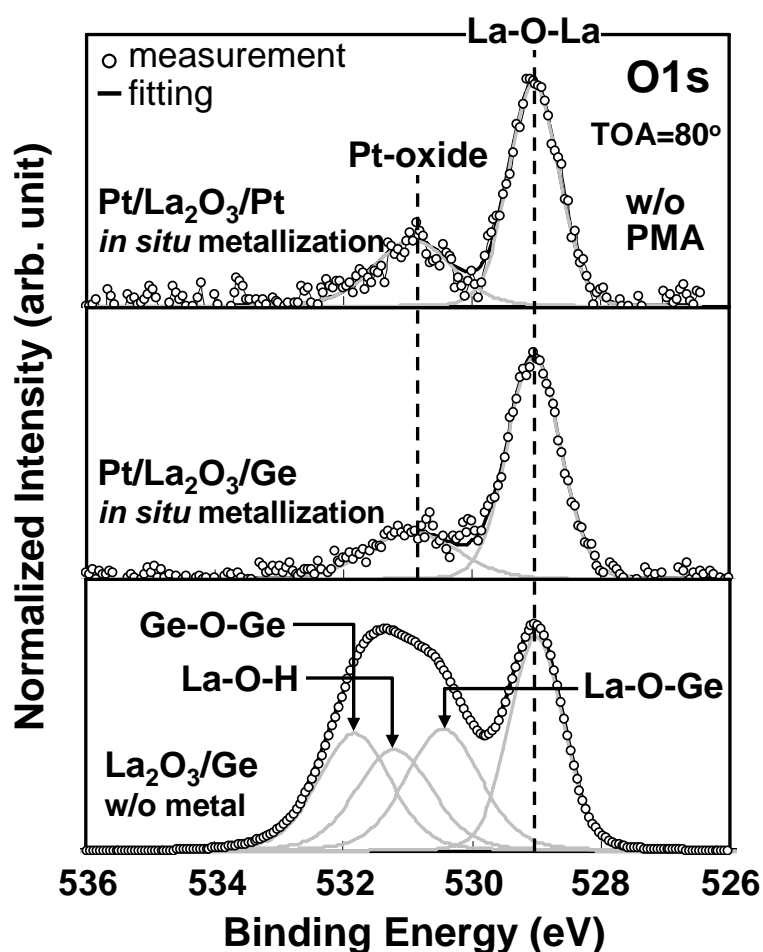


Figure 5-9. O 1s spectra arising from Pt/La₂O₃/Ge and Pt/La₂O₃/Pt structure prepared by *in situ* metallization process and La₂O₃/Ge structure prepared without metallization. All samples were not annealed.

Figure 5-10 shows Ge $2p_{3/2}$ photoelectron spectra arising from (a) Pt(6nm)/La₂O₃(4nm)/Ge and (b) W(6nm)/La₂O₃(6nm)/Ge structures prepared by *in situ* metallization process. PMA was performed in N₂ ambient at the temperature from 300 °C to 500 °C for 5 minutes. As already shown in O $1s$ spectra in Fig. 5-9, very little chemical reaction at La₂O₃/Ge interfaces was observed for both structures of Pt/La₂O₃/Ge and W/La₂O₃/Ge in as-deposited condition. The suppression of interfacial-layer growth was also observed after PMA at 300 °C; however, a large amount of interfacial reaction was observed in Pt/La₂O₃/Ge structure after PMA at 500 °C as shown in Fig. 5-10-(a). This interfacial reaction was thought to be enhanced by the adsorbed oxygen on the Pt electrode. Surface oxygen would be moved through the Pt electrode as shape of atoms or ions [5-11], finally oxidized the Ge substrate. Interfacial reaction can be controlled by changing the gate metal to tungsten (W) as shown in Fig. 5-10-(b). Although tungsten film also contains the oxygen and it was reported that interfacial reaction advances in W/La₂O₃/Si system after PMA at 500 °C [5-5], interfacial reaction decreased significantly using W electrode compared with Pt electrode in La₂O₃/Ge MOS structure. Furthermore, amounts of intensities from La-germanate spectra detected in the La $3d_{5/2}$ spectrum was far smaller than those of La-silicate spectra measured from W(6nm)/La₂O₃(6nm)/Si structure (see Fig. 5-11). This indicates the formation energy of La-germanate is higher than that of La-silicate. Moreover, considering the little formation of La-germanate, one can guess the growth interfacial layer would be Ge sub-oxide layer.

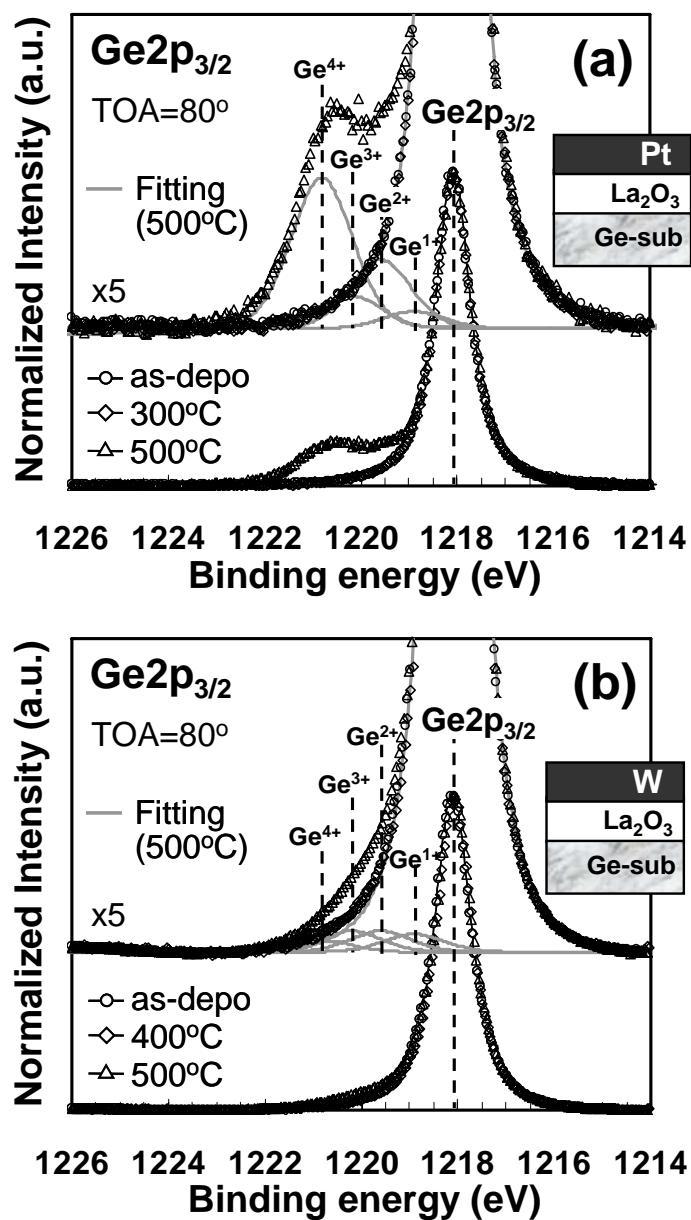


Figure 5-10. Ge $2p_{3/2}$ photoelectron spectra measured from (a) Pt(6nm)/ La_2O_3 (4nm)/Ge and (b) W(6nm)/ La_2O_3 (6nm)/Ge structure prepared by *in situ* metallization process.

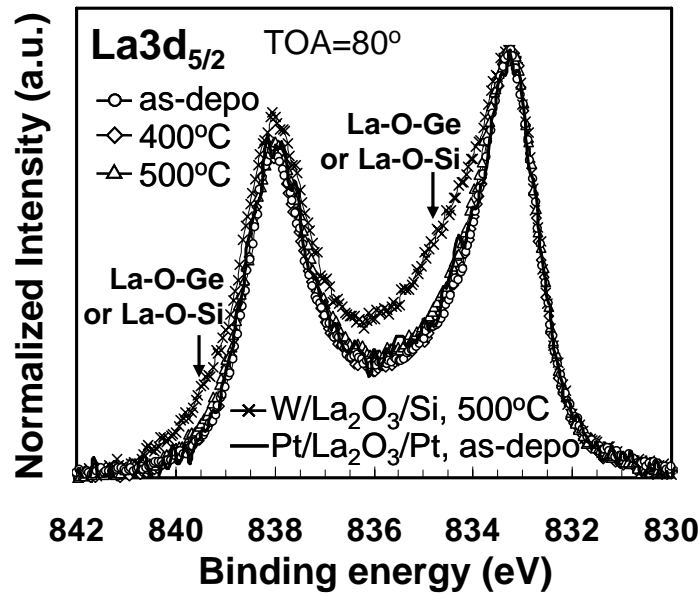


Figure 5-11. La $3d_{5/2}$ spectra measured from W(6nm)/ La_2O_3 (6nm)/Ge, W(6nm)/ La_2O_3 (6nm)/Si and Pt(6nm)/ La_2O_3 (4nm)/Pt structure prepared by *in situ* metallization process.

Figure 5-12 shows C - V characteristics of W/ La_2O_3 /Ge structure prepared by *in situ* metallization process. Tungsten was selected as gate electrode of MOS capacitors because of thermal stability for the leakage current density. The patterns of MOS capacitors were defined by lithography and SF_6 chemistry based reactive ion etching (RIE). Very small EOT of 0.55 nm with leakage current density of $2.7 \times 10^{-1} \text{ A/cm}^2$ at gate voltage of 1 V was achieved from the as-deposited film although very large D_{it} of $9 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ and frequency dispersion was observed. The small EOT for the sample without PMA tremendously increased and D_{it} reduced to $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ by 500 °C PMA corresponding to increase of interfacial reaction as shown in Fig. 5-10. C - V hysteresis was observed like the results for the samples with PDA in oxygen ambient.

Further improvement of D_{it} and $C-V$ hysteresis could not be achieved by PMA in 3%-H₂+N₂ (FG) (not shown) in contrast to W/La₂O₃/Si structure prepared by *in situ* metallization after FG annealing [5-12]. Figure 5-13 shows dependence of D_{it} and $C-V$ hysteresis on EOT for W/La₂O₃/Ge structure with various thickness of La₂O₃ after PMA at 500 °C. D_{it} and $C-V$ hysteresis became worse slightly with decreasing of EOT as can be seen in Fig. 5-13. Degradation of D_{it} is considered to be due to the influence of diffused W atoms because more W atoms could reach to interface by decreasing the thickness of the La₂O₃ layer; similar results was reported on W/La₂O₃/Si system [5-13]. $C-V$ hysteresis increment would be attributed to increase of gate electric field because gate voltage range was kept on same range despite decrease of EOT.

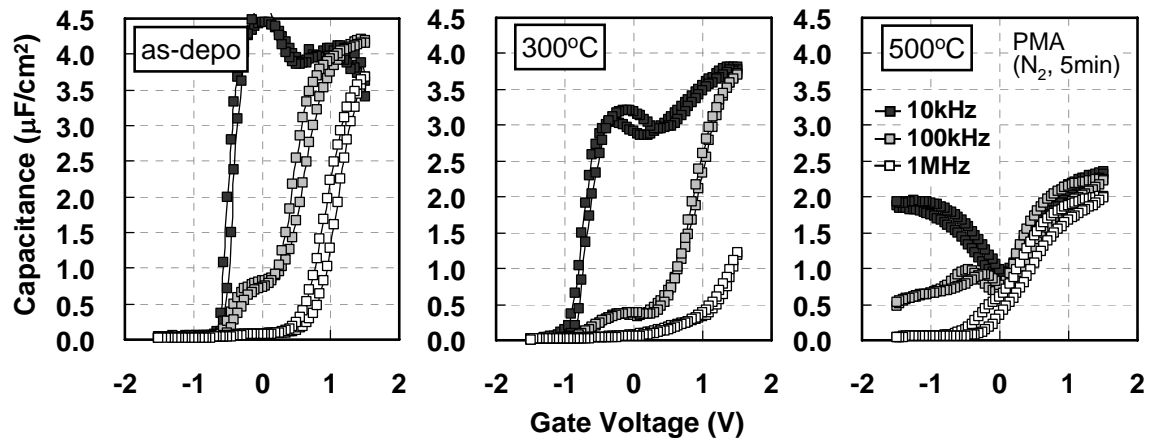


Figure 5-12. $C-V$ characteristics of W/La₂O₃/Ge structure prepared by *in situ* metallization process. Tungsten electrode was used for MOS capacitors because of thermal stability and easy formation of capacitors pattern by lithography and dry etching. PMA was conducted in N₂ ambient for 5 minutes.

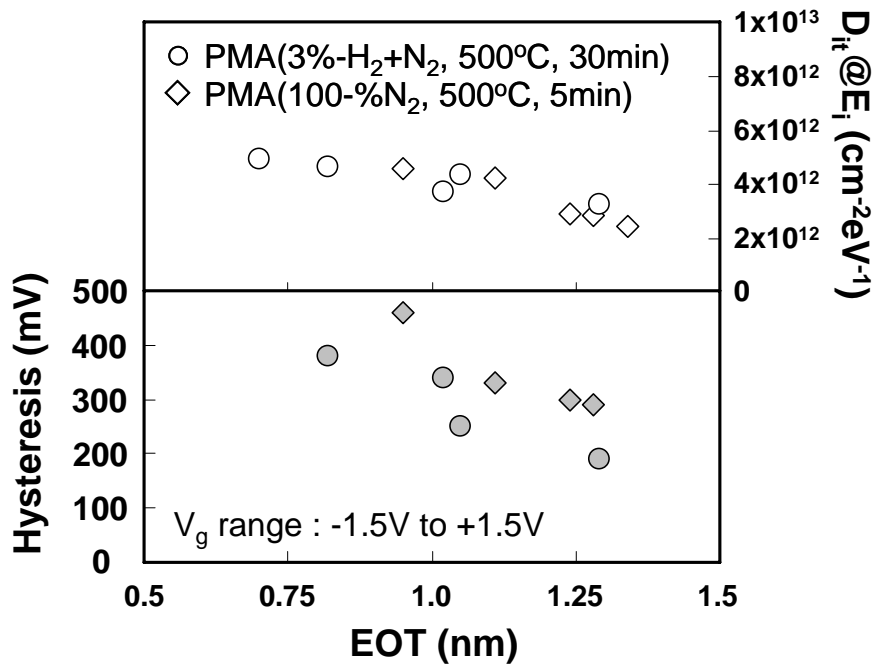


Figure 5-13. Dependence of D_{it} and $C-V$ hysteresis on EOT for W/La₂O₃/Ge structure with various thickness of La₂O₃ after PMA at 500 °C.

Figure 5-14 shows leakage current density ($J_g@1$ Volt) as a function of EOT for the samples prepared by *in situ* metallization process. J_g -EOT characteristics for Ge-MOS structure using other high-k material is also plotted as references [5-14 ~ 5-19]. Impressive J_g -EOT characteristics can be achieved with little interfacial layer, e.g. in as-deposited condition and after PMA at 300 °C. Although larger leakage current density for same EOT was observed for the samples after PMA at 500 °C than those without PMA, satisfactory results were obtained compared to those with other high-k materials.

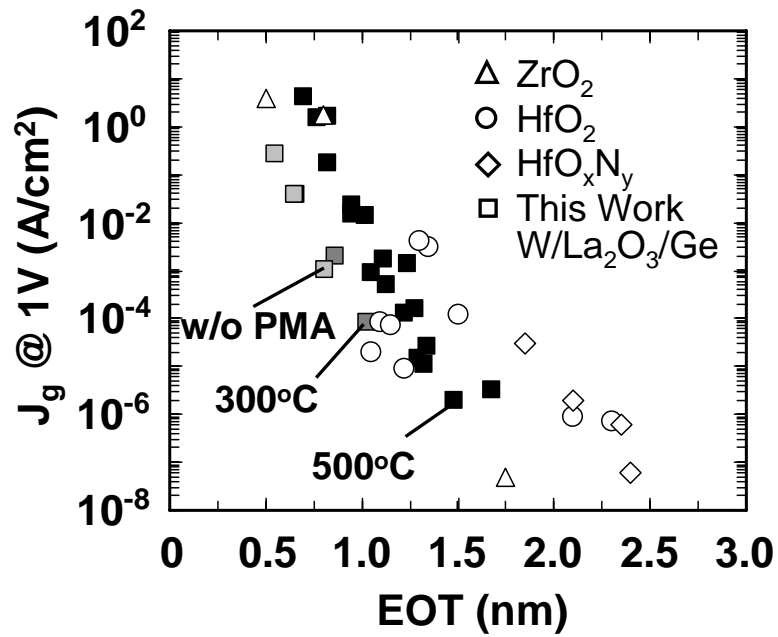


Figure 5-14. Leakage current density (J_g @1Volt) as a function of EOT for the samples prepared by *in situ* metallization process. J_g -EOT characteristics for Ge-MOS structure using other high-k material is also plotted as references.

5.5 Introduction of Atomic-hydrogen with Al-capping Layer on Tungsten Electrode

In W/La₂O₃/Ge structure, improvement of D_{it} or $C-V$ hysteresis could not be observed by PMA in 3%-H₂+N₂ ambient as mentioned in previous sub-chapter. In order to examine the impact of hydrogen annealing effectively, atomic hydrogen was introduced by an Aluminum (Al) capping layer on W gate electrode. It is well known that Al generates the atomic hydrogen by decomposing the water on W [5-20]. The effect of atomic hydrogen with the Al-capping layer on W/La₂O₃/Si system was already demonstrated with achieving low D_{it} of $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ [5-12]. Figure 5-15 shows $C-V$ characteristics for W/La₂O₃/Ge structure with or without the Al-capping layer. W/La₂O₃/Ge structure was prepared by *in situ* metallization process. PMA was performed in 3%-H₂+N₂ (FG) ambient at 400 °C for 30 minutes. In contrast the W/La₂O₃/Si structure, no improvement in D_{it} and hysteresis was observed for W/La₂O₃/Ge structure with Al-capping layer. Figure 5-16 shows dependence of D_{it} on PMA temperature for W/La₂O₃/Ge structure with of without Al-capping layer on W electrode. The effect of atomic hydrogen was not observed in any temperature of PMA. Ineffectiveness of hydrogen termination on Ge surface is thought to be due to the low temperature (250 - 300 °C) of hydrogen desorption from Ge and instability of dihydride on Ge surface [5-21].

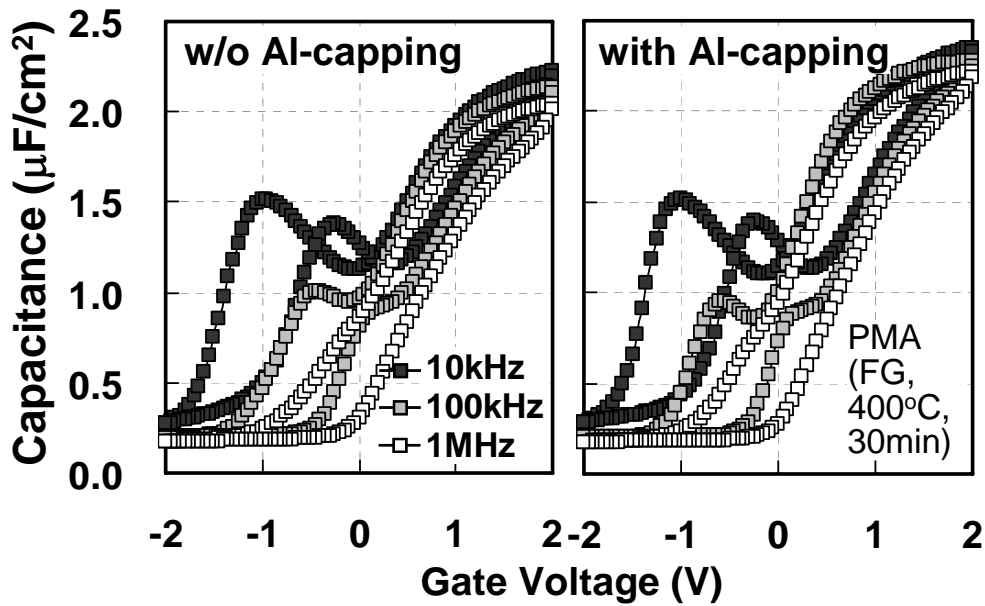


Figure 5-15. C - V characteristics for $\text{W}/\text{La}_2\text{O}_3/\text{Ge}$ structure with or without the Al-capping layer. $\text{W}/\text{La}_2\text{O}_3/\text{Ge}$ structure was prepared by *in situ* metallization process.

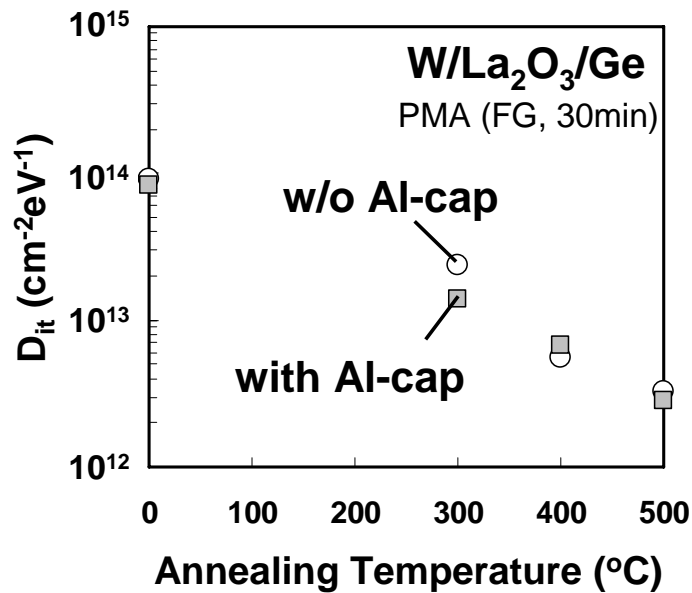


Figure 5-16. Dependence of D_{it} on PMA temperature for $\text{W}/\text{La}_2\text{O}_3/\text{Ge}$ structure with or without Al-capping layer on W electrode.

5.6 Conclusion

In this chapter, thermodynamic stability of metal/La₂O₃/Ge structure with various metal-gate electrodes after PMA at 300-500 °C and *in situ* metallization process for gate electrode has been studied. In case of using Pt electrode, leakage current density increases after PMA, which is attributed to Pt-germanide reaction by diffused Ge and Pt in the La₂O₃ film. This kind of leakage current increment can be suppressed by controlling the reaction between gate electrode and Ge, e.g. using metal electrodes which react with Ge at high temperature such as W or Ta.

On the other hand, suppression of moisture absorption in the La₂O₃ film has been confirmed with *in situ* gate metallization. Very small EOT of 0.55 nm with leakage current density of 2.7×10^{-1} A/cm² has been observed for the sample prepared by *in situ* gate metallization using W gate electrode without annealing although it shows very large D_{it} . As it seems very hard to obtain improvement of interface property in La₂O₃/Ge structure by hydrogen annealing even in case using atomic hydrogen, interfacial layer should be needed for reduction of D_{it} . Therefore, it can be said that there is trade-off relation between achievement of small EOT with lower leakage current density and improvement of interfacial property in La₂O₃/Ge MOS structure.

References

- [5-1] T. Nishimura, M. Toyama, K. Kita, K. Kyuno, and A. Toriumi, "Ion-Implanted p/n Junction Characteristics p- and n-type Germanium," Ext. Abstr. of 2005 International Conference on Solid State Devices and Materials (SSDM), pp.520 (2005).
- [5-2] T. Nishimura, S. Sakata, K. Nagashio, K. Kita, and A. Toriumi, "Low Temperature Phosphorus Activation in Germanium through Nickel Germanidation for Shallow n⁺/p Junction," Appl. Phys. Express vol. 2, pp. 021202 (2009).
- [5-3] T. Gougousi, M. J. Kelly, D. B. Terry, and G. N. Parsons, "Properties of La-silicate high-K dielectric films formed by oxidation of La on silicon," J. Appl. Phys., vol. 95, pp. 1691 (2004).
- [5-4] Y. Zhao, M. Toyama, K. Kita, K. Kyuno, and A. Toriumi "Moisture Absorption-Induced Permittivity Deterioration and Surface Roughness Enhancement of Lanthanum Oxide Films on Silicon," Ext. Abstr. 2005 SSDM, pp. 546 (2005).
- [5-5] K. Tachi, K. Kakushima, P. Ahemt, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "Effect of Oxygen for Ultra-Thin La₂O₃ Film Deposition," ECS Trans., vol. 3, pp. 425 (2006).
- [5-6] O.Yu. Khyzhun, Ya.V. Zaulychny, and EA. Zhurakovsky, "Electronic structure of tungsten and molybdenum germanides synthesized at high pressures," J. Alloys and Compounds, vol. 244, pp. 107 (1996).
- [5-7] M. W. Ruckman, M. Giudice, and J. H. Weaver, "Temperature-dependent growth morphology of a semiconductor-metal interface: Ge/Ta(110)," Phys. Rev. B, vol. 32, pp. 1077 (1985).
- [5-8] K. Kobayashi, M. Yabashi, Y. Takata, T. Tokushima, S. Shin, K. Tamasaku, D. Miwa, T. Ishikawa, H. Nohira, T. Hattori, Y. Sugita, O. Nakatsuka, A. Sakai, S. Zaima, Appl. Phys. Lett. **83**, 1005 (2003).
- [5-9] P.R. Norton, "An investigation of the adsorption of oxygen and oxygen containing

species on platinum by photoelectron spectroscopy,” *Surface Science*, vol. 47, pp. 98 (1975).

[5-10] H. J. Osten, E. Bugiel, and A. Fissel, “Epitaxial praseodymium oxide: a new high-*K* dielectric,” *Solid-State Elec.* vol. 47, pp. 2161 (2003).

[5-11] T. Kubota, Y. Nakato, K. Yoneda, H. Kobayashi, “Platinum-enhanced oxidation of GaAs,” *Phys. Rev. B*, vol. 56, pp. 7428 (1997).

[5-12] K. Tachi, K. Kakushima, P. Ahemt, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, “Improvement of Interface Properties of W/La₂O₃/Si MOS Structure Using Al Capping Layer,” *ECS Trans.*, vol. 11, pp. 191 (2007).

[5-13] K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Analysis of electron mobility in nMOSFETs with W/La₂O₃ gate stack down to sub-1.0 nm EOT,” 55th Japan Society of Applied Physics (JSAP) Spring Meeting, 28p-H-19, Nihon University, Japan, March, 2008.

[5-14] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, “A sub-400°C germanium MOSFET technology with high-*k* dielectric and metal gate,” *IEEE IEDM 2002 Tech. Dig.*, pp. 437 (2002).

[5-15] K. C. Saraswat, C. O. Chui, T. Krishnamohan, A. Nayfeh, and P. C. McIntyre, “Ge based high performance nanoscale MOSFETs,” *Microelectronic Engineering*, vol. 80, pp. 15 (2005).

[5-16] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, “Ge MOS Characteristics with CVD HfO₂ Gate Dielectrics and TaN Gate Electrode,” *VLSI Symp. 2003 Tech. Dig.*, pp. 121 (2003).

[5-17] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, and B. J. Cho., “Effect of surface NH₃ anneal on the physical and electrical properties of HfO₂ films on Ge substrate,” *App. Phys. Lett.*, vol. 84, pp. 3741 (2004).

[5-18] Q. C. Zhang, N. Wu, C. X. Zhu, “The Electrical and Material Properties of HfO_xN_y Dielectric on Germanium Substrate,” *Jpn. J. Appl. Phys.*, vol. 43, pp. L1208

(2004).

[5-19] C. -C. Cheng, C. -H. Chien, C. -W. Chen, S. -L Hsu, M. -Y. Yang, C. -C. Huang, F. -L. Yang, and C. -Y. Chang, "Impact of post-deposition-annealing on the electrical characteristics of HfO_xN_y gate dielectric on Ge substrate," *Microelectronic Engineering*, vol. 80, pp. 30 (2005).

[5-20] H. Shang, M. H. White, K. W. Guarini, P. Solomon, E. Cartier, F. R. McFeely, J. J. Yurkas, and W-C Lee, "Interface studies of tungsten gate metal–oxide–silicon capacitors," *Appl. Phys. Lett.*, vol. 78, pp. 3139 (2001).

[5-21] L. B. Lewis, J. Segall, and K. C. Janda, "Recombinative desorption of hydrogen from the Ge(100)–(2×1) surface: A laser-induced desorption study," *J. Chem. Phys.*, vol. 102, pp. 7222 (1995).

Chapter 6.

Introduction of Ultrathin Si Passivation Layer on Ge Surface

- 6.1 Introduction
- 6.2 Reduction of $C-V$ Hysteresis with Ultrathin Si Passivation Layer
- 6.3 Dependence of Interface Trap Density on the Condition of Si-layer
- 6.4 Dependence on Si-layer Thickness
- 6.5 Conclusion

6.1 Introduction

Considering the results studied in chapter 3 to 5, it seems difficult to achieve satisfactory interfacial properties by forming La₂O₃ directly on Ge substrate, and better characteristics have been obtained with growth of the interfacial Ge oxide and/or La-germanate layer. In case of interfacial-layer growth, however, large amount of hysteresis in $C-V$ characteristic was observed due to simultaneously grown Ge sub-oxide. In this chapter, the effect of ultrathin Si passivation layer on the surface of Ge substrate in order to suppress the growth of Ge sub-oxide by blocking oxygen from the La₂O₃ film to the Ge substrate and control Ge diffusion into the La₂O₃ film. The Si-layer simply deposited by electron-beam evaporation method before the La₂O₃ deposition without air exposure (*in situ* process).

6.2 Reduction of $C-V$ Hysteresis with Ultrathin Si Passivation Layer

Figure 6-1 shows the $C-V$ characteristics of the W/La₂O₃/Ge MOS capacitors with or without a Si-passivation layer on a Ge substrate. The samples were annealed in N₂ at 500 °C for 5 minutes. The initial thickness of the Si-passivation layer before PMA is about 1.5 nm as indicated in Fig. 6-2. As shown in Fig. 6-1, the $C-V$ hysteresis dramatically decreased by inserting 1.5-nm-thick Si passivation layer. The reduction of $C-V$ hysteresis is mainly due to the suppression of Ge sub-oxide (GeO_x) growth and La-silicate formation during the PMA, as will be described later. On the other hand, interface-trap density (D_{it}) was still higher than 10^{13} cm⁻²eV⁻¹ as opposed to other reports using Si passivation layer on Ge substrate [6-1, 6-2]. Specific study about D_{it} will be discussed next sub-chapter.

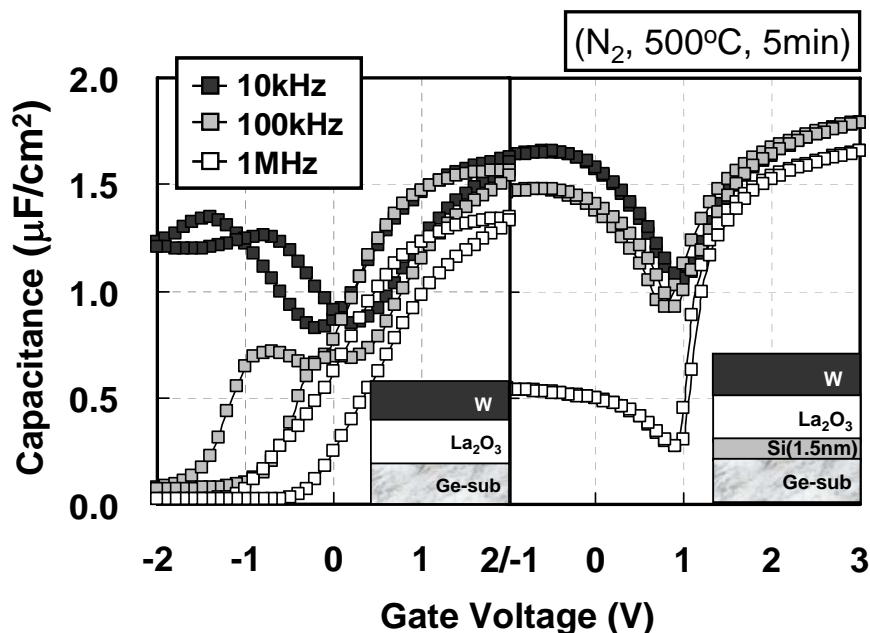


Figure 6-1. $C-V$ characteristics of W/La₂O₃/Ge MOS capacitors with or without Si passivation layer on Ge substrate.

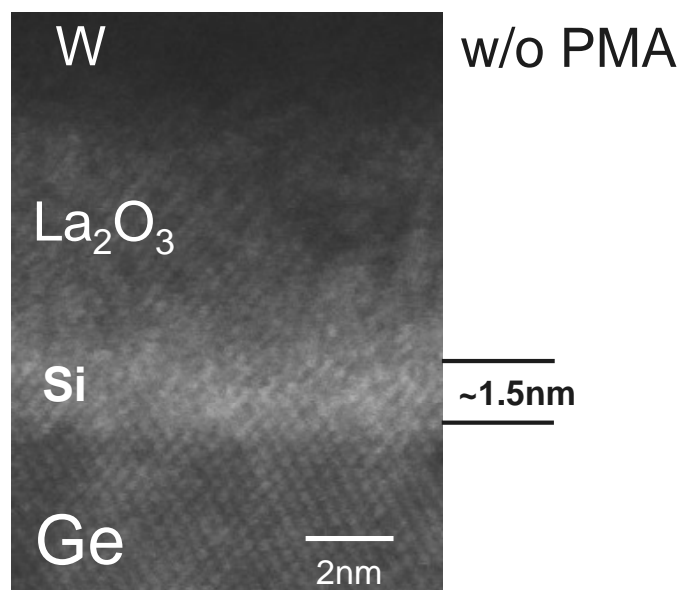


Figure 6-2. Cross-sectional TEM image of the capacitor with 1.5-nm-thick Si passivation layer obtained for as-deposited condition.

Figure 6-3 shows dependence of (a) $C-V$ hysteresis and (b) EOT on PMA temperature for W/La₂O₃/Ge structures with or without a Si layer. The results for W/La₂O₃/Si structure are also shown as references. The sample with a Si layer on a Ge substrate exhibited almost same characteristics as those of reference sample using a Si substrate. $C-V$ hysteresis reduction and EOT increment by 500 °C PMA in W/La₂O₃/Si structures are considered to be due to the formation of an interfacial La-silicate layer [6-3]. It seems to need not only suppression of GeO_x but also the formation of La-silicate for reduction of oxide trapped charge ($C-V$ hysteresis).

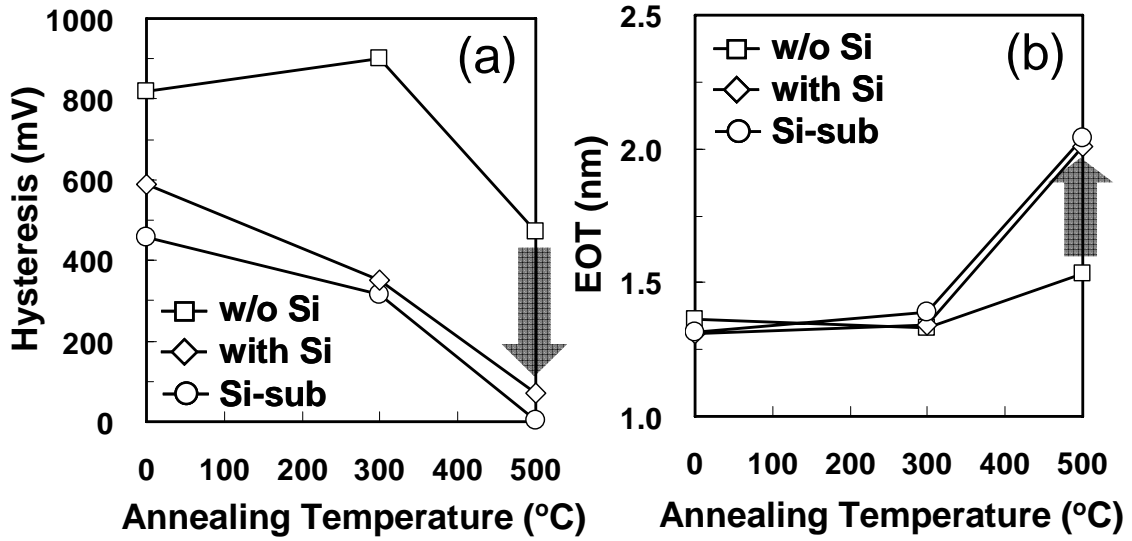


Figure 6-3. Dependence of (a) C - V hysteresis and (b) EOT on PMA temperature for $W/La_2O_3/Ge$ structures with or without a Si layer. The results for $W/La_2O_3/Si$ structures are also shown as references.

In order to examine the effect of Si passivation layer for suppressing the growth of GeO_x based on the result of C - V hysteresis reduction as shown in Fig. 6-1, the chemical bonding configuration of Ge was analyzed by XPS using high-energy x-ray radiation source ($h\nu = 7940$ eV) at BL47XU of SPring-8. Figure 6-4 shows Ge $2p$ spectra measured from the samples with Si layer of 1 nm and without Si layer. In order to detect Ge $2p$ spectra, the thickness of gate electrode and La_2O_3 was controlled to 6nm and 7nm, respectively. With Si layer of 1 nm, diffusion of Ge and growth of GeO_x seems to be completely suppressed after PMA up to 500 °C.

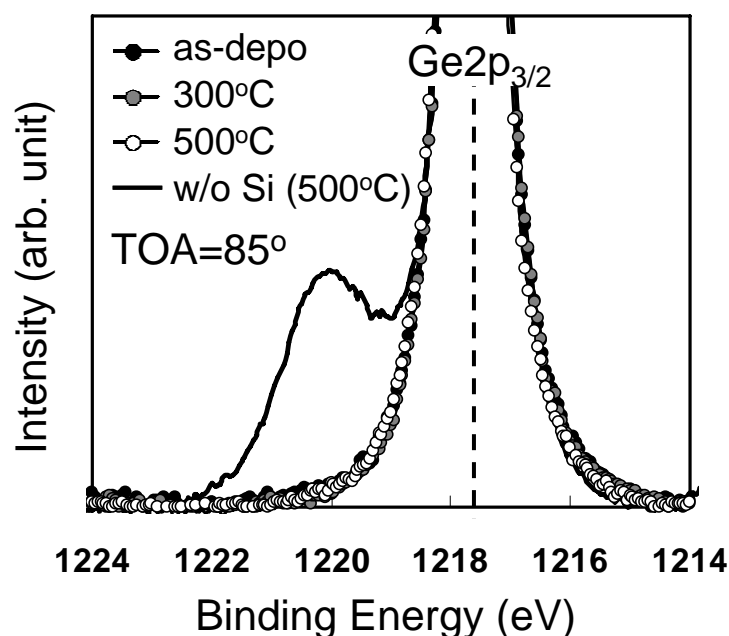


Figure 6-4. Ge 2p XPS spectra measured from the samples with Si layer of 1 nm and without Si layer.

Figure 6-5 shows dependence of Si 1s spectra on PMA temperature measured from W/La₂O₃/Ge structure with Si layer of 1 nm. Si 1s spectra gathered from W/La₂O₃/Si structure are also showed as a reference. The intensities of spectra from the samples with Si layer and those on Si substrate were normalized by the intensity of Ge 2p_{3/2} and that of Si 1s, respectively. The intensity of Si layer decreased and that of interfacial La-silicate layer increased with rising the PMA temperature, which supported the dependence of EOT on PMA temperature. Furthermore, the reactions between La₂O₃ and Si layer for the samples with Si-passivation layer on Ge substrate showed almost same characteristics with those on Si substrate. These suggest that interfacial properties between La₂O₃ and Si- passivation layer correspond to the results on Si substrate.

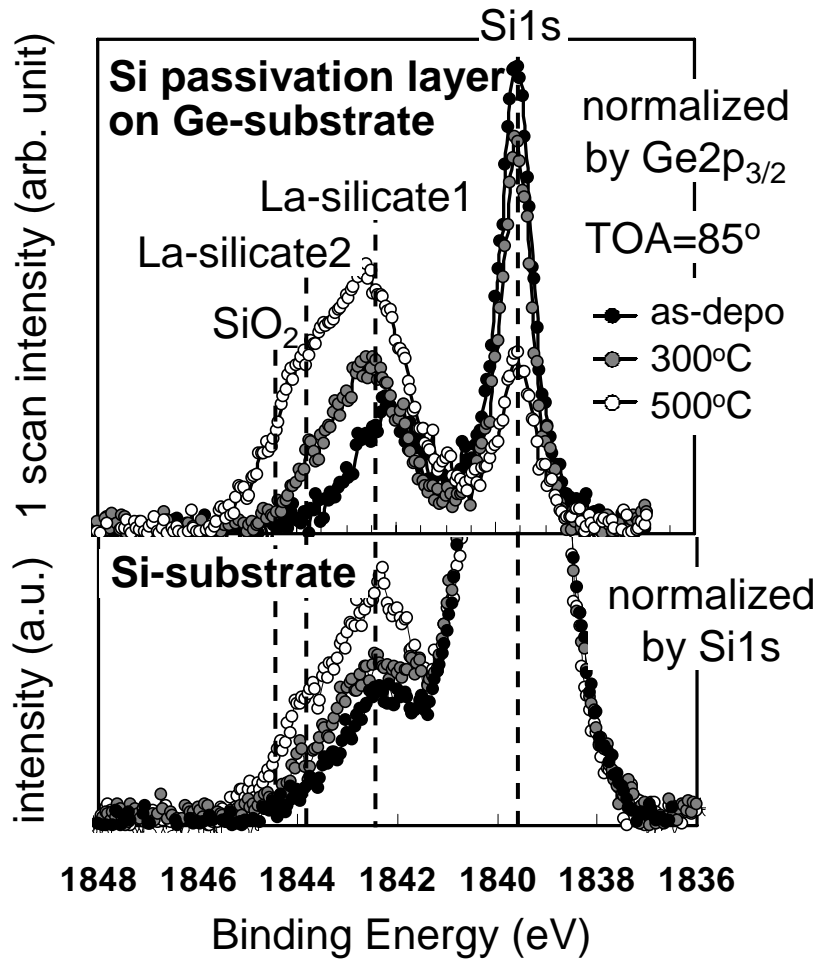


Figure 6-5. Dependence of Si $1s$ spectra on PMA temperature measured from $\text{W}/\text{La}_2\text{O}_3/\text{Ge}$ structure with Si layer of 1 nm and $\text{W}/\text{La}_2\text{O}_3/\text{Si}$ structure.

Figure 6-6 shows Ge $2p$ spectra arising from the samples with three different thicknesses of Si passivation layer and without Si layer. PMA was conducted at 500 °C in N_2 ambient for 5 minutes. Any growth of GeO_x was not observed with the thickness of Si layer more than 1.0 nm, whereas GeO_x seemed to grow in the case of Si layer under 0.5-nm thick. In case of 0.5-nm-thick Si layer, deposited Si layer react with La_2O_3 completely so that no Si bonding is observed as shown in Fig. 6-7. The GeO_x growth

resulted in a large amount of C - V hysteresis with no regard to introduction of Si layer, which can be seen in Fig. 6-8. In fact, a slight growth of GeO_x and the corresponding C - V hysteresis observed for the sample with 0.5-nm-thick Si layer might be attributed to island growth of the Si layer, which allows the Ge substrate to contact with La_2O_3 film directly, resulting in the diffusion of Ge and formation of GeO_x . In any case, the growth of GeO_x can cause the hysteresis on C - V curve regardless of the Si insertion and formation of La-silicate. These results suggest that the suppression of GeO_x growth is essential to reduce oxide trap density which appears as C - V hysteresis in the Ge MOS structures.

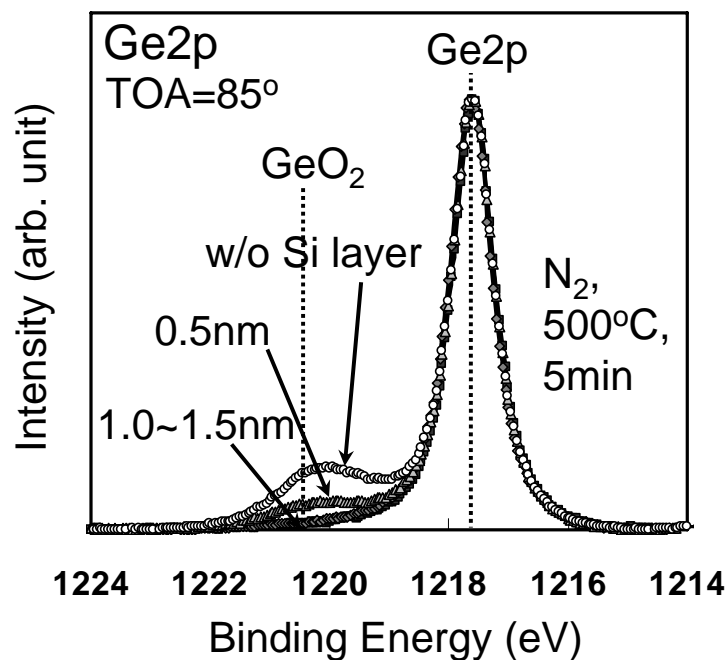


Figure 6-6. Ge 2p spectra arising from the samples with three different thicknesses of Si passivation layer and without Si layer.

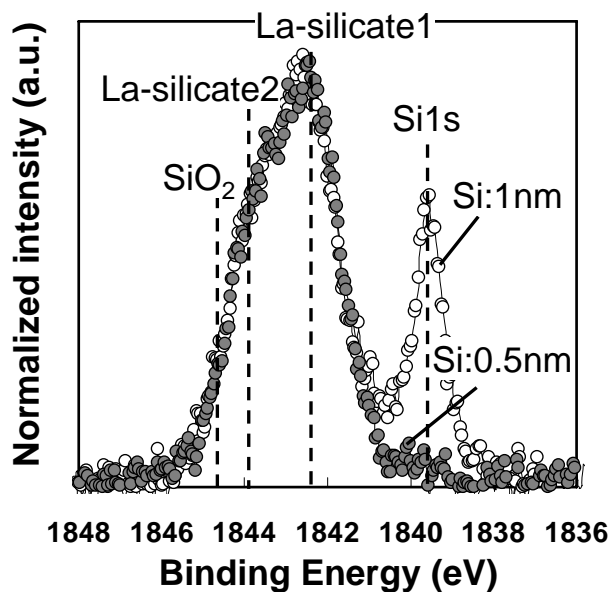


Figure 6-7. Si *1s* spectra measured from the samples with 1.0 nm or 0.5 nm Si passivation layer. All Si was consumed to form the La-silicate in case of 0.5-nm Si layer.

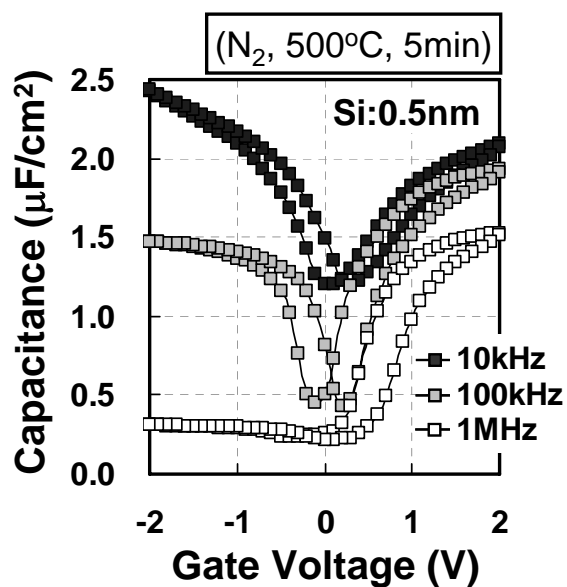


Figure 6-8. *C-V* characteristics of W/ La_2O_3 /Si/Ge MOS capacitors with 0.5-nm-thick Si passivation layer. Large amount of *C-V* hysteresis was observed with no regard to introduction of Si layer.

6.3 Dependence of Interface Trap Density on the Condition of Si-layer

Although significant improvement can be achieved in terms of oxide trap density by Si passivation layer as shown in previous chapter, advancement of D_{it} can not be observed in this method. This high D_{it} value could not be reduced even after annealing with atomic hydrogen generated by Al-capping layer on W electrode as shown in Fig. 6-9. Considering the achievement of low D_{it} about 10^{11} cm⁻²eV⁻¹ in the interface between La₂O₃ and Si after annealing with atomic hydrogen [6-4], the high D_{it} values observed in W/La₂O₃/Si/Ge structure seems to originate in the interface between the Si passivation layer and the Ge substrate.

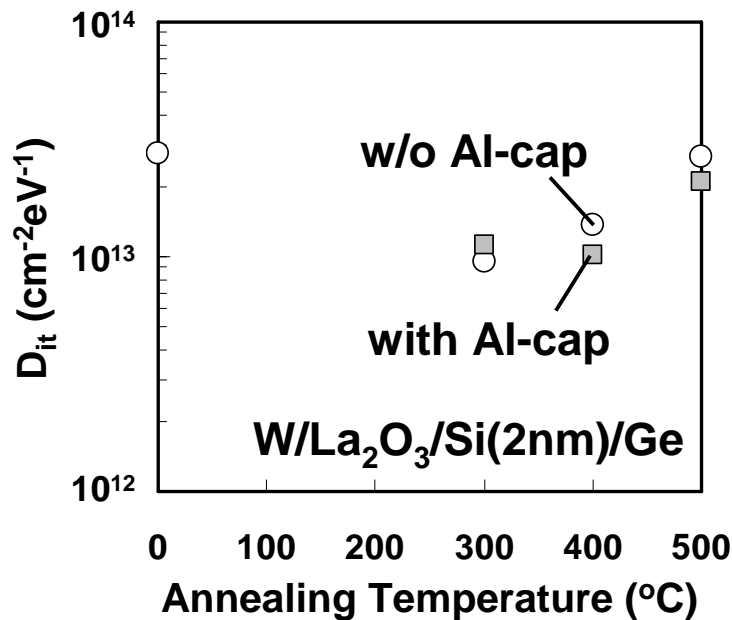


Figure 6-9. Interface trap density for the W/La₂O₃/Si(2nm)/Ge structure with or without Al-capping layer on W electrode. Improvement of D_{it} can not be achieved with Al-capping layer.

In the previous sub-chapter, all Si layer was deposited at the substrate temperature of 250 °C, which was same with that of La₂O₃ deposition. Deposited Si layer was all crystallized and epitaxial growth was partially observed according to the TEM image as shown in Fig. 6-2. The perfect epitaxial growth of Si layer on Ge substrate is tough by using simple electron-beam evaporation method due to the 4% lattice mismatch between Si and Ge, of which the mismatch is considered to generate the defects in the interface and increase the D_{it} . Therefore, some other deposition conditions on Si passivation layer were examined for reduction of the interface trap density.

Figure 6-10 shows reflection high energy electron diffraction (RHEED) pattern of samples (a) without Si layer (only Ge substrate) after ultra-high vacuum (UHV) annealing at 500 °C (measured at room temperature), (b) after deposition of 2-nm-thick Si layer at room temperature (RT), (c)-(f) with 2-nm-thick Si layer deposited at RT and UHV annealing at 200-500 °C, respectively. The RHEED pattern of Ge substrate shown in Fig. 6-10-(a) completely disappeared after deposition of 2-nm-thick Si layer at RT (Fig.6-10-(b)), which means the Si layer was amorphous phase. After the Si deposition, UHV annealing was performed *in situ* and solid phase epitaxy (SPE) growth of Si layer was observed for the sample after UHV annealing at 200 °C (Fig.6-10-(c)), which was maintained up to 400 °C (Fig.6-10-(d),(e)). The SPE-grown Si layer finally showed island growth continuous UHV annealing at 500 °C (Fig.6-10-(f)).

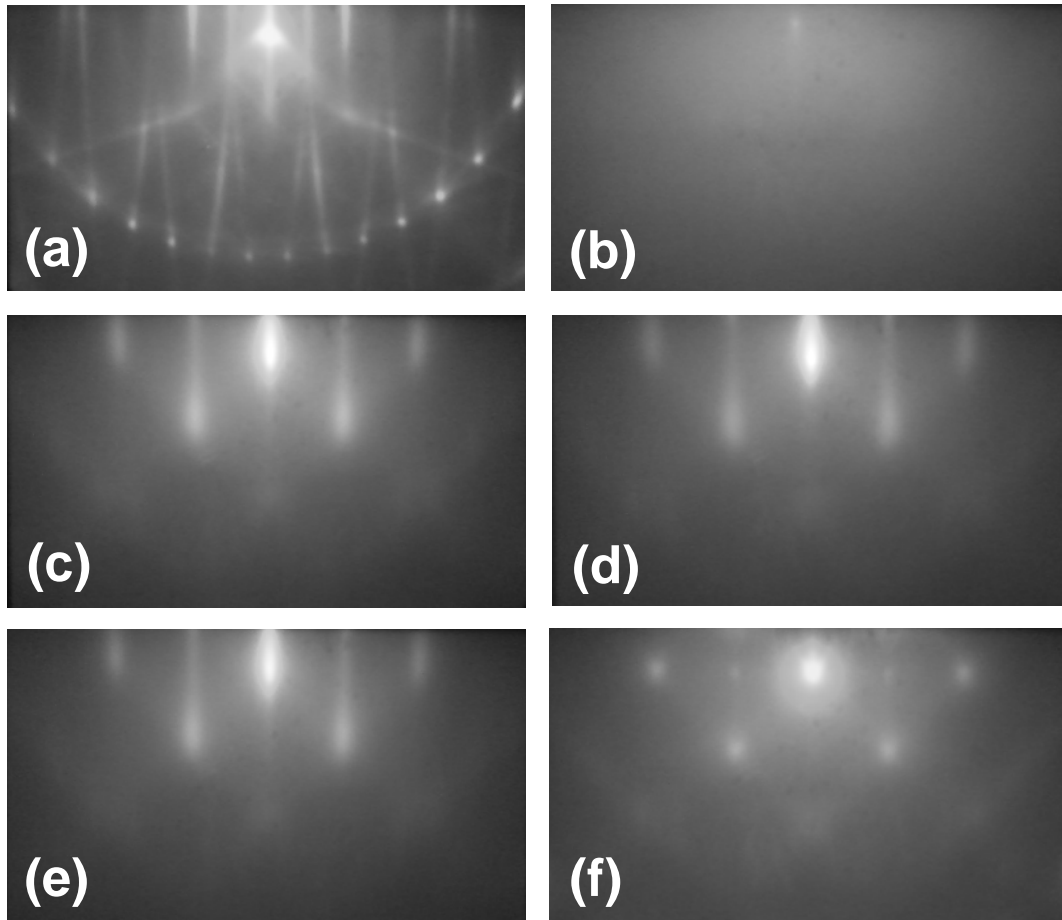


Figure 6-10. RHEED image of samples (a) without Si layer (only Ge substrate) after UHV annealing at 500 °C (measured at room temperature), (b) after deposition of 2-nm-thick Si layer at room temperature (RT), (c)-(f) with 2-nm-thick Si layer deposited at RT and UHV annealing at 200-500 °C, respectively.

Figure 6-11 shows $C-V$ characteristics of Al/W/La₂O₃/Si/n-Ge structures with (a) amorphous Si layer, (b) SPE-grown Si layer and (c) island-grown Si layer. The thickness of deposited Si layer was 2.0 nm, which was monitored by thickness sensor using quartz crystal. In case of the amorphous Si layer, La₂O₃ film was deposited at room temperature in order to keep on amorphous phase of the Si layer. The SPE-grown Si layer and the island-grown Si layer were formed by *in situ* UHV annealing at 300 °C

and 500 °C, respectively, and La₂O₃ film was deposited at the substrate temperature of 300 °C in both cases. Al-capping layer was deposited on W electrode for introduction of atomic hydrogen. PMA was carried out in 3%-H₂+N₂ (FG) ambient at 300 °C for 30 minutes. As shown in Fig. 6-11, lowest capacitance value around flat band voltage (V_{fb}) on low frequency (1kHz) $C-V$ curve for the sample with amorphous Si layer is smaller than that for the sample with SPE-grown Si layer., which indicates lower D_{it} in the sample with the amorphous Si layer. Actually, examined D_{it} by conductance method for the samples with the amorphous Si layer and the SPE-grown Si layer was $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ and $1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, respectively. It is considered that the defects originated by lattice mismatch between Si and Ge during crystallization of Si layer were not generated in case of amorphous Si layer. In case of island-grown Si layer, accumulation region of $C-V$ characteristics can not be measured rightly due to the large leakage current density.

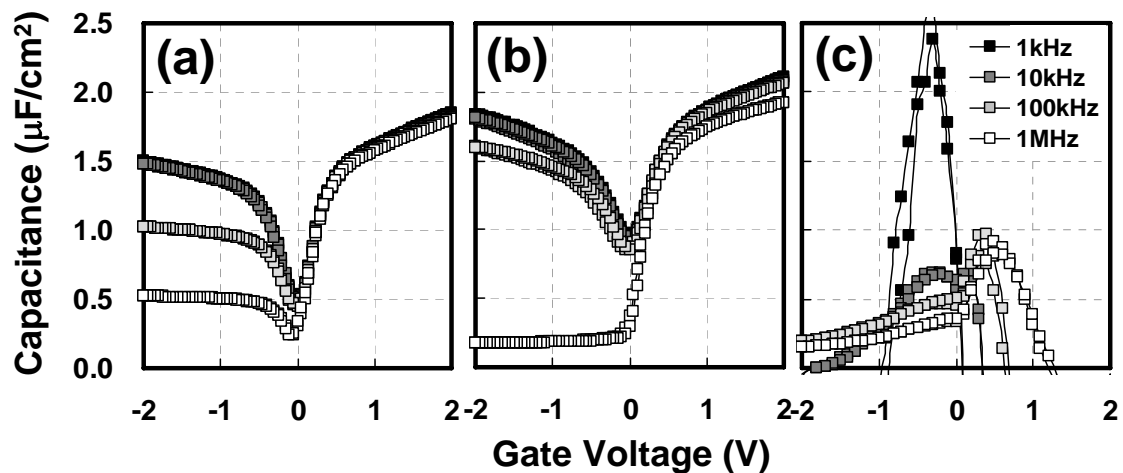


Figure 6-11. $C-V$ characteristics of Al/W/La₂O₃/Si/n-Ge structure with (a) amorphous Si layer, (b) SPE-grown Si layer and (c) island-grown Si layer. PMA was carried out in 3%-H₂+N₂ (FG) ambient at 300 °C for 30 minutes.

Figure 6-12 shows dependence of D_{it} on PMA temperature for the samples with the amorphous Si layer and the SPE-grown Si layer. The result for the sample on the Si substrate is also showed as reference. Open and close diagrams indicate the samples with or without Al-capping layer on W electrode, respectively. The D_{it} between La₂O₃ and Si can be lower by the PMA over 300 °C, which means the effect of atomic hydrogen affects by PMA over 300 °C. In the case of sample with the amorphous Si layer, D_{it} can be also reduced by using Al-capping layer due to improvement of interface property between La₂O₃ and Si. The achievement of lower D_{it} with PMA at 300 °C for the sample using the amorphous Si layer and Al-capping layer come to worse with rising of PMA temperature, which finally draw up to that for sample with SPE-grown Si layer. Keeping the low D_{it} between La₂O₃ and Si on the basis of the result on Si substrate in mind, interface property between Si-layer and Ge-substrate would become worse with increasing PMA temperature above 350 °C. Considering the large D_{it} for the sample with the SPE-grown Si layer, increase of SPE growth of the Si layer can be thinkable reason for the increase of defects with rising of PMA temperature.

The SPE growth of amorphous Si layer with increasing PMA temperature was examined by TEM observation, which can be seen in Fig. 6-13. Increase of crystallization area near the interface between Si-layer and Ge-substrate can be observed for the sample after PMA at 500 °C. The crystallized area was confirmed to be the Si layer by the z-contrast image of TEM observation as shown in Fig. 6-14. These results suggest that SPE-growth of the Si layer with rise in PMA temperature has responsible for increase in D_{it} .

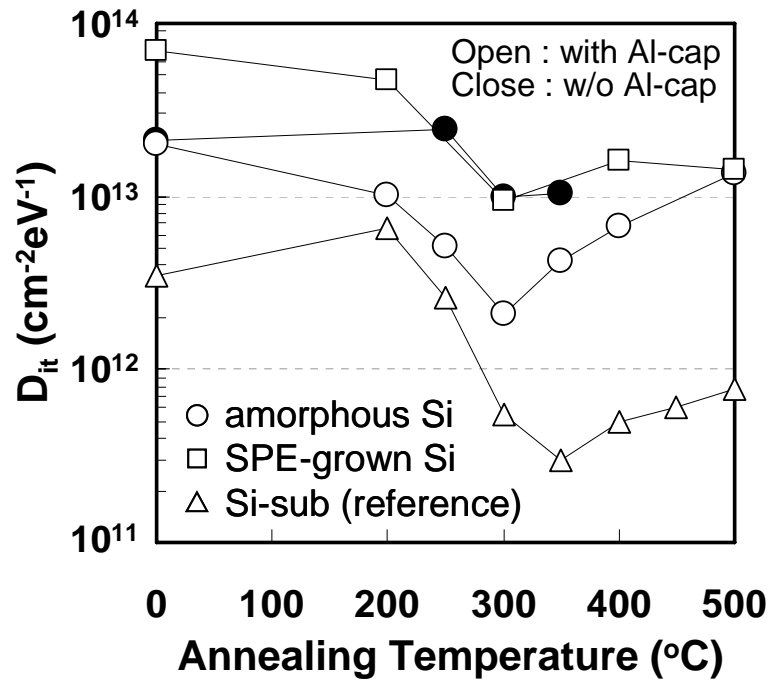


Figure 6-12. Dependence of D_{it} on PMA temperature for the samples with the amorphous Si layer and the SPE-grown Si layer. The result for the sample on the Si substrate is also showed as reference.

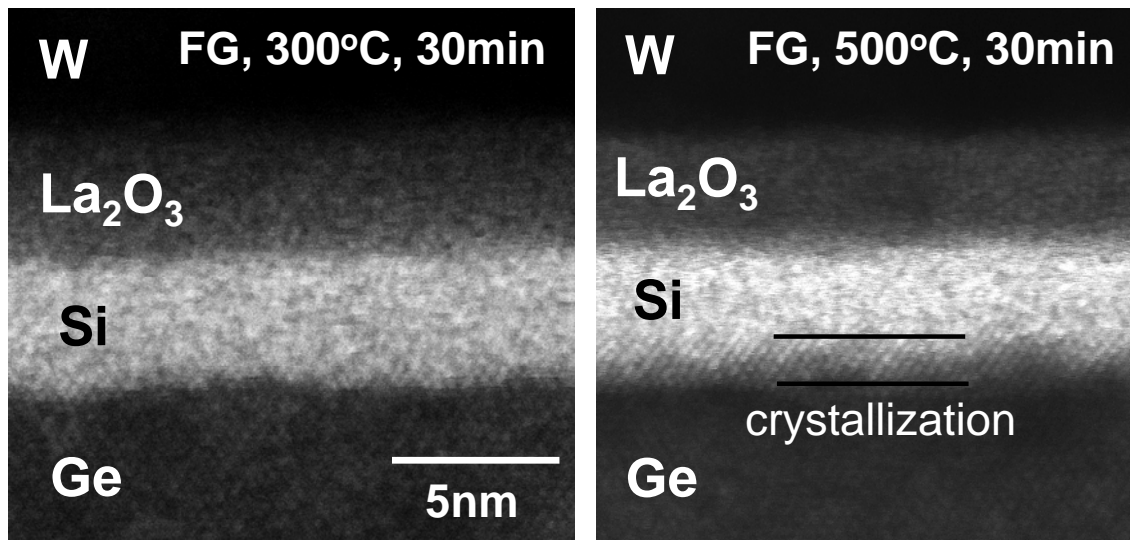


Figure 6-13. Cross-sectional TEM image for the samples with the amorphous Si layer after PMA at 300 °C or 500 °C.

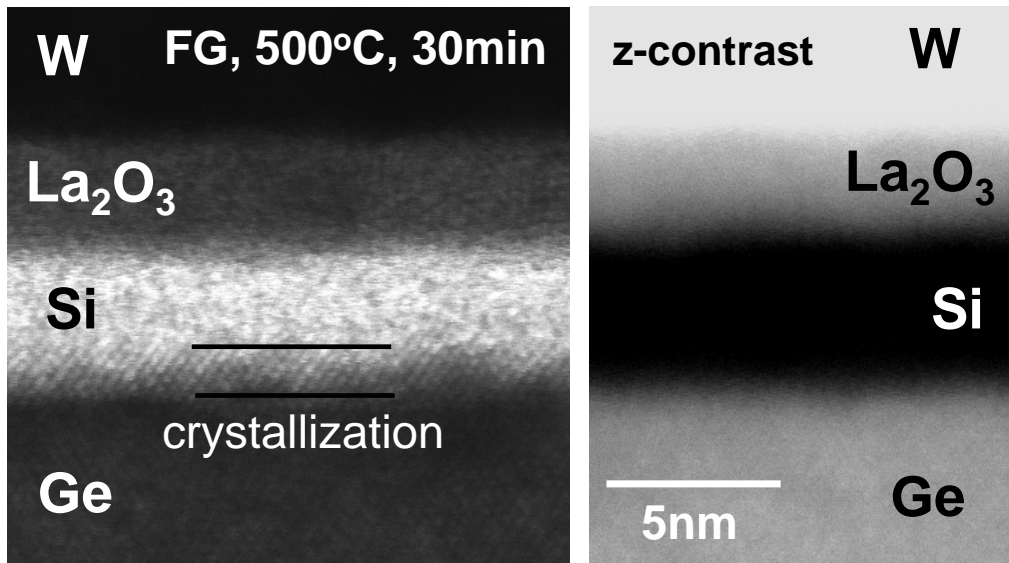


Figure 6-14. Cross-sectional TEM image and z-contrast image for the samples with the amorphous Si layer after PMA at 500 °C.

6.4 Dependence on Si-layer Thickness

D_{it} dependence on the thickness of the Si layer was examined using the condition indicating the lowest D_{it} ; with the amorphous Si layer and the introduction of atomic hydrogen by Al-capping layer on W electrode after PMA at 300 °C. Figure 6-15 shows 10kHz $C-V$ characteristics for the samples with four different thicknesses of Si layer. Very different $C-V$ characteristic was observed for the sample with 0.7-nm-thick Si layer. A slight increase of $C-V$ hysteresis indicates the growth of Ge sub-oxide and D_{it} increment can be comprehended by rise of lowest capacitance value around V_{fb} for the sample with 0.7-nm-thick Si layer. Increase of D_{it} thought to be due to the growth of GeO_x under the La-silicate layer (all Si might be consumed for the formation of La-silicate) suggests that the interfacial property between GeO_x and La-silicate would

not be good. With over 1.5-nm-thick Si layer, i.e. the thickness of the Si-layer is enough to suppress GeO_x completely, lowest capacitance values around V_{fb} were almost same, which implies almost same value of D_{it} can be achieved. Specific value of D_{it} on difference of Si-layer thickness is shown in Fig. 6-16.

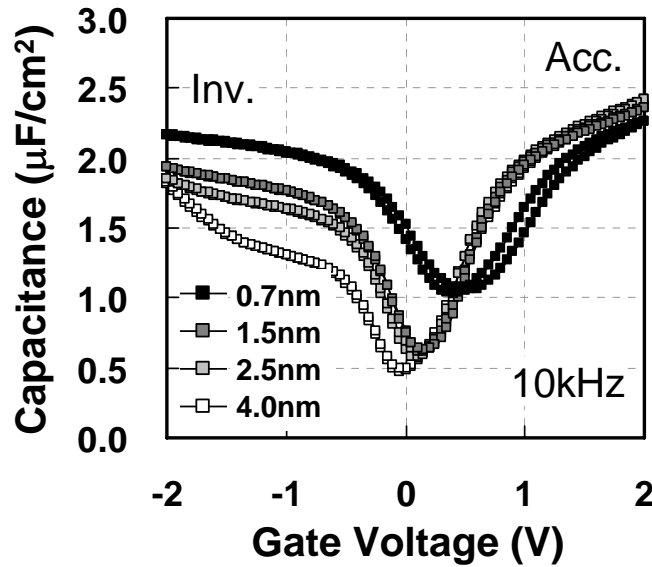


Figure 6-15. 10kHz C - V characteristics for Al/W/La₂O₃/Si/nGe-sub structure with four different thicknesses of the Si layer. PMA was conducted at 300 °C in FG ambient.

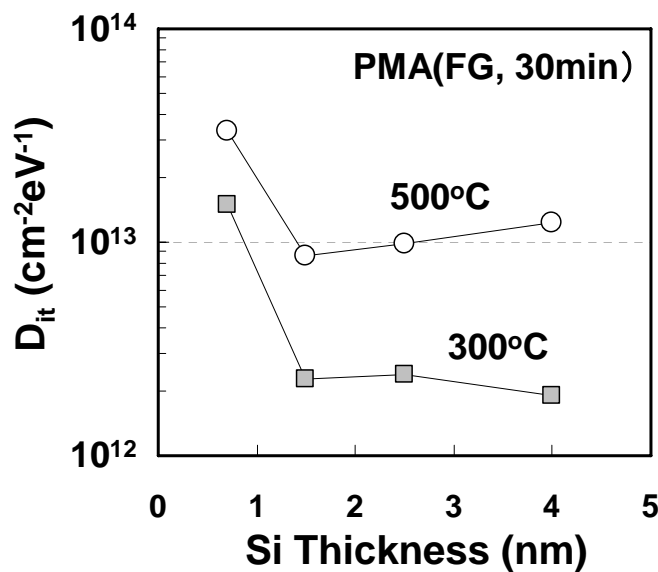


Figure 6-16. Dependence of D_{it} on the thickness of the Si layer.

In the meantime, inversion capacitance decreased with increasing in Si-layer thickness, while accumulation capacitance completely same in all thickness of Si layer as shown in Fig. 6-15. In contrast, accumulation capacitance decreased with increasing of Si-layer thickness in case of using p-Ge substrate, as can be seen in Fig. 6-17. That is to say, capacitance dependence on Si-layer thickness can be seen in the case when induced carrier is hole.

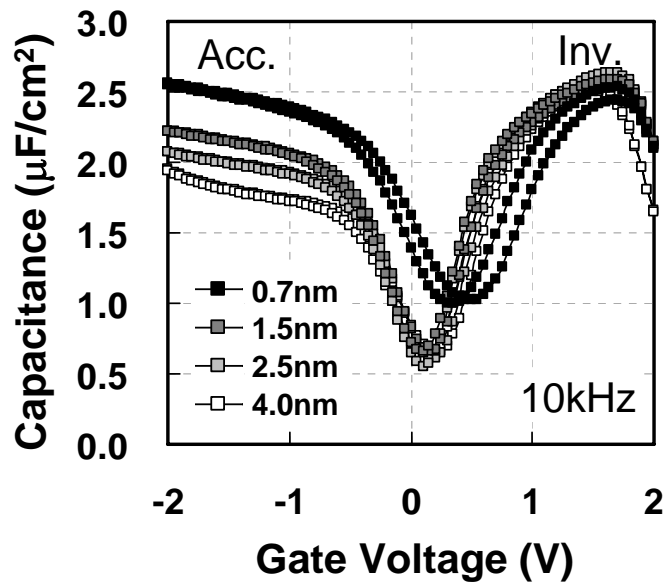


Figure 6-17. 10kHz $C-V$ characteristics for Al/W/La₂O₃/Si/pGe-sub structure with four different thicknesses of the Si layer. PMA was conducted at 300 °C in FG ambient.

The reason which capacitance dependence on Si-layer thickness was observed only in the case related to hole-carrier can be found in the relation of energy-band between of Si and Ge. Figure 6-18 shows energy-band diagram drawn in relation for a Si layer and Ge substrate. Here, specification of work function of gate electrode, the fixed charge and interface dipole is ignored. In silicon, the difference between vacuum level and conduction band (called the electron affinity) is 4.05 eV, which almost same

with Ge of 4.0 eV [6-5]. Thus, in the case of accumulation for n-type Ge and inversion for p-type Ge, induced electrons on Ge substrate presumably slide to Si layer so that electric field terminates at the surface of Si layer. In consequence, accumulation capacitance of n-type Ge and inversion capacitance of p-type Ge is invariable with no regard to the thickness of the Si layer. On the other hand, Ge has smaller band-gap of 0.66 eV compared with Si of 1.12 eV. Therefore, holes would be induced on the surface of Ge substrate in inversion for n-type Ge and accumulation for p-type Ge. In this case, electric field can be reached to surface of Ge substrate through the Si layer, which results in dependence of inversion capacitance for n-type Ge and accumulation capacitance for p-type Ge on the thickness of the Si layer.

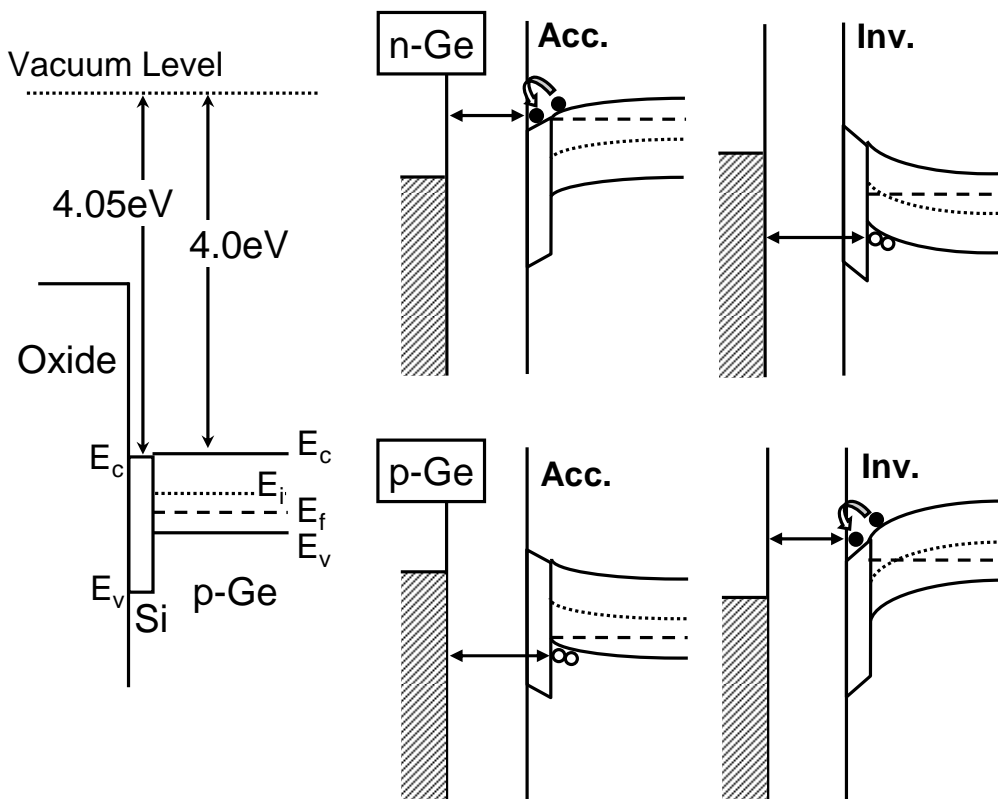


Figure 6-18. Energy-band diagram drawn in relation for a Si layer and Ge substrate. Si and Ge have similar electron affinities of 4.05 and 4.0 eV, respectively.

The influence of Si-layer thickness on EOT was investigated as compared with GeO₂ layer. Figure 6-19 shows the dependence of inversion EOT (EOT_{inv}) on the thickness of the Si layer for the sample shown in Fig. 6-15. From the slope of fitted line, effective dielectric constant of Si layer ($\epsilon_{Si,eff}$) was extracted as 17, which is larger than the dielectric constant of Si ($\epsilon=12$). The increment of effective dielectric constant of Si layer is considered to be due to the carrier (hole) concentration in La₂O₃/Si interface as shown in Fig. 6-20. EOT increase by the 1.5nm-thick Si layer is about 0.3 nm, while that by 1.5nm-thick GeO₂ layer ($\epsilon=5.8$) is almost 1 nm. Thus, it can be said that Si layer is better than GeO₂ layer with respect to the EOT scaling. Figure 6-21 shows leakage current density (J_g) - EOT plot for the various Ge-MOS structure. Quiet good J_g - EOT characteristics were obtained for the samples with Si passivation layer comparable to the sample without Si passivation layer.

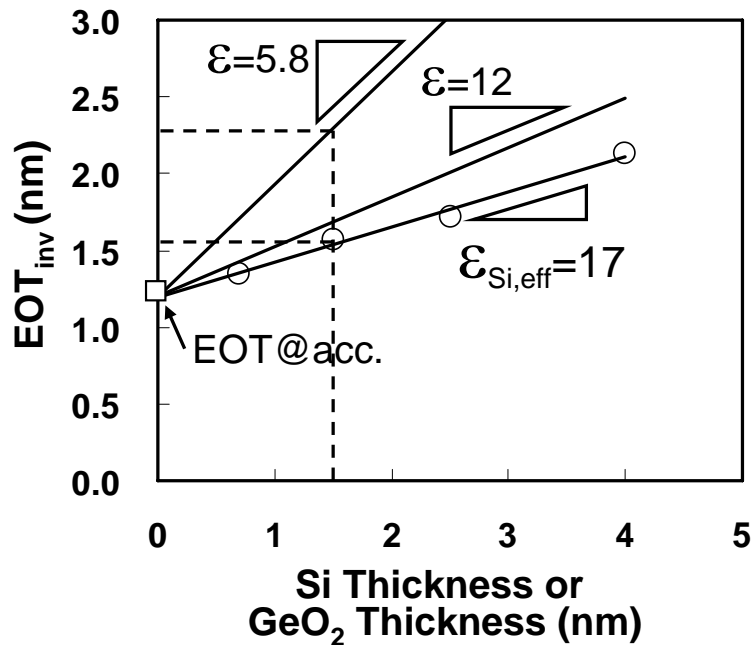


Figure 6-19. Dependence of inversion EOT (EOT_{inv}) on Si-layer thickness for the samples with different thickness of Si layer.

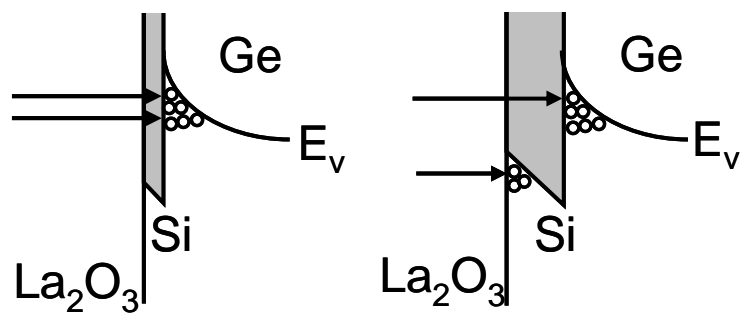


Figure 6-20. Schematic diagram of carrier concentration in $\text{La}_2\text{O}_3/\text{Si}$ and Si/Ge interface with different thickness of Si layer.

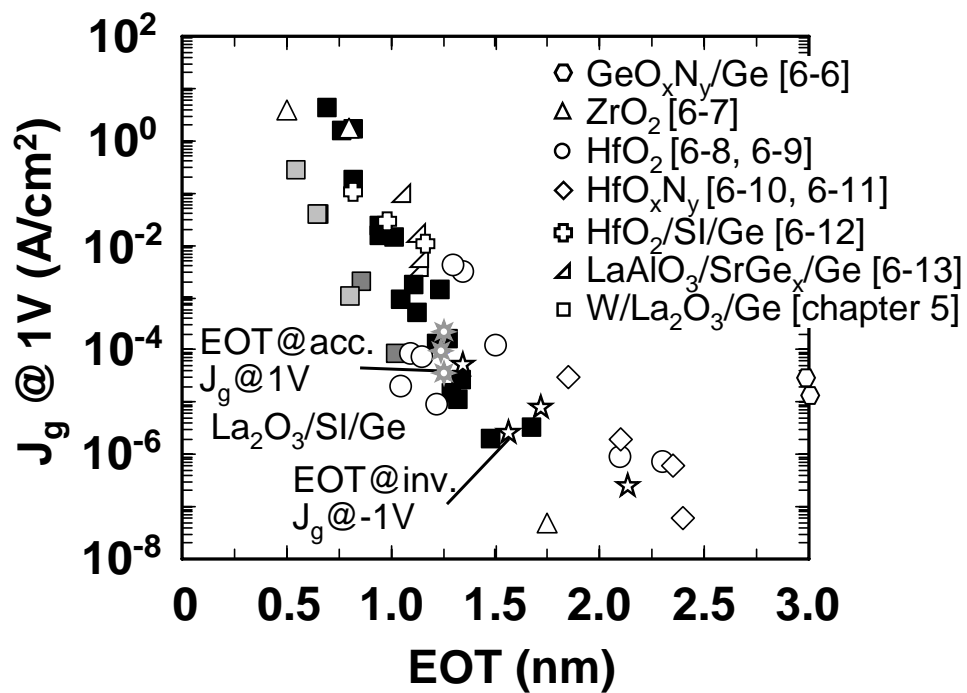


Figure 6-21. Leakage current density (J_g) - EOT plot for the various Ge-MOS structure.

6.5 Conclusion

The effect of ultrathin Si passivation layer between La₂O₃ gate dielectric and Ge substrate has been examined. C - V hysteresis can be significantly reduced by introduction of the Si passivation layer with thickness over 1 nm due to complete suppression of Ge sub-oxide growth and the simultaneous formation of La-silicate during PMA. Despite the great improvement of C - V hysteresis reduction, some defects resulting in increase of D_{it} are generated by crystallization of Si layer. Lattice mismatch between Si and Ge would have responsible for degrade in D_{it} since perfect epitaxial growth of Si layer is very hard by deposition using simple electron-beam evaporation method. Interface property between a Si layer and a Ge substrate might be advanced by progress in epitaxial growth method of Si layer. In this study, an amorphous Si layer has been found out as alternative solution to be effective in improvement of D_{it} . Moreover, almost same value of D_{it} could be achieved without regard of the Si-layer thickness if the thickness of the Si layer is sufficient to suppress the Ge sub-oxide. Although quiet good J_g -EOT characteristics can be achieved with Si passivation layer, since the increase of Si-layer thickness causes the decrease of inversion capacitance for p-MOSFET, optimization of Si-layer thickness should be needed for smaller EOT.

Reference

- [6-1] S. V. Hattangady, M. J. Mantini, G. G. Fountain, R. A. Rudder, and R. J. Markunas, "The role of an ultrathin silicon interlayer at the SiO₂-Ge interface," *J. Appl. Phys.*, vol. 71, pp. 3842 (1992).
- [6-2] B. De Jaeger, R. Bonzom, F. Leys, O. Richard, J. V. Steenbergen, G. Winderickx, E.V. Moorhem, G. Raskin, F. Letertre, T. Billon, M.Meuris, and M. Heyns, "Optimisation of a thin epitaxial Si layer as Ge passivation layer to demonstrate deep sub-micron n- and p-FETs on Ge-On-Insulator substrates," *Microelec. Eng.*, vol. 80, pp. 26 (2005).
- [6-3] K. Tachi, K. Kakushima, P. Ahemt, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "Effect of Oxygen for Ultra-Thin La₂O₃ Film Deposition," *ECS Trans.*, vol. 3, pp. 425 (2006).
- [6-4] K. Tachi, K. Kakushima, P. Ahemt, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "Improvement of Interface Properties of W/La₂O₃/Si MOS Structure Using Al Capping Layer," *ECS Trans.*, vol. 11, pp. 191 (2007).
- [6-5] S. O. Kasap and P. Capper, *Springer handbook of electronic and photonic materials*, Springer, 2006, p.495.
- [6-6] K. C. Saraswat, C. O. Chui, T. Krishnamohan, A. Nayfeh, and P. C. McIntyre, "Ge based high performance nanoscale MOSFETs," *Microelectronic Engineering*, vol. 80, pp. 15 (2005).
- [6-7] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A sub-400°C germanium MOSFET technology with high-k dielectric and metal gate," *IEEE IEDM 2002 Tech. Dig.*, pp. 437 (2002).
- [6-8] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS Characteristics with CVD HfO₂ Gate Dielectrics and TaN Gate Electrode," *VLSI Symp. 2003 Tech. Dig.*, pp. 121 (2003).

[6-9] N. Wu, Q. C. Zhang, C. X. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, and B. J. Cho., "Effect of surface NH₃ anneal on the physical and electrical properties of HfO₂ films on Ge substrate," *App. Phys. Lett.*, vol. 84, pp. 3741 (2004).

[6-10] Q. C. Zhang, N. Wu, C. X. Zhu, "The Electrical and Material Properties of HfO_xN_y Dielectric on Germanium Substrate," *Jpn. J. Appl. Phys.*, vol. 43, pp. L1208 (2004).

[6-11] C. -C. Cheng, C. -H. Chien, C. -W. Chen, S. -L Hsu, M. -Y. Yang, C. -C. Huang, F. -L. Yang, and C. -Y. Chang, "Impact of post-deposition-annealing on the electrical characteristics of HfO_xN_y gate dielectric on Ge substrate," *Microelectronic Engineering*, vol. 80, pp. 30 (2005).

[6-12] J. Mitard, B. D. Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D.P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C.H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, M. M. Heyns, "Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," *IEEE IEDM 2008 Tech. Dig.*, pp. 1 (2008).

[6-13] Y. Kamata, A. Takashima, Y. Kamimuta, and T. Tezuka, "New Approach to Form EOT-Scalable Gate Stack with Strontium Germanide Interlayer for High-k/Ge MISFETs," *VLSI Symp. 2009 Tech. Dig.*, pp. 78 (2009).

Chapter 7.

Characteristics of Ge MOSFET

7.1 Introduction

7.2 Ge p-MOSFET

7.3 Ge n-MOSFET

7.4 Conclusion

7.1 Introduction

The interface properties in La₂O₃/Ge MOS structure has been successfully advanced by introduction of Si-passivation layer on Ge substrate resulting in decrease of oxide trap density. Furthermore, interface trap density can be also reduced by using the amorphous Si as a passivation layer. In this chapter, Ge MOSFETs with La₂O₃ gate dielectric will be demonstrated in terms of the samples with or without Si-passivation layer.

Ge p-MOSFETs were fabricated with a conventional self-aligned process, which specific process flow was shown in chapter 2. A ring-shaped gate electrode was used for simplicity, because the isolation process is not necessary. The gate-stack fabrication processes of MOSFETs were same with those of MOS capacitors using the same substrate and prepared by in situ metallization process.

7.2 Ge p-MOSFET

Figure 7-1 shows drain current - drain voltage (I_d - V_d) characteristics of W/La₂O₃/Ge p-MOSFET after PMA 500 °C. The gate length and width (L/W) of MOSFETs are 10 μm and 200 μm, respectively. Well behaved p-MOSFET operation was confirmed with appropriate threshold voltage of -0.25 V.

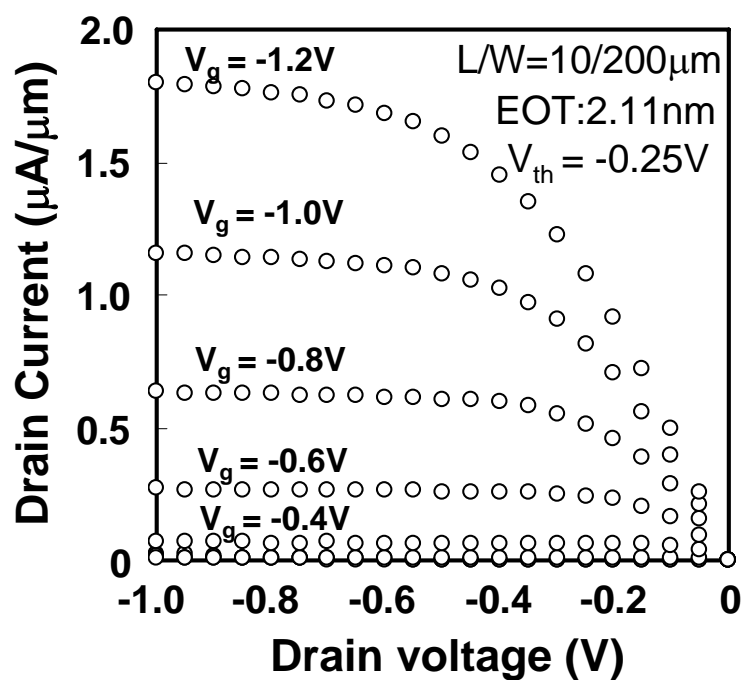


Figure 7-1. I_d - V_d characteristics of W/La₂O₃/Ge p-MOSFET after PMA 500 °C. The gate length and width (L/W) of MOSFETs are 10 μm and 200 μm, respectively.

Figure 7-2 shows 100kHz $C-V$ characteristics for W/La₂O₃/Ge p-MOSFET with or without Si-passivation layer. Si layer was deposited at 250 °C same with La₂O₃ deposition, i.e. Si layer was crystallized. PMA was performed at 500 °C in N₂ ambient for 5 minutes. 100kHz $C-V$ characteristics behaved like low frequency $C-V$ characteristics due to injection of inversion carriers from source and drain (S/D) region. As shown in chapter 6, very small $C-V$ hysteresis can be achieved with 2-nm-thick Si-passivation layer.

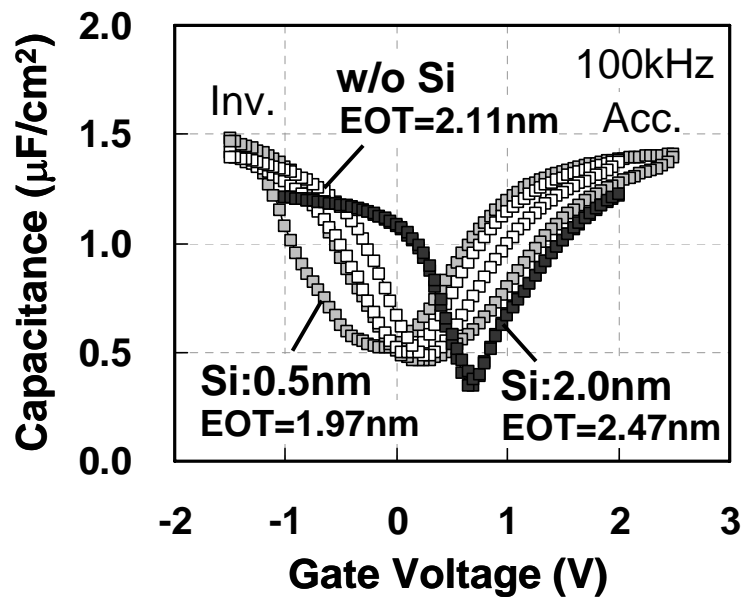


Figure 7-2. 100kHz $C-V$ characteristics for W/La₂O₃/Ge p-MOSFET with or without Si-passivation layer.

Reduction of C - V hysteresis was well affected MOSFET performance. Figure 7-3 shows normalized drain current (I_{ds}) (with reference to EOT in inversion region) of W/La₂O₃/Ge p-MOSFET with or without Si layer. Larger drive current was observed at the gate voltage of $V_{th}+1$ V for the sample with 2-nm-thick Si layer. Since D_{it} did not improved in this case of Si-passivation layer because of using the crystallized Si (c-Si) layer, superior MOSFET performance was attributed to reduction of oxide trap density by suppress the Ge suboxide growth and La-silicate formation with the Si-passivation layer. On the other hand, lower I_{ds} with 0.5-nm-thick Si layer compared to that without Si layer is thought to be due to the inferior interface property between La-silicate and Ge oxide and/or Ge substrate.

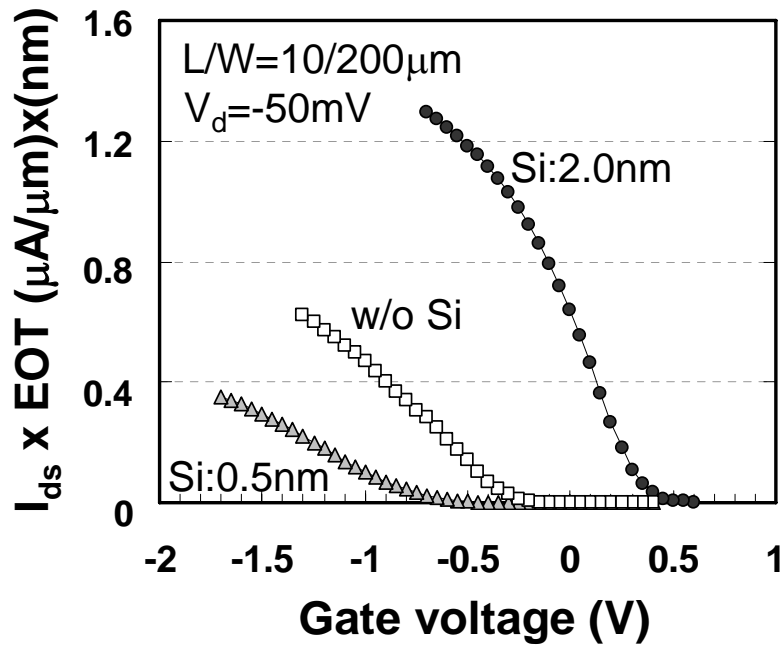


Figure 7-3. Normalized I_{ds} by EOT of W/La₂O₃/Ge p-MOSFET with or without Si layer.

I_{ds} was recorded up to gate voltage of $V_{th}+1$ V to negative direction.

Next, the effect of amorphous Si (a-Si) as a passivation layer was examined for the performance of Ge p-MOSFET. Figure 7-4 shows normalized 1kHz $C-V$ characteristics for W/La₂O₃/Ge p-MOSFET with a-Si and c-Si layer. In case of a-Si layer, PMA was conducted at 300 °C to maintain the amorphous phase of Si layer. Interface property between La₂O₃ and Si-layer was improved by atomic hydrogen using Al-capping layer on W electrode. As already demonstrated in chapter 6, D_{it} decrement was observed for the sample with a-Si layer.

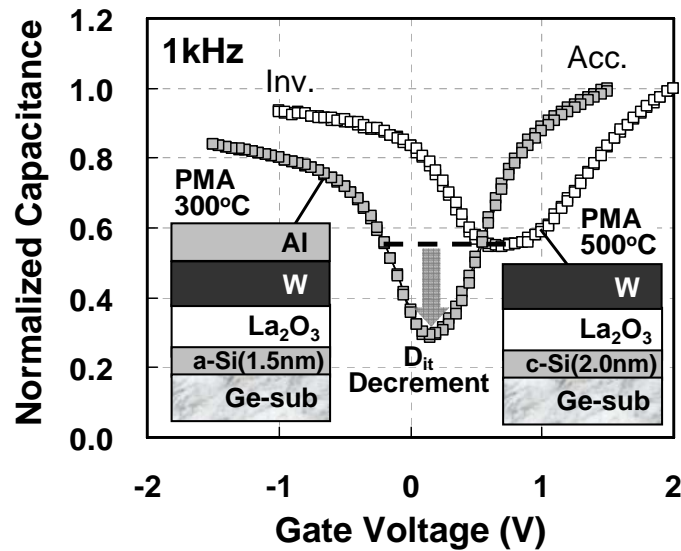


Figure 7-4. Normalized 1kHz $C-V$ characteristics for W/La₂O₃/Ge p-MOSFET with a-Si and c-Si layer. D_{it} decrement can be confirmed with a-Si layer.

D_{it} well has to do with effective mobility [7-1] and subthreshold slope (SS) [7-2] of MOSFET, which characteristics was also examined. Figure 7-5 shows logarithmic scale of I_{ds} against gate voltage for the sample with a-Si layer and c-Si. In the Subthreshold region, I_{ds} decreased more sharply in the case of using a-Si layer

indicating improvement of on-off current ratio in same gate voltage range. Specific values of subthreshold slope for the samples with a-Si and c-Si were 78.8 and 122.3 mV/dec, respectively. On the other hand, threshold voltages difference was observed between the samples with a-Si and c-Si. Threshold voltages (V_{th}) of the sample with a-Si and c-Si layer were -0.08 and 0.35 V, respectively, and V_{th} of sample with a-Si is preferable for p-MOSFET. Furthermore, considering the effective work function of tungsten [7-3] and dipole between La₂O₃ and Si [7-4], flat band voltage (V_{fb}) in sample with c-Si excessively shifted to positive direction. Therefore, large amount of negative fixed-charge originated in c-Si layer can be reduced by using a-Si layer.

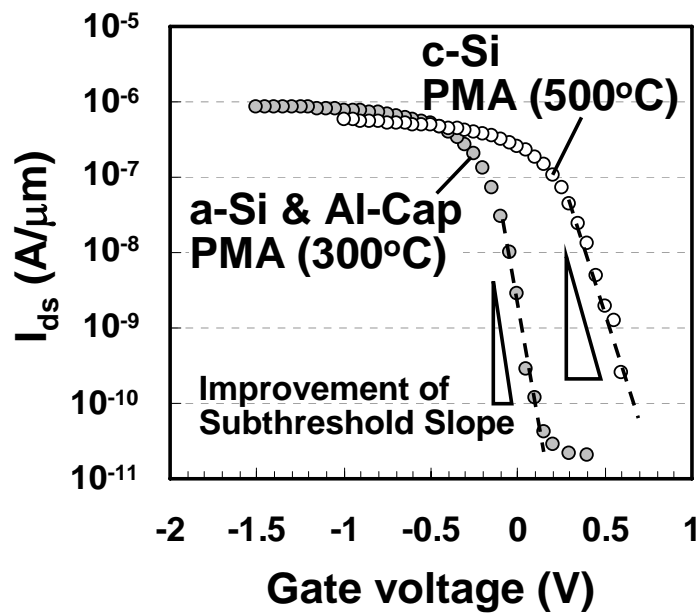


Figure 7-5. Logarithmic scale of I_{ds} against gate voltage for the samples with a-Si layer and c-Si. Improvement of subthreshold slope can be achieved with a-Si layer.

Effective mobility (μ_{eff}) was calculated by split $C-V$ method for p-MOSFETs. Figure 7-6 shows effective hole-mobility as a function of inversion charge density (N_{inv}) for the samples with a-Si and c-Si. Hole-mobility of SiO₂/Si structure was also added as a reference. EOTs in inversion region (EOT_{inv}) for the samples with a-Si and c-Si were 1.98 and 2.47 nm, respectively. D_{it} and fixed charge reduction observed for the sample with a-Si is well demonstrated in mobility increment. Furthermore, hole-mobility for the sample with a-Si layer was 1.5 times higher than that of SiO₂/Si structure at high N_{inv} region. Specific comparison in p-MOSFET characteristics for the samples with a-Si and c-Si are summarized in table 7-1. Figure 7-7 shows Peak hole-mobility vs. EOT_{inv} plot for various high-k/Ge p-MOSFET. The highest hole-mobility with small EOT has been achieved by Sr-Germanide (SrGe_x) interfacial layer up to date. La₂O₃/Ge p-MOSFET with Si-passivation layer indicates quiet promising mobility, showing similar value with HfO₂-based Ge p-MOSFET with Si passivation layer.

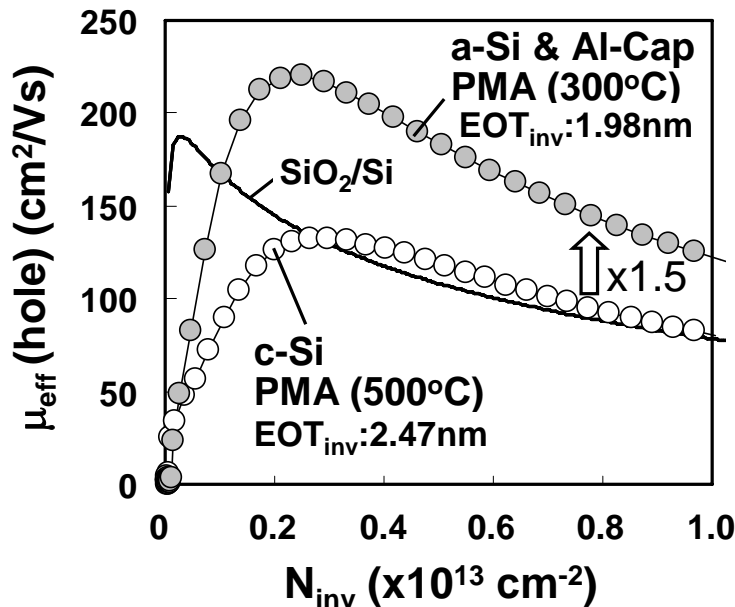


Figure 7-6. Effective hole-mobility as a function of N_{inv} for the samples with a-Si or c-Si. Hole-mobility of SiO₂/Si structure was also included as a reference.

Table 7-1. Summary of W/La₂O₃/Ge p-MOSFET with a-Si or c-Si layer as a passivation layer of Ge substrate.

	a-Si & Al-cap PMA (300°C)	c-Si PMA(500°C)
EOT (nm)	1.98	2.47
V _{th} (V)	-0.08	0.35
SS (mV/dec)	78.8	122.3
Hysteresis(mV)	15~32	10~27
Peak μ_{eff} (hole) (cm ² /Vs)	221	132

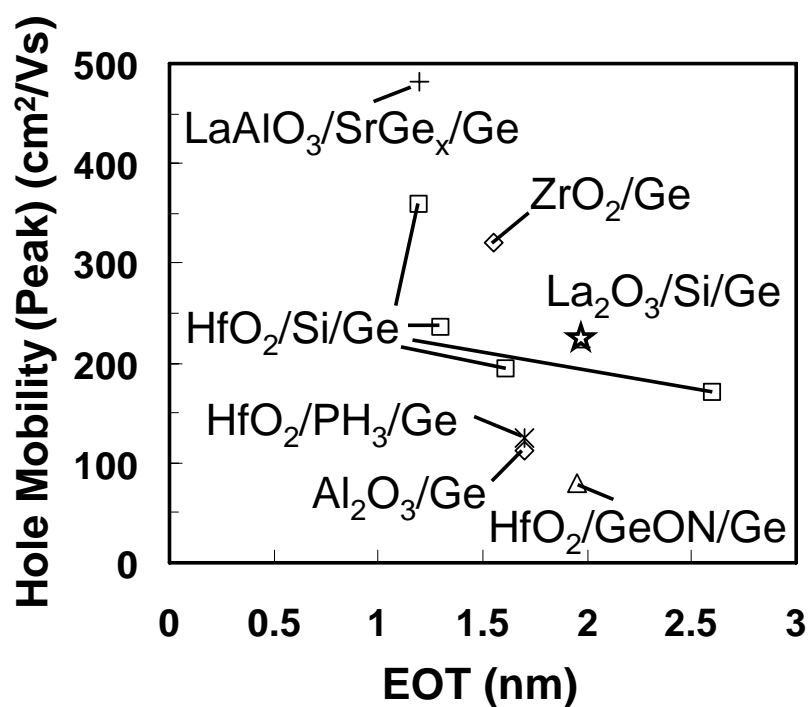


Figure 7-7. Peak hole-mobility vs. EOT_{inv} plot for various high-k/Ge p-MOSFET [7-5 - 7-12].

7.3 Ge n-MOSFET

W/La₂O₃/Ge n-MOSFETs with the a-Si passivation layer and Al-capping on W electrode were also fabricated and PMA was performed at 300 °C. Figure 7-8 shows comparison of drain current (I_{ds}) in n- and p-MOSFET with 1.5-nm-thick a-Si passivation layer. I_{ds} was normalized with reference to EOT in inversion region. It is notable that I_{ds} of n-MOSFET was smaller than that of p-MOSFET. Inferior I_{ds} characteristic is mainly due to the degradation of effective mobility as can be seen in Fig. 7-9. Very small peak mobility of 18 cm²/Vs obtained in n-MOSFET although bulk mobility of electron is twice larger than that of hole in Ge. This degradation of electron mobility is considered to originate in band structure of Si and Ge. As described in chapter 6-4, induced electron-carriers on a Ge substrate in an inversion region of n-MOSFET might slide to the Si layer due to the similar electron affinity of Si and Ge, resulting in no dependence of inversion capacitance on Si-layer thickness. As many of electrons are transported in the a-Si layer which has very low mobility, effective electron mobility is degraded with inserting of a-Si layer. Similar degradation of electron mobility was also observed in HfO₂/SiO₂/Si/Ge structured n-MOSFET with epitaxial grown Si passivation layer [7-5]. As perfect epitaxial growth is very difficult due to the lattice mismatch between Si and Ge, some strains and defects could remain in the epitaxial-grown Si layer, which would degrade electron mobility being transported in the Si layer.

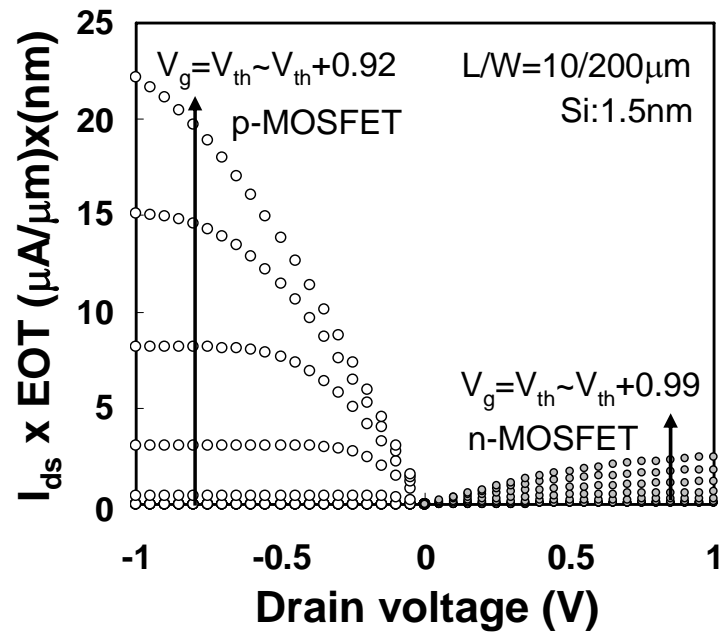


Figure 7-8. Normalized I_{ds} of n- and p-MOSFET with 1.5-nm-thick a-Si passivation layer. Saturated I_{ds} in n-MOSFET was smaller than that in p-MOSFET.

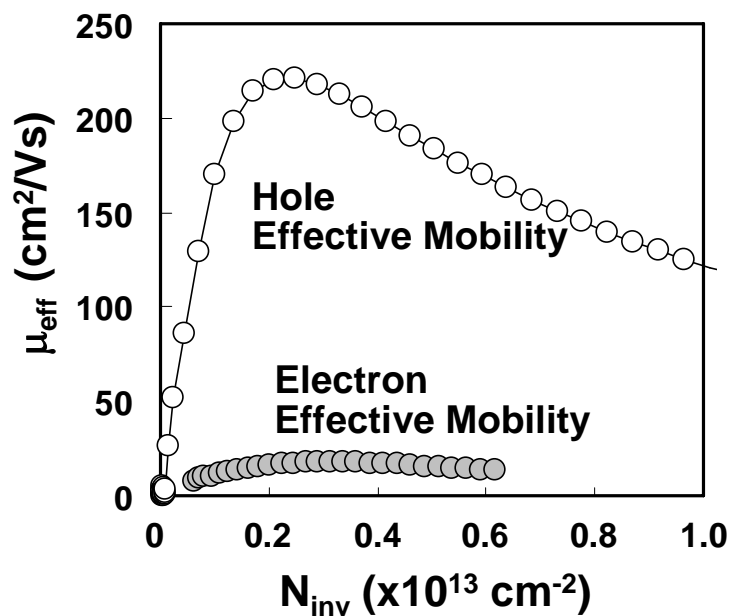


Figure 7-9. Effective mobility of electron and hole for the sample with 1.5-nm-thick a-Si passivation layer.

7.4 Summary

Ge MOSFETs with La₂O₃ gate dielectric have been demonstrated with or without Si-passivation layer. Well behaved MOSFET operation was confirmed with and without Si-passivation layer. Drain-current increase with the Si-passivation layer has been observed in p-MOSFET and the superior performance is attributed to reduction of oxide trap density by the Si-passivation layer. Further improvement in subthreshold characteristics and effective hole-mobility can be achieved by using of amorphous Si layer with decreasing interface trap density and fixed charge. On the other hand, critical degradation of effective electron-mobility has been found for n-MOSFET with a Si layer. The degradation of electron mobility is considered to originate in band structure of Si and Ge which has similar electron affinity, causing the transport of electron carriers in inversion region to take place in the Si layer. Further research on alternative passivation method of the Ge surface for n-MOSFET is needed.

Reference

- [7-1] J. A. Ng, N. Sugii, K. Kakushima, P. Ahmet, K. Tsutsui, T. Hattori, and H. Iwai, "Effective mobility and interface-state density of La₂O₃ nMISFETs after post deposition annealing," *IEICE ELEX*, vol. 3, pp. 316 (2006).
- [7-2] S. M. Sze and Kwok K. Ng, *Physics of Semiconductor* 3rd edition, Wiley, 2007, chapter 6, p. 316.
- [7-3] M. Adachi, K. Okamoto, K. Kakushima, P. Ahmet, N. Sugii, K. Tsutsui, T. Hattori, and H. Iwai, "Control of Flat Band Voltage by Partial Incorporation of La₂O₃ or Sc₂O₃ into HfO₂ in Metal/HfO₂/SiO₂/Si MOS Capacitors," *ECS Trans.*, vol. 11, pp. 157 (2007).
- [7-4] K. Kakushima, K. Okamoto, M. Adachi, K. Tachi, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Origin of flat band voltage shift in HfO₂ gate dielectric with La₂O₃ insertion," *Solid-State Electronics*, vol. 52, pp. 1280 (2008).
- [7-5] B. De Jaeger, R. Bonzom, F. Leys, O. Richard, J. V. Steenbergen, G. Winderickx, E.V. Moorhem, G. Raskin, F. Letertre, T. Billon, M.Meuris, and M. Heyns, "Optimisation of a thin epitaxial Si layer as Ge passivation layer to demonstrate deep sub-micron n- and p-FETs on Ge-On-Insulator substrates," *Microelec. Eng.*, vol. 80, pp. 26 (2005).
- [7-6] Y. Kamata, A. Takashima, Y. Kamimuta, and T. Tezuka, "New Approach to Form EOT-Scalable Gate Stack with Strontium Germanide Interlayer for High-k/Ge MISFETs," *VLSI Symp. Tech. Dig.*, pp. 78 (2003).
- [7-7] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," *IEEE IEDM Tech. Dig.*, pp. 655 (2006).
- [7-8] J. Mitard, B. De Jaeger, F.E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken,

C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M.M. Heyns, "Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," IEEE IEDM Tech. Dig., pp. 873 (2008).

[7-9] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, A. Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. O. Sin, D. L. Kwong, "A TaN-HfO₂-Ge pMOSFET with Novel SiH₄ surface passivation," IEEE Elect. Dev. Lett., vol. 25, pp. 631 (2004).

[7-10] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A sub-400°C germanium MOSFET technology with high-k dielectric and metal gate," IEEE IEDM Tech. Dig., pp. 437 (2002).

[7-11] C. H. Huang, M. Y. Yang, Albert Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very Low Defects and High Performance Ge-On-Insulator p-MOSFETs with Al₂O₃ Gate Dielectrics," Symp. VLSI Tech. Dig., pp. 119 (2003).

[7-12] S. J. Whang, S. J. Lee, F. Gao, N. Wu, C. X. Zhu, J. S. Pan, L. J. Tang, and D. L. Kwong, "Germanium p- & n-MOSFETs fabricated with novel surface passivation (plasma-PH₃ and thin AlN) and TaN/HfO₂ Gate stack," IEEE IEDM Tech. Dig., pp. 307 (2004).

Chapter 8.

Conclusions

8.1 Summary of this Study

8.2 Discussion to the Further Work for L₂O₃/Ge Structure

8.1 Summary of this Study

As the scaling limit of planar SiO₂/Si MOS devices, researches for alternative channel material and high dielectric constant (high-k) gate insulator have been necessary for further device improvement. In this study, gate-stack process of Ge-MOS structure with La₂O₃ high-k gate dielectric has been investigated for future Ge-channel MOSFET.

First of all, since interfacial properties between a high-k film and a substrate are very influential to device performance, interfacial properties between the La₂O₃ layers and the Ge substrate has been studied under various annealing conditions. From the results after PDA treatment in inert N₂ ambient, it has been found that interfacial reaction between La₂O₃ and Ge is less than that between La₂O₃ and Si, which indicates formation energy of La-germanate is larger than that of La-silicate. Despite less reaction with the La₂O₃ film, thermodynamic diffusion of Ge atoms by PDA is larger than that of Si atoms. It is notable that Ge can certainly diffuse to the surface of the La₂O₃ film by PDA at 600 °C for practical devices with EOT under 1 nm. On the other hand, it has been found that D_{it} can be remarkably reduced by PMA treatment in N₂ compared to PDA treatment in N₂. This improvement in D_{it} is attributed to growth of interfacial layer due to the oxidation of Ge substrate by hydroxyl group absorbed in the La₂O₃ film.

On the basis of the results that D_{it} can be improved by the growth of interfacial layer during PMA, interfacial layer has been grown intentionally by PDA in oxygen ambient. The grown interfacial layer is thought to be Ge sub-oxide considering the XPS spectra and the dielectric constant of 5.8. The Ge sub-oxide layer can effectively decreases D_{it} with thickness over 1.5 nm. Low dielectric constant (5.8) of Ge sub-oxide would be an obstacle for EOT scaling. Not only thermally grown interfacial layer but

also chemically formed GeO₂ layer before deposition of the La₂O₃ film has been examined. Once reductions in both $C-V$ hysteresis and D_{it} was observed in the case using the chemical GeO₂ layer with proper PDA treatment, while large amount of $C-V$ hysteresis is generated in case of thermally grown Ge sub-oxide layer. This would be attributed to the formation of La-germanate at the interface of La₂O₃ and Ge substrate. However, remained Ge sub-oxide in the La₂O₃ film causes increase of $C-V$ hysteresis with decreasing in EOT (strengthening of gate electric field). In order to remove the $C-V$ hysteresis in La₂O₃/Ge structure, growth of Ge sub-oxide should be completely suppressed.

In addition to interface properties, thermodynamic stability has been studied for metal/La₂O₃/Ge structure with various metal gate-electrodes after PMA at 300-500 °C. In case of using Pt electrode to focus interfacial properties between the La₂O₃ layer and the Ge substrate because of inert property of Pt, increase in leakage current density has been observed after PMA. The increase in leakage current density is attributed to the Pt-germanide formation by diffused Ge and Pt atoms in the La₂O₃ film, which can be suppressed by controlling the reaction between gate electrode and Ge; i.e. by using Ta and W as a gate electrode which has high-reaction temperature with Ge. On the basis of the low leakage current with W electrode, very small EOT of 0.55 nm with leakage current density of 2.7×10^{-1} A/cm² can be achieved by *in situ* fabrication of W electrode after the La₂O₃ deposition (without air expose after the deposition of La₂O₃ film). However, large amount of D_{it} has been observed in this case due to the little interfacial layer and which can not be improved after hydrogen annealing even in using atomic hydrogen as opposed to W/La₂O₃/Si structure. Interfacial layer should be necessary for reduction of D_{it} and it can be said that there is trade-off relation between achievement of

small EOT with lower leakage current density and improvement of interfacial property in La₂O₃/Ge MOS structure.

It seems difficult to achieve satisfactory interfacial properties by fabrication of the La₂O₃ film directly on the Ge substrate due to the diffusion of Ge and the growth of Ge sub-oxide layer. Introduction of ultrathin Si passivation layer on the Ge surface can effectively suppress the diffusion of Ge and the growth of Ge sub-oxide. Moreover, La-silicate formation by reaction between the La₂O₃ and Si layer during annealing also helps to decrease the oxide trap density (*C-V* hysteresis) caused by oxygen vacancy of La₂O₃. In addition, interface properties between the La₂O₃ and Si layer follow results on La₂O₃/Si-sub MOS structure. Interface properties between Si layer and Ge substrate become degraded by crystallization of the Si layer resulting in increase of D_{it} over 10^{13} cm⁻²eV⁻¹. Lower D_{it} of 10^{12} cm⁻²eV⁻¹ can be obtained with amorphous-phase Si layer by the deposition of the Si and La₂O₃ layer at room temperature and keeping the PMA temperature under 300 °C, where interface property between the La₂O₃ and Si layer being advanced by introduction of atomic hydrogen with the Al-capping layer on the W electrode. Although quiet good J_g - EOT characteristics can be achieved with Si passivation layer, since increase of the Si-layer thickness causes the decrease of inversion capacitance for p-MOSFET, optimization of the Si-layer thickness should be necessary for smaller EOT.

Finally, Ge MOSFETs with La₂O₃ gate dielectric has been demonstrated with or without the Si-passivation layer. Increase of drain-current in p-MOSFET with the Si-passivation layer has been observed, which is attributed to reduction of oxide trap density by the Si-passivation layer. Further improvement in subthreshold slope and effective hole-mobility can be achieved by using amorphous Si-layer instead of

crystallized Si-layer with decreasing D_{it} and fixed charge. In this study, peak hole-mobility of 221 cm²/Vs was achieved at the EOT of 1.98 nm; however, smaller EOT will be necessary for practical device. In general, effective mobility becomes degraded with decreasing in EOT around 1 nm due to influence of the metal/high-k interface (see Fig. 8-1). Considering the mobility degradation in accordance with decrease of EOT in La₂O₃/Si MOSFET, the hole-mobility in Ge p-MOSFET with the Si passivation layer will be expected as 150 cm²/Vs at the EOT of 1 nm and 60 cm²/Vs at the EOT of 0.5 nm.

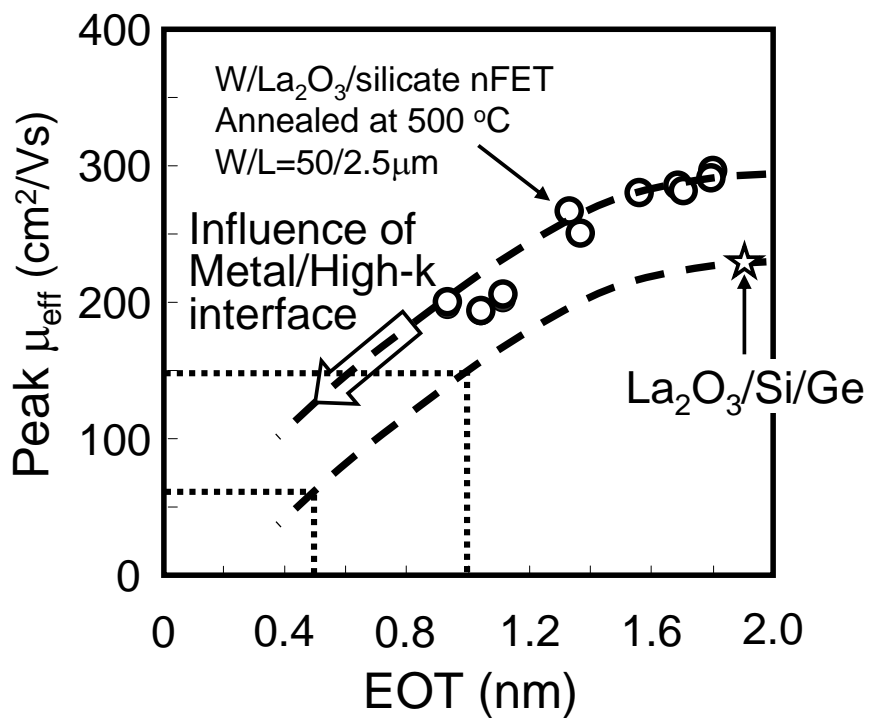


Figure 8-1. Mobility degradation with decreasing EOT.

On the other hand, despite the advanced performance in p-MOSFET, critical degradation in electron mobility has been found for n-MOSFET with the Si passivation layer. The degradation of electron mobility is considered to originate in band structure of Si and Ge which has similar electron affinity, causing most of electron transport in channel region to take place in low-mobility Si layer. Research on alternative passivation layer of Ge surface will be needed for improvement of Ge n-MOSFET.

8.2 Discussion to the Further Works

As described in this study, it seems tough to achieve satisfactory interfacial properties in direct contact of the La₂O₃ film on the Ge substrate. Although La₂O₃/Ge p-MOSFET with the Si passivation layer is quiet promising, introduction of the Si passivation layer should not be always the best option for La₂O₃/Ge MOSFET, i.e. as degradation of electron mobility in n-MOSFET with the Si passivation layer. Actually, achieving prominent characteristic for Ge n-MOSFET is said to be difficult because charge neutrality level (CNL) of Ge is located close to the valence band edge [8-1]. Most of interface states below Fermi level are negatively charged during the n-MOSFET operation (see Fig. 8-2), which works as coulomb scattering center resulting in degradation of electron mobility. Thus, usage of Ge-channel only for p-MOSFET with n-MOSFET using Si-channel [8-2] or compound semiconductor (III-V) channel [8-3] is a kind of way. For appliance of La₂O₃/Ge p-MOSFET with Si passivation layer to CMOS technology, there is still a lot of works to solve such as MOSFET characterization at sub-1nm EOT, controllability of threshold voltage, reliability, etc.

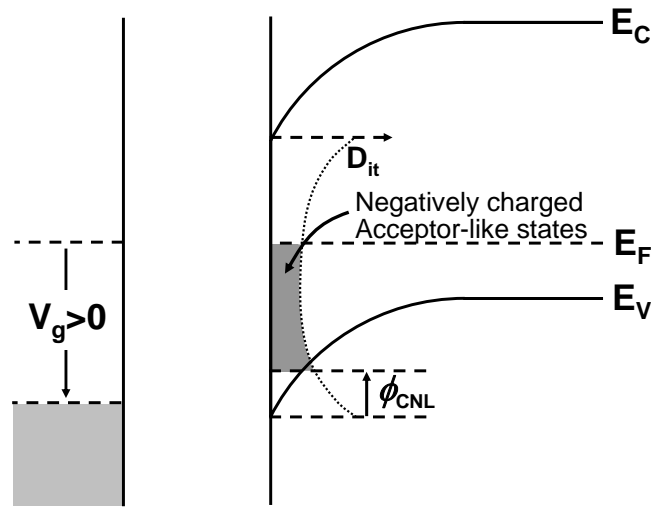


Figure 8-2. Energy-band diagram of p-type Ge MOS structure with a positive voltage applies to the gate.

In order to realize high electron-mobility for Ge n-MOSFET, very small D_{it} below $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ should be necessary to minimize the influence of negatively charged interface coulomb scattering. In general, low D_{it} can be easily achieved by thermally grown Ge oxide; however, large amount of oxide trap density (shown in C - V hysteresis) is generated due to the simultaneously grown Ge sub-oxide [8-4]. Despite the severe obstacles in the interfacial properties for Ge n-MOSFET, high electron-mobility almost same with Si universal mobility has been obtained recently in GeO_2/Ge structure achieving very low D_{it} below $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ and small C - V hysteresis by using high pressure oxidation (HPO) method [8-5]. The GeO_2 layer grown by HPO method seems to be effective as the interlayer of rare-earth oxide gate dielectric for achieving low D_{it} and small C - V hysteresis, while large amount of C - V hysteresis still remained in case of Hf-oxide gate dielectric [8-6]. The HPO method is considered to be effective for $\text{La}_2\text{O}_3/\text{Ge}$ system to decrease D_{it} with small C - V hysteresis. However, the interfacial

GeO₂ layer has critical problem in EOT scaling issue. As shown in this study, 1.5-nm-thick interfacial Ge-oxide layer will be necessary to attain the D_{it} of 10^{12} cm⁻²eV⁻¹. Considering dielectric constant of GeO₂ ($\epsilon_{\text{GeO}_2}=5.8$), high-k film can not be introduced for EOT of 1 nm.

Ge nitride (Ge₃N₄) or oxynitride is also one of the candidates of interfacial layer for high-k/Ge systems. Quiet good interface property with very little C - V hysteresis has been reported with Ge₃N₄ gate dielectric grown by direct nitridation of Ge substrate with atomic nitrogen radicals [8-7, 8-8]. Furthermore, dielectric constant of Ge₃N₄ is 9.5 [8-8], which is larger than that of GeO₂. The Ge₃N₄ has been demonstrated as interfacial layer of HfO₂, resulting in improving the interfacial property in HfO₂/Ge structure [8-9]. In fact, Ge₃N₄ already examined as an interfacial layer for La₂O₃/Ge structure. Low D_{it} below 10^{12} cm⁻²eV⁻¹ and sub-1nm EOT could be easily achieved with the Ge₃N₄ layer and leakage current density also decreased due to suppression of Ge oxide growth. However, mobility degradation has been reported by using nitride as a gate dielectric and increase of nitrogen in dielectric for Si MOS structures [8-10 - 8-12]. Actually, so far reported effective mobility for high-k/Ge MOSFET with the interfacial nitride layer is not as high as expected [8-13 - 8-15]. Thus, increase of effective mobility by optimization of nitridation condition or thickness of nitride layer will be the key for introduction of interfacial Ge nitride.

The most valuable interfacial layer is thought to be a La-germanate layer containing little sub-oxide such as a La-silicate layer on a Si substrate. Indeed, the La-germanate layer is also high-k due to large dielectric constant. Researches of La-germanate as interlayer of high-k have increased recently due to possibility of low D_{it} and scale down of EOT [8-16 ~ 8-18]; while C - V hysteresis can not be removed

completely in any of researches. For the formation of La-germanate without sub-oxide, some extra process such as radical oxidation of La₂O₃/Ge structure in high-vacuum condition and spike annealing at high-temperature over 800 °C with or without a GeO₂ layer have been also investigated in our group; however *C-V* hysteresis can not be reduced in any case. If high-quality La-germanate layer containing little sub-oxide would be fabricated, feasible high-k/Ge devices can be expected. In general, Ge sub-oxide is generated by the reaction of GeO₂ and Ge substrate as shown below [8-19].



In fact, a GeO₂ layer deposited by sputtering method on Si substrate do not decomposed after annealing at 600 °C in N₂ ambient resulting in very small *C-V* hysteresis [8-6]. Recently our group confirmed the very small *C-V* hysteresis for Si-MOS capacitors with the rare-earth-oxide-germanate layer fabricated by deposition of rare-earth-oxide and Ge atoms on Si substrate and followed annealing. Since the reaction between Ge oxide and Ge substrate has responsible for the generation of Ge sub-oxide, La-germanate deposition by CVD or sputtering method on the Ge substrate directly and control of annealing below 400 °C would be effective for fabrication of high-quality La-germanate layer without Ge sub-oxide.

Finally, further increase of peak mobility has been reported recently for Ge n-MOSFET fabricated on Ge(111) substrate. This increment of mobility can be achieved due to the lower effective mass on the Ge(111) substrate compared with that on the Ge(100) substrate by quantum effect in the two dimension inversion layer [8-20]. It has been also found the difference in oxidation rate and volatilization rate of a GeO₂ layer [8-21]. Interface properties and electrical characteristics for La₂O₃/Ge MOSFET on Ge(111) substrate also draws lots of interest.

Reference

- [8-1] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, "Fermi-level pinning and charge neutrality level in germanium," *Appl. Phys. Lett.*, vol. 89, pp. 252110 (2006).
- [8-2] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Hirashita, E. Toyoda, N. Sugiyama, T. Mizuno, and S. Takagi, "A new strained-SOI/GOI dual CMOS technology based on local condensation technique," *Symp. VLSI Tech. Dig.*, p. 80 (2005).
- [8-3] S. Takagi, T. Tezuka, T. Irisawa, S. Nakaharai, T. Numata, K. Usuda, N. Sugiyama, M. Shichijo, R. Nakane, and S. Sugahara, "Device structures and carrier transport properties of advanced CMOS using high mobility channels," *Solid-State Electronics*, vol. 51, pp. 526 (2007).
- [8-4] A. Toriumi, *IEDM 2006, short course* (2006).
- [8-5] C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Ge/GeO₂ Interface Control with High-Pressure Oxidation for Improving Electrical Characteristics," *Appl. Phys. Express* vol. 2, pp. 071404 (2009).
- [8-6] A. Toriumi, T. Tabata, C. H. Lee, T. Nishimura, K. Kita, and K. Nagashio, "Opportunities and challenges for Ge CMOS - Control of interfacing field on Ge is a key," *Microelectronic Engineering*, vol. 86, pp. 1571 (2009).
- [8-7] T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, and Y. Morita, and S. Takagi, "Pure germanium nitride formation by atomic nitrogen radicals for application to Ge metal-insulator-semiconductor structures," *J. Appl. Phys.*, vol. 100, pp. 014101 (2006).
- [8-8] T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, and Y. Morita, "Ge metal-insulator-semiconductor structures with Ge₃N₄ dielectrics by direct nitridation of Ge substrates," *Appl. Phys. Lett.*, vol. 85, pp. 3181 (2004).
- [8-9] S. Takagi, T. Maeda, N. Taoka, M. Nishizawa, Y. Morita, K. Ikeda, Y. Yamashita, M. Nishikawa, H. Kumagai, R. Nakane, S. Sugahara and N. Sugiyam, "Gate dielectric

formation and MIS interface characterization on Ge,” *Microelectronic Engineering*, vol. 84, pp. 2314 (2007).

[8-10] A. Kamgar, J. T. Clemens, A. Ghetti, C. T. Liu, and E. J. Lloyd, “Reduced Electron Mobility due to Nitrogen Implant Prior to the Gate Oxide Growth,” *IEEE Elec. Dev. Lett.*, vol. 21, pp.227 (2000).

[8-11] K. J. Yang, T. -J. King, C. Hu, S. Levy, and H. N. Al-Shareef, “Electron mobility in MOSFETs with ultrathin RTCVD silicon nitride/oxy-nitride stacked gate dielectrics,” *Solid-State Electronics*, vol. 47, pp. 149 (2003).

[8-12] A. Nakajima, H. Ishii and S. Yokoyama, “Carrier Mobility in Metal–Oxide–Semiconductor Field Effect Transistor with Atomic-Layer-Deposited Si–Nitride Gate Dielectrics,” *Jpn. J. Appl. Phys.*, vol. 44, pp. L903 (2005).

[8-13] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, A. Du, N. Balasubramanian, M. F .Li, A. Chin, J. K. O. Sin, D. L. Kwong, “A TaN-HfO₂-Ge pMOSFET with Novel SiH₄ surface passivation,” *IEEE Elect. Dev. Lett.*, vol. 25, pp. 631 (2004).

[8-14] A. Ritenour, A. Khakifirooz, D. A. Antoniadis, R. Z. Lei, W. Tsai, A. Dimoulas, G. Mavrou, and Y. Panayiotatos, “Subnanometer-equivalent-oxide-thickness germanium p-metal-oxide-semiconductor field effect transistors fabricated using molecular-beam-deposited high-k/metal gate stack,” *Appl. Phys. Lett.*, vol. 88, pp. 132107 (2006).

[8-15] M. Houssa, T. Conard, F. Bellenger, G. Mavrou, Y. Panayiotatos, A. Sotiropoulos, A. Dimoulas, M. Meuris, M. Caymax, and M. M. Heyns, “Electrical Properties of Atomic-Beam Deposited GeO_{1-x}N_x/HfO₂ Gate Stacks on Ge,” *J. Electrochem. Soc.*, vol. 153, pp. G1112 (2006).

[8-16] G. Mavrou, S.F. Galata, A. Sotiropoulos, P. Tsipas, Y. Panayiotatos, A. Dimoulas, E.K. Evangelou, J.W. Seo, and Ch. Dieker, “Germanium metal-insulator-semiconductor capacitors with rare earth La₂O₃ gate dielectric,” *Microelectronic Engineering*, vol. 84, pp. 2324 (2007).

[8-17] G. Mavrou, S.F. Galata, A. Sotiropoulos, P. Tsipas, Y. Panayiotatos, A. Dimoulas, E.K. Evangelou, J.W. Seo, and Ch. Dieker, “Electrical properties of La₂O₃ and

HfO₂/La₂O₃ gate dielectrics for germanium metal-oxide-semiconductor devices,” *J. Appl. Phys.*, vol. 103, pp. 014506 (2008).

[8-18] C. Andersson, C. Rossel, M. Sousa, D.J. Webb, C. Marchiori, D. Caimi, H. Siegart, Y. Panayiotatos, A. Dimoulas, and J. Fompeyrine, “Lanthanum germanate as dielectric for scaled Germanium metal–oxide–semiconductor devices,” *Microelectronic Engineering*, vol. 86, pp. 1635 (2009).

[8-19] K. Prabhakaran F. Maeda, Y. Watanabe, and T. Ogino, “Distinctly different thermal decomposition pathways of ultrathin oxide layer on Ge and Si surfaces,” *Appl. Phys. Lett.*, vol. 76, pp. 2244 (2000).

[8-20] F. Stern and W. E. Howard, “Properties of Semiconductor Surface Inversion Layers in the Electric Quantum Limit,” *Phys. Rev.*, vol. 163, pp. 816 (1967).

[8-21] C. H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita and A. Toriumi, “Record-high Electron Mobility in Ge n-MOSFETs exceeding Si Universality,” *IEEE IEDM Tech. Dig.*, pp. 457 (2009).

Publications and Presentations

Publications

1. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Characteristics of Ultrathin Lanthanum Oxide Films on Germanium Substrate: Comparison with Those on Silicon Substrate,” *Jpn. J. Appl. Phys.*, Vol. 46, No. 16, pp. L376, 2007.
2. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Improvement of interfacial properties with interfacial layer in La₂O₃/Ge Structure,” *Microelectronic Engineering*, Elsevier, vol. 84, pp. 2336, 2007
3. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Effect of Ultrathin Si Passivation Layer for Ge MOS Structure with La₂O₃ Gate Dielectric,” *ECS Transactions*, vol. 16, pp.285, 2008.
4. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Post metallization annealing study in La₂O₃/Ge MOS structure,” *Microelectronic Engineering*, Elsevier, vol. 86, issue. 7-9, pp. 1638, 2009.

International Presentations

1. **J. Song**, A. Fukuyama, K. Kakushima, P. Ahmet, K. Tsutsui, T. Hattori, H. Iwai “Characteristics of La₂O₃/Ge MIS Capacitors on Annealing Condition” *The E-MRS 2006 Spring Meeting*, T9-05, Nice, France, May, 2006.

2. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Improvement of interfacial properties with interfacial layer in La₂O₃/Ge Structure,” Insulating Films on Semiconductors (INFOS) 2007, session 7-24, Athens, Greece, June, 2007.
3. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Effect of Ultrathin Si Passivation Layer for Ge MOS Structure with La₂O₃ Gate Dielectric,” ECS 214th Meeting, Abs. #1945, Hawaii, USA, Oct, 2008.
4. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Post metallization annealing study in La₂O₃/Ge MOS structure,” Insulating Films on Semiconductors (INFOS) 2009, session 11a, Cambridge, UK, July, 2009.
1. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Effect of Ultrathin Si Passivation Layer for La₂O₃/Ge MOS structure,” G-COE Int. Symposium, P-27, Tokyo, Japan, 2009.

Domestic Presentation

1. **J. Song**, A. Fukuyama, K. Kakushima, K. Tsutsui, H. Iwai, “Characteristics of La₂O₃/n-Ge(100) MIS Capacitors,” 66th *Japan Society of Applied Physics (JSAP) Autumn Meeting*, Tokushima University, Japan, September, 2005
2. **J. Song**, A. Fukuyama, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “XPS Analysis of La₂O₃/n-Ge(100) Interface on Annealing,” 53rd *Japan Society of Applied Physics (JSAP) Spring Meeting*, 23p-V-14, Musashi Institute of Technology, Japan, March, 2006
3. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, H. Iwai, “Electrical Characterization of La₂O₃/Ge MIS capacitor,” Semiconductor Technology Academic Research Center (STARC) *Symposium 2006*, B-21, Yokohama, Japan, September, 2006.
4. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Improvement of interfacial properties with interfacial layer growth in La₂O₃/Ge

structure,” *54th Japan Society of Applied Physics (JSAP) Spring Meeting*, 29p-ZH-18, Aoyama Gakuin University, Japan, March, 2007.

5. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, H. Iwai, “Improvement of electrical characteristics of La₂O₃/Ge MOS structure with surface passivation of Ge substrate,” *Semiconductor Technology Academic Research Center (STARC) Symposium 2007*, B-35, Osaka, Japan, September, 2007.

6. **J. Song**, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “The effect of ultrathin interfacial Si layer insertion on electrical characteristics of La₂O₃/Ge MIS structure,” *68th Japan Society of Applied Physics (JSAP) Autumn Meeting*, 7p-ZM-13, Hokkaido Institute of Technology, Japan, September, 2007.

7. **J. Song**, K. Tachi, K. Okamoto, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Electrical characterization of high-k/Si MOS structure with interfacial La-silicate layer,” *55th Japan Society of Applied Physics (JSAP) Spring Meeting*, 28p-H-20, Nihon University, Japan, March, 2008.

8. **J. Song**, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Electrical characterization of high-k/Si MOS structure with interfacial La-silicate layer,” *56th Japan Society of Applied Physics (JSAP) Spring Meeting*, 31p-S-5, University of Tsukuba, Japan, March, 2009.

Patents

1. Under Pending

“Ge channel Device and its Fabrication Method”

Hiroshi Iwai, Takeo Hattori, Kazuo Tsutsui, Kuniyuki Kakaushima, Parhat Ahmet,

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