

Master Thesis

2010

**Electrical Characteristics of Rare Earth
(La, Ce, Pr and Tm)
Oxides/Silicates Gate Dielectric**

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1.1. Background of this study

In recent years, Information Technology society developed dramatically, for example the tremendous growing population of using internet, mobile phone, car navigation and many kinds of so called “IT products”. There is no doubt that the progress of recent Information Technology is realized by the improvement of the electronics, especially by the Silicon based Large Scale Integrated (LSI) circuits technology. The improvement of LSI has been achieved by the downsizing of its components such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Because of the downsizing, capacitance of the components reduces, resulting in high-speed, high-frequency and low power operation of the circuits. Of course, size reduction and high-integration of the circuits can be also realized at the same time with the performance improvement. Gordon Moore who is one of the founder of Intel Corporation, predicted that exponential growth in the number of transistors per integrated circuit and predicted this trend would continue, in a popular article written in 1965[1]. This law notes that the device feature size decreases each year and the number of transistors on a LSI doubled every two years. This simple statement is the foundation of semiconductor and computing industries. The International Technology Roadmap for Semiconductor (ITRS) [2] defines how the device parameters are scaled for the next technology node.

1.2. Scaling Method of MOSFETs

The downsizing of the components has been accomplished by the scaling method [3]. In the electrical design of modern CMOS transistor, the power-supply voltage is reduced with the physical dimension in some coordinated manner. A great deal of design detail goes into determining the channel length, or separation between the source and drain, accurately, maximizing the on current of the transistor while maintaining an adequately low off current, minimizing variation of the transistor characteristics with process tolerances, and minimizing the parasitic resistances and parasitic capacitances [4]. To make circuit speed up, devices dimensions and the power-supply voltage must be scaled down. Figure 1.1 and Table 1.1 shows the schematic model of MOSFET constant-electric-field scaling by the same factor S .

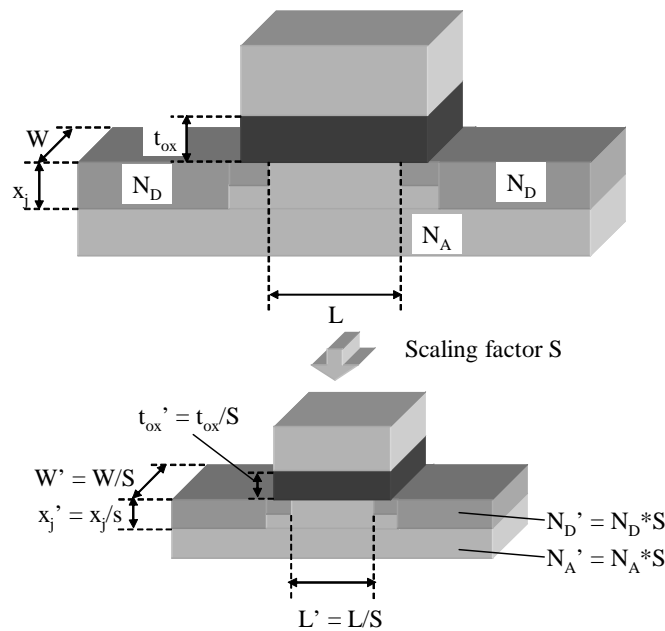


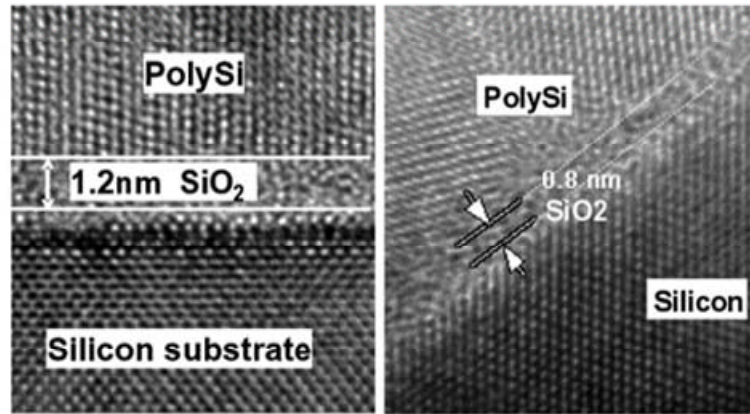
Figure 1.1 Scaling method

Table 1.1 Scaling of MOSFET by a scaling factor of S.

<i>Quantity</i>	<i>Before scaling</i>	<i>After scaling</i>
Channel length	L	$L' = L/S$
Channel width	W	$W' = W/S$
Device area	A	$A' = A/S^2$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Gate capacitance per unit area	C_{ox}	$C_{ox}' = S * C_{ox}$
Junction depth	x_j	$x_j' = x_j/S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0}/S$
Doping densities	N_A	$N_A' = S * N_A$
	N_D	$N_D' = S * N_D$

1.3. Scaling Limits of SiO₂

According to Moore's law, SiO₂ gate film has become thin, however extremely thin gate oxide has large leakage current caused by direct-tunneling current. Now the thickness of SiO₂ reached sub-1nm. This thickness corresponds to 3 layers of atoms (fig. 1.2). The thickness of gate oxide and other physical sizes are downsized along with ITRS roadmap, from this roadmap, Equivalent oxide thickness (EOT) was required to be reduced to 0.5 nm in near future (Table.1.2 and fig.1.3).



- **1.2nm physical SiO₂ in production (90nm logic node)**
- **0.8nm physical SiO₂ in research transistors**

Figure 1.2 TEM cross section micrographs of polysilicon/SiO₂/Si with SiO₂ thickness of 1.2 nm and 0.8 nm, respectively.

Table 1.2. International Technology Roadmap for Semiconductors (2009).

Year	2009	2011	2013	2015
Physical Gate Length (nm)	29	24	20	17
EOT(nm)	1	0.88	0.65	0.53
Gate Leakage Current Density(A/cm ²)	0.65	0.9	1.1	1.3

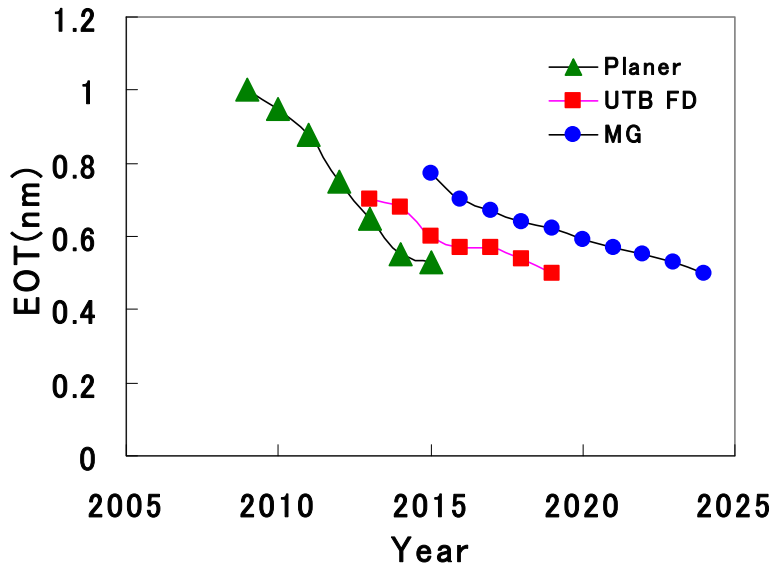


Figure 1.3 EOT scaling road map of various structures MOS transistors (ITRS2009).

However, as transistor geometries scale to the point where the traditional SiO_2 gate dielectric film becomes just a few atomic layers thick, direct tunneling current leakage and the resulting increase in power dissipation and heat become critical issues. In the case of conventional SiO_2 gate dielectrics, the leakage current of 100 A/cm^2 flows through 1 nm thick SiO_2 as shown in Fig.1.4[5,6].

So, new materials for gate oxide, gate metal, and substrate and new structure MOS devices are eagerly studied.

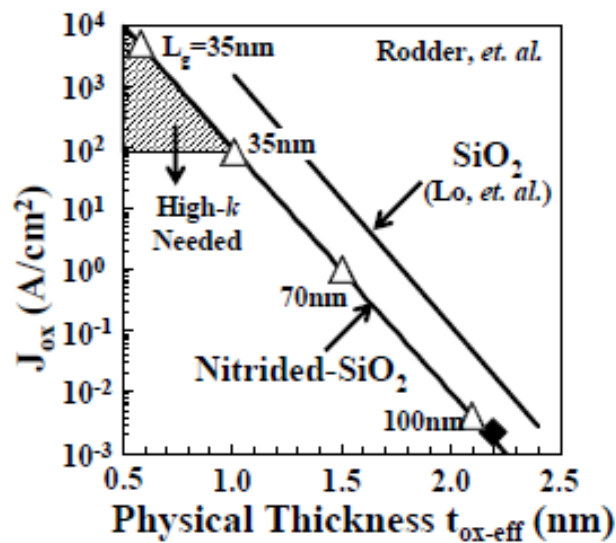


Figure 1.4 Gate leakage current vs. EOT for SiO_2 and nitrided SiO_2 .

1.4. Introduction of High-k Materials

To overcome this problem, high-k (high-dielectric constant) materials have been attracted much attention. Replacing conventional SiO₂ with high-k materials for gate insulator, the required physical gate thickness for the same EOT becomes thicker, and thus, the leakage current could be suppressed. Figure 1.5 represents the schematic description of differences between the cases using SiO₂ and high-k material for gate insulator.

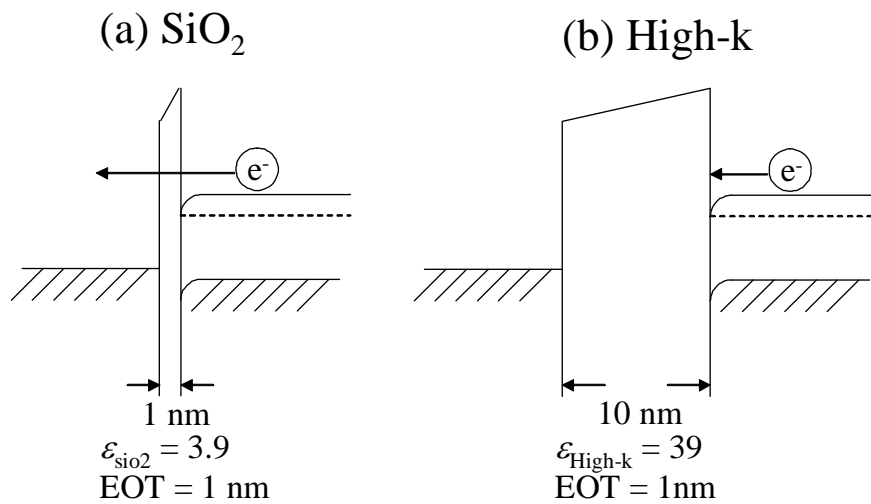


Figure 1.5 Schematic description of differences between the cases using (a) SiO₂ and (b) High-k for the gate insulator in MIS structure.

Therefore, we must find alternative materials for gate oxide, high-k materials which has larger relative dielectric constant introduction is effective materials for further scaling. There are many high-k materials studied for gate oxide such as HfO₂, Al₂O₃, La₂O₃ and so on. The above requirement is that dielectric constant should be preferably 25~30, a very high dielectric constant is undesirable. Because there is the trade off between dielectric constant and band offset, which requires a reasonably large band gap. Figure 1.6 [7] shows the dielectric constant of candidate oxides tends to vary inversely with the band gap.

Figure 1.7 shows a recent trend of high-k reports which had been reported in VLSI symposium and IEDM symposium. Among the candidate high-k materials, Hf-based materials are the most promising candidate.

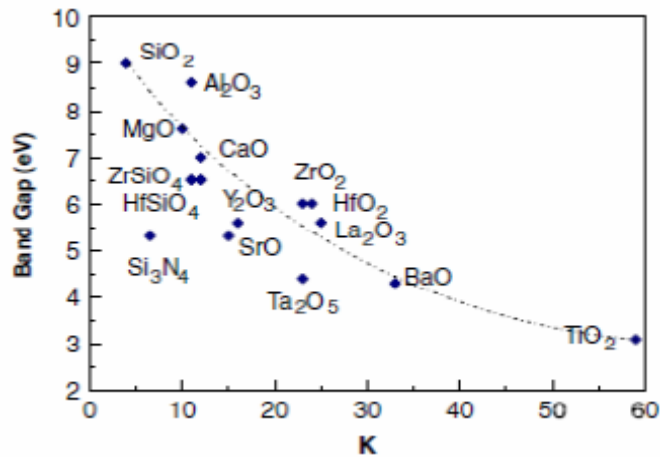


Figure 1.6 Band gap vs. dielectric constant plot of various high-k materials studied for gate insulator.

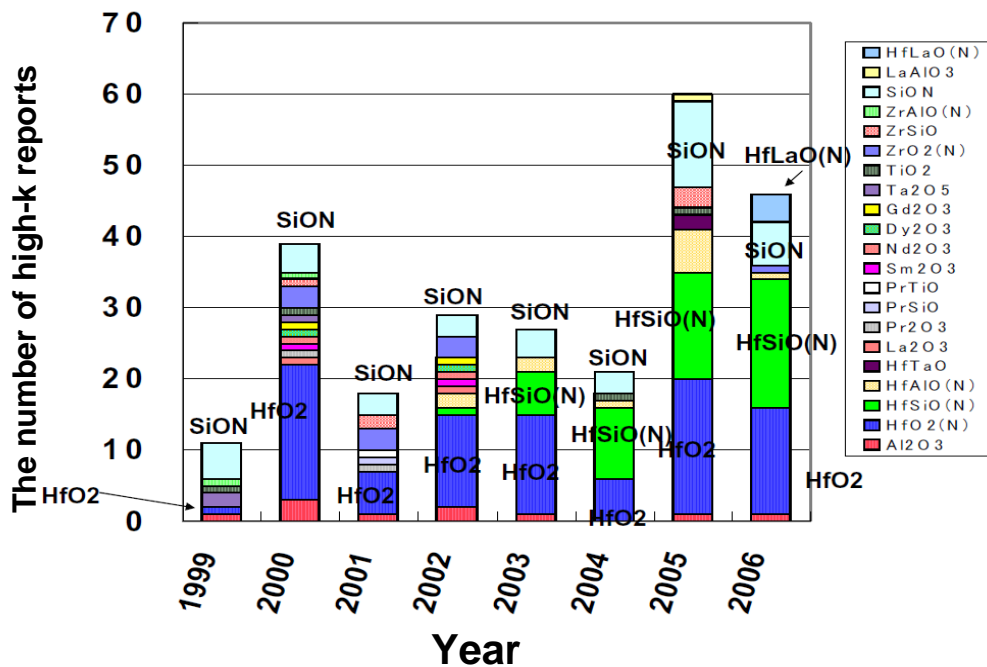


Figure 1.7 Recent trend of high-k reports which had been reported in VLSI symposium and IEDM symposium.

1.5. Issue of High-k Materials

Today, high-k materials are not only subject of research, but also practical application. Intel Corps has released the first group to use the Hf-based high-k material in 2007. However, high-k MOSFET has large obstacles to overcome though eager study for high-k has been continued. For example difficulty in controlling threshold voltage and thermal endurance carrier mobility problems were one of the main issues of high-k MOSFET. Generally, a thin layer of SiO₂ or SiON layer with a thickness ranging from 0.5 to 0.7 nm is inserted as an interfacial layer (IL) beneath high-k layer to overcome the issue. Popular structure of Hf-based materials is shown in fig. 1.8 [8], to realize good interface quality SiO(N) interfacial layer (IL) was inserted at the Si interface. Fig. 9 shows the leakage current density versus EOT plot for both SiO₂ and HfSiON/SiO₂ gate stack.

However, to achieve 0.5 nm EOT which is the ultimate specification in ITRS roadmap, high-k should be directly contacted on Si substrate and SiO₂ IL should be removed. Indeed 0.5 nm EOT gate stack with HfSiO(N)/Si [9] without IL was reported, the number of reports which study sub-0.5 nm gate stack has not been enough. Figure 1.12 shows 0.5 nm MOS structure reported in IEDM 2007. This MOS structure realized high-k/Si directly contacted interface, however fabrication process of this MOS transistor was complex. In addition, Hf-based materials have large V_{th} even n-metals are used as gate metal, so especially for n-MOSFET, proper choice of gate metal has been eagerly studied. Recent research shows that not only gate metal choice but also high-k choice is the key to realize low V_{th} n-MOSFET. Rare earth oxides such as La₂O₃, Sc₂O₃ are remarked because they could reduce high V_{th} .

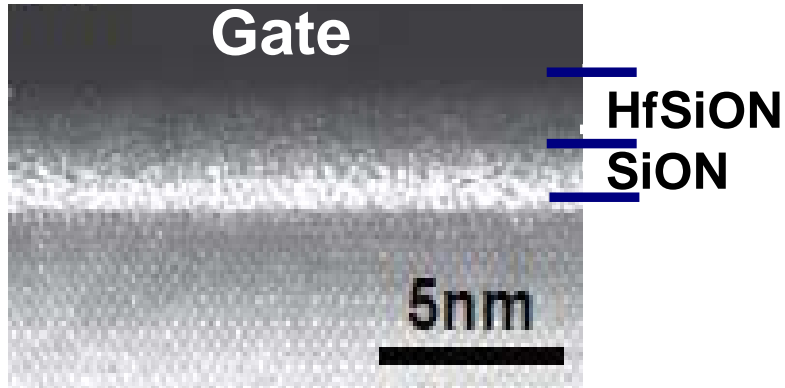


Figure 1.8 Hf-based MOS structure [10]; To realize good interface quality SiO(N) interfacial layer (IL) was inserted at the Si interface.

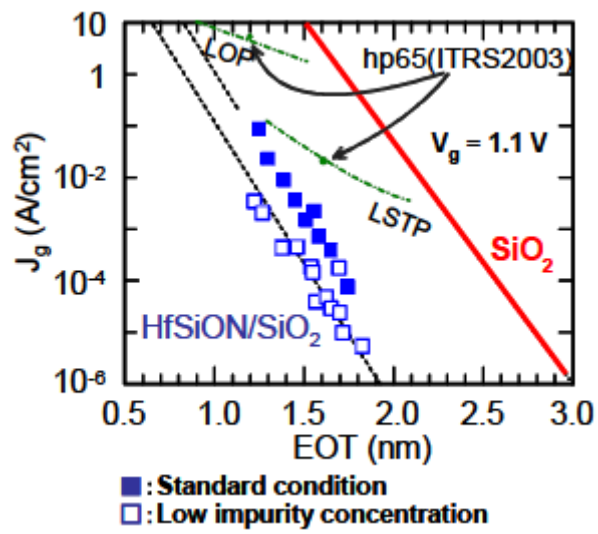


Figure 1.9 Leakage current density versus EOT plot for SiO₂ and HfSiON/SiO₂.

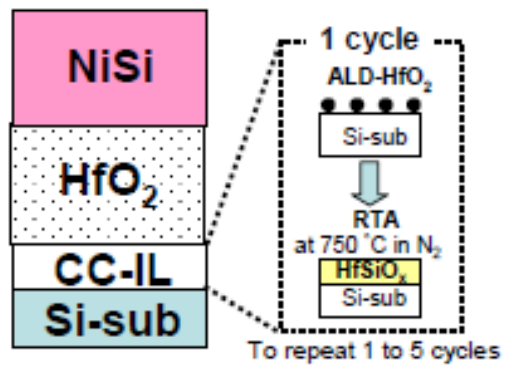


Figure 1.10 0.5 nm MOS structure reported in IEDM 2007 [11]; high-k/Si directly contacted interface could be realized.

1.6. Rare Earth Oxides as Gate Dielectric

It has reported that Hf-based films have reduced scattering when a SiO₂-based interfacial layer of 0.5 to 0.7 nm is inserted, however, this attempt increases the EOT. To achieve an EOT down to 0.5 nm, which is the ultimate specification in ITRS roadmap [2], the high-k layer should be directly contacted on the Si substrate. Usually, when the EOT becomes small, the effective mobility tends to decrease due to scattering in the high-k layer or at the interface between the high-k layer and the substrate. It is reported the directly contact in Hf-based oxide is achieved by a choice of proper metal electrode, improving effective mobility and reliability is necessary.

On the other hand, rare earth (RE) oxides which have large dielectric constant react with Si to form RE-silicate by annealing [10]. RE-silicate layers generally have dielectric constants more than 8, so that a directly contact structure can be easily achieved. There are some rare earth metal oxides like La₂O₃, Pr₂O₃ and so on.

These materials are expected to suit for gate insulators of MOSFETs. However, mobility degradation of MOSFETs with La₂O₃/La-silicate in EOT below 0.5 nm has been one of the major issues [11]. The degradation is caused by fixed charges in high-k, and the correlation with a shift in flat band voltage is known. Therefore, another method to reduce the fixed charges is required. Another RE oxides which CeOx, PrOx, and TmOx were used for overcome that issue.

La based materials are also remarked for next generation gate oxide thanks to its advantage of leakage current, which means that La based materials can realize smaller EOT. Figure 1.11 shows the MOS structure with LaAlO₃ which achieve 0.3 nm EOT in gate last process.

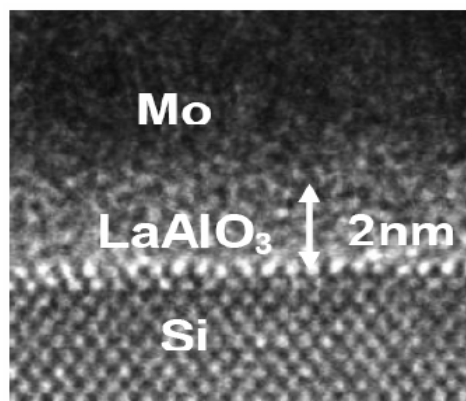


Figure 1.11 0.3 nm EOT MOS structure with LaAlO₃ which was reported in IEDM 2005.

Candidates ■

● Gas or liquid at 1000 K
○ Radio active

● Unstable at Si interface

●	H	① Si + MO _x → M + SiO ₂										●	B	C	N	O	F	Ne			
●	Li	Be	② Si + MO _x → MSi _x + SiO ₂										●	B	C	N	O	F	Ne		
○	Na	Mg	③ Si + MO _x → M + MSi _x O _y										●	Al	Si	P	S	Cl	Ar		
○	K	Ca	Sc	②	①	①	①	①	①	①	①	①	①	①	●	As	Se	Br	Kr		
●	Rh	Sr	Y	Zr	①	①	①	①	①	①	①	①	①	①	●	In	Sn	Sb	Te	I	Xe
●	Cs	Ba	★	Hf	①	①	①	①	①	●	Pt	Au	Hg	●	Tl	Pb	Bi	Po	At	Rn	
○	Fr	Ra	★	Rf	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
★	La	Ce	Pr	Nd	○	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu					
★	Ac	Th	Pa	U	○	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr					

Table 1.3 Candidates for the metal, oxide of which has possibility to be used as high-k gate insulator on periodic table.

Table 1.4 Physical properties for various high-k materials.

	SiO ₂	Si ₃ N ₄	Al ₂ O ₃	La ₂ O ₃	HfO ₂	ZrO ₂
Contact stability with Si (kJ/mol) Si+MO _x →M+SiO ₂	stable	stable	+63.4	+98.5	+47.6	+42.3
Bandgap (eV)	9.0	6.0	8.8		5.7	5.2-7.8
Structure type	amorphous	amorphous	amorphous	amorphous	crystal T>700 °C	crystal T>400 - 800 °C
Effective K value	3.9	7.0	8.5-10	~25	~25	~25

1.7. Purpose of this study

To overcome those issues there is a possibility of improving the interface properties by combining RE-silicate and RE oxides. Table 1.3 shows Specifics of RE (La, Ce, Pr and Tm) oxides/silicates. In this report, the dependence of flat band voltage (V_{fb}) shift on EOT of MOS capacitors with RE (La, Ce, Pr and Tm) oxides/silicates were investigated.

Table 1.5 Physical properties for La_2O_3 , CeO_x , PrO_x and TmO_x .

	La_2O_3	CeO_x	PrO_x	TmO_x
K value	27	38	13	13
Bandgap[eV]	5.4	0.72	3.9	5.0

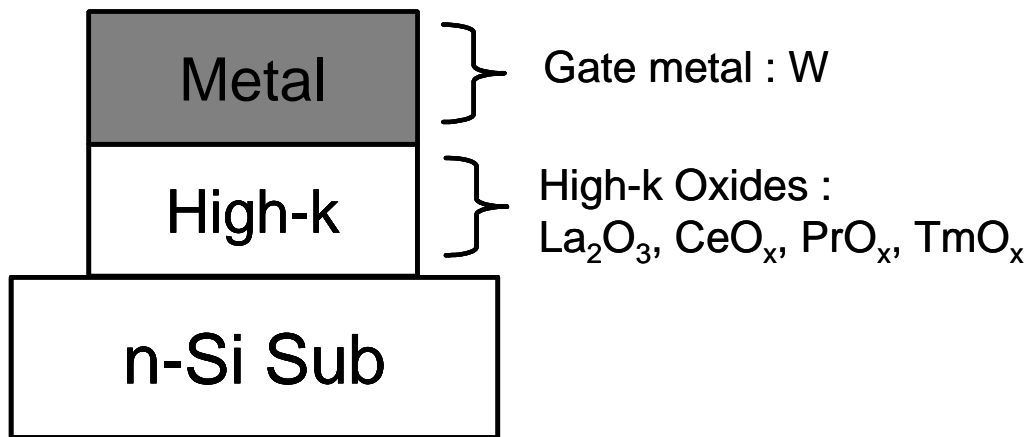


Figure 1.16 MOS structure in this study. Various materials were used.

1.8. Reference

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2.1. Introduction

In this chapter, detail fabrication steps on MOS capacitors (MOSCAPs) will be discussed. The principles of measurement and the experiment instruments such as electron beam epitaxy and RF sputtering are also shown.

2.2. Fabrication Procedure for MOS Capacitors

Figure 2.1 shows the fabrication process flow of high-k gated MOS capacitors. High-k dielectrics were deposited on a 300-nm-thick SiO₂ isolated n-Si(100) wafer with thermally grown interfacial oxide layer (IL) with a thickness of 3.5 nm. La₂O₃, CeO_x, PrO_x and TmO_x were deposited by electron beam evaporation. Substrate temperature during depositing was set to 300 °C and the deposition rate of high-k was controlled to be 0.3 nm/min. After high-k deposition, 60 nm-thick tungsten (W) was *in-situ* deposited using sputtering without exposing the wafers to air in order to avoid any moisture or carbon-related contamination absorption. W was patterned by reactive ion etching (RIE) using SF₆ chemistry to form gate electrode for MOS capacitors. Wafers were then post-metallization annealed (PMA) using a rapid thermal annealing (RTA) furnace in forming gas (F.G) (N₂:H₂=97%:3%) ambient at 500 °C for 30 min. Backside Al was deposited as a bottom electrode by thermal evaporation. Capacitance-voltage (C-V) characteristics of MOS capacitors were measured at 100 kHz and 1 MHz using Agilent 4284A precision LCR meter. The thickness of IL is chosen to be sufficient to avoid any formation of oxygen vacancy in high-k. Moreover, as the annealing temperature studied in this work is below 500 °C, the Fermi level pinning effect on V_{fb} can be neglected.

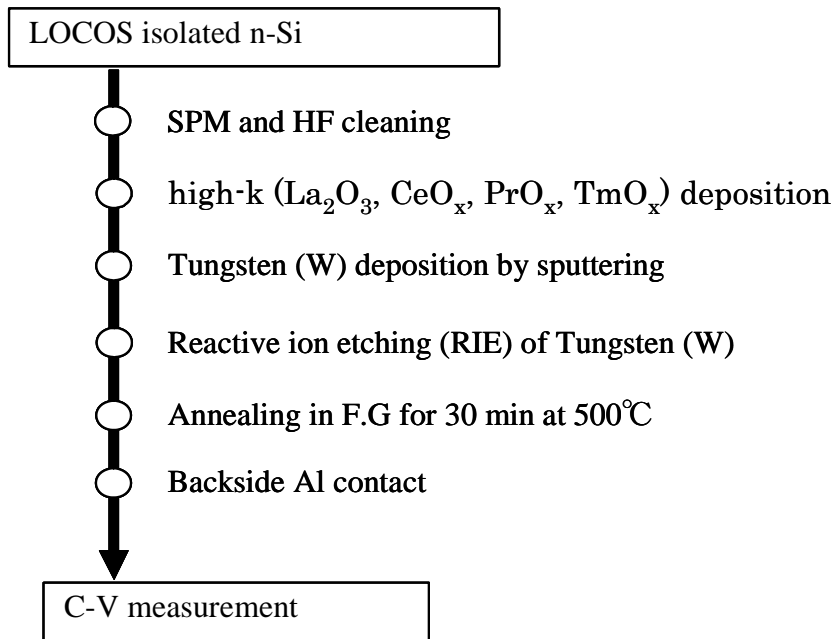


Figure 2.1 Fabrication process flow of high-k gated MOS capacitors

2.3. Instrument used in Fabrication Process

2.3.1. Wet Cleaning

For deposition of thin film maintaining the quality requires quite clean surface of Si substrate. There are many method of cleaning substrate. But one of the most used methods is wet cleaning by chemical liquid. There are some kinds of the liquids which are used in wet cleaning process shown in Table 2.1. And these liquid have each effect against substrate pollutions. So, one liquid can't eliminate all pollutions. In this Study, I used the process like fig.2.2 First step is SPM Cleaning ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=4 : 1$) eliminates metal and organic materials. And then, the native or chemical oxide was removed by diluted hydrofluoric acid ($\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:100$).

Table 2.1 Main Cleaning Process

The name of Cleaning	Chemical liquid	The Characteristic
APM Cleaning	$\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$	The effect of elimination against organic materials and particles
FPM Cleaning	$\text{HF}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$	The effect of elimination against metal and oxidation layer
HPM Cleaning	$\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$	The effect of elimination against metal
SPM Cleaning	$\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$	The effect of elimination against metal and organic materials
DHF Cleaning	$\text{H}_2\text{O}_2/\text{H}_2\text{O}$	The effect of elimination against metal and oxidation layer
BHF Cleaning	$\text{HF}/\text{NH}_4\text{F}/\text{H}_2\text{O}$	The effect of elimination against oxidation layer

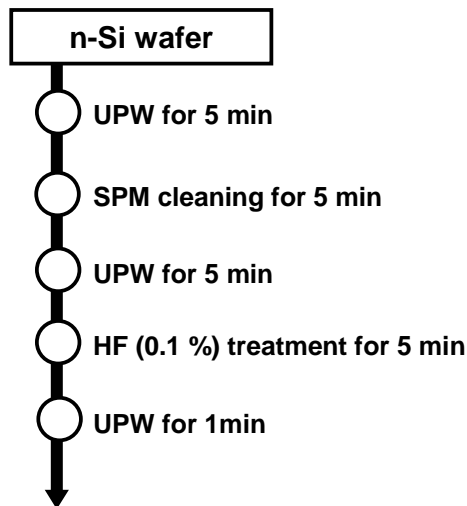


Figure 2.2 Wet cleaning process of MOS capacitors and MOS transistors used in this study

2.3.2. Molecular Beam Epitaxy (MBE)

As discussed and reported in various literatures, there are many ways to deposit high-k dielectric films on Si substrate. Various deposition methods have been proposed. These include MOCVD, LPCVD, ALD, PLD and e-beam evaporation. In this study, e-beam evaporation method was adopted. High-k materials were deposited in ultra high vacuum chamber as shown in figure 2.3. There are four compartments to allocate same/difference solid sources at the bottom of the chamber. La_2O_3 , CeO_x , PrO_x and TmO_x were placed there and subsequently heated by the e-beam which was located near the each high-k source. The electron beam was controlled by a magnetic sweep controller, and the power of the beam is set to be 5 kV. The base pressure inside growth chamber is maintained at 10^{-8} Pa by TMP, when high-k was deposited the pressure inside the chamber increased to 10^{-7} Pa. Then, since the chamber is maintained at the ultra high vacuum state, the La_2O_3 molecule begins to evaporate when the temperature is reported as 3620 °C. In deposition, the physical thickness of each high-k film was measured by crystal oscillator and the sample folder was rotated. Deposition rate was set to be 0.3 nm/s, the rate was important for the film quality. Too fast deposition rate made the quality worse than slow deposition rate.

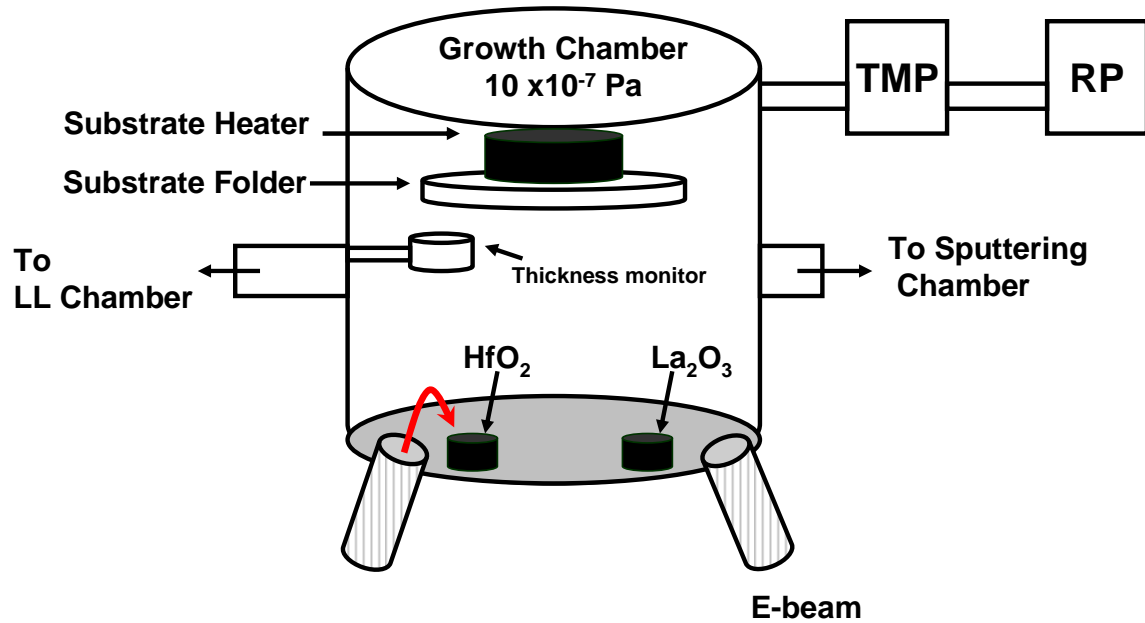


Figure 2.3 Schematic model of molecular beam epitaxy (MBE)

2.3.3. RF Sputtering

In this experiment, gate metals W was deposited using RF sputtering. The base pressure of sputtering chamber was maintained to be 10^{-7} Pa by TRP and RP (shown in Fig.2.4). In sputtering, Ar was flowed into the chamber and the pressure of which was set to be 10^{-4} Pa, the AC current power was 150W.

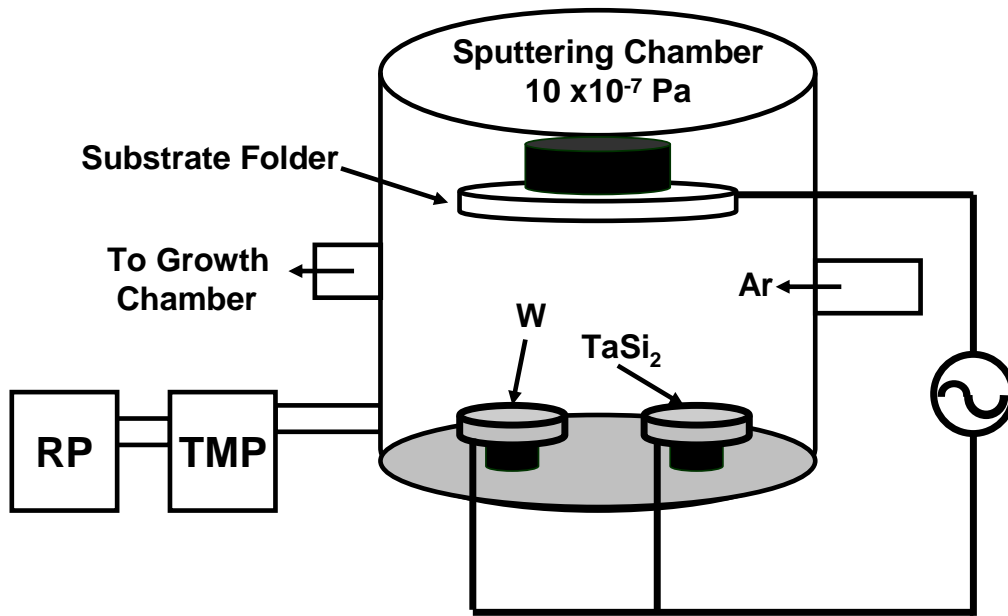


Figure 2.4 Schematic model of RF Sputtering

2.3.4. Photolithography

The process flow of photolithography that used throughout this study is shown in Figure 2.5. An electrical hotplate is used for baking purposes. The spin-coated layer photoresist was aligned and exposed through tungsten coated e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. MJB4 of Karl Suss contact-type mask aligner as shown in Figure 2.6 was used for aligning and exposure purposes. The exposure duration was set to 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.) after dipping into the solvent for 2 minutes and baked at 130 °C for 5 minutes.

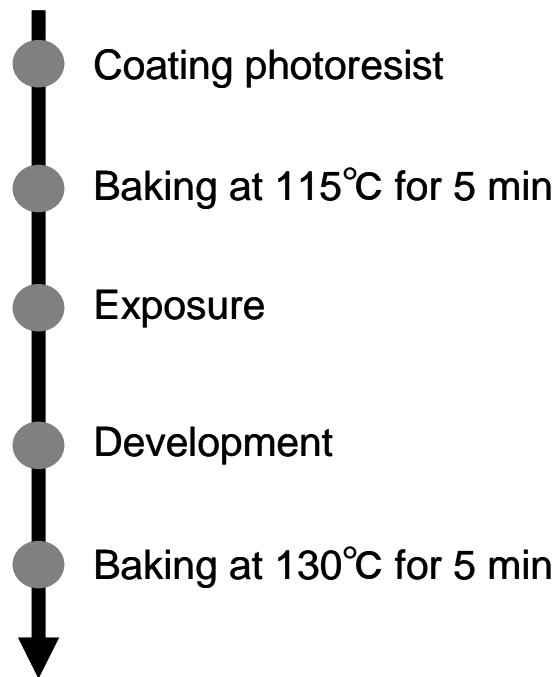


Figure 2.5 The process flow of photolithography

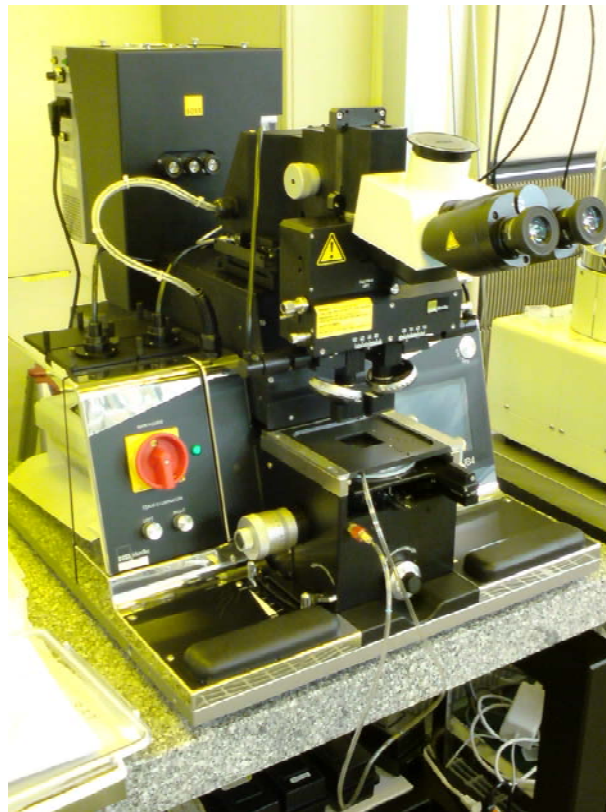


Figure. 2.6 Photo of mask aligner

2.3.5. Reactive Ion Etching (RIE)

Reactive Ion Etching (RIE) which uses one of chemical reactive plasma to remove materials deposited on wafers was adopted to etch gate electrode in this study. There are two electrodes in vacuum chamber (shown in fig. 2.7). One is usually connected to ground and gas is put into the chamber and exits to the pump, in this study SF₆ and O₂ are used to remove gate W and resist each. And plasma is generated and ion direct for substrate and remove gate electrode and resist chemically.

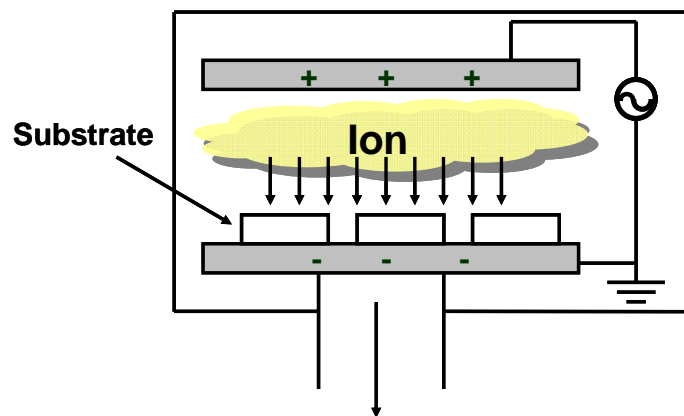


Figure 2.7 Schematic illustration of Reactive Ion Etching (RIE).

2.3.6. Rapid Thermal Annealing (RTA)

Thermal annealing processes (shown in fig. 2.8) are often used in modern semiconductor fabrication for defects recovery, lattice recovery and impurity electrical activation of doped or ion implanted wafers. In this study, MOS capacitors were post metallization annealed after gate electrode deposition.

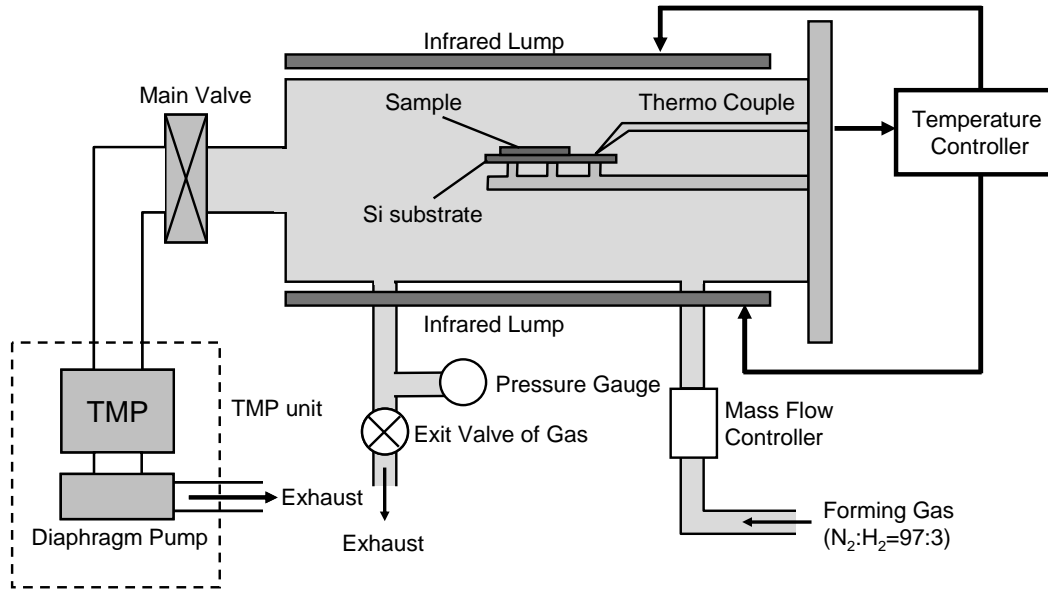


Figure 2.8 schematic image of infrared annealing furnace

2.3.7 Vacuum Thermal Evaporation Method

All of Al metals in this work were obtained from deposition with bell jar vacuum thermal evaporation shown as Figure. 2.9 and 2.10 illustrates a schematic drawing for vacuum thermal evaporation system. Filament is made of tungsten, was used for heating the Al source up to its vapor temperature. Both filaments and Al sources are made of Nilaco, inc. with material purity of 99.999%.

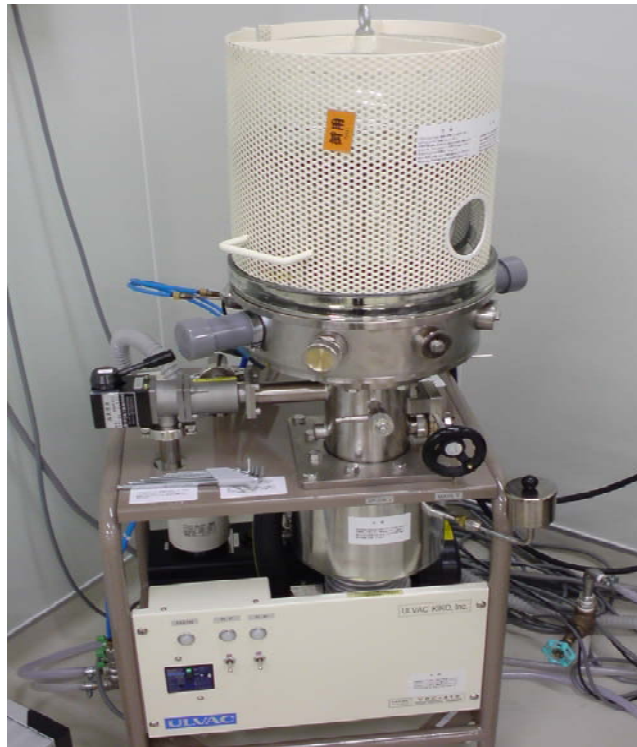


Figure. 29 Photo of bell jar

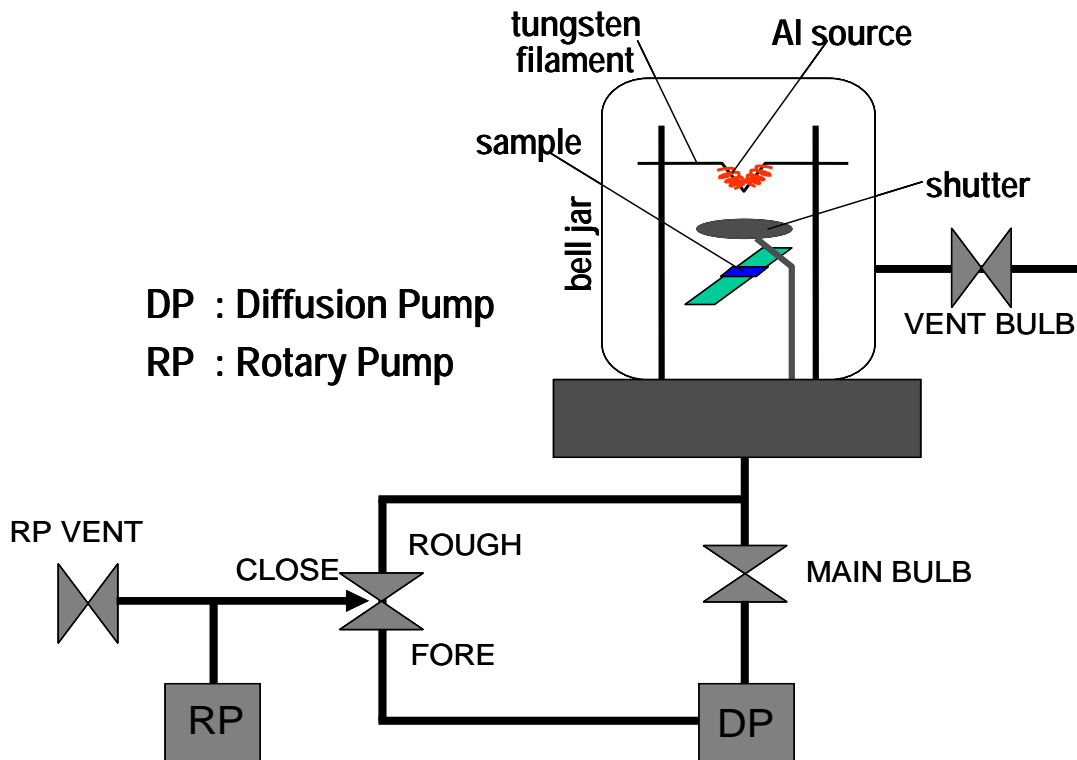


Fig. 2.10 Schematic drawing for vacuum thermal evaporation system.

The physics of vacuum thermal evaporation is based on thermodynamics of the evaporated materials. There have been experiments performed for evaluating the thermodynamic properties of material. Careful evaluation may reveal that the vapor pressure of liquid Al is given by the following.

$$\log P_{\text{torr}} = \frac{15,993}{T} + 12.409 - 0.999 \log T - 3.52 \times 10^{-6} T \quad (3.1)$$

Neglecting the last two terms, the Arrhenius character of log P vs. 1/T can be essentially preserved. Two modes of evaporation can be distinguished in practice, depending whether the vapor effectively emanates from liquid or solid source. Usually, a melt will be required if the element in question does not achieve a vapor pressure greater than 10^{-3} torr at its melting point. Most metals, like Al, Ag, Au, and so on, fall into this category, and effective film deposition is attained only when the source is heated into the liquid phase. On the other hand, elements such as Cr, Ti, Mo, Fe, and Si reach sufficiently high vapor pressures of 10^{-2} torr some 500°C below the melting point.

2.4. Measurement Method

After fabricating MOS capacitors we measured electrical characteristics of those devices. In this study, we mainly focused on EOT, gate leakage current J_g and effective electron mobility m and interface states density D_{it} using various method. In this section the method to estimate each parameter is explained.

2.4.1. C-V measurement

Detail introduction of C-V and its basic operating principles will not be discussed. High frequency C-V measuring technique was used to evaluate the C-V curves in terms of frequency dependency (1 kHz – 1 MHz), magnitude of hysteresis, flatband voltage (V_{fb}) shift and EOT determination. In this study, C-V hysteresis was estimated from capacitance difference between forward and back ward sweeps at $V_g = V_{fb}$. V_{fb} shift is accurate determined by plotting $(1/C^2)$ versus V_g . The lower knee of this curve occurs at $V_g = V_{fb}$. Such a transition is sometimes difficult to determine due to distortion on initial C-V curve. Differentiating this curve and finding the maximum slope of the left flank of this differential curve a second time results in a sharply peaked curve whose peak coincide with V_{fb} . For comparison purposes, CVC program developed by North Carolina State University was also used to estimate EOT and V_{fb} and C-V curves are measured using Agilent 4284A precision LCR meter.

2.4.2. J_g -V measurement

The is done using HP4156A semiconductor analyzer with minimum measurement count 10 times for every samples to confirm proper distribution on leakage current density.

Chapter 3. Characteristics of MOS Capacitor

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3.1 Introduction

In this chapter, electrical properties of La_2O_3 , CeO_x , PrO_x and TmO_x structured MOS capacitor were investigated. By comparing each property, the effect of stacking was discussed.

3.2 Analysis of Leakage Current

For the investigation of Leakage Current, La_2O_3 , CeO_x , PrO_x and TmO_x single structured MOS capacitor were fabricated and measured. First of all, leakage mechanism in each sample was estimated.

3.2.1 Leakage Mechanism of Each Layered Capacitors

For estimated the leakage mechanism, the electrical properties of single layered capacitors at the all most same EOT value were investigated. The results were compared.

3.2.2 La-Oxide Single Layered Capacitor

First, the electrical properties of La_2O_3 single layered capacitor were investigated. Fabricated capacitor structure was shown in Fig. 3.1. Here, it's expected that the La-silicate was formed at the $\text{La}_2\text{O}_3/\text{Si}$ -substrate interface after annealing. It is expected that, if thickness is small, most of the La_2O_3 layer reacted with Si and formed La-silicate. EOT of this sample is about 1nm, it's so thin. Therefore, it's assumed that the La_2O_3 layer completely reacted with Si to forme La-silicate.

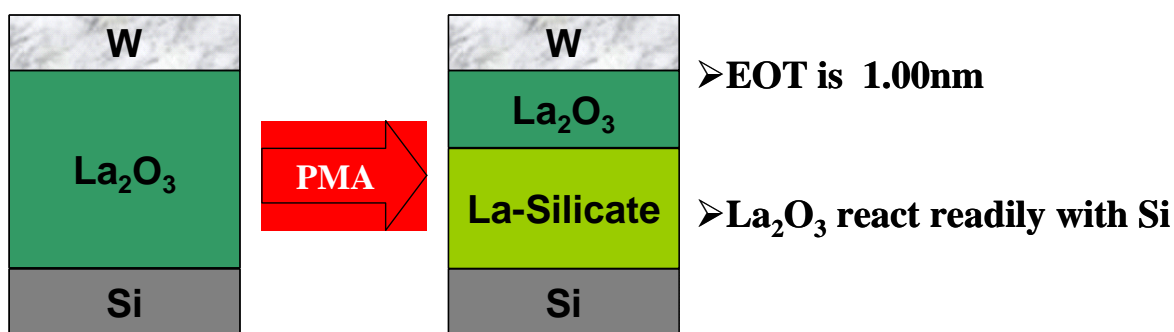


Fig. 3.1 fabricated La_2O_3 single layered capacitor structure

The J - V and C - V characteristics were measured. Those results were shown as Fig.3.2 (a),(b), respectively. From the C - V characteristics, the EOT was estimated to be 1.00 nm. The density of interface trap was low because of little hump in the C - V curve.

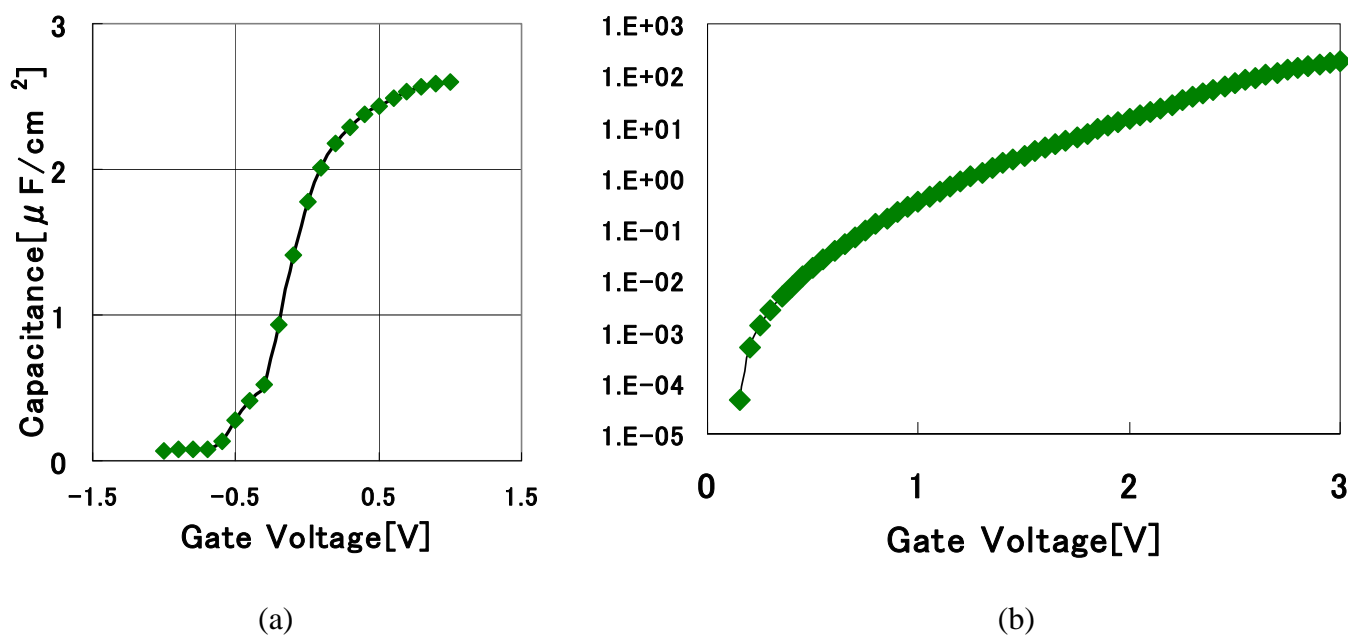


Fig. 3.2 La_2O_3 single layered capacitor (a) C - V characteristic, (b) J - V characteristic

3.2.3 Ce-Oxide Single Layered Capacitor

The electrical properties of CeO_x single layered capacitor were investigated. Fabricated capacitor was shown in Fig. 3.3. It's expected that the CeO_x layer completely reacted with Si to form Ce-silicate.

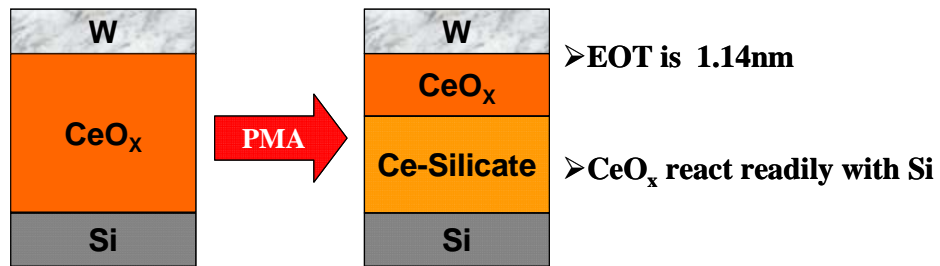


Fig. 3.3 fabricated CeO_x single layered capacitor structure

The J - V and C - V characteristics were measured. Those results were shown as Fig.3.4 (a),(b), respectively. From the C - V characteristics, the EOT and the dielectric constant were estimated to be 1.14 nm. A small hump in the C - V curve is due to the density of interface trap and a capacitance decrease at large gate voltage is due to large leakage current. From the leakage-current analysis, it was found that leakage current value in the CeO_x was not compared with other samples. Because, CeO_x has small band-gap and band-offset ($\sim 0.72\text{eV}$).

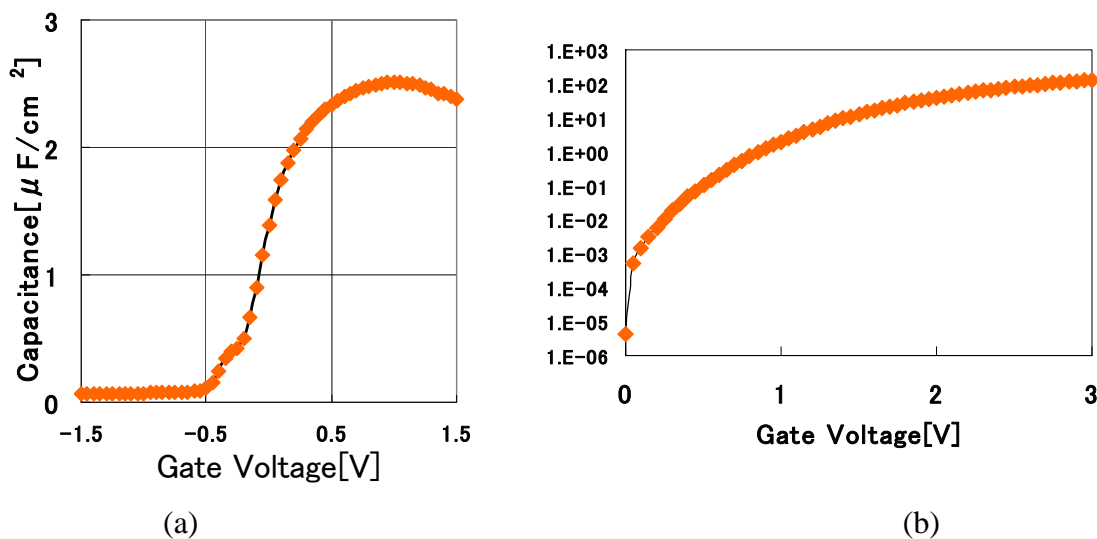


Fig. 3.4 CeO_x single layered capacitor (a) C - V characteristic, (b) J - V characteristic

3.2.4 Pr-Oxide Single Layered Capacitor

The electrical properties of PrO_x single layered capacitor were investigated. Fabricated capacitor was shown in Fig.3.5. It's expected that the PrO_x layer completely reacted with Si to form Pr-silicate.

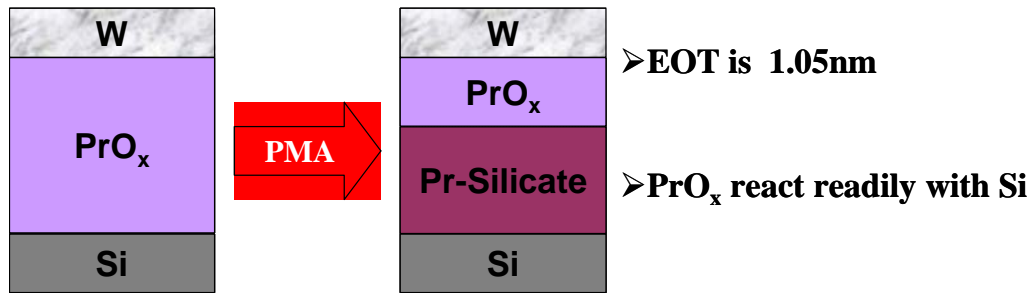


Fig. 3.5 fabricated PrO_x single layered capacitor structure

The *J-V* and *C-V* characteristics were measured. Those results were shown as Fig.3.6 (a),(b), respectively. From the *C-V* characteristics, the EOT and the dielectric was estimated to be 1.05 nm. A small hump in the *C-V* curve is due to the density of interface trap. From the leakage-current analysis, PrO_x was suppressed compare with the other samples.

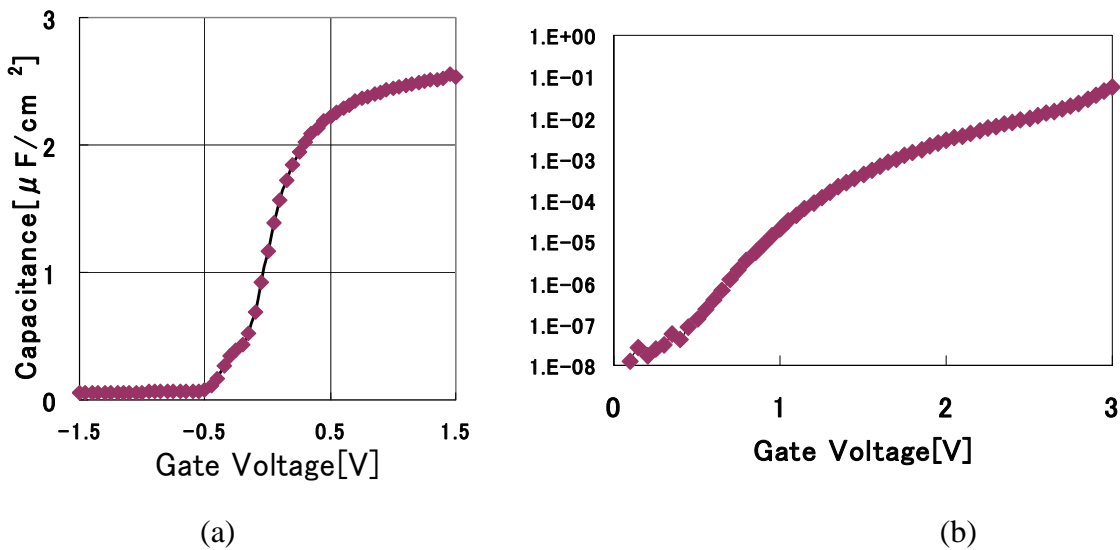


Fig. 3.6 PrO_x single layered capacitor (a) *C-V* characteristic, (b) *J-V* characteristic

3.2.5 Tm-Oxide Single Layered Capacitor

The electrical properties of TmO_x single layered capacitor were investigated. Fabricated capacitor was shown in Fig. 3.7. It's expected that the TmO_x layer completely reacted with Si to form Ce-silicate.

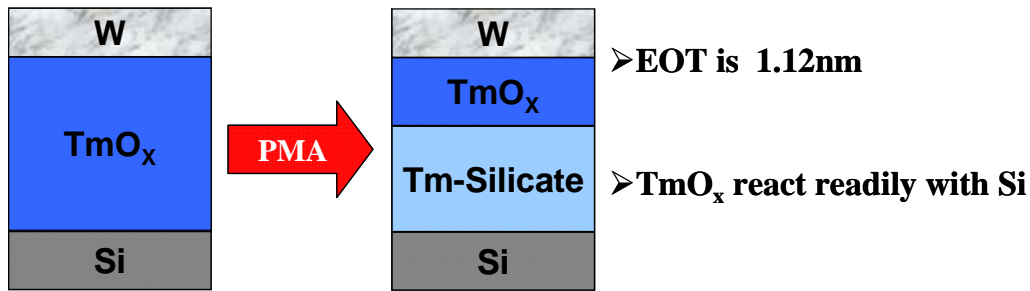


Fig. 3.7 fabricated TmO_x single layered capacitor structure

The J - V and C - V characteristics were measured. Those results were shown as Fig.3.2 (a),(b), respectively. From the C - V characteristics, the EOT and the dielectric constant were estimated to be 1.00 nm and 27. A small hump in the C - V curve is due to the density of interface trap and a capacitance decrease at large gate voltage is due to large leakage current. From the leakage-current analysis, TmO_x was suppressed by one order compare with La_2O_3 and CeO_x .

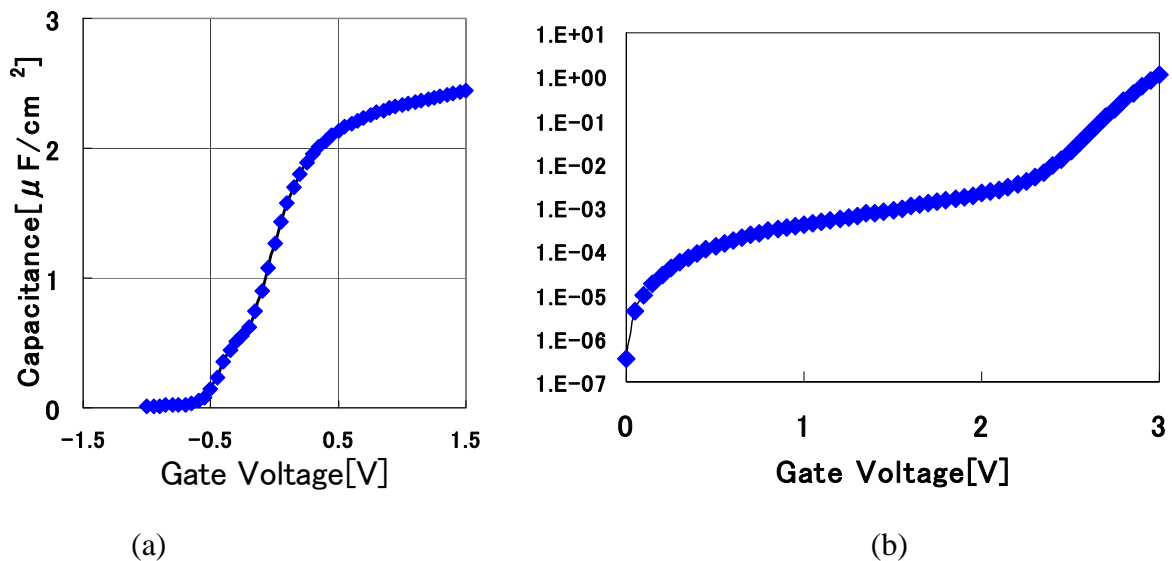


Fig. 3.8 TmO_x single layered capacitor (a) C - V characteristic, (b) J - V characteristic

Fig.3.9 shows the C - V characteristics of the single-layered structures at the same EOT which about 1 nm values. From the figure we can see that there are no differences about V_{fb} at EOT 1 nm. It' expected that oxygen supply in oxides bring flat band voltage to negative direction.

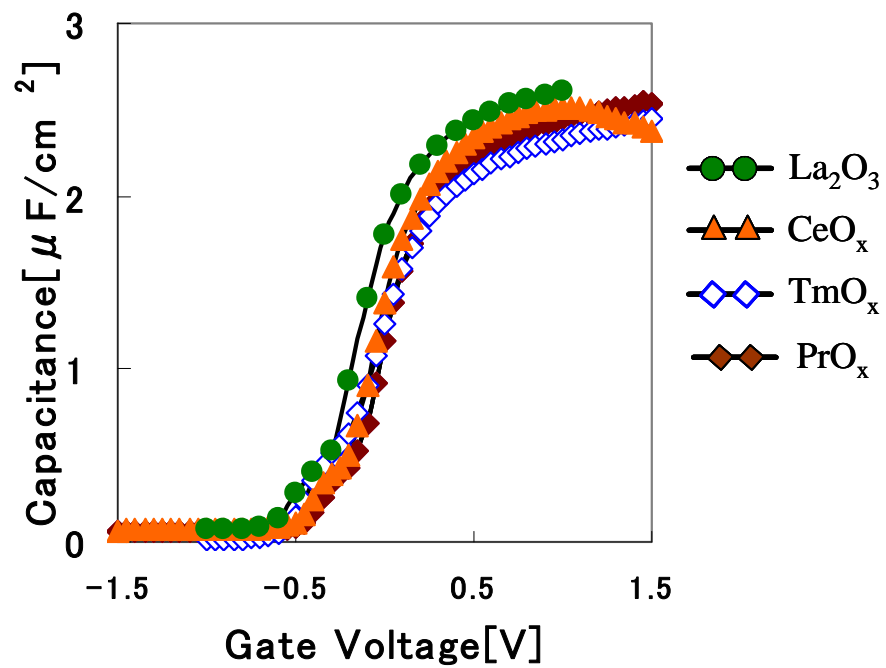


Fig. 3.9 Single layered capacitor C - V characteristic at the same EOT

3.3 Compared Leakage Current Value

Additionally, leakage current v.s. EOT plot for La_2O_3 and TmO_x samples is shown in Fig. 3.9. Smaller leakage currents were obtained for the TmO_x structure samples of the same EOT. In the EOT range over 1.2 nm, leakage current was increased both La_2O_3 and TmO_x . The reason was that physical thickness can be small with decreasing EOT.

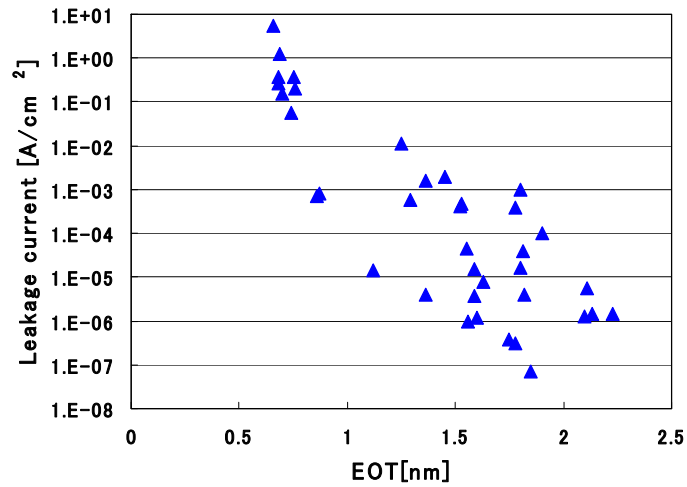


Fig. 3.10 Single layered capacitor C - V characteristic at the same EOT

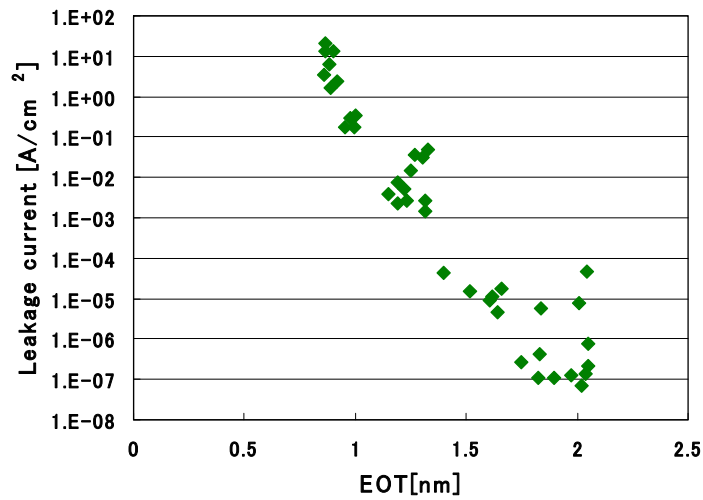


Fig. 3.11 Single layered capacitor C - V characteristic at the same EOT

3.4 Fixed Charge in Dielectric Film

In this section, the quantity of fixed charge in each layer was estimated and compared those values. The change of V_{fb} value by ration of RE oxides was investigated.

3.4.1 Calculation Method of Fixed Charge

The amount of charge due to defect is usually described in terms of the change in gate voltage, which is a readily measurable parameter, necessary to counter the effect of he oxide charge or to restore the surface potential corresponding to the flat-band state.

Let us consider an MOS structure biased at flat-band condition. Let us assume that a sheet of oxide charge Q is placed at a distance x from the gate electrode, and a gate voltage δV_g has been applied to restore the MOS structure to its original, *i.e.*, flat-band, condition. With the surface potential restored to its original value, the sheet of oxide charge has induced no change in the charge distribution in the silicon, which is a function of the surface potential, but a charge of magnitude $-Q$ on the gate electrode. This is illustrated in Fig. 3.12

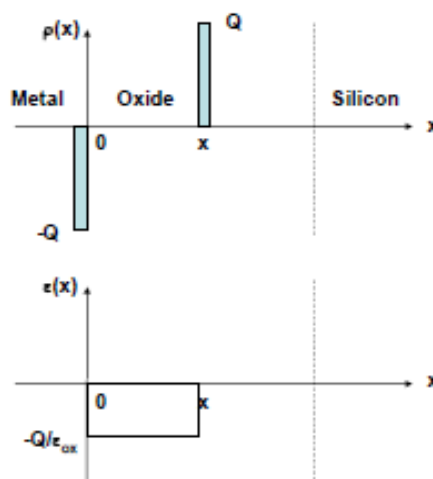


Fig. 3.12 schematic illustrating the effect of a sheet charge of areal density Q within the oxide layer of an MOS capacitor biased at flat-band condition

Gauss's law implies that the electric field in the oxide between 0 and x due to the sheet of oxide charge and its image charge on the gate electrode is $-Q/\epsilon_{ox}$ this is also illustrated in Fig. 3.12. The potential difference supporting this electric field is $-xQ/\epsilon_{ox}$, which is provided by the applied gate voltage. Therefore,

$$\delta V_g = -\frac{xQ}{\epsilon_{ox}} \quad (3.1)$$

The gate voltage necessary to offset the effect of an arbitrary oxide charge distribution can be obtained by superposition of individual elements of the charge distribution and applying Eq. (3.1) to each element. For an oxide charge distribution of $\rho(x, \psi_s) = \rho(x) + Q_{it}(\psi_s)\delta(x - t_{ox})$, which consists of an arbitrary distribution $\rho(x)$ that is independent of the surface potential and a delta-function distribution of the interface trap charge located at $x=t_{ox}$ the gate voltage necessary to offset it is

$$\Delta V_g = -\frac{1}{\epsilon_{ox}} \left(\int_0^{t_{ox}} x\rho(x)dx + Q_{it}(\psi_s)t_{ox} \right) \quad (3.2)$$

$\rho(x)$ includes the mobile charge, the oxide trap charge, and the fixed oxide charge.

It is a common practice to define an *equivalent oxide charge per unit area*, Q_{ox} , by

$$Q_{ox} = \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho(x)dx + Q_{it}(\psi_s) \quad (3.3)$$

Equation (3.2) can then be rewritten in the simple form

$$\Delta V_g = -\frac{Q_{ox}(\psi_s)}{\epsilon_{ox}} t_{ox} \quad (3.4)$$

This equation states that the effect of an arbitrary oxide charge distribution is equivalent to an oxide sheet charge $Q_{ox}(\psi_s)$ located at the oxide-silicon interface.

For simplicity of calculation, it is assumed that all charge in film exists at the bottom of oxide. On this basis, Eq.(3.4) is rewritten as

$$\Delta V_g = V_{fb} = -\frac{Q_{it}}{\epsilon_{ox}} EOT \quad (3.5)$$

Where Q_{it} is density of charge value, this value can be determined from the relationship between flat-band voltage (V_{fb}) and EOT.

In Eq.(3.5), Q_{it} is proportional to V_{fb} . Hence, this value is requested illustration of V_{fb} v.s EOT plot.

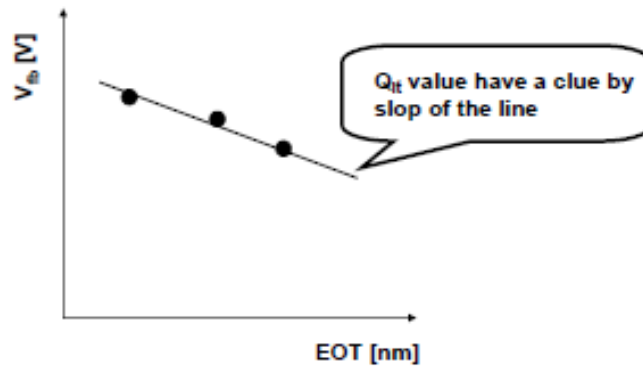


Fig. 3.13 V_{fb} v.s EOT plot

In this study, in V_{fb} -EOT plots, it is found that there are the two lines with different slopes. Line fitting was given to one at large EOT region.

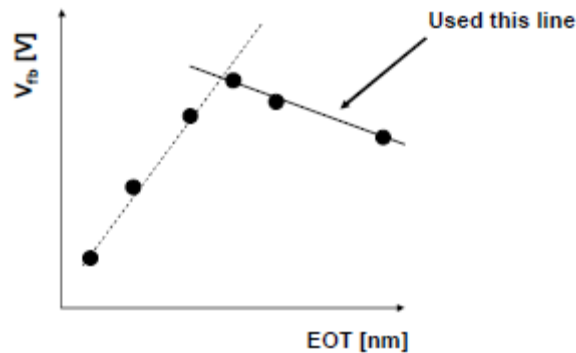


Fig. 3.14 V_{fb} v.s EOT plot. line fitting was given to general slop line

In order to investigate the density of fixed charge, each single film capacitors with different thickness rations were fabricated. In each sample, density of fixed charge was estimated by using line fitting.

3.4.2 Quantifying Fixed Charge in Each Film

V_{fb} dependence on EOT of the capacitor with La_2O_3

Figure 3.15 shows the dependence of V_{fb} on EOT for $\text{La}_2\text{O}_3/\text{La-silicate}$ MOS capacitors. In this figure, two linear regions were observed. From the slope of the dependence of flatband voltage on EOT, the effective fixed charges density (Q_{fix}) at the interfaces of RE-oxide/RE-silicate and RE-silicate/Si can be extracted.

The EOT ranges from 0.9-1.3 nm, and 1.3-2 nm in $\text{La}_2\text{O}_3/\text{La-silicate}$ samples exhibited the Q_{fix} of -2.2×10^{13} and $-6.6 \times 10^{12} \text{ cm}^{-2}$, respectively. At the cross-point of these linear regions, physical thickness is about 4 nm, and it is considered that a diffusion of tungsten atoms cause to increase fixed charges below this thicknesses.

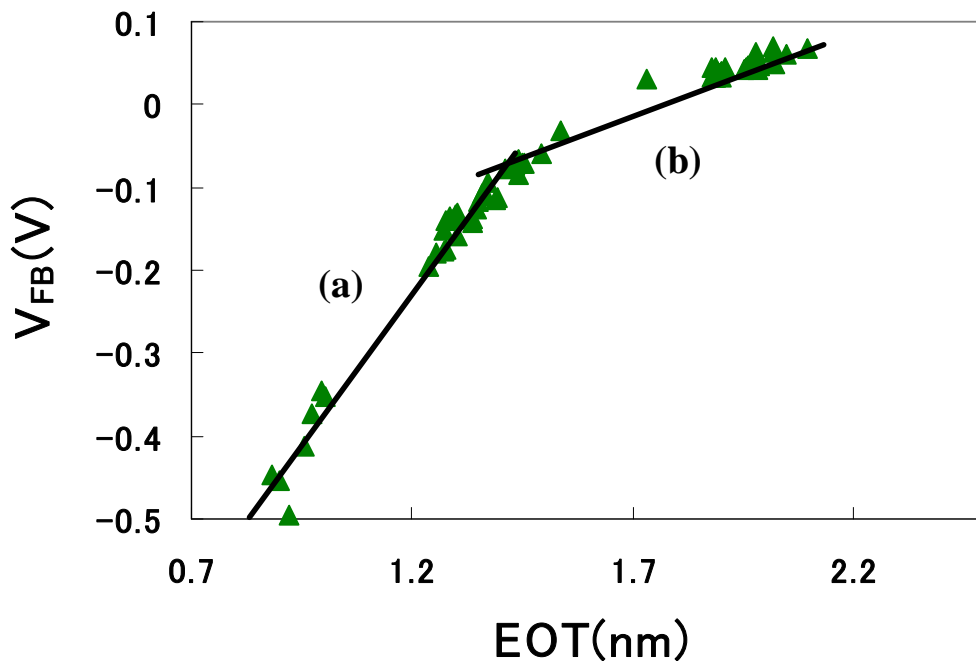


Figure 3.15. V_{fb} as a function of EOT for $\text{W}/\text{La}_2\text{O}_3/\text{Si}$ capacitors after annealing at 500°C

V_{fb} dependence on EOT of the capacitor with CeO_x

Figure 3.16 shows the dependence of the V_{fb} on EOT for CeO_x/Ce -silicate MOS capacitors. In this figure, two linear regions were observed. The EOT ranges from 1.0~1.2, 1.2~1.4, and 1.4~1.6 nm in CeO_x/Ce -silicate samples exhibited the Q_{fix} of -6.6×10^{13} , $+6.1 \times 10^{12}$ and $+6.3 \times 10^{11} \text{ cm}^{-2}$, respectively. In EOT range below 1.2 nm, a diffusion of tungsten atoms might cause to increase fixed charges like the La_2O_3/La -silicate samples. In the EOT range over 1.2 nm, we consider that negative fixed charges in the CeO_x layer cause the flatband shift,. The smaller crosspoint than La_2O_3 is due to its higher dielectric constant. Fixed charges in CeO_x have much effect on V_{fb} shift

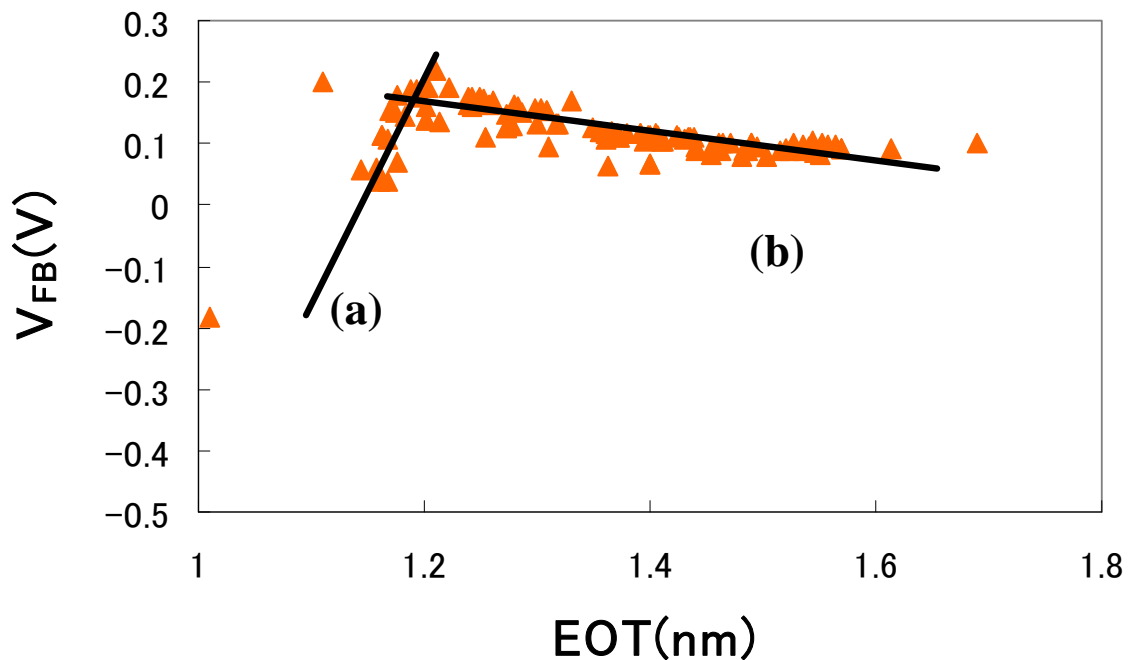


Figure 3.16 V_{fb} as a function of EOT for $W/CeO_x/Si$ capacitors after annealing at 500 °C

V_{fb} dependence on EOT of the capacitor with PrO_x

Figure 3.17 shows the dependence of V_{fb} on EOT for $\text{PrO}_x/\text{Pr-silicate}$ MOS capacitors. In this figure, two linear regions were observed. The EOT ranges from 0.7~1.2, 1.2~2.3 nm, $\text{PrO}_x/\text{Pr-silicate}$ exhibited the Q_{fix} of -1.4×10^{13} , $-2.7 \times 10^{12} \text{ cm}^{-2}$, respectively. This result is similar to that of $\text{La}_2\text{O}_3/\text{La-silicate}$ samples. Therefore, a diffusion of tungsten atoms probably causes to increase fixed charges like the La_2O_3 case.

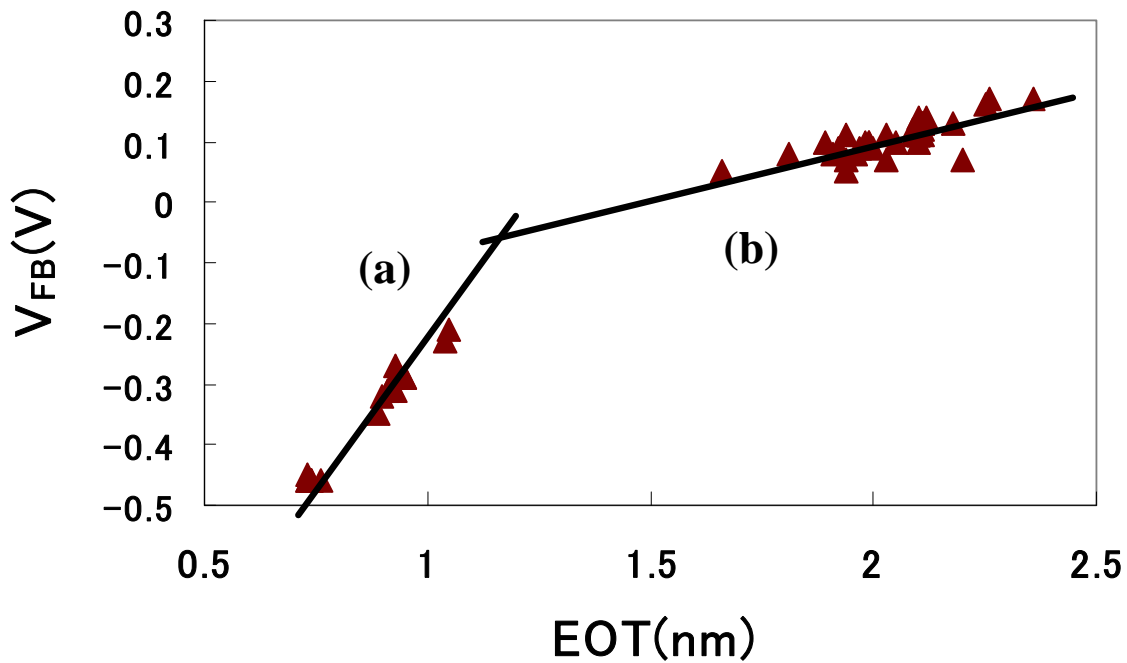


Figure 3.17 V_{fb} as a function of EOT for $\text{W}/\text{PrO}_x/\text{Si}$ capacitors after annealing at 500°C

V_{fb} dependence on EOT of the capacitor with TmOx

Figure 3.18 shows the dependence of V_{fb} on EOT in TmO_x/Tm-silicate MOS capacitors. In this figure, two linear regions were observed.

The EOT ranges from 0.6~1.8, and 1.8~3.0 nm in TmO_x/Tm-silicate samples exhibited the Q_{fix} of -6.5×10^{12} , and $-3.3 \times 10^{12} \text{ cm}^{-2}$, respectively. This behavior is also similar to that of La₂O₃/La-silicate samples. However, the value of the Q_{fix} was the lowest value among the samples of the current study.

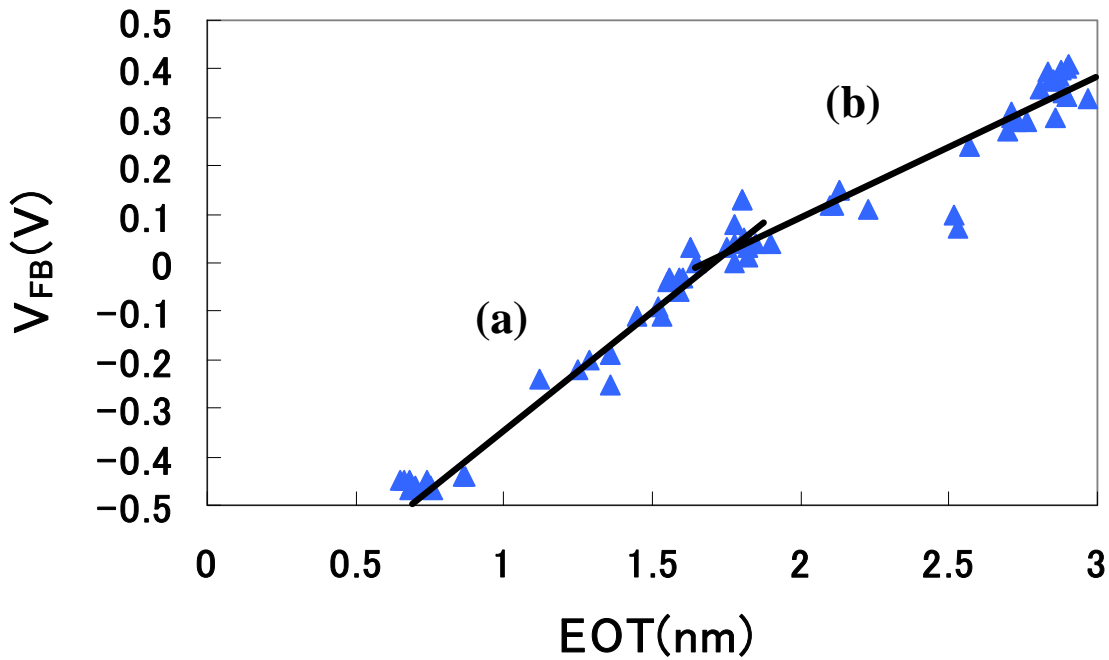


Figure 3.18 V_{fb} as a function of EOT for W/TmO_x/Si capacitors after annealing at 500 °C

3.5 Model of the location of fixed charges

Figure 3.19 shows the schematic illustration of the location of fixed charges in La_2O_3 , PrO_x and TmO_x . From the slope of (a) as shown in Figs. 2-5, the fixed charges at $\text{La}_2\text{O}_3/\text{silicate}$, $\text{CeO}_x/\text{silicate}$, $\text{PrO}_x/\text{silicate}$, and $\text{TmO}_x/\text{silicate}$ interfaces are found to be negative, presumably because the tungsten (W) atoms are located near the interface and the diffusion of W atoms toward the interface is not negligible. However, in the region (b), the fixed charges at $\text{La}_2\text{O}_3/\text{silicate}$, $\text{PrO}_x/\text{silicate}$, and $\text{TmO}_x/\text{silicate}$ interfaces decrease, because the distance from W electrode to these interface increases and the diffusion of W atoms to the interface is negligible.

Figure 3.20 shows the schematic illustration of the location of fixed charges in CeO_x layers. In the region (b) as shown in Fig 3, negative fixed charges in the CeO_x layer increase owing to the increase in CeO_x layer thickness, while the negative fixed charges at $\text{CeO}_x/\text{silicate}$ interface decreases. CeO_x can achieve the same EOT with physical thickness larger than those of La_2O_3 , PrO_x and TmO_x owing to its high dielectric constant. Therefore, an amount of fixed charge in CeO_x layer has much effect on V_{fb} shift.

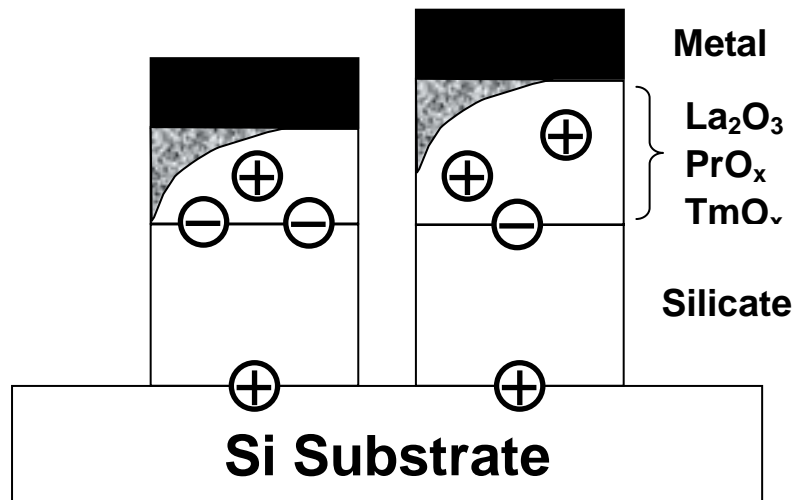


Figure 3.19 Schematic illustration of fixed charges generation in the oxide and oxide/silicate interface for two thicknesses of La₂O₃, PrO_x and TmO_x layers.

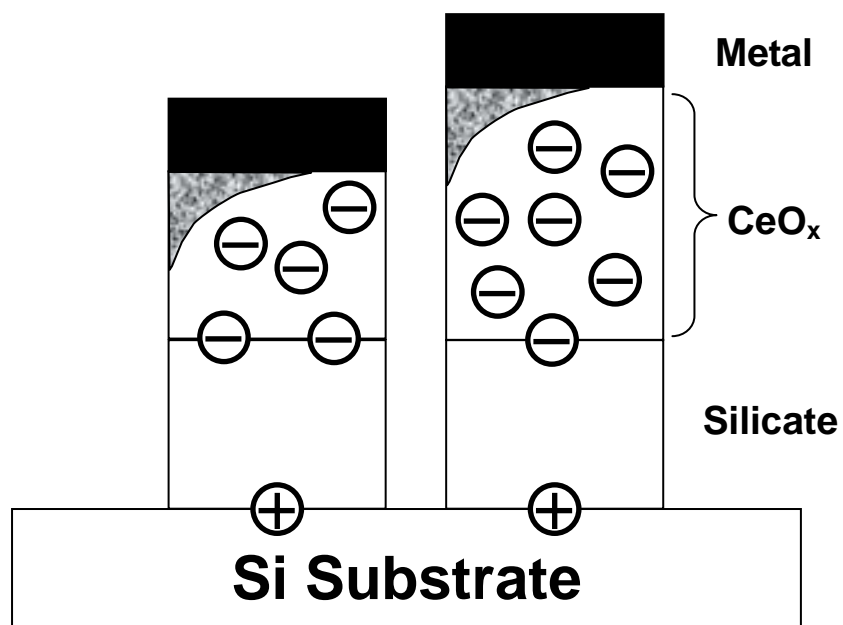


Figure 3.20 Schematic illustration of fixed charges generation in the oxide and oxide/silicate interface for two thicknesses of CeO_x layer.

Chapter 4. Conclusion

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4.2 Future Issues-----p50

Acknowledgement-----p51

4.1 Conclusion of This Study

Dependence of V_{fb} shift on EOT of MOS capacitors with rare earth (La, Ce, Pr and Tm) oxides/silicates are investigated. In the small EOT region, a diffusion of gate metal atoms from gate electrode increases fixed charge at the interface between RE-oxide and RE-silicate. With the increase in EOT, the effect of fixed charge in the RE-oxide film on V_{fb} shift increases. TmO_x/Tm -silicate capacitor exhibits small Q_{fix} of $-6.5 \times 10^{12} \text{ cm}^{-2}$ in the low EOT region.

4.2 Future Issues

Rare earth oxides have been the promising candidates for the next generation gate dielectric. In this study, a novel Rare earth oxides of gate insulator was suggested focused on La_2O_3 , CeO_x , PrO_x and TmO_x . We proposed model of the location of fixed charges in La_2O_3 , CeO_x , PrO_x and TmO_x . XPS analysis is introduced as the experimental and theoretical methodology, electrical properties of several materials will be explored in more detail.

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