Master Thesis

Fabrication of SB-MOSFETs on SOI Substrates Using Ni Silicide with Er Interlayer

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INTRODUCTION

1.1 Background of This Study

About a half century ago, W. Brattain, J. Bardeen and W. Shockley succeeded in inventing the first transistor in 1947. Then, an integrated circuit (IC) is made by J. Killby in 1948. After the invention of the IC, the numbers of transistors included in a chip have increased according to Moore's law and the semiconductor technologies have accomplished wonderful development.

CMOS (Complementary Metal Oxide Semiconductor) technology evolution in the past years has followed the path of device scaling for achieving density, speed, and power improvements. MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) scaling was propelled by the rapid advancement of lithographic techniques for delineating fine lines of 1μm width and below.

In constant-field scaling, it was proposed that one can keep short-channel effects under control by scaling down the vertical dimensions (gate insulator thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionally decreasing the applied voltages and increasing the substrate doping concentration (decreasing the depletion width). This is shown schematically in Fig. 1.1. The principle of constant-field scaling lies in scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor, $\kappa(>1)$, so that the electric field remains unchanged. This assures that the reliability of the scaled device is not worse than that of the original device. Table 1.1 shows the scaling rules for various device parameters and circuit performance factors. The doping concentration must be increased by the scaling factor κ in order to keep Poisson's equation invariant with respect to scaling.

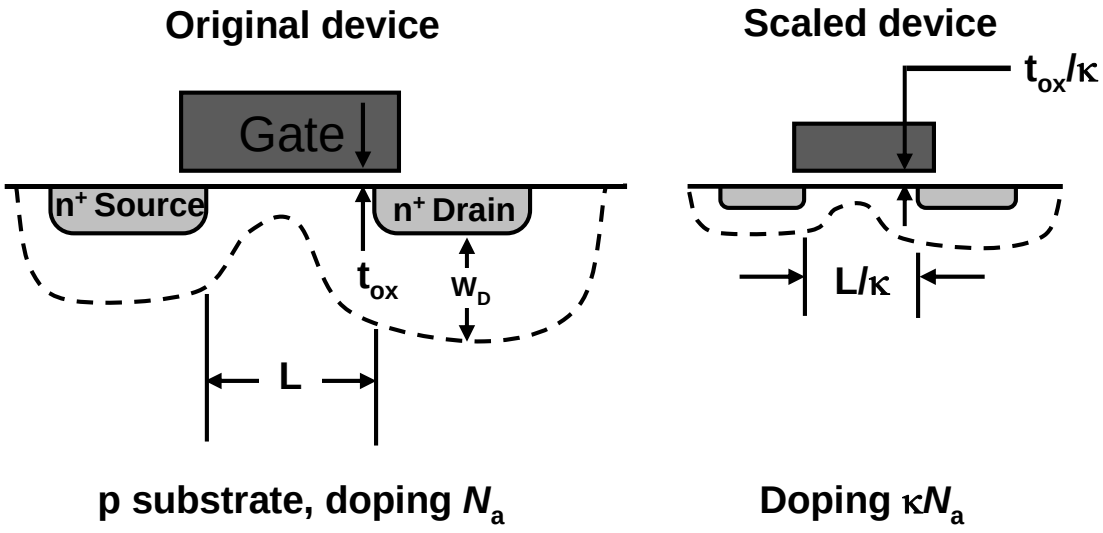


Fig. 1.1 Principles of MOSFET constant-electric-field scaling

Table 1.1 Scaling of MOSFET Device and Circuit Parameters

	MOSFET Device and Circuit Parameters	Multiplicative Factor (κ>1)
Scaling assumptions	Device dimensions(tox, L, W, χj)	1/κ
	Doping concentration (Na, Nd)	κ
	Voltage (V)	1/κ
Derived scaling behavior of device parameters	Elecric field (ξ)	1
	Carrier velocity (υ)	1
	Depletion –layer width (Wd)	1/κ
	Capacitance (C=εA/t)	1/κ
	Inversion-layer charge density (Qi)	1
	Current, drift (I)	1/κ
	CRchhannel resistance (Rch)	1
Capacitance behavior of circuit Power parameters	Circuit delay time (τ~CV/I)	1/κ
	Power dissipation per circuit (P~VI)	$1/\kappa^2$
	Power-delay product per circuit (Pτ)	$1/\kappa^3$
	Circuit density (∞ 1/A)	κ^2
	Power density (P/A)	1

The gate length of MOSFET came to be lower than 100nm since the year of 2000 and 29nm for the year of 2009 as shown in Fig. 1.2 according to the ITRS roadmap 2009 update [1]. With continuous scaling of device dimensions, IC performance is becoming more and more dependent upon the parasitic series resistance of the source/drain junctions and their contacts.

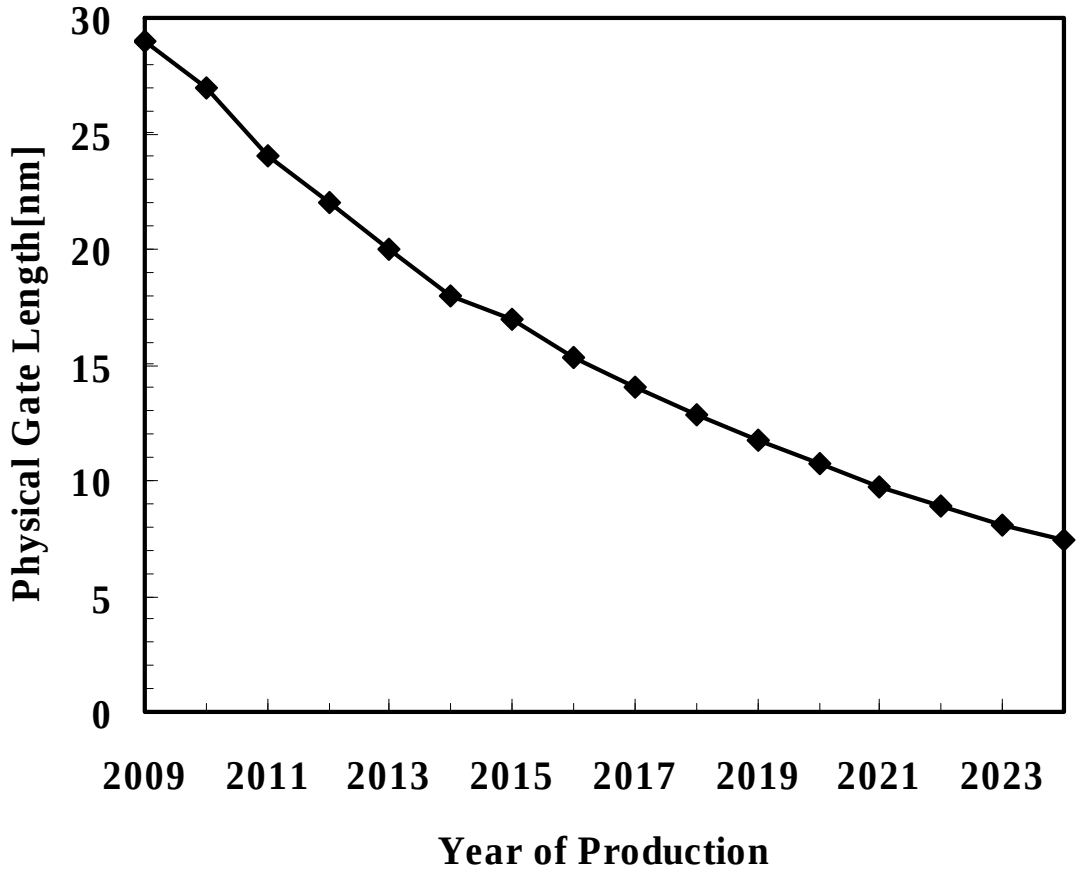


Fig. 1.2 the International Technology Roadmap for Semiconductors (2009 update)

1.2 Problem of the VLSI

The physical limit comes for the scaling. Now, the biggest problem is the scaling of the gate oxide. The scaling of gate oxide for improving MOSFET performance is required. A few nm gate oxide technique is required, but the present SiO_2 range doesn't suppress the gate leakage current. This limit is said to be 1.2-1.5nm. The recent research for this problem uses high-k dielectric which k value is higher than that of the conventional SiO_2. If we use the material which k value is five times lager, we can obtain the same capacitance with the physical oxide thickness five times larger. However, we require that k is higher than 10, the band is higher than 1eV and the thermal stability, single crystal or amorphous, and small defect density are needed. The scaling of gate oxide is proceeding, it is not ignored that capacitance. That is to say, it is inversion capacitance of the channel surface and depletion conductance of polysilicon for the gate electrode. The inversion capacitance is not ignored. The problem of the depletion capacitance of the gate electrode is controlled the high gate impurity concentration. However, its limit comes up. Thinking for the measure is to use the polysilicon gate in stead of metal gate. The scaling has the problem of thin junction depth in source and drain range. The junction depth in source and drain for the scaling requires shallower junction depth. But the shallow junction profile has high resistance. The source and drain high impurity concentration makes the resistance low. This problem's limit also comes up.

1.3 Schottky Barrier MOSFET

Before section, it explain that the VLSI is forced various problem and solution. For these problem solutions, the various methods suggest and experiment on. In these suggestion, schottky barrier MOSFET is suggested by S.M.Sze in 1968 [2]. The conventional MOSFET and schottky barrier MOSFET are shown in Fig. 1.3.

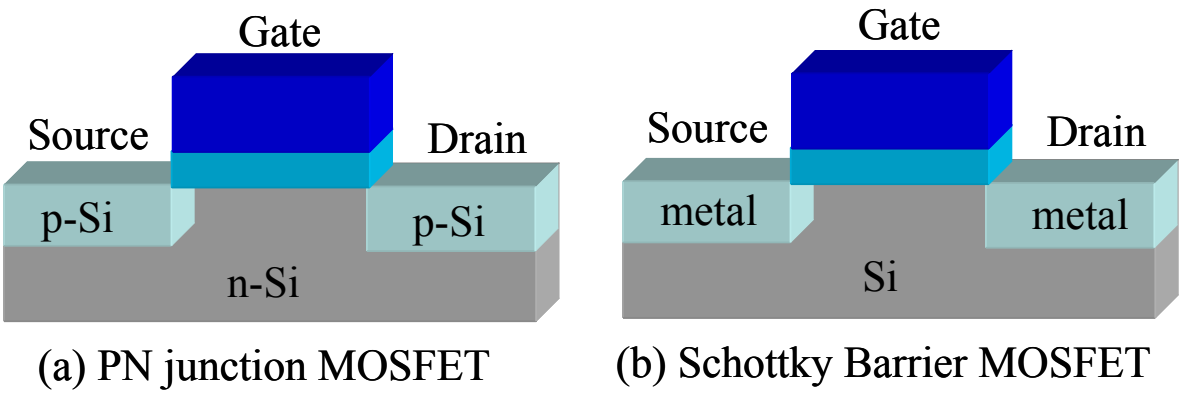


Fig. 1.3 The conventional n-MOSFET and schottky barrier MOSFET

The schottky barrier MOSFET adopts alloy of Si and metal that called silicide in source and drain range. The schottky barrier MOSFET formed schottky contact in Si and silicide interface operate as well as conventional MOSFET. The next paragraphs show advantages and issues of schottky barrier MOSFET.

Advantages

1. As the junction depth becomes smaller, the sheet resistance becomes higher. However, in terms of scaling, we need to have smaller sheet resistance as well as smaller junction depth. For the solution of this problem, Schottky barrier MOSFET is considered. [3,4]

2. The schottky barrier MOSFET can be done a low temperature process compared with the pn junction MOSFET.

3. The schottky barrier MOSFET doesn't require to form diffusion range in source and drain. That can permit scaling device area. The integration of circuit can be raised.

4. The doping in channel range doesn't need to control carrier by schottky barrier height. The problem that means dispersion of impurity by short channel effect is avoided.

Issues

1. The drive current is limited by schottky barrier height. Because schottky barrier height acts as resistance. [5,6]

2. The schottky barrier MOSFET has a large leakage current compared with the pn junction MOSFET because of tunneling current between Si substrate and silicide for schottky barrier.

1.4 Silicide for Schottky Barrier MOSFET

Silicide materials I using for schottky barrier MOSFET are listed table 1.2.

Table1.2 Silicide material for schottky barrier MOSFET

Silicide	Schottky Barrier Height (eV)
NiSi	0.65～0.75
ErSi	0.27～0.36

The Er silicide has been proposed for n-channel schottky barrier MOSFET because of very low schottky barrier height of 0.27-0.36eV for electrons. [7] On the other hand, the schottky barrier height of Ni silicide is around middle gap of Si. It's 0.65-0.75eV for electron and hole. Though Ni silicide has a middle gap of Si, it has advantages for schottky barrier MOSFET. Ni silicide has a very low resistance compared with other materials as shown Fig. 1.4. And the other characteristics of Ni silicide are low Si consumption, low temperature for silicidation and lack of narrow-width effect.

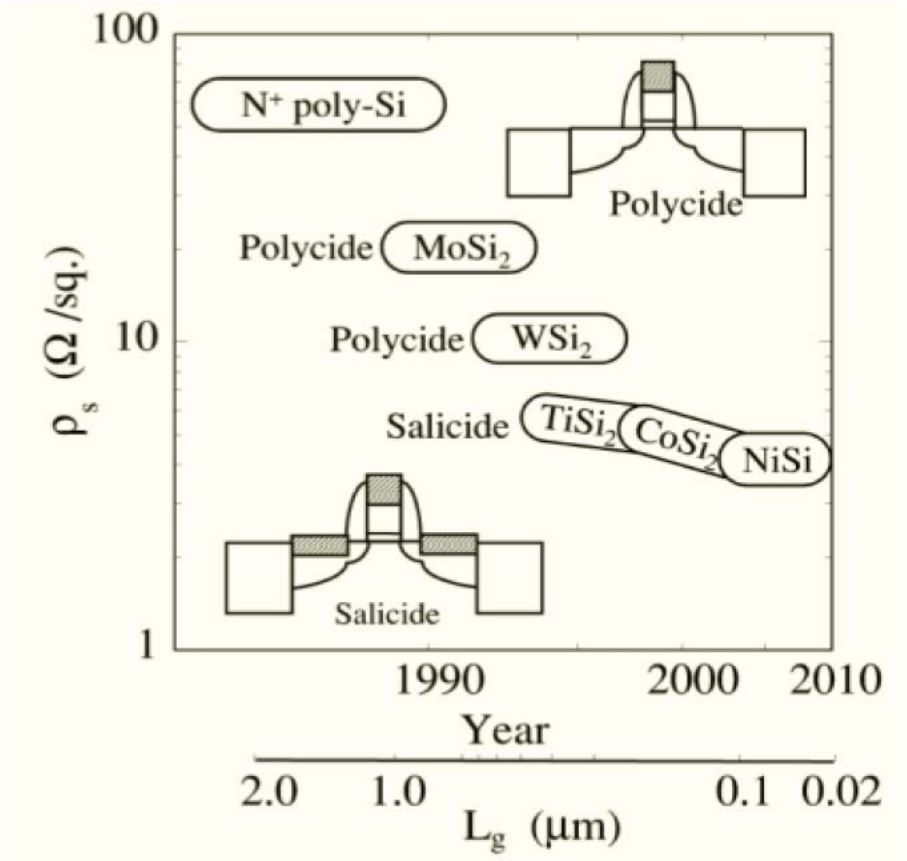


Fig. 1.4 resistance of various silicide [9]

1.5 Purpose of This Study

In this work, we investigated Φ_b modulation of Ni silicide which has good characteristics (Low Si consumption, Low temperature for silicidation and lack of narrow-width effect) by inserting an Er at the Ni/Si interface before silicidation, and applied this technique to SB-nMOSFETs fabrication on SOI and discussed Er insertion effect..

Chapter 2
SCHOTTKY BARRIER DIODE AND MOSFET

2.1 Schottky Diode

In the case of metal and silicon contact, the potential that is called schottky barrier height is formed metal and silicon interface that is the same commutation characteristics of pn junction. The work function of metal and semiconductor is ϕ_m and ϕ_σ ,respectively, and the electron affinity is χ . When the relationship $\phi_m > \phi_\sigma > \chi$ among ϕ_m,ϕ_σ and χ is defined $\phi_m > \phi_\sigma > \chi$, the schottky barrier height is

$$\phi_B = \phi_m - \chi \text{ . (2.0)}$$

The commutation is appeared from this potential. But, in fact the schottky barrier height is measured that dose not depend against metal work function ϕ_m. In generalization, the dependence on work function is small against ideal it. That reason is existence interfacial trap and interfacial layer. A lot of model are suggested in relationship among Fermi level pinnning. In this case, the only ideal case is considerd. The transportation structure pass through thermal electron emission obtains over the potential and tunneling structure pass through schottky potential as shown in Fig. 2.1.

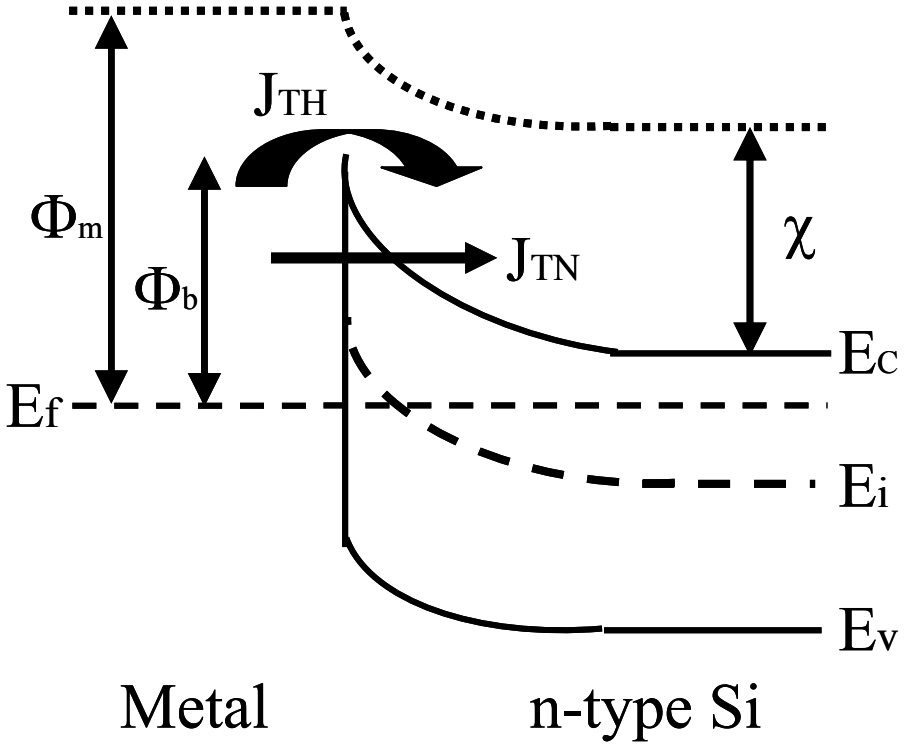


Fig. 2.1 schematic illustration of schottky diode band diagram [10]

2.1.1 Thermal Electron Emission Structure

It is mentioned thermal emission structure. First of all, the electron current j_2 is considered about from semiconductor to metal as shown in Fig. 2.2. The electron does not collision in distance of space electron charge layer. The electron current pass over this layer to metal. The electron emission metal is higher electron energy than E_0 as shown Fig. 2.2.

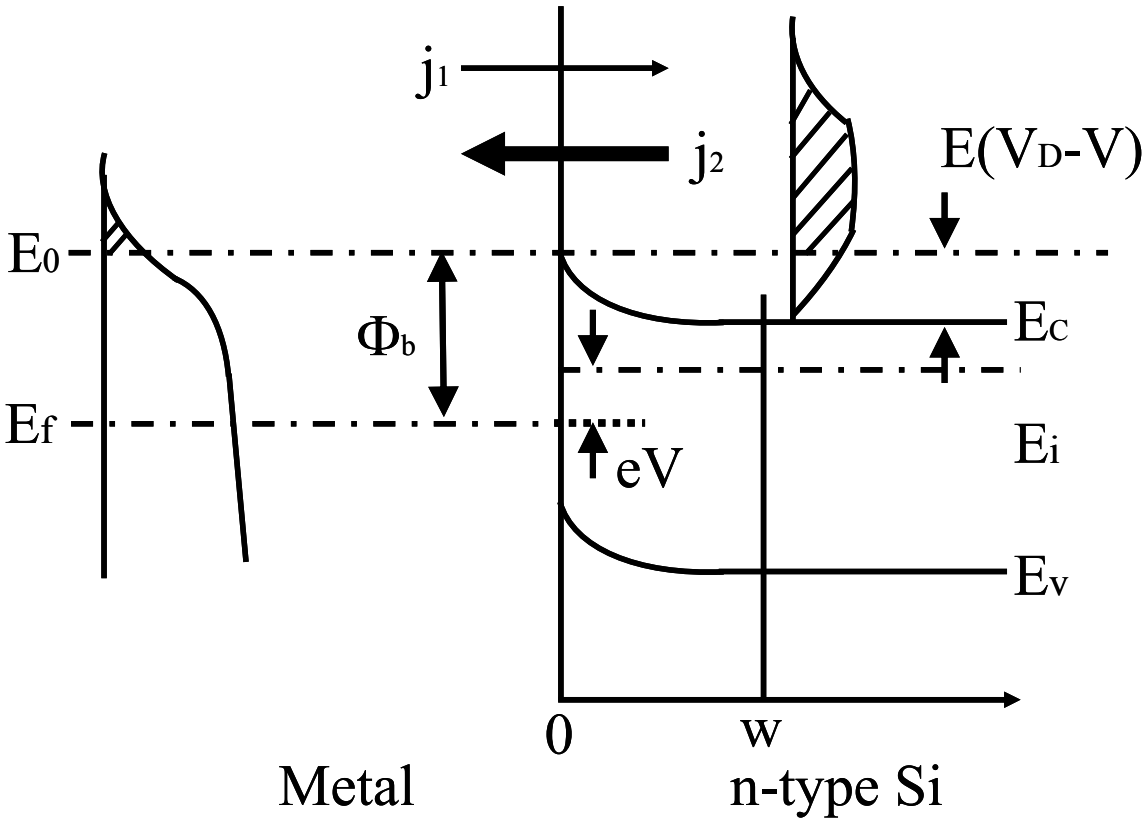


Fig. 2.2 schematic illustration of rectification of schottky contact [10]

$$j_2 = -\int v_x \, dn = -\int_{j_x>0} V_x \cdot Z(E) f(E) dE$$

$$= -\int_0^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} v_x \cdot 2\frac{1}{8\pi^3} \cdot f(E) dk_x dk_y dk_z$$

$$= -\frac{1}{4\pi^3}\int_0^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} v_x \left\{\exp\left(-\frac{E-E_f}{kT}\right)\right\} dk_x dk_y dk_z \quad (2.1)$$

But, Z(E) is state density of electron, f(E) is distribution function of electron, v_x is velocity element of x direction of electron, and m_e* is actual mass of electron in semiconductor. The v_x is written

$$v_x = \frac{\hbar k_x}{m_e^*}. \quad (2.2)$$

$$E = E_0 + \frac{\hbar}{2m_e^*}(k_x^2 + k_y^2 + k_z^2) \quad (2.3)$$

The equation (2.1) is equal to

$$j_2 = -\frac{1}{4\pi^3}\int_0^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \frac{\hbar k_x}{m_e^*} \exp\left\{-\frac{\hbar^2\left(k_x^2 + k_y^2 + k_z^2\right)}{2m_e^* kT}\right\}\left\{\exp\left(-\frac{E_0 - E_f}{kT}\right)\right\} dk_x dk_y dk_z$$

$$= -\frac{4\pi m_e^* k^2 T^2}{h^3}\exp\left(-\frac{E_0 - E_f}{kT}\right) \quad (2.4)$$

The semiconductor side is defined

$$E_0 - E_f = \phi_m - \chi - qV \quad (2.5)$$

$$\phi_B = \phi_m - \chi. \quad (2.6)$$

The current pass through from semiconductor to metal is

$$j_2 = -\frac{4\pi m_e^* k^2 T^2}{h^3}\exp\left(-\frac{\phi_B - qV}{kT}\right) \quad (2.7)$$

And, the current from metal to semiconductor is $\phi_m - \chi - qV$ replaced by $\phi_m - \chi$.

$$j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \quad (2.8)$$

The net current is

$$j_2 - j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.9)$$

and current density is

$$j_{TH} = -\frac{4\pi q m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.10)$$

The current about thermal emission structure is

$$j_{TH} = J_0 \exp\left\{\left(\frac{qV}{nkT}\right) - 1\right\} \quad [8]. \quad (2.11)$$

$$j_0 = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \quad (2.12)$$

$$A^* = \frac{4\pi q m_e^* k^2}{h^3}. \quad (2.13)$$

A* is Richardson constant, k is Bltzmann's constant, h is Planck's constant and T is absolute temperature. The n that is called ideal factor is n=1 in ideal schottky contact, but in fact n>1. The reason of it is transport current in diffusion current, bias dependence of schottky barrier height in image force, injection of minority carrier, and dependence of schottky barrier in interfacial trap. The ϕ_b is written as

$$\phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_0}\right). \quad (2.14)$$

The ϕ_b can be looked for I-V measurement of schottky diode. The other method for look for schottky barrier height is relationship depletion capacitance and bias current.

2.1.2 Tunneling Structure

Next, it is considered about Tunneling structure. The tunneling is gave next equation [11]

$$J_{TN} = \frac{q^2 F^2}{8\pi h \phi_B} \exp\left[-\frac{8\pi}{3hqF} \sqrt{2m_e^* (q\phi_B)^3} \right]. \quad (2.15)$$

But, F is field electric of vertical direction of semiconductor surface. The image of the image charge is added in schottky barrier ϕ_b

$$\phi_B = \phi_{B0} - \sqrt{\frac{qF}{4\pi\varepsilon}}. \quad (2.16)$$

The ϕ_b is schottky barrier height when the field electric is not added, and the ε is silicon permittivity. The phenomenon that is lowered schottky barrier height in electric field is called schottky effect. The current in schottky interface expresses the sum of thermal emission current and tunneling current

$$J_{total} = J_{TH} + J_{TN}. \quad (2.17)$$

2.1.3 Space Charge capacitance of Schottky Contact

The space charge capacitance of schottky contact can be considered a kind of capacitor as well as pn junction. That has electric capacitance. If the potential in paint x is φ(x), Poisson's equation is

$$\frac{d^2 \varphi(x)}{dx^2} = -\frac{qN_D}{\varepsilon_0 \varepsilon_S}. \quad (2.18)$$

The (2.18) is done integral is

$$\frac{d\ \varphi(x)}{dx} = -\frac{qN_D}{\varepsilon_0 \varepsilon_S} x + C_1 \quad (2.19)$$

$$\varphi(x) = -\frac{qN_D}{\varepsilon_0 \varepsilon_S} x^2 + C_1 + C_2. \quad (2.20)$$

The x axis express Fig. 2.2,and beginning condition is $\varphi(x)= \varphi_0=0$ when x is equal to 0.

$$C_2 = 0 \quad (2.21)$$

x=w, and $d\varphi(x)/dx=0$

$$C_1 = -\frac{qN_D}{\varepsilon_0 \varepsilon_S} w. \quad (2.22)$$

The potential is

$$\varphi(x) = \frac{qN_D}{\varepsilon_0 \varepsilon_s}\left(wx - \frac{x^2}{2} \right). \quad (2.23)$$

x=w, and $\varphi(w)=V_D-V$

$$w = \left\{ \frac{2\varepsilon_0 \varepsilon_s (V_0 - V)}{qN_D} \right\}^{\frac{1}{2}}. \quad (2.24)$$

The electrostatic capacitance is

$$C = \frac{\varepsilon_0 \varepsilon_s}{w} = \left\{ \frac{q\varepsilon_0 \varepsilon_S N_D}{2(V_D - V)} \right\}^{\frac{1}{2}} \quad (2.25)$$

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_0 \varepsilon_s N_D}(V_D - V). \quad (2.26)$$

The N_D and V_D can be search, if the function of $1/C^2$ versus bias V.

2.2 Schottky Barrier MOSFET

2.2.1 The Principle of The Schottky Barrier MOSFET

The schottky barrier MOSFET works a different principle of the conventional pn junction MOSFET. Schottky barrier height has two mechanism; thermal electron emission structure and tunneling structure. The working MOS transistor is concerned closely with these structures.

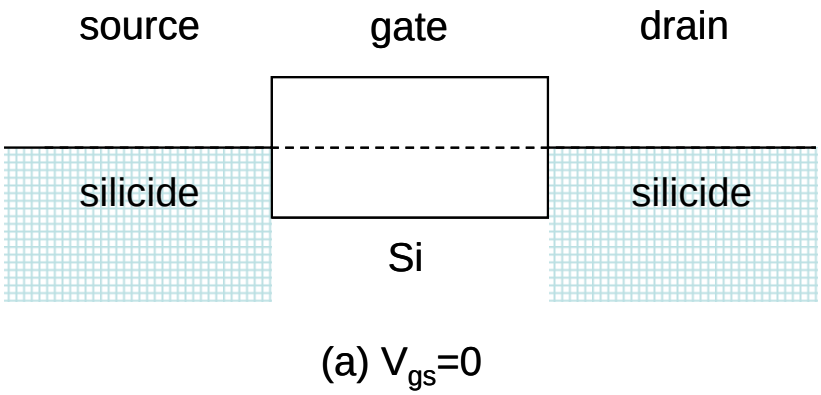
Fig. 2.3 shows a band structure of SB-MOSFET in the case of using middle gap silicide for source and drain. Fig. 2.3 (a) shows the case that there are no bias applied for gate and drain electrode. In this state, the thermal emission current obtaining over schottky barrier height flow as a leak current. A transistor is off state.

Fig. 2.3 (b) shows the case that there are drain bias (Vds>0) and no gate bias (Vgs=0). In this state, electron and hole cannot tunnel for the schottky barrier width of the edge of source and drain. A major current is a thermal emission current and a transistor is still off state.

Fig. 2.3(c) shows the case that there are plus bias applied for gate and drain electrode. In this state, it's enough to flow a tunneling current because schottky barrier width become very thin at the edge of source. The schottky barrier width becomes more thickness at the edge of drain, so thermal emission current flow. Then, transistor is on state and a dependence of a on current is stronger by tunneling current.

Fig. 2.3 (d) shows the case that there are plus drain voltage (Vds>0) and minas gate voltage (Vgs<0). In this state, transistor is also on. SB-MOSFET can work for both p-type and n-type with one structure. In the case of using middle gap silicide, MOSFET especially work like that. This means that a leak current always flows.

On current of SB-MOSFET is controlled by a tunneling current at the source edge. The tunneling current depends on schottky barrier height, so it's so important to select materials. SB-MOSFET is need to be controlled by not middle gap silicide but also n-metal or p-metal. In this study, Er or Hf (n-metal) was inserted between Ni (middle gap) and Si and schottky barrier height was modulated by this technique.



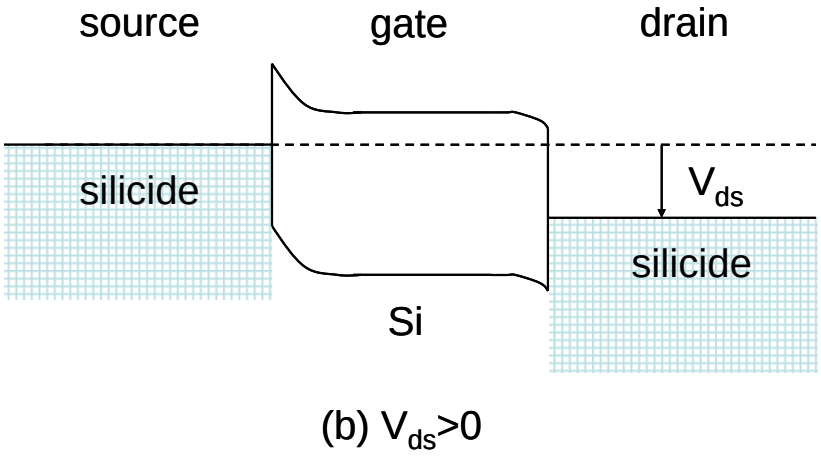
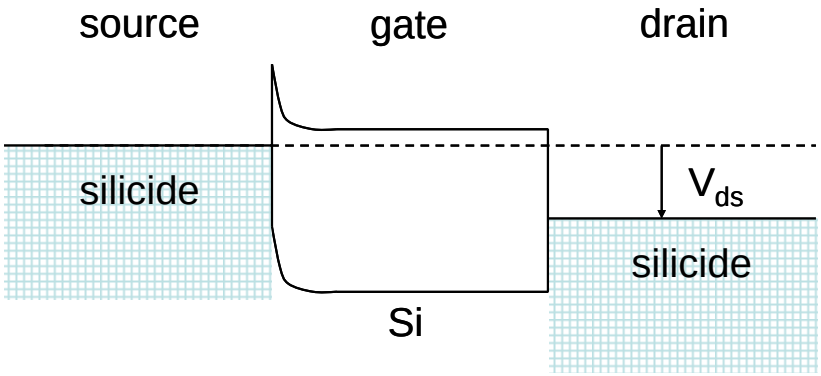
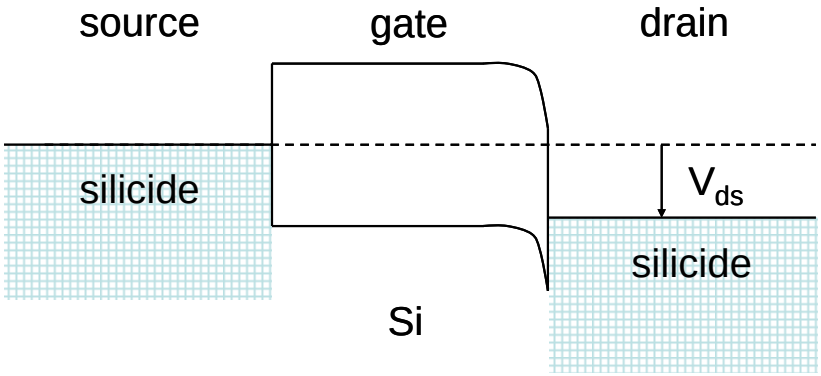


Fig. 2.3 The band structure of SB-MOSFET [10]



(c) $V_{gs}>0$



(d) $V_{gs}<0$

Fig. 2.3 The band structure of SB-MOSFET [10]

Chapter 3

FABRICATION AND CHARACTERIZATION METHODS

3.1 Experimental Procedure

3.1.1 Si Substrate Cleaning Process

High quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. It's considered that this substrate cleaning process is very important to realize desirable device operation and its reproducibility.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25^{o}C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩcm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the Si substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The steps are shown in Fig. 3.1. The first step, which use a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4: H_2O_2=4:1, called by SPM), was performed to remove any organic material and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:99). Then the cleaned wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber to deposit as soon as it was dried by air gun.

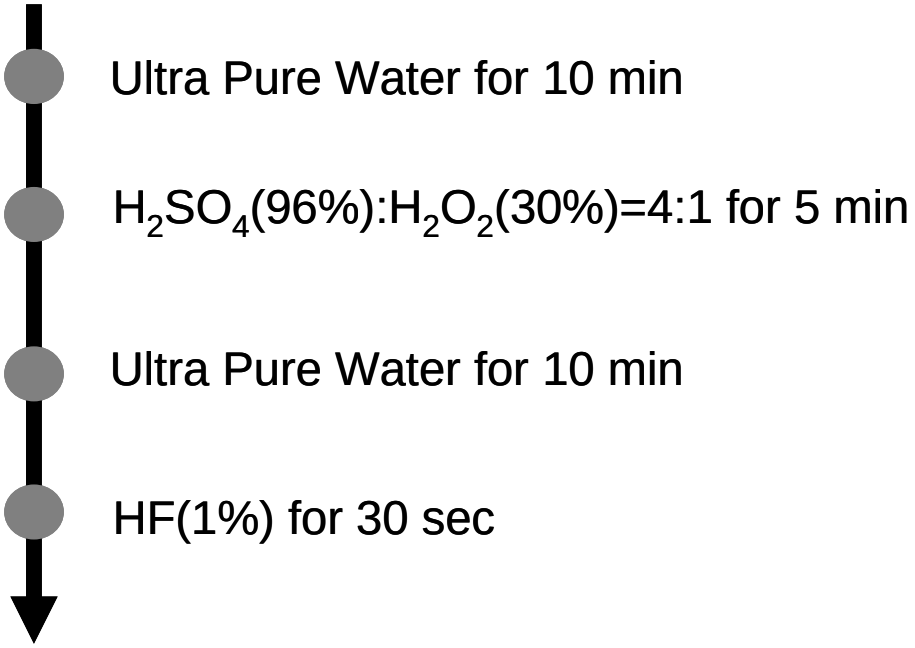


Fig. 3.1 Si Substrate Cleaning Process Flow

3.1.2 UHV-Sputtering System

After cleaned by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive except Ni.) and Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. It is performed by applying a high voltage across a low-pressure gas (usually argon at about 5 millitorr)to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike a “target,” composed of the desired coating material, and cause atoms from that target to be ejected with enough energy to travel to, and bond with the substrate.

An UHV-sputtering system is used for thin film formations of electronic devices, for experiments of GMR, and for creating new materials of high temperature superconductors. In this study, UHV Multi Target Sputtering System ES-350SU shown as Fig. 3.2 was conducted. structure of UHV sputtering system is shown as Fig.

3.3. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. As for other details, Table 3.1 is attached for reference.

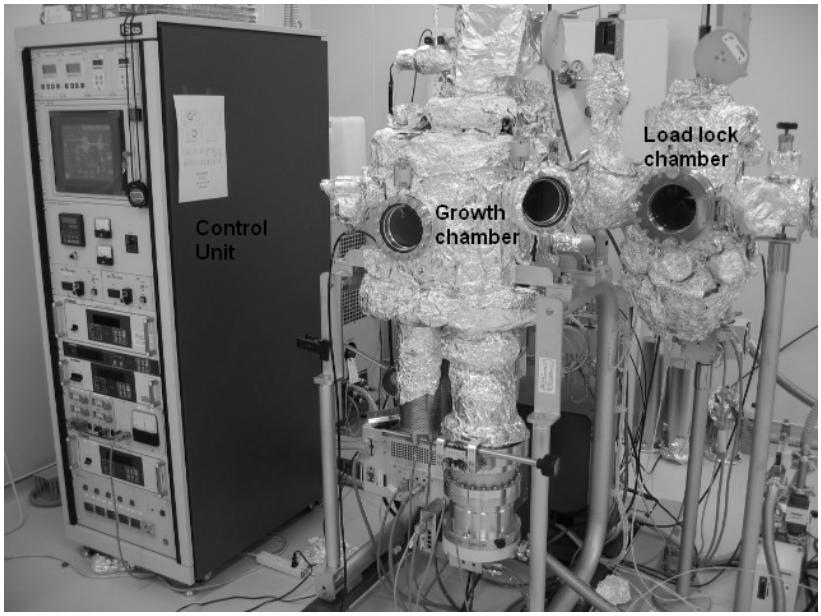


Fig. 3.2 Photo of UHV Multi Target Sputtering System ES-350SU

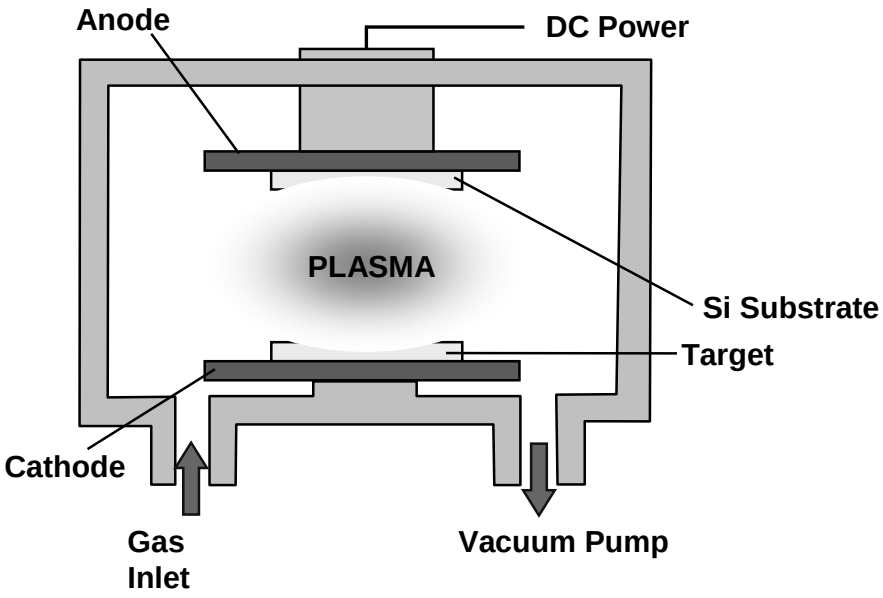


Fig. 3.3 structure of UHV sputtering system

Table 3.1 Specifications for UHV Multi Target Sputtering System ES-350SU

Growth chamber	1. Ultimate pressure	1.5 x 10^{-6}Pa
	2. Substrate size	2 inch in diameter
	3. Heating temperature	600ºC
	4. Heater type	Lamp type heater
	5. Target	3 inch x 5 pieces (motor-driven)
Load lock chamber	6. Vacuum pumps	TMP 500L/sec and RP 250L/min
	7.Ultimate pressure	6.6 x 10^{-5}Pa
	8. Vacuum pumps	TMP60L/sec and RP90L/min
	9. Substrate holder with cooling function / Substrate holder with heating function /Cleaning function / Radical beam source	

3.1.3 Infrared Annealing Furnace

After formation from UHV sputtering system, thin films of Ni/Si, Ni/M/Si, M/Ni/Si were moved to annealing furnace to hold thermal process.

In order to obtain high quality films, annealing process after deposition is required. The annealing after deposition is considered to bring the suppression of leakage current because of the defects in the films and surface roughness. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation was QHC-P610CP (ULVAC RIKO Co. Ltd). Fig. 3.4 is the photo of the infrared annealing furnace, whose schematic illustration was shown as Fig. 3.5. The annealing was performed by six infrared lamps surrounding the sample stage which were made of carbon and coated by

SiC. The heating temperature was controlled by thermocouple feedback.

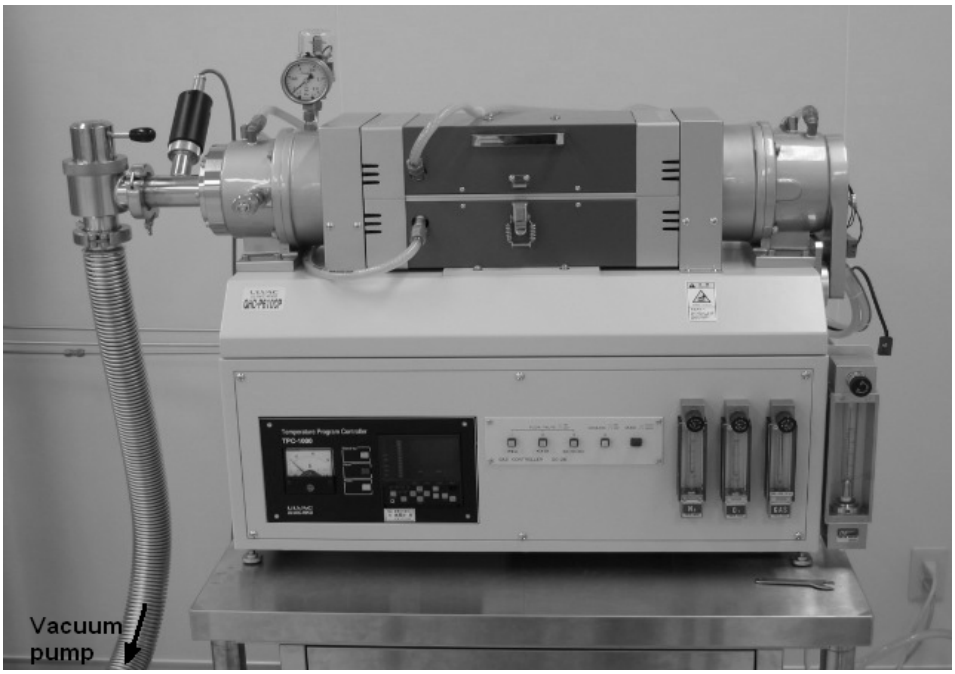


Fig. 3.4 Photo of infrared annealing furnace

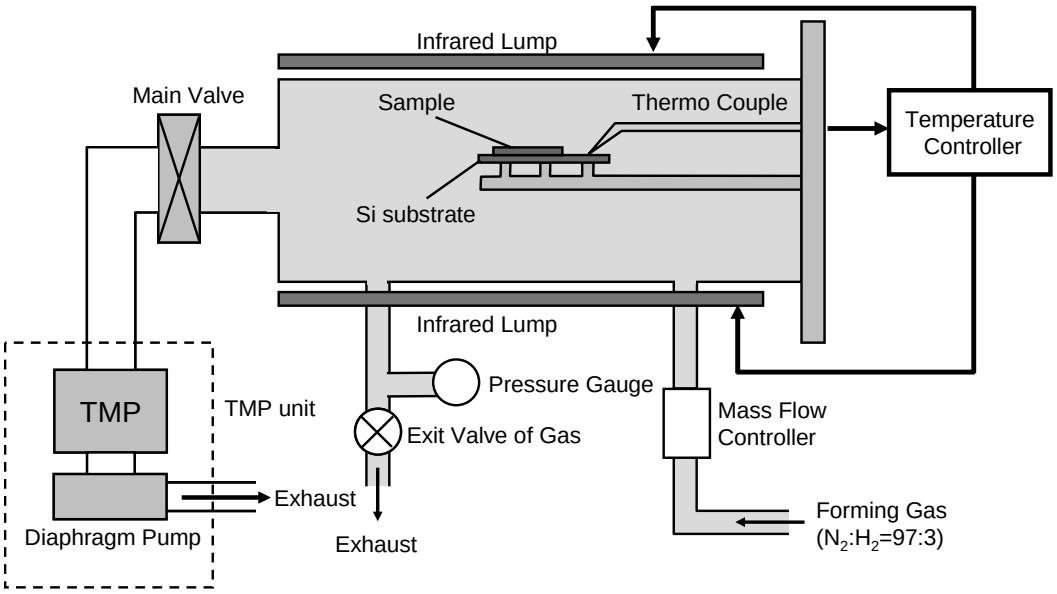


Fig. 3.5 schematic image of infrared annealing furnace

3.1.4 Vacuum Thermal Evaporation Method

All of Al metals in this work were obtained from deposition with bell jar vacuum thermal evaporation shown as Fig. 3.6. Fig. 3.7 illustrates a schematic drawing for vacuum thermal evaporation system. Filament is made of tungsten, was used for heating the Al source up to its vapor temperature. Both filaments and Al sources are made of Nilaco, inc. with material purity of 99.999%.

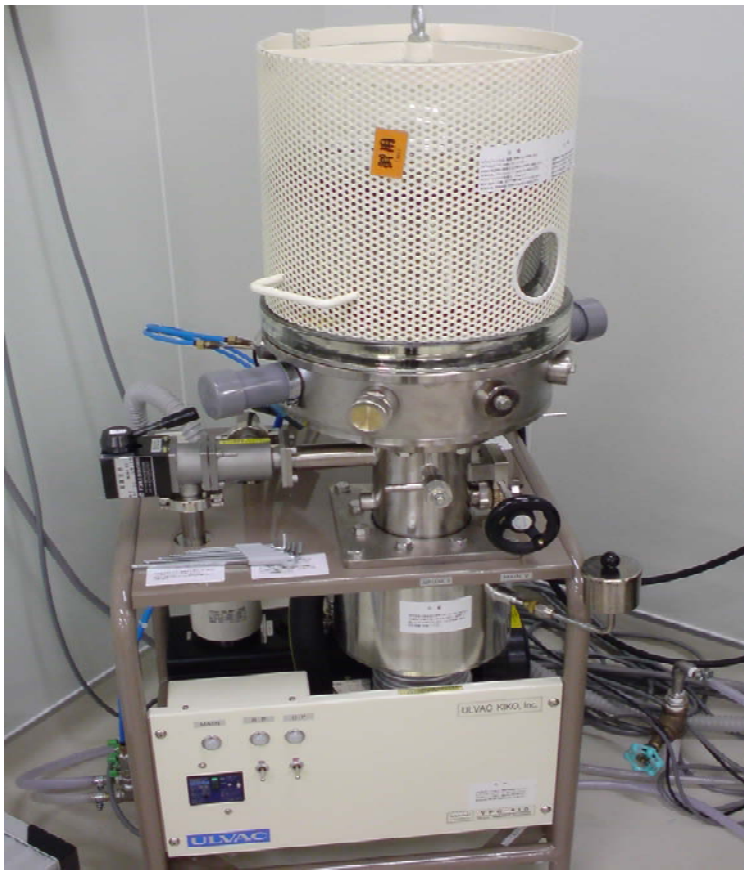


Fig. 3.6 Photo of bell jar

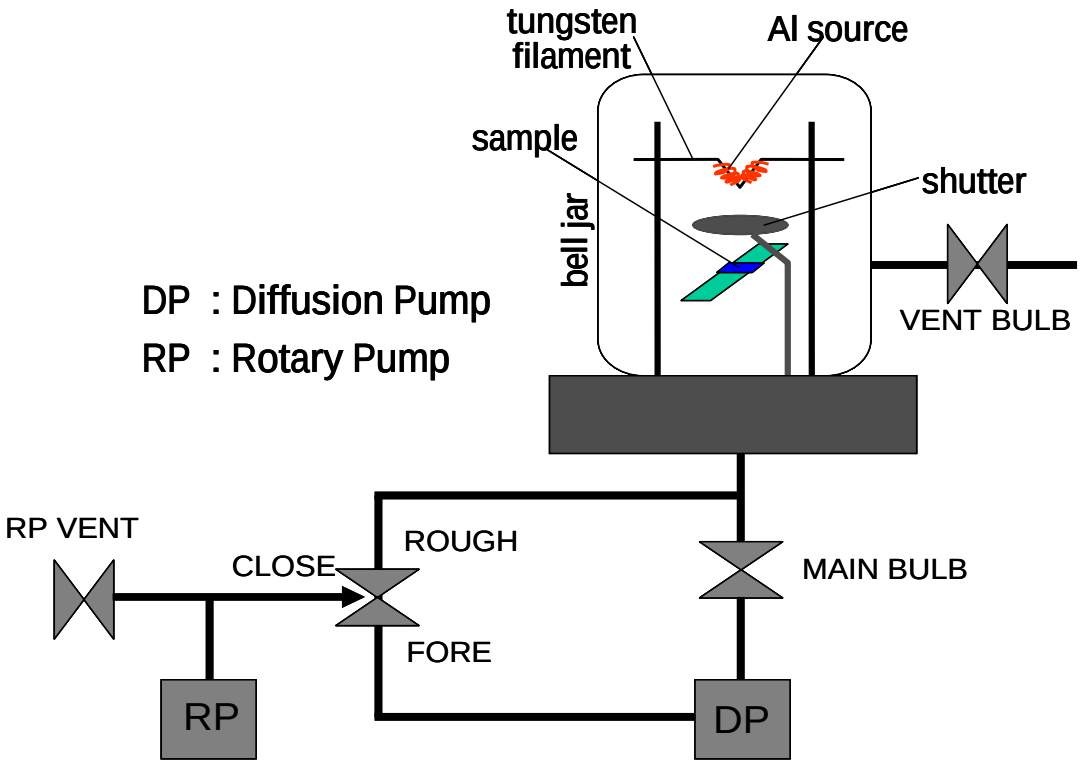


Fig. 3.7 Schematic drawing for vacuum thermal evaporation system.

The physics of vacuum thermal evaporation is based on thermodynamics of the evaporated materials. There have been experiments performed for evaluating the thermodynamic properties of material. Careful evaluation may reveal that the vapor pressure of liquid Al is given by the following.

$$\log P_{torr} = \frac{15{,}993}{T} + 12.409 - 0.999 \log T - 3.52 \times 10^{-6} T \qquad (3.1)$$

Neglecting the last two terms, the Arrhenius character of log P vs. 1/T can be essentially preserved. Fig. 3.8 presents thermal equilibrium for metal evaporations in form of Arrhenius plots. The dot marks are the metal melting points. Two modes of evaporation can be distinguished in practice, depending whether the vapor effectively emanates from liquid or solid source. Usually, a melt will be required if the element in

question does not achieve a vapor pressure greater than 10^{-3} torr at its melting point. Most metals, like Al, Ag, Au, and so on, fall into this category, and effective film deposition is attained only when the source is heated into the liquid phase. On the other hand, elements such as Cr, Ti, Mo, Fe, and Si reach sufficiently high vapor pressures of 10^{-2} torr some 500°C below the melting point.

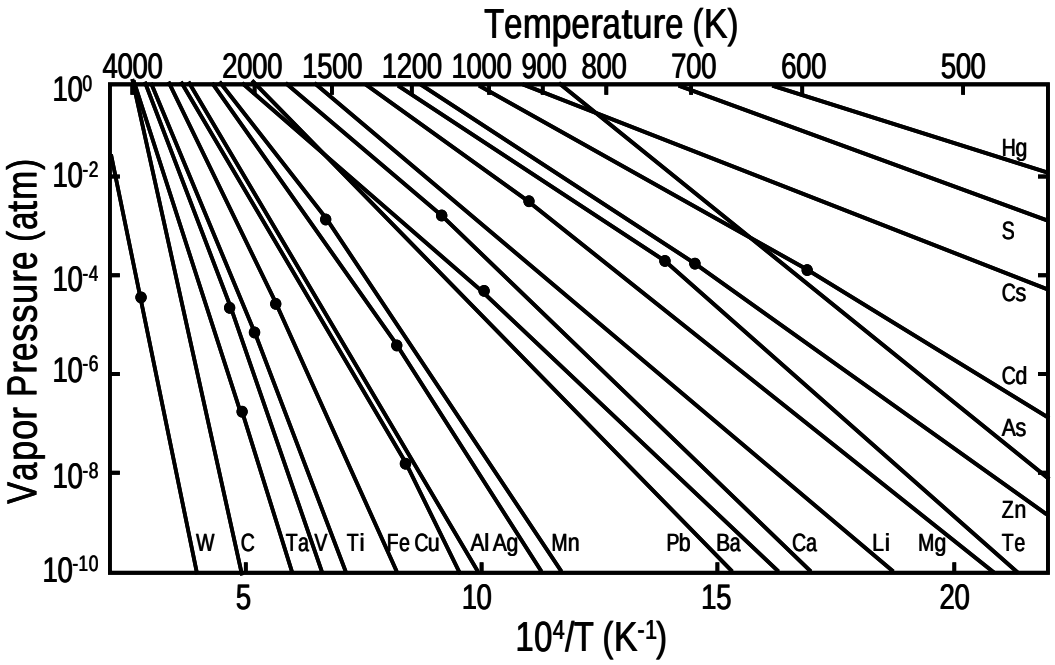


Fig. 3.8 Thermal equilibrium for metal evaporations in form of Arrhenius plots. The dot marks are the metal melting points.

3.1.5 Photolithography

The process flow of photolithography that used throughout this study is shows in Fig. 3.9. Electrical hotplate is used for baking purposes. The spin-coated layer photoresist was aligned and exposed through tungsten coated e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. MJB4 of Karl Suss contact-type mask aligner as shown Fig. 3.10 was used for aligning and exposition purposes. The exposure duration was set to 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.) after dipped into the solvent for 2 minute and baked at 130 ˚C for 5 minutes.

Fig. 3.9 The process flow of photolithography

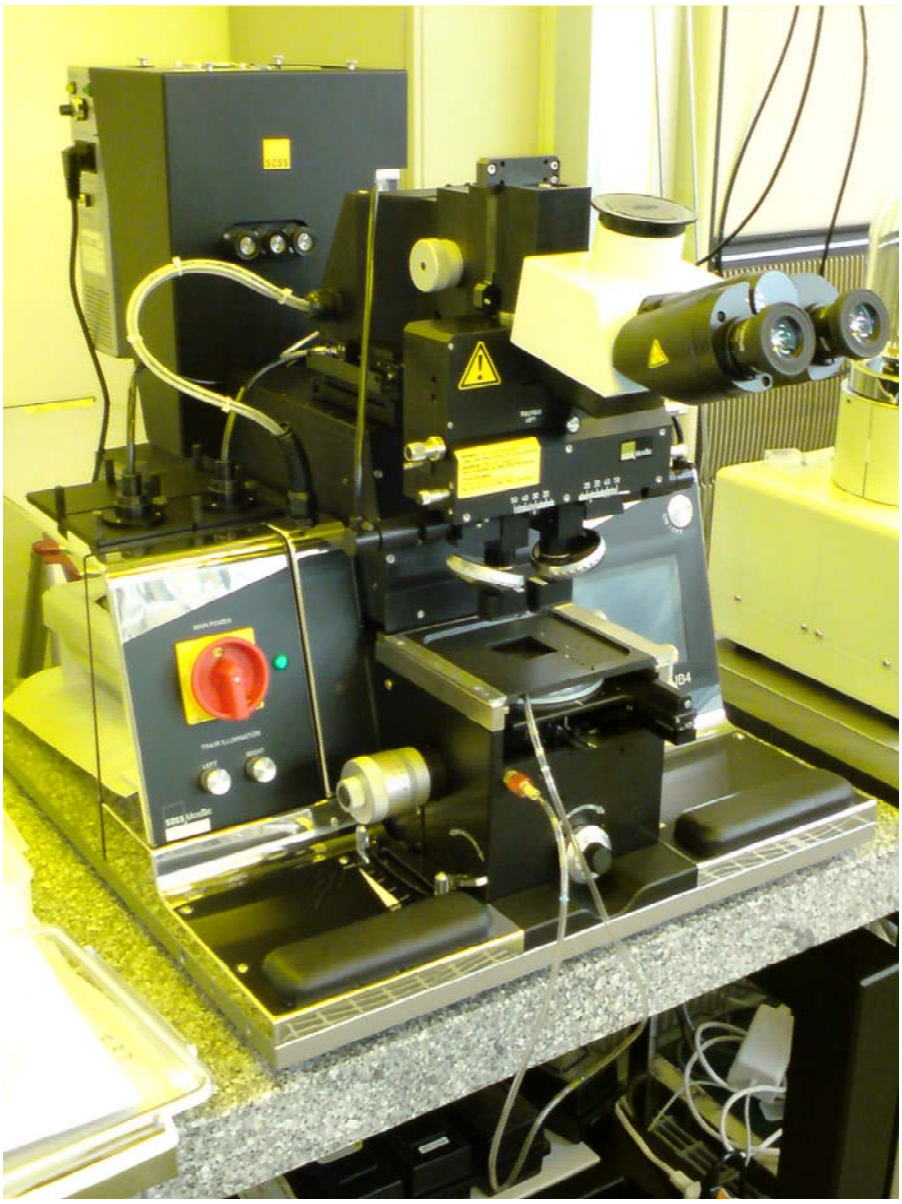


Fig. 3.10 Photo of mask aligner

3.2 Measurement Methods

3.2.1 Scanning Electron Microscope (SEM)

The Scanning Electron Microscope (SEM) as shown Fig. 3.11 is a microscope that uses electrons rather than light to form an image. There are many advantages to using the SEM instead of a light microscope. The SEM has a large depth of field, which allows a large amount of the sample to be in focus at one time. The SEM also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. Preparation of the samples is relatively easy since most SEMs require the sample to be conductive. The combination of higher magnification, larger depth of focus, greater resolution, and ease of sample observation makes the SEM one of the most heavily used instruments in research areas today. The SEM uses electrons instead of light to form an image. A beam of electrons is produced at the top of the microscope by heating of a metallic filament. The electron beam follows a vertical path through the column of the microscope. It makes its way through electromagnetic lenses which focus and direct the beam down towards the sample. Once it hits the sample, other electrons (backscattered or secondary) are ejected from the sample. Detectors collect the secondary or backscattered electrons, and convert them to a signal that is sent to a viewing screen similar to the one in an ordinary television, producing an image.

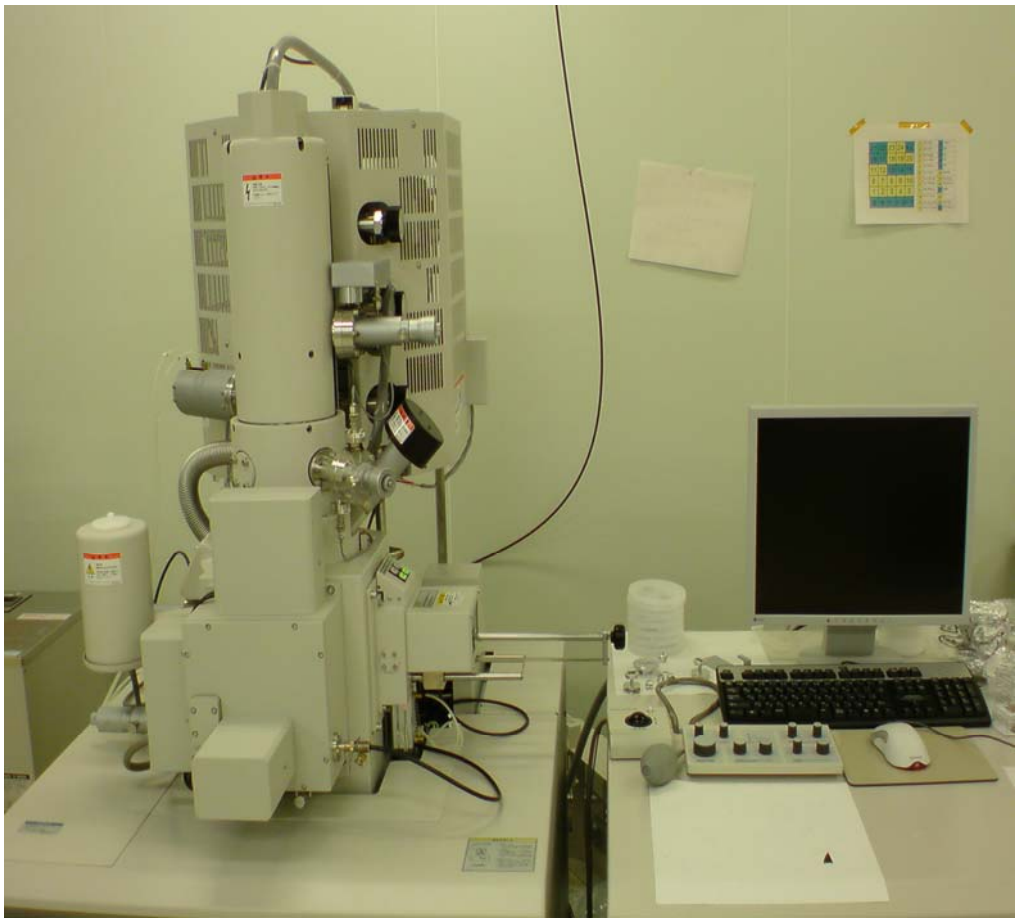


Fig. 3.11 Photo of SEM

3.2.2 Four-Point Probe Technique

The sheet resistance of Ni silicide was measured by four-point probe technique. The phase of Ni can be ascertained according to the sheet resistance of Ni silicide thin film, because the sheet resistance of $NiSi_2$ is greatly different from that of Ni monosilicide (NiSi) or other phase such as Ni_2Si.

The four-point probe technique is one of the most common methods for measuring the semiconductor resistivity because two-point probe method is difficult to interpret. The sheet resistance is calculated form potential difference between inside 2 terminals (between B probe and C probe) after applying the current between outside 2 terminals (between A probe and D probe) as shown in Fig. 3.13. The resistance by two-probe technique is higher than accurate resistance because it includes the contact resistance (R_C) between metal probe and semiconductor surface and spreading resistance (R_{SP}) of each probe. Neither R_C nor R_{SP} can be accurately calculated so that semiconductor resistance (R_S) cannot be accurately extracted from the measured resistance. On the other hand, four-probe technique can neglect these parasitic resistances because the current value which flows between terminals is very small and potential drop can be disregarded. In this study, sheet resistance was measured by four-probe technique.

For an arbitrarily shaped sample the sheet resistance (ρ_{sh}) is given by

$$\rho_{sh} = V/I * CF \qquad (3.2)$$

where *CF* is correction factor that depends on the sample geometry. If the distance among probes (s; in this study, s=1 mm) is greatly shorter than the width of a sample (d), *CF* equals to $\pi/\ln(2)=4.53$.

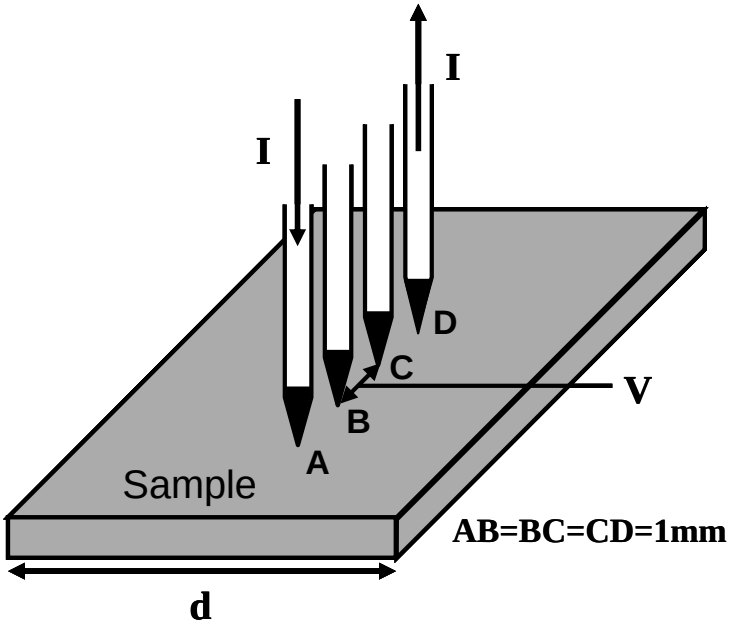


Fig. 3.12 illustration of four point probe system

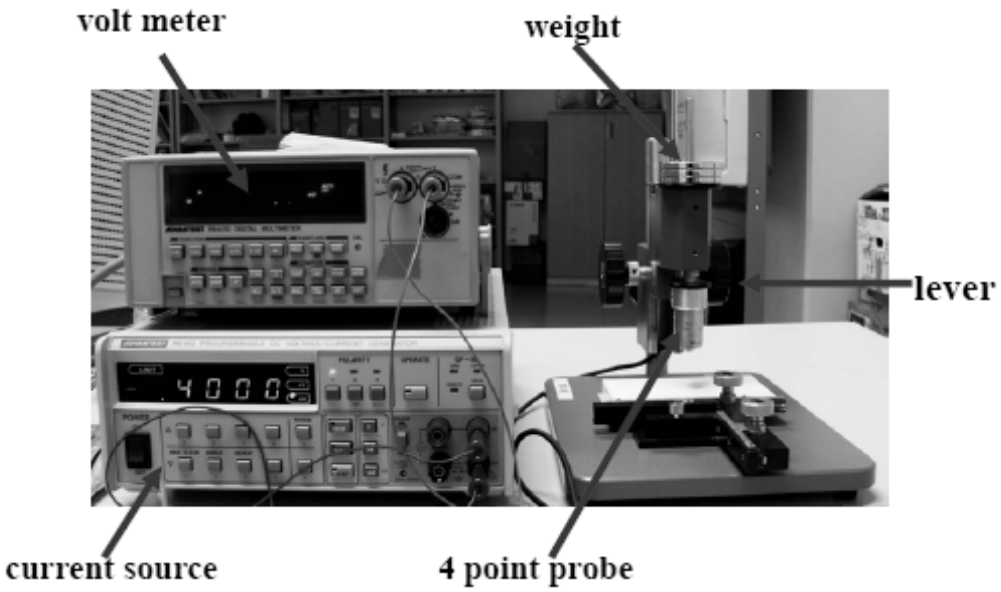


Fig. 3.13 Photo of four probe system

3.2.4 J-V (Leakage Current Density – Voltage) Measurement

To estimate the leakage current density, *J-V* characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard.).

3.2.5 Evaluation of Schottky Barrier Height Based J-V Characteristics

When, the case of V>>kT/q, the index term is more larger than 1, it can be ignored. The current density **(*J*)** of schottky contacts is defined

$$J = J_0 e^{qV/kT} \qquad (3.3)$$

However, the current density of obtaining actual characteristics increases the index function against bias voltage. The increasing rate is less than (3.3). Therefore, the ideal factor **(*n*)** is used as same as pn junction

$$J = J_0 e^{qV/nkT} \qquad (3.4)$$

If n is equal to 1, (3.4) accords with (3.3), and the current density flows along theory, but usually $n>1$.

Another, J_0 is expressed

$$J_0 = A^* T^2 e^{-\phi_B/nkT} = \frac{4\pi q m_e^* k^2 T^2}{h^3} e^{-\phi_B/kT} \qquad (3.5)$$

A^*, k and m^*_e are Richaldson constant, Boltman's Constant and effective mass. From (3.5), ϕ_B can be got from J_0.

Chapter 4

CHARACTERISTICS OF Ni Silicide SCHOTTKY DIODE

4.1 Ni Silicide Schottky Diode with Er Interlayer

4.1.1 Introduction

As stated chapter 2, it's so important for schottky barrier MOSFET to select materials because on current of SB-MOSFET is controlled by a tunneling current at the source edge and a tunneling current depends on schottky barrier height. NiSi has an experimental SBH of 0.65 eV on n-Si(100). This high SBH value hinders the application of NiSi in SB-MOSFETs. If we can lower the SBH of silicides to very low value, the device exhibits the same intrinsic performance as conventional MOSFET but also benefits from the advantages of SB-MOSFETs as mentioned chapter 1. At the same time, keeping resistance of silicide low value is also important.

In this chapter, we use a Schottky-barrier-height modulation for Ni silicide by inserting a thin Er interlayer between Ni and Si before silicidation process. We measure resistivity of Ni silicide on SOI substrate with Er interlayer, and using the value of resistivity we optimize annealing temperature of Ni silicide with Er interlayer. In the optimum range of annealing temperature we modulate schottky barrier height for Ni silicide.

4.1.2 Fabrication Process of samples for measuring sheet resistance

Figure 4.1 shows fabrication process of the sample for measuring sheet resistance of the (NiEr)Si layer. The SOI wafers with 100-nm-thick p-type SOI layer were used as substrates. The wafers were cleaned in a mixed solution of H_2SO_4 and H_2O_2 followed by a chemical oxide removal by diluted HF. 55-nm-thick or 200-nm−thick Ni film was deposited onto the substrates. And Er interlayer with various thickness was inserted at interface between the 55-nm-thick Ni and Si. Silicidation was performed in N_2 at various temperatures for 1 minute. The un-reacted metal was removed by SPM. Finally, sheet resistance of samples were measured by the four terminals method.

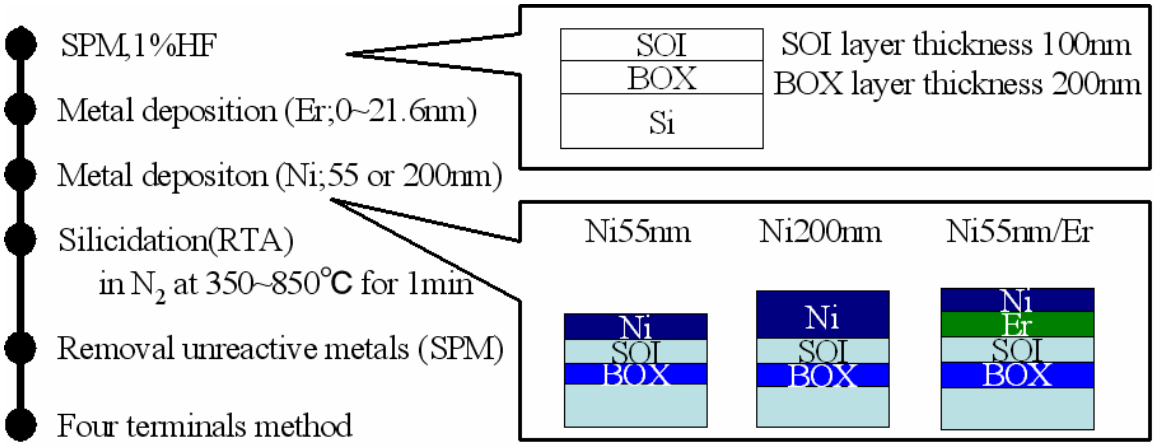


Figure 4.1 Fabrication process of samples for measuring sheet resistance.

4.1.3 Analysis of Ni Silicide

We measured sheet resistance of two samples described in Fig 4.1. In these two sampels Ni layer having the thickness of 55nm and 200nm was deposited on the SOI substrate, respectively. Figure 4.2 shows resistivity of the NiSi layer evaluated from sheet resistance measured. The same resistivity was obtained for both the Ni thickness of 55nm and 200nm. According to the reference, resistivity of NiSi, as indicated by a red line, is 14 $\mu\Omega$ · cm. [16]. At the annealing temperatures in the range from 450 to 850 ^{o}C, the resistivity obtained for two samples were close to that obtained for NiSi, indicating the formation of NiSi by silicidation at the temperatures of 450-850 ^{o}C.

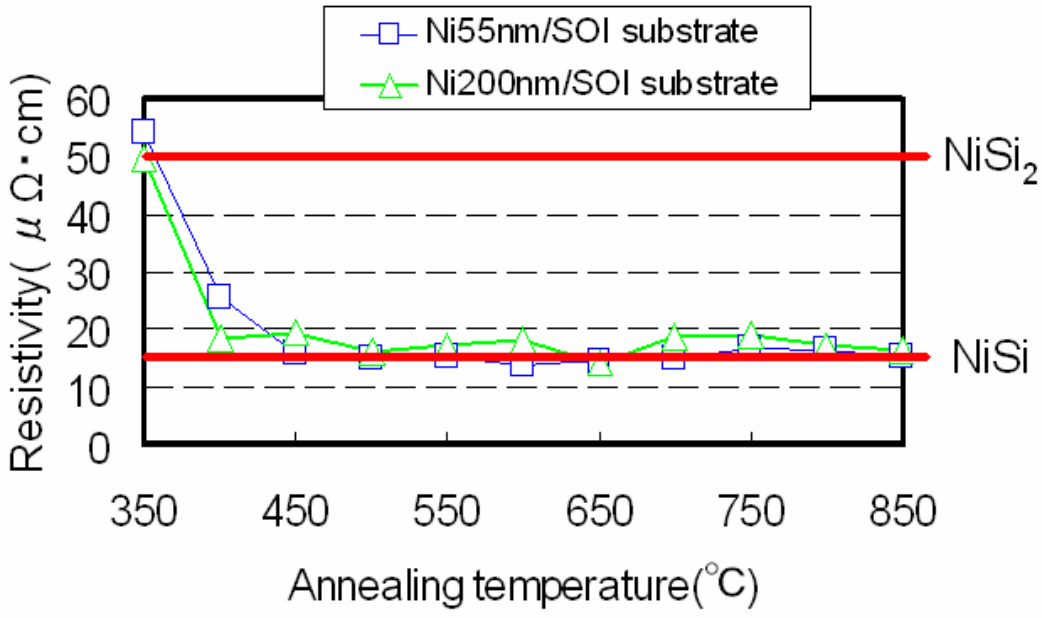


Figure 4.2 Resistivity of Ni-Si films on insulator as a function of annealing temperature.

4.1.4 Analysis of Ni Silicide with Er Interlayer

Figure 4.3 shows the resistivity of the sample with an Er interlayer with various thickness at the Ni/Si interface. The resistivity was slightly increased by inserting the Er interlayer. The resistivities of samples which inserted Er interlayer than annealing temperature 750°C significantly increased that indicates poor thermal stability. In particular when the Er thickness increased, the degradation became pronounced. Figure 4.3 also show that the annealing temperatures lower than 500°C were not enough to form NiSi in the samples inserted with Er interlayer. So in this structures, the optimum range of annealing temperature was 500-750 °C.

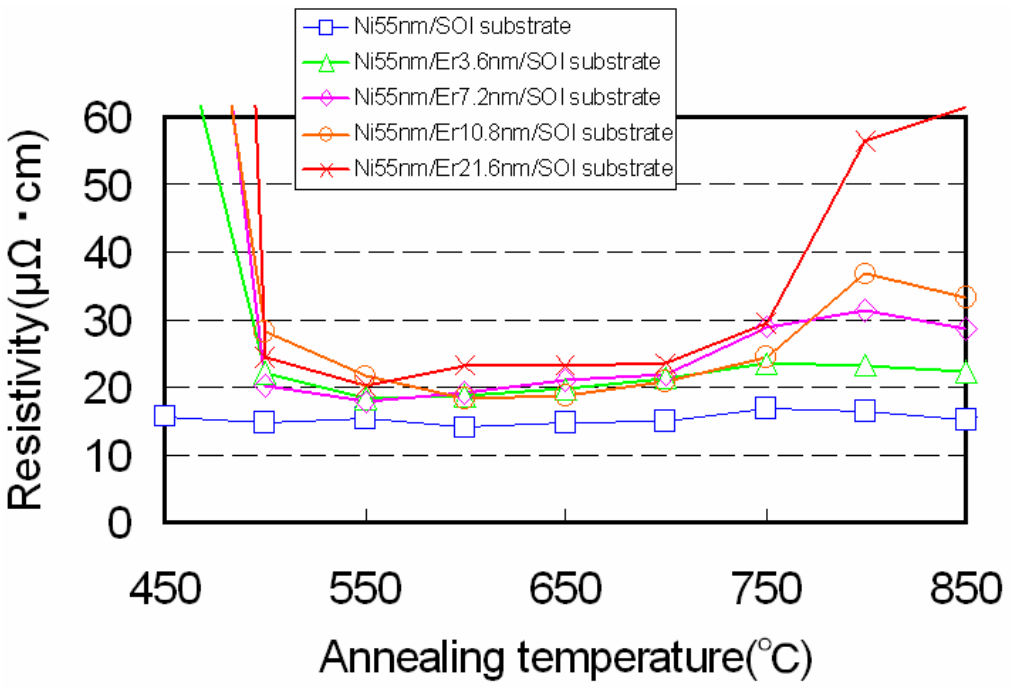


Figure 4.3 Resistivity of Ni silicide formed on SOI structures with or without Er versus annealing temperature.

4.1.5 Fabrication Process of Schottky Diode

Figure 4.4 shows fabrication process of Schottky diode. The diode was formed on SiO_2 isolated p-type bulk (100) Si wafers. The patterned wafers were cleaned in mixed solution of H_2SO_4 and H_2O_2 followed by chemical oxide removal by diluted HF. Pure metals of Er and Ni were deposited subsequently on to the substrates by DC sputtering in Ar gas at a pressure of 5.5×10^{-1} Pa. The layered structures of Ni/Er/Si consisting of 55-nm-thick Ni layer and Er layer of 0~21.6-nm-thick were formed. The samples were then annealed in N_2 at temperatures of 500~750^{o}C for 1 min. The un-reacted metal was removed by SPM. The backside Al-contact was finally formed. The Schottky barrier heights of the fabricated diodes were evaluated from current voltage (*I-V*) characteristics.

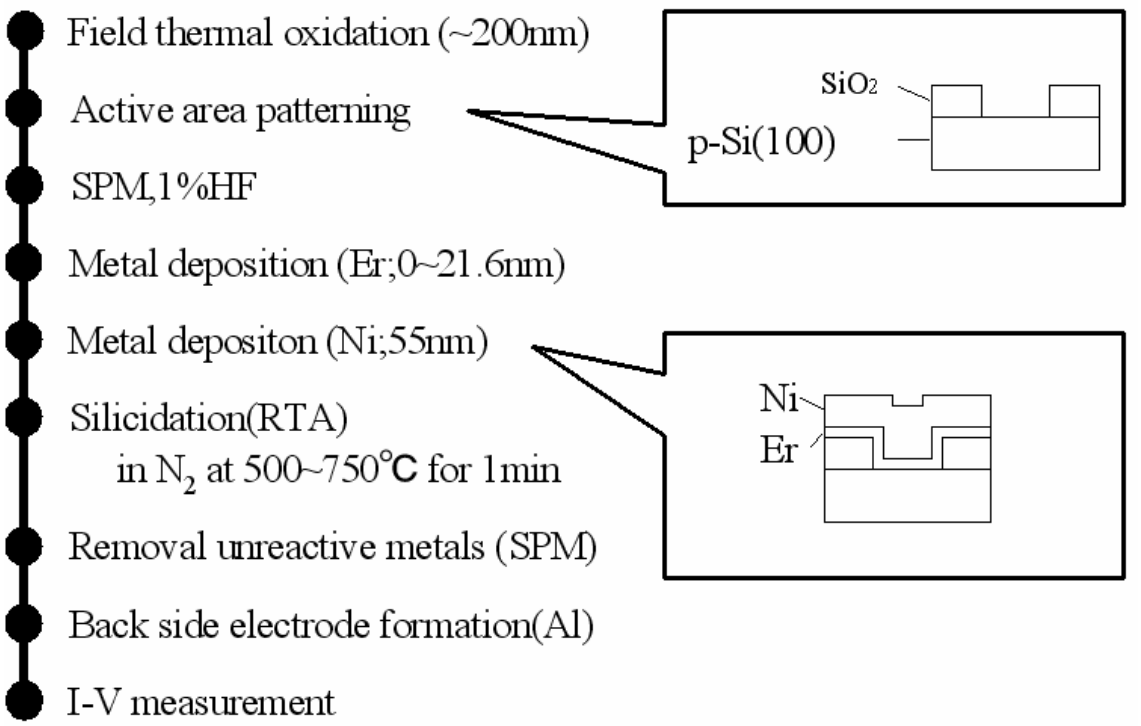


Fig. 4.4 Fabrication process of the Schottky barrier diodes from the initial structure of Ni/Er/Si

4.1.6 Characteristics of Ni Silicide Schottky Diode

Φ_b of the Ni(55nm)/p-Si structure was evaluated from the *I-V* characteristics in the forward bias region. Typical current-voltage (*I-V*) and curves of Schottky diodes of annealing temperature from 500°C to 750°C are shown in Fig. 4.5-4.6. Φ_b obtained by *I-V* characteristics were plotted against the annealing temperatures in Fig. 4.7. The observed Φ_b for holes were 0.431-0.440eV in the annealing temperature range of 500-750°C.

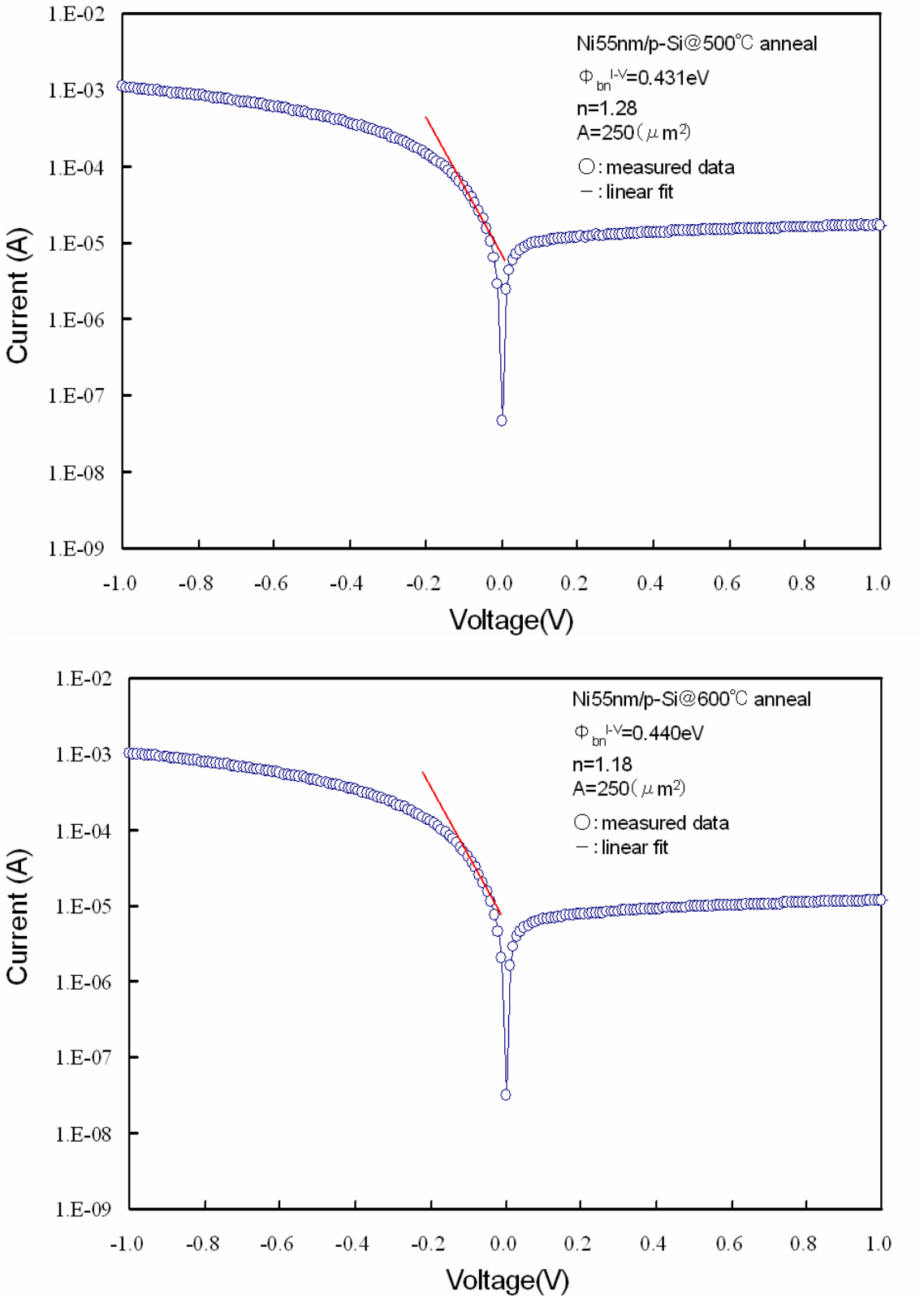


Fig. 4.5 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 500°C and 600°C

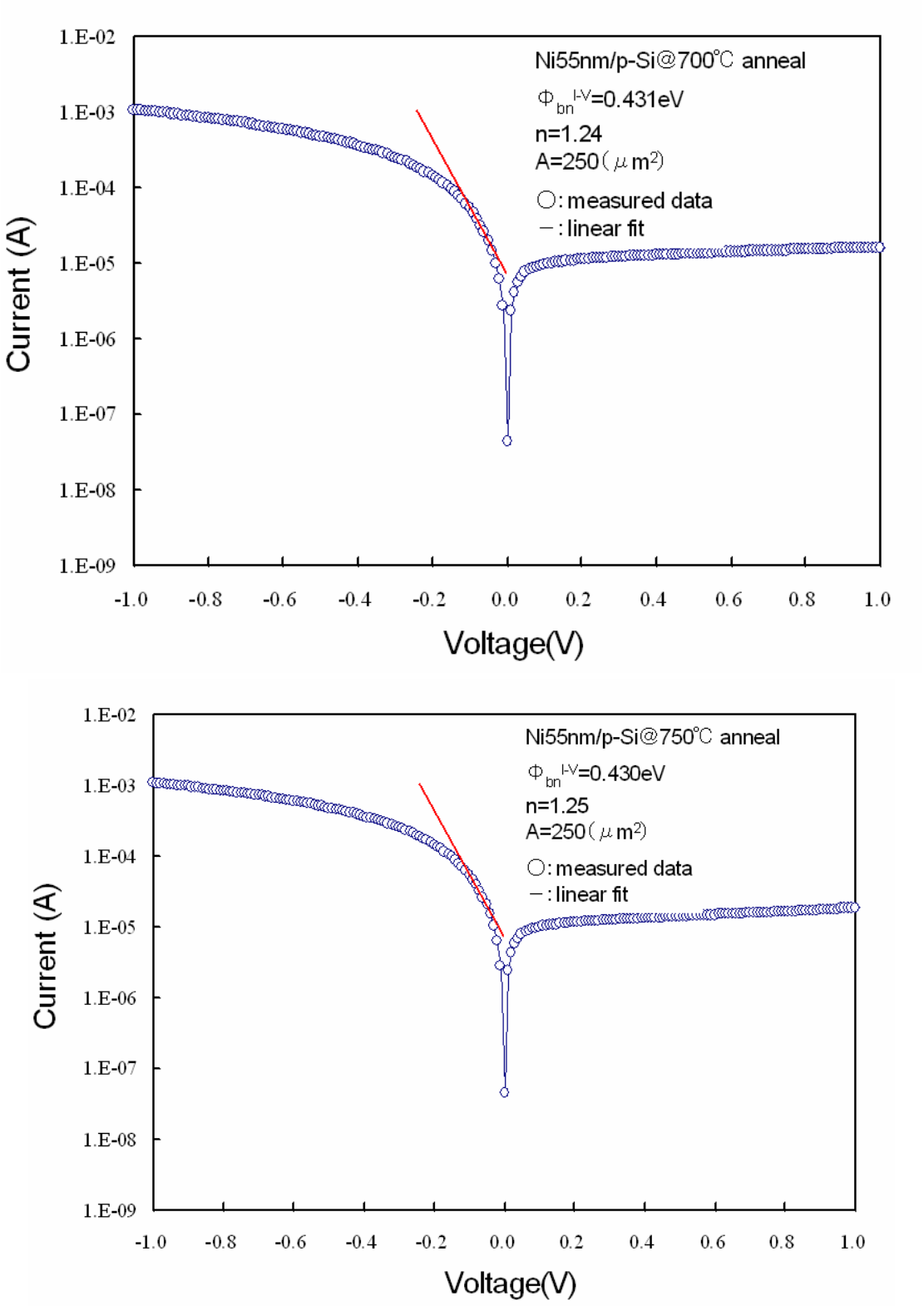


Fig. 4.6 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 700°C and 750°C

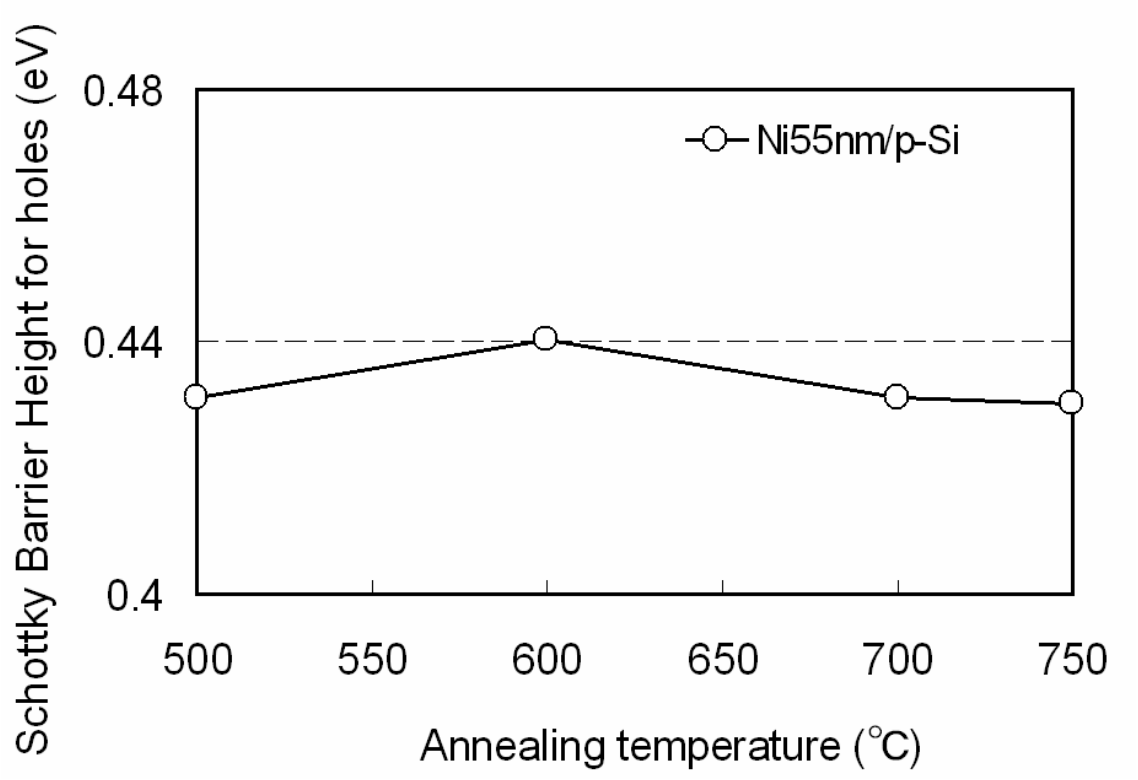
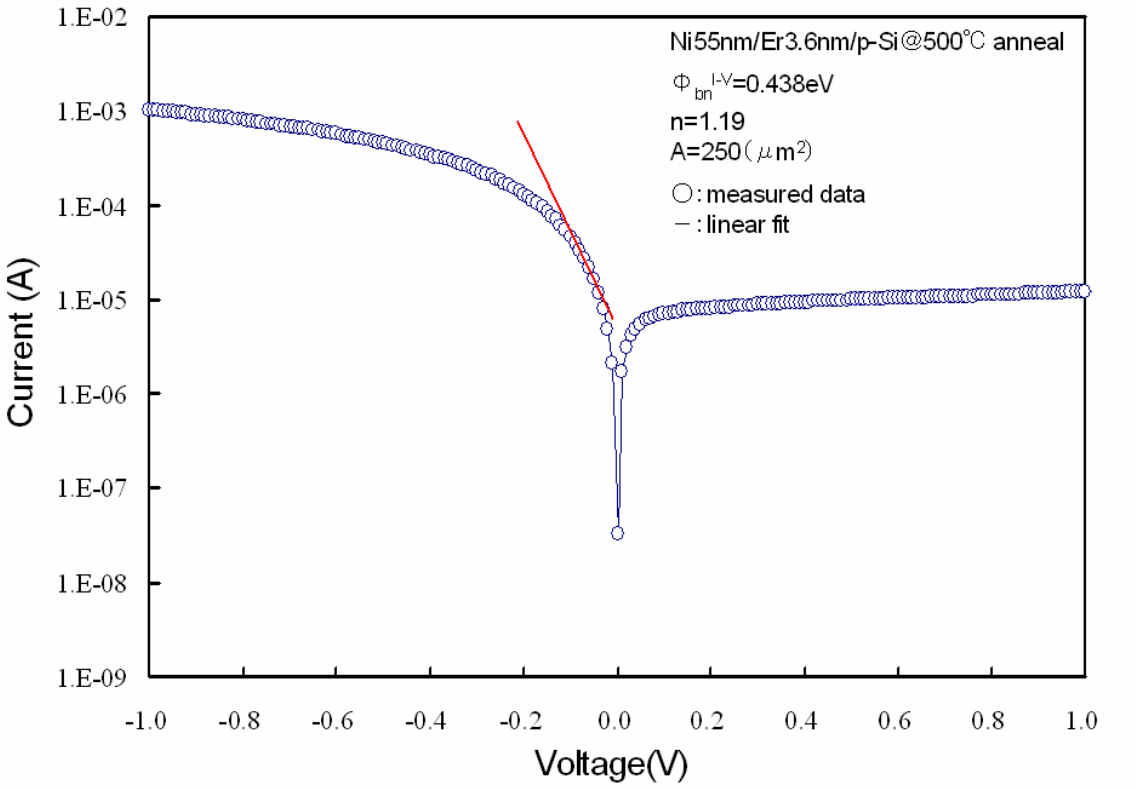


Fig. 4.7 Annealing temperatures dependence of Scottky barrier heights measured by I-V characteristics formed from the initial structures of Ni/p-Si.

4.1.7 Characteristics of Ni Silicide Schottky Diode with Er Interlayer

Typical current-voltage (*I-V*) curves of Schottky diodes of annealing temperature from 500°C to 750°C fabricated from the Ni/Er/p-Si structure is shown in Fig. 4.10-4.15. The Φ_b values for electrons evaluated from the *I-V* corves in the forward bias region are plotted as a function of the annealing temperature as shown in Fig. 4.16. The Φ_b for holes increased by inserting Er. This means that the Φ_b for electrons was lowered by the insertion of Er interlayer. The largest increase by 0.146eV in Φ_b for holes was observed for sample inserted with 21.6-nm-thick Er interlayer at 750°C. The modulation of Φ_b by 0.051eV was observed for sample inserted with 7.2-nm-thick Er interlayer at 600 °C compared with that of the samples without Er interlayer. In contrast, the sample inserted with 21.6-nm-thick Er was modulated only 0.015eV comparing to with 7.2-nm-thick Er. Therefore, the optimum thickness of Er interlayer might be around 7.2nm if the thermal stability of the Ni silicide films is also considered.



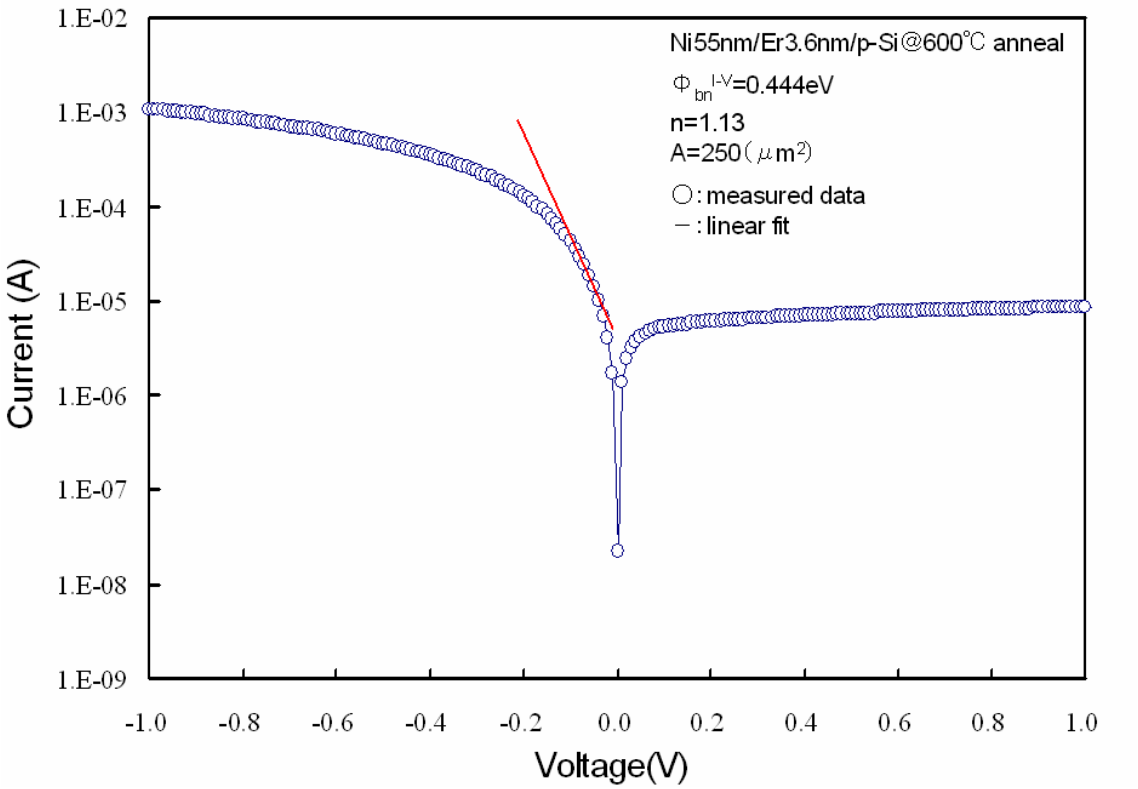
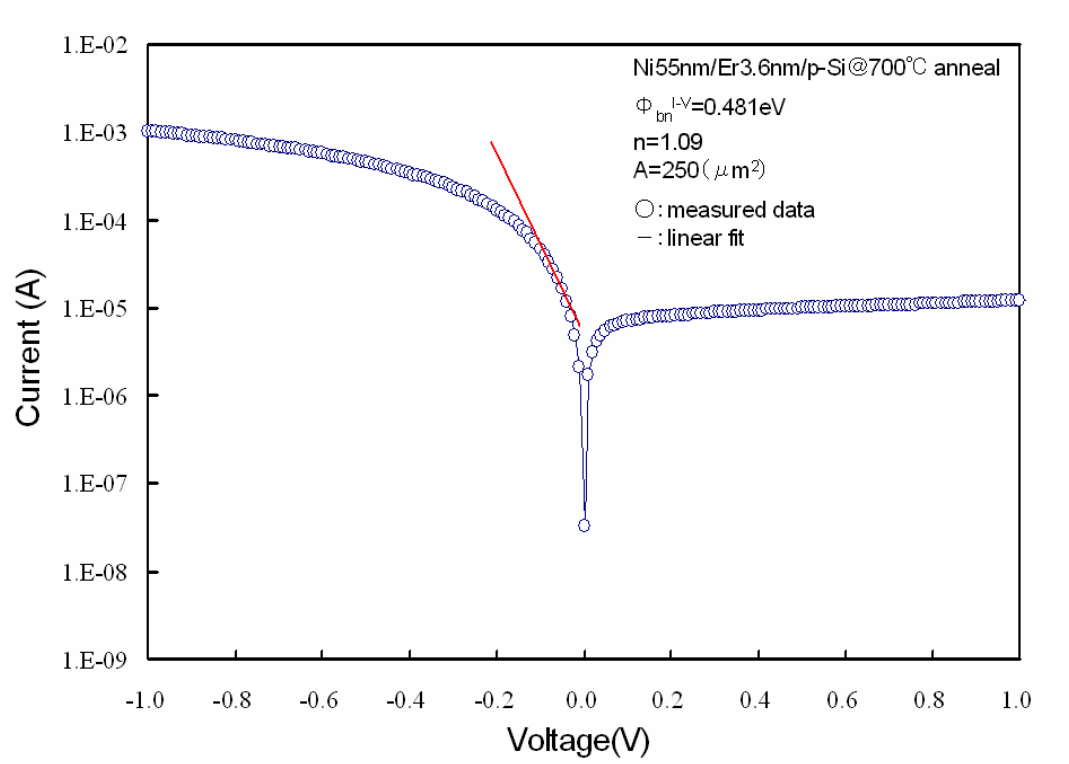


Fig. 4.8 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 500°C and 600°C



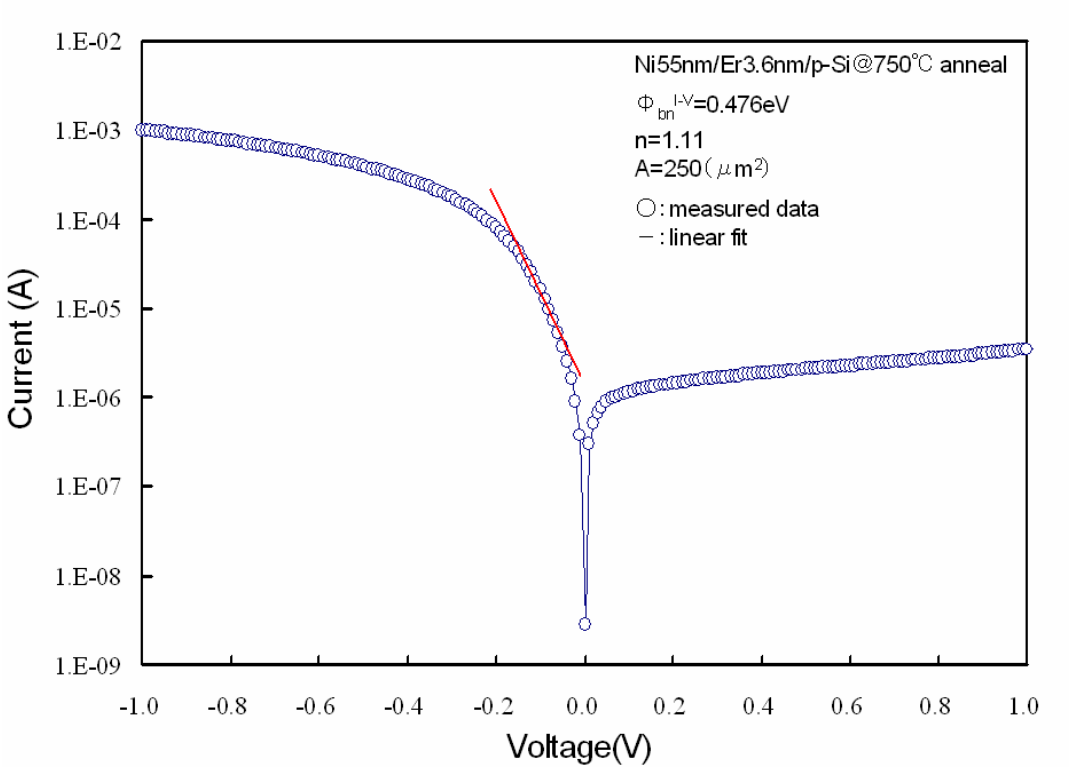
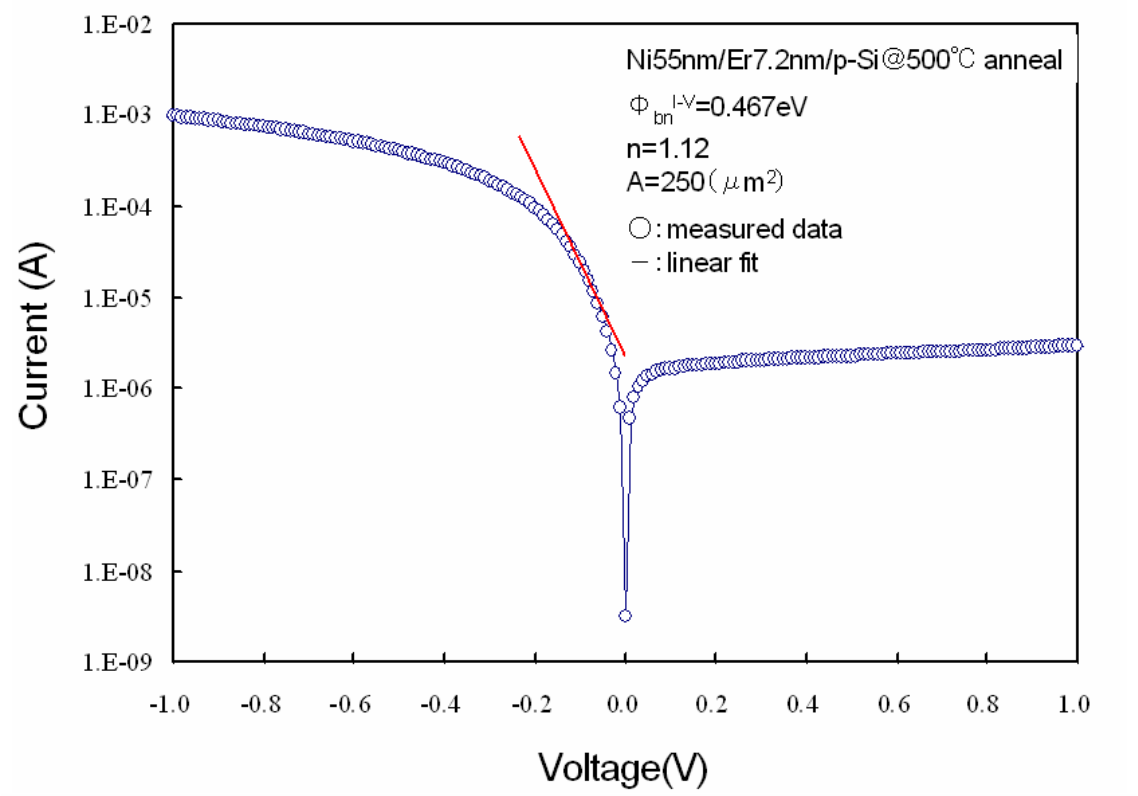


Fig. 4.9 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 700°C and 750°C



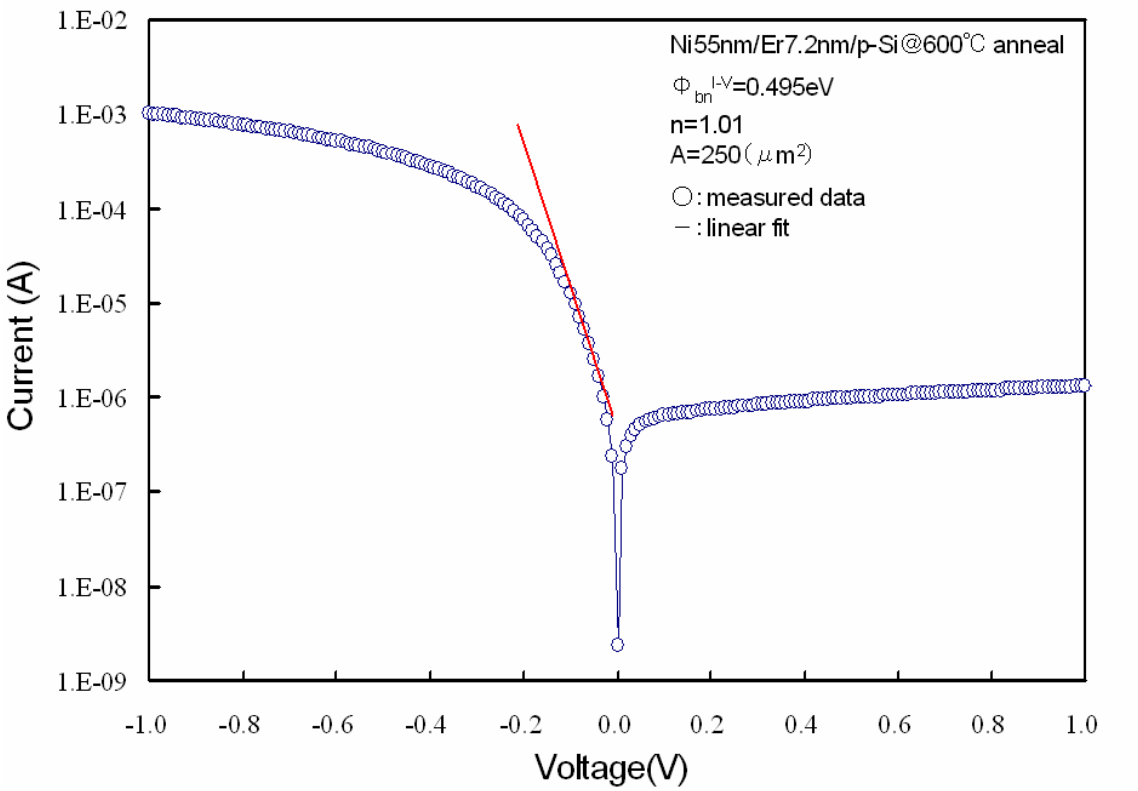


Fig. 4.10 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 500°C and 600°C

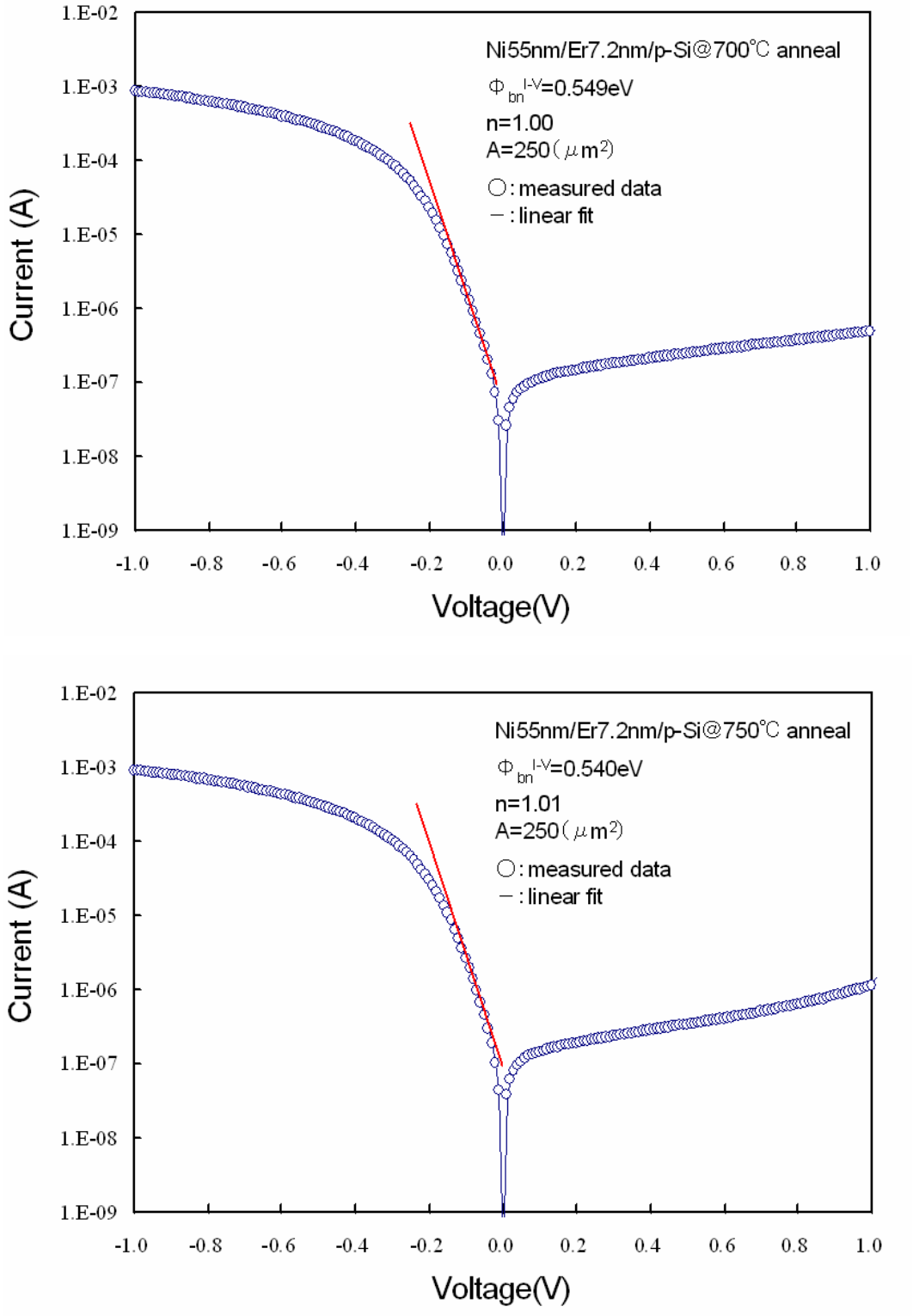


Fig. 4.11 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 700°C and 750°C

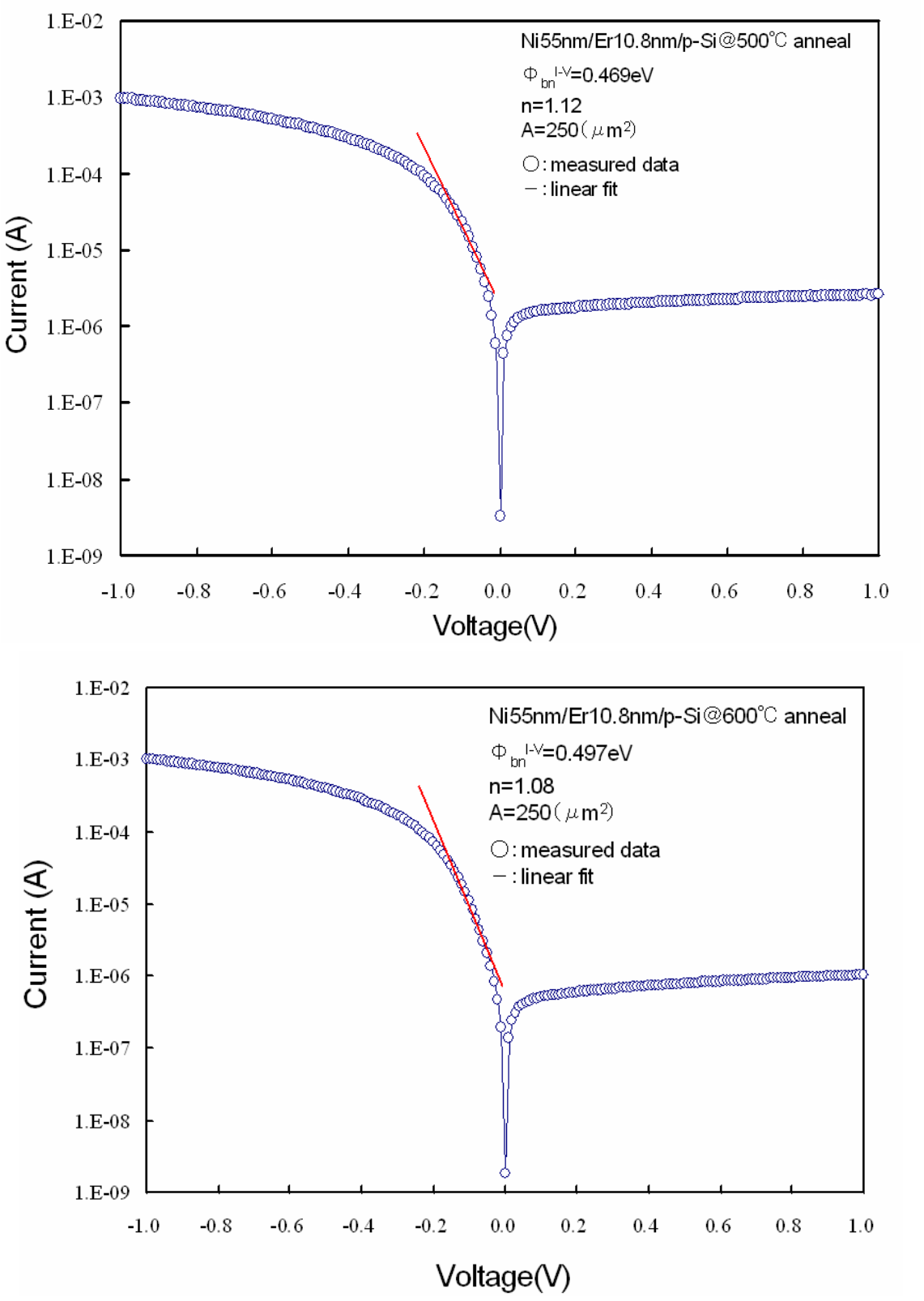


Fig. 4.12 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 500°C and 600°C

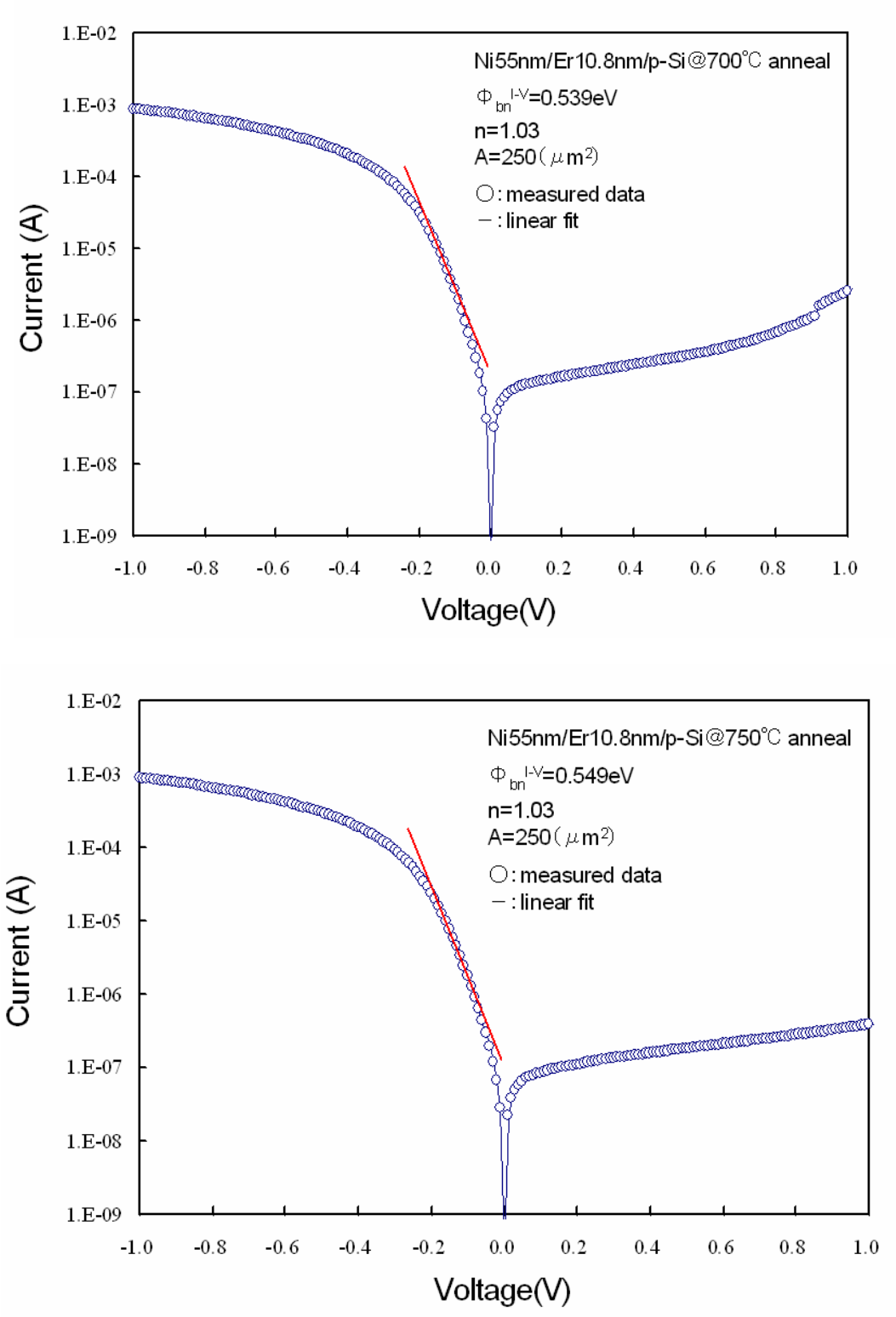


Fig. 4.13 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 700°C and 750°C

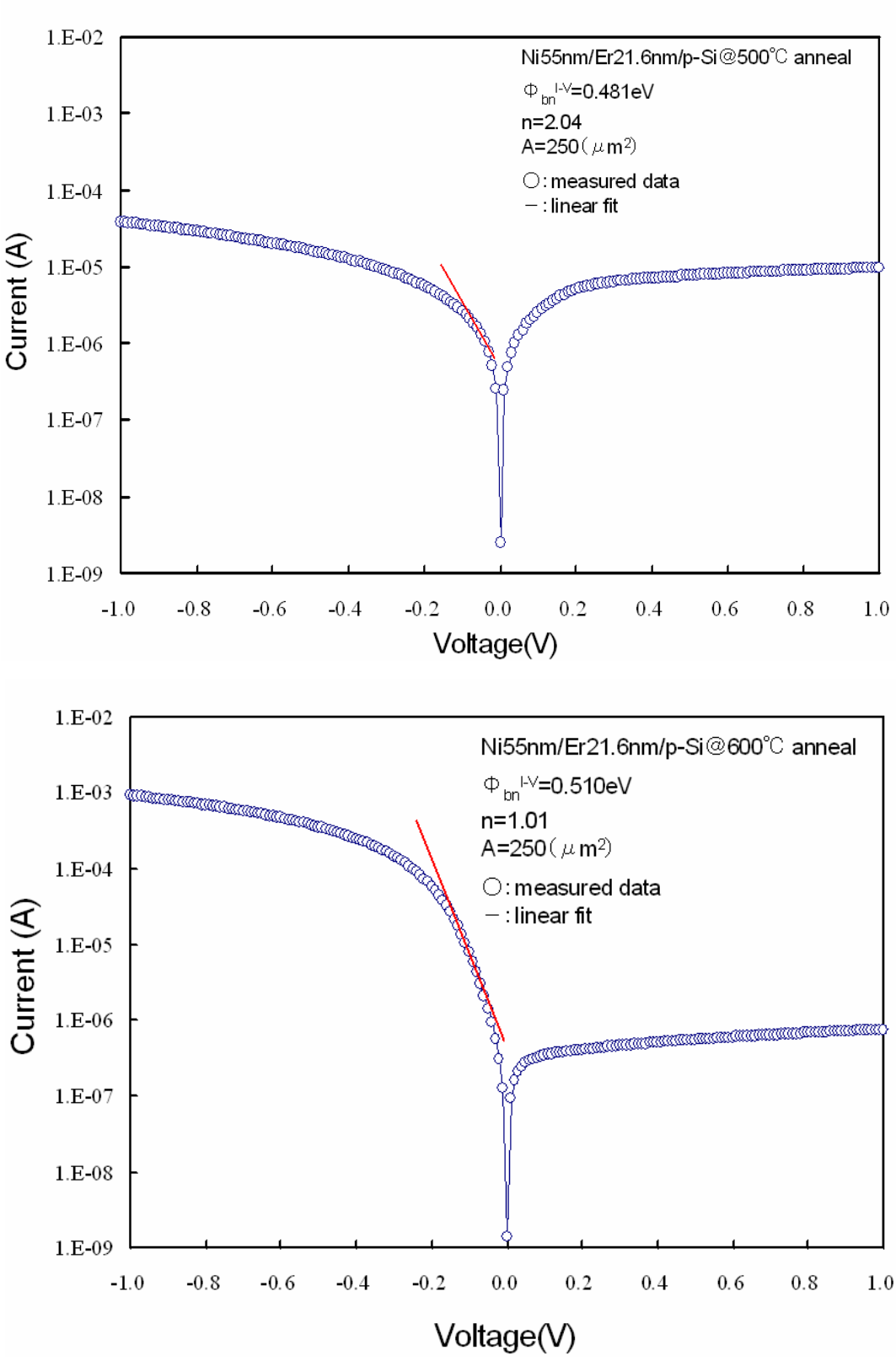


Fig. 4.14 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 500°C and 600°C

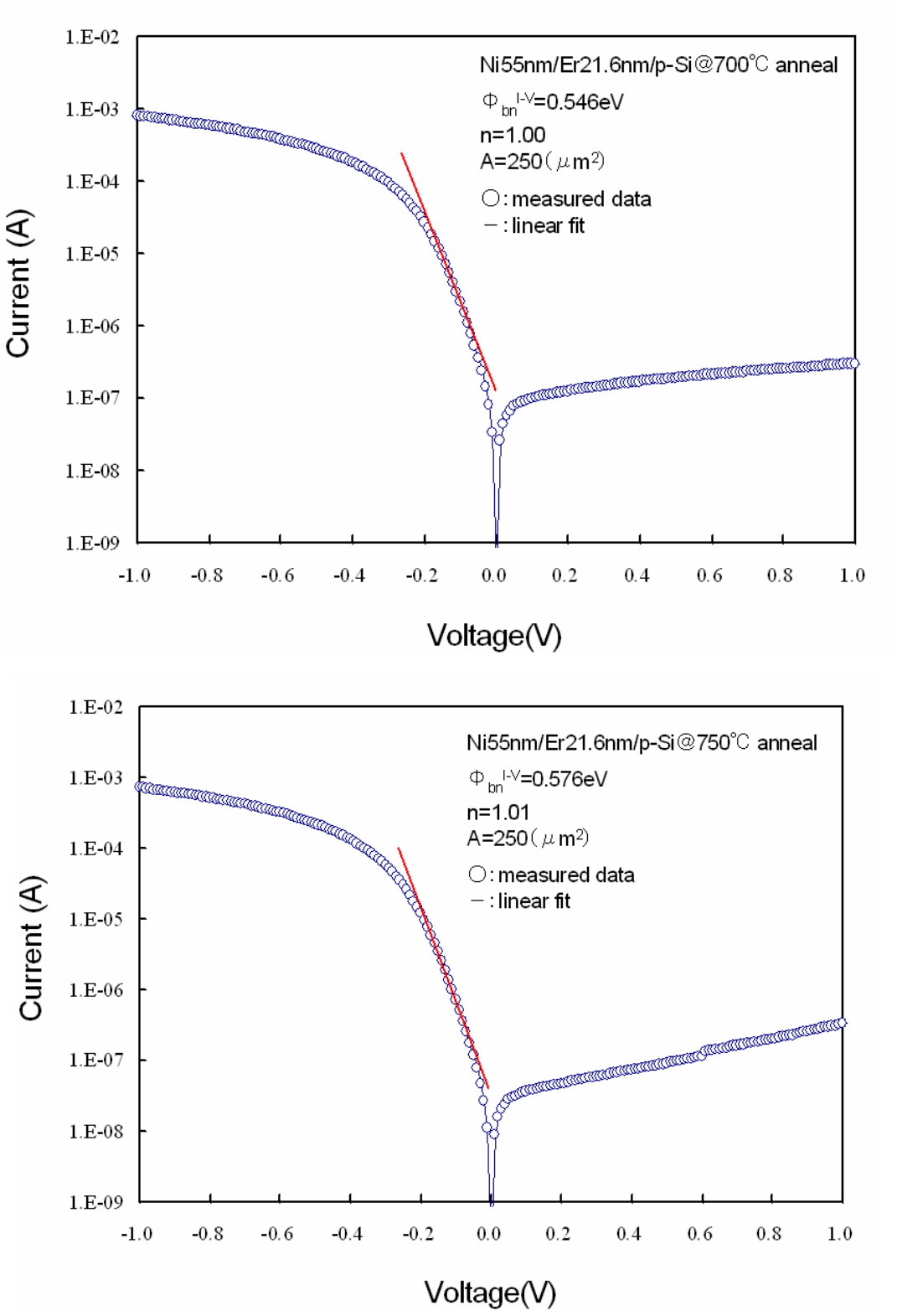


Fig. 4.15 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 700°C and 750°C

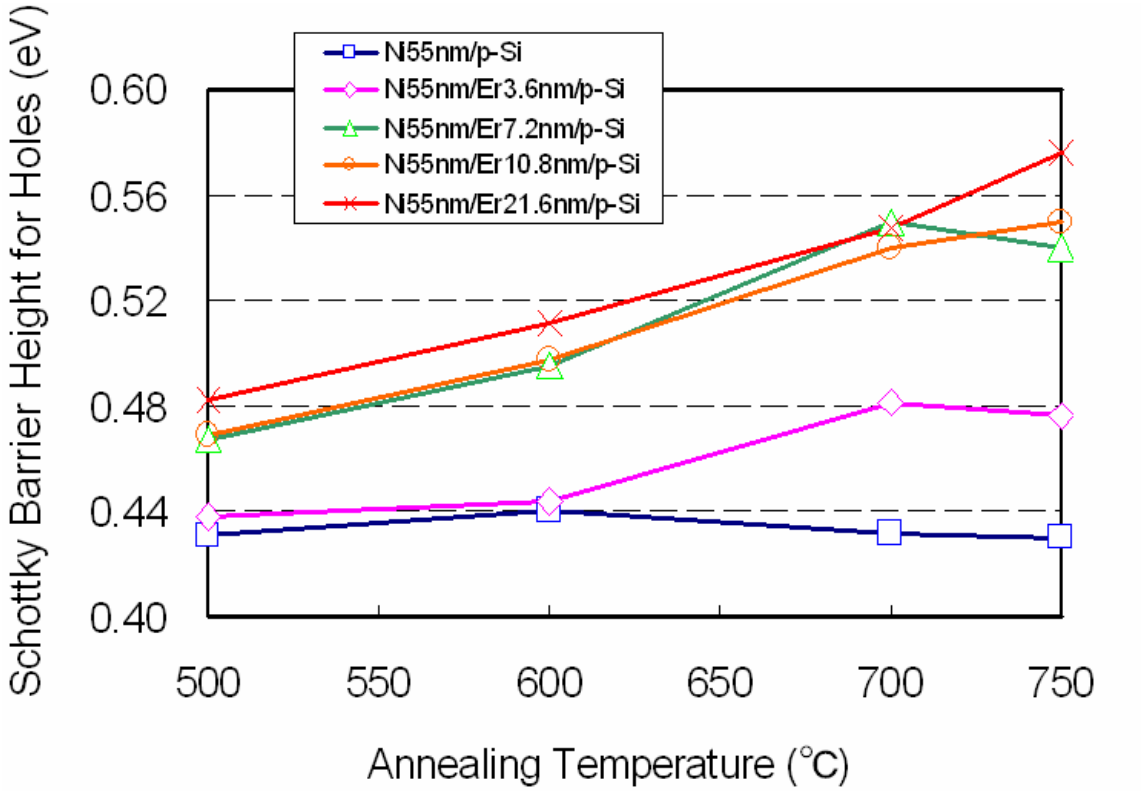


Fig. 4.16 Schottky barrier height for holes depending on annealing temperatures with various thicknesses of Er interlayer.

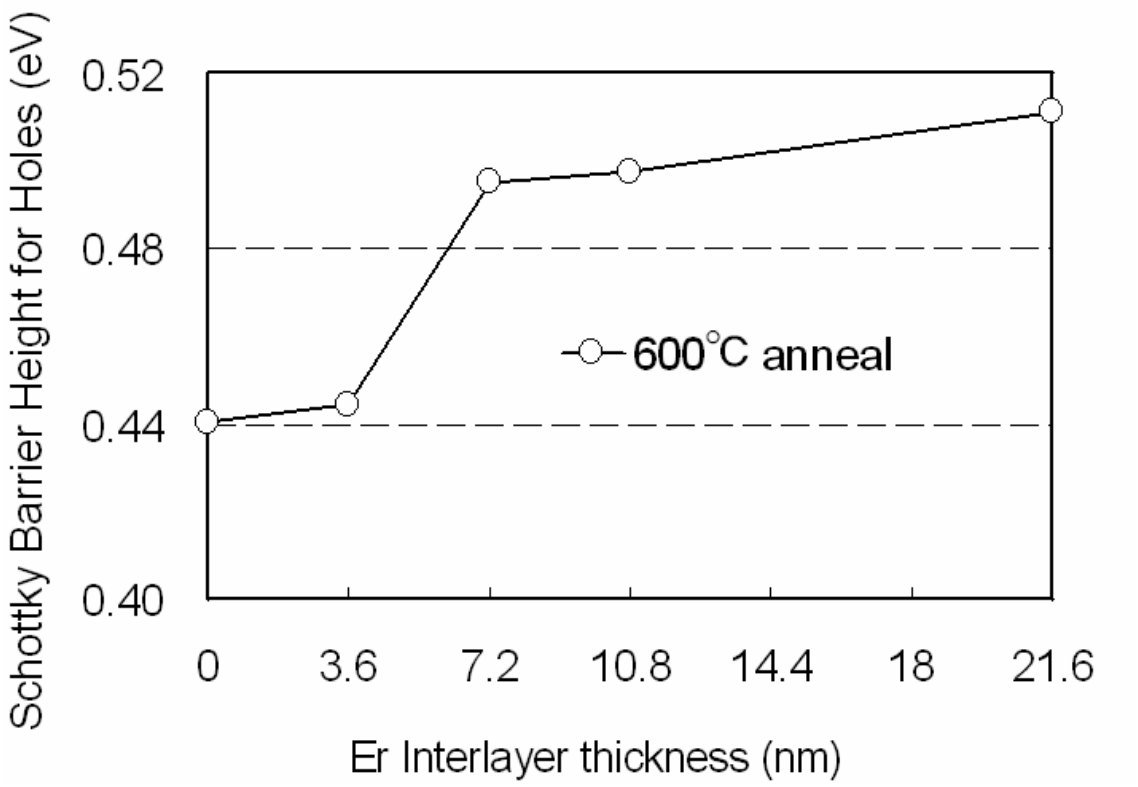


Fig. 4.17 Schottky barrier height for holes after annealing at 600°C depending on thickness of Er interlayer in the initial layered structure.

Chapter 5

SILICON ON INSULATOR SCHOTTKY BARRIER MOSFET WITH Er INTERLAYER

5.1 Introduction

The Schottky barrier source/drain MOSFET (SB-MOSFET) is one of promising candidates for next generation devices, thanks to its shallow junction depth with low electrode resistance and low process temperature [3,4]. However, the high barrier height (Φ_b) severely limits the drive current of SB-MOSFETs [14,15]. The Er silicide has been proposed for n-channel SB-MOSFETs because of very low Φ_b of 0.27-0.36 eV for electrons [7]. However, previous reports indicated that middle gap materials such as NiSi also had the great possibility for applications to SB-MOSFETs by employing the Φ_b modulation techniques [5].

In this chaper, we applied the technique of the Φ_b modulation by Er interlayer to n-channel SOI SB-MOSFETs fabrications and discussed Er insertion effect.

5.2 Ni Silicide SOI Schottky Barrier MOSFETs by With Er Interlayer

5.2.1 Fabrication Process and The Structure of SOI SB-MOSFET

Figure.5.1 shows fabrication process of SOI SB-nMOSFET. The MOSFET was formed on the SOI wafers with a 100-nm-thick p-type SOI layer and a 200-nm-thick BOX layer. The SOI layer was patterned by dry etching and SiO_2 layer was formed on the SOI layer by sputtering. After removing the SiO2 layer on the source/drain region, 55-nm-thick Ni films with and without 7.2-nm-thick Er interlayer were deposited. Silicidation was performed in N_2 at 600^oC for 1 minute. The un-reacted metal was removed by SPM. The backside Al gate electrode was finally formed.

Schematic of the fabricated SOI SB-MOSFET is shown in Fig. 5.2. Source and drain are formed by Schottky junction so that operation of SOI SB-MOSFET is realized. The SEM image of SB-MOSFET is shown in Fig. 5.3. Silicide is confirmed in the region of sorurce and drain. The thickness of SiO_2 was 200nm. The side of SiO2 was etched a little by the process. But it was not effected strongly to characteristiecs of SOI SB-MOSFETs.

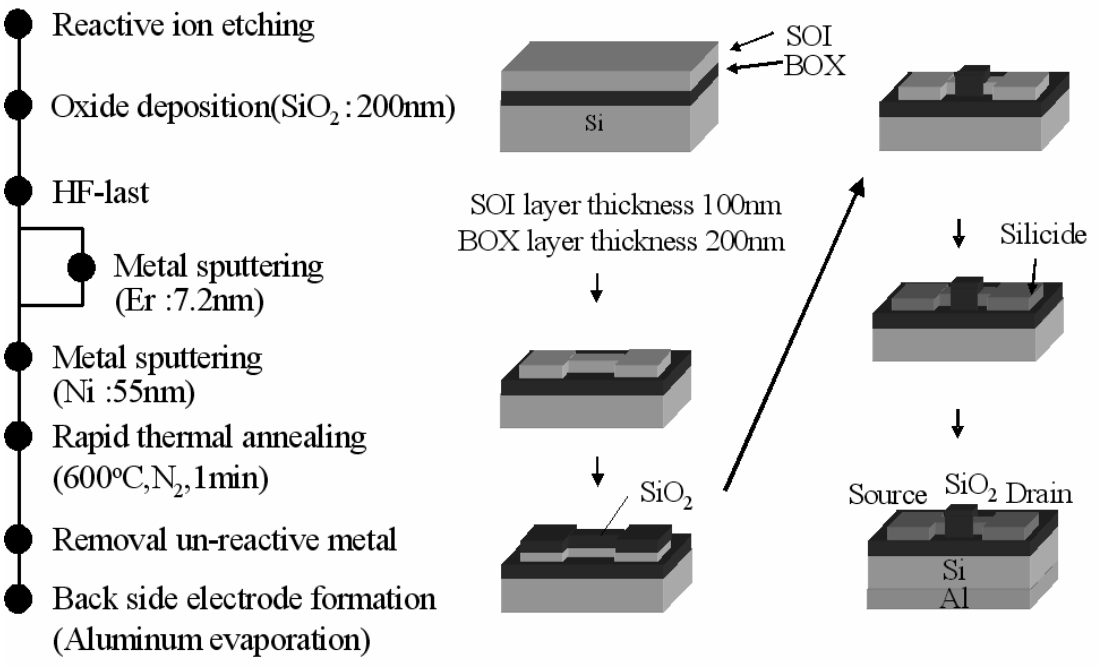


Figure.5.1 Fabrication process of SOI SB-nMOSFET.

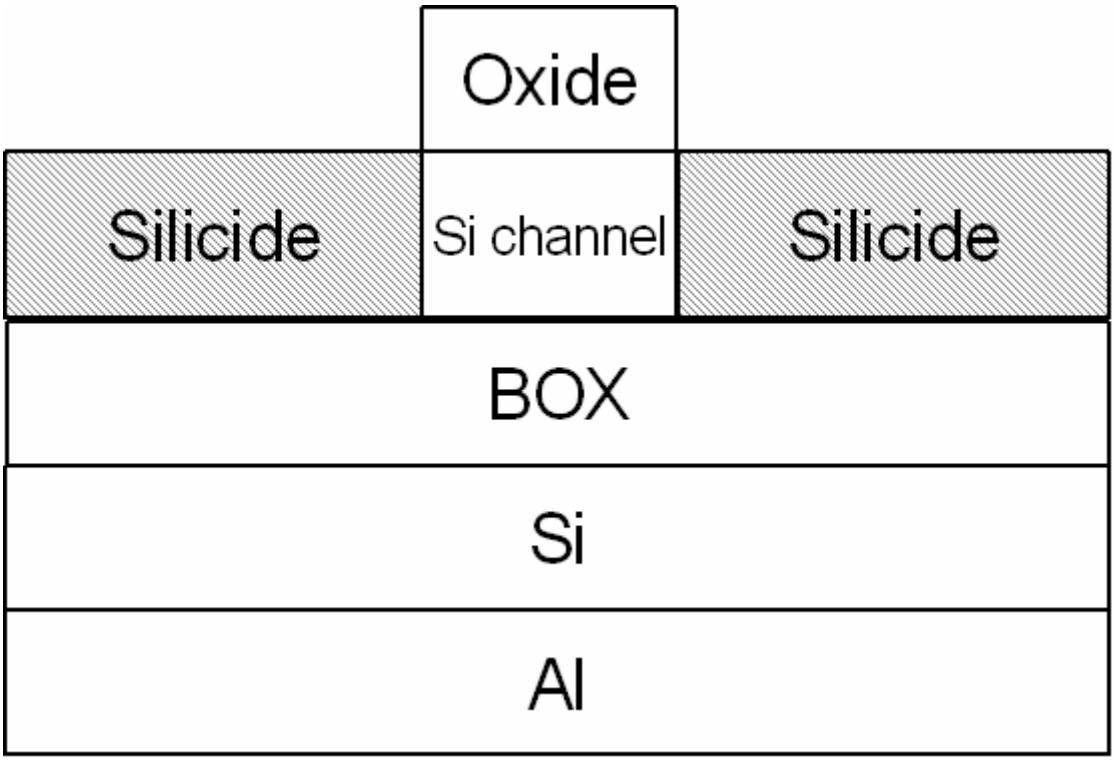


Fig. 5.2 Structure of SOI SB-nMOSFET fabricated

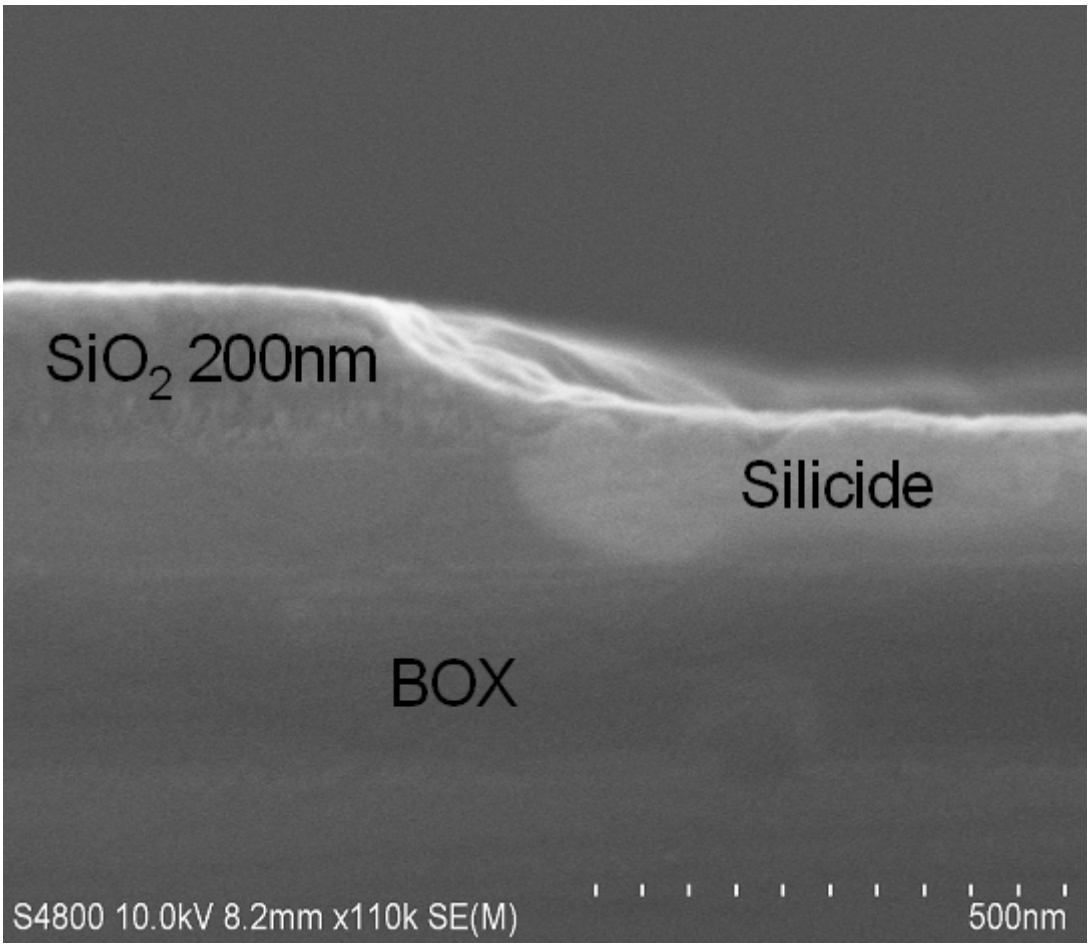


Fig. 5.3 SEM image of a part of SOI SB-nMOSFET fabricated

5.2.2 Characteristics of Ni Silicide Schottky Barrier MOSFETs with Er Interlayer

We fabricated the SB-nMOSFETs on SOI using Er contained Ni silicide. 7.2-nm-thick Er interlayer was inserted at the Ni/SOI interface and the silicidation was carried out at the annealing temperatures of 600 ^{o}C. Figure 5.4 shows I_d-V_d characteristics of Ni silicide SOI SB-nMOSFET. We confirmed FET operation of the SOI SB-nMOSFETs.

Figure 5.5 shows I_d-V_g characteristics of Ni silicide SOI SB-nMOSFET. Threshold voltages were 11.9V at the device with Er interlayer, and 11.6V at the device without Er. We were not able to observe much difference of threshold voltage. Drain current in the device significantly increased compared with the reference device of pure Ni silicide S/D SB-nMOSFET without Er interlayer. The schottky barrier height for electrons measured by schottky diode was lower by 0.05 eV with Er interlayer.This increase of drain current can be understood as the effect of Er interlayer on the lowering of Φ_b for electron.

Fig. 5.6 shows I_d-V_d characteristics of the fabricated SOI SB-nMOSFETs. After all, drain current was significantly improved by inserting Er interlayer. As stated above, the Φ_b value was lower by 0.05eV, so it became easier for electrons to flow a tunneling current. The tunneling current depends strongly on Φ_b, so lowering Φ_b for electrons by Er insertion is effective for I_d increasing.

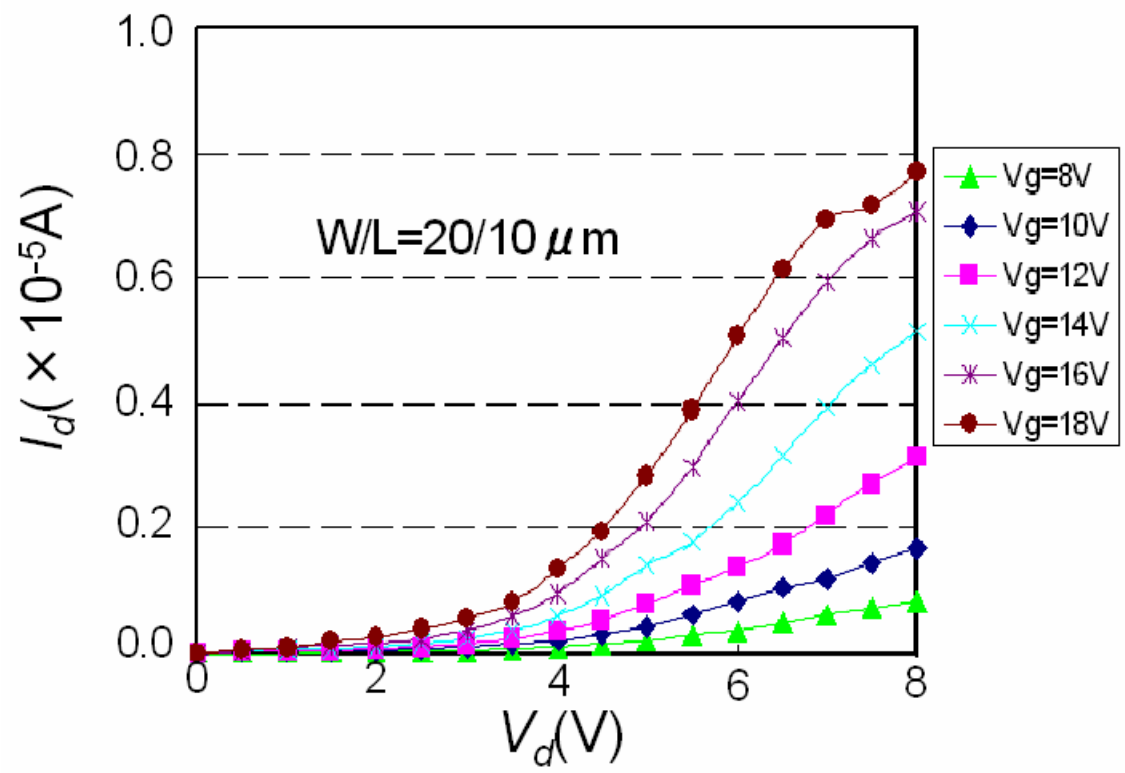


Fig. 5.4 I_d-V_d characteristics of Ni silicide SOI SB-nMOSFET.

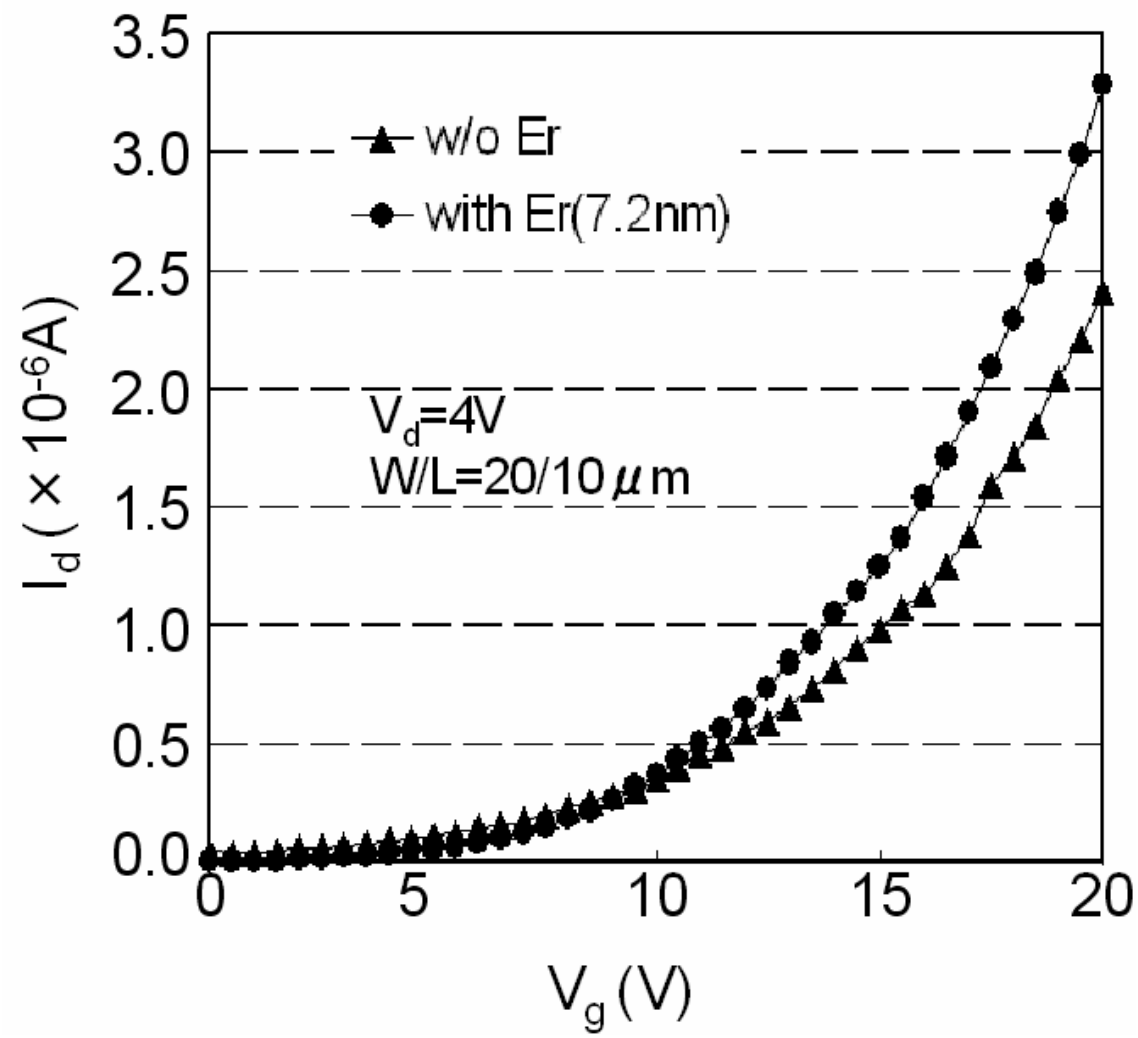


Fig. 5.5 I_d-V_g characteristics of SOI SB-nMOSFETs.

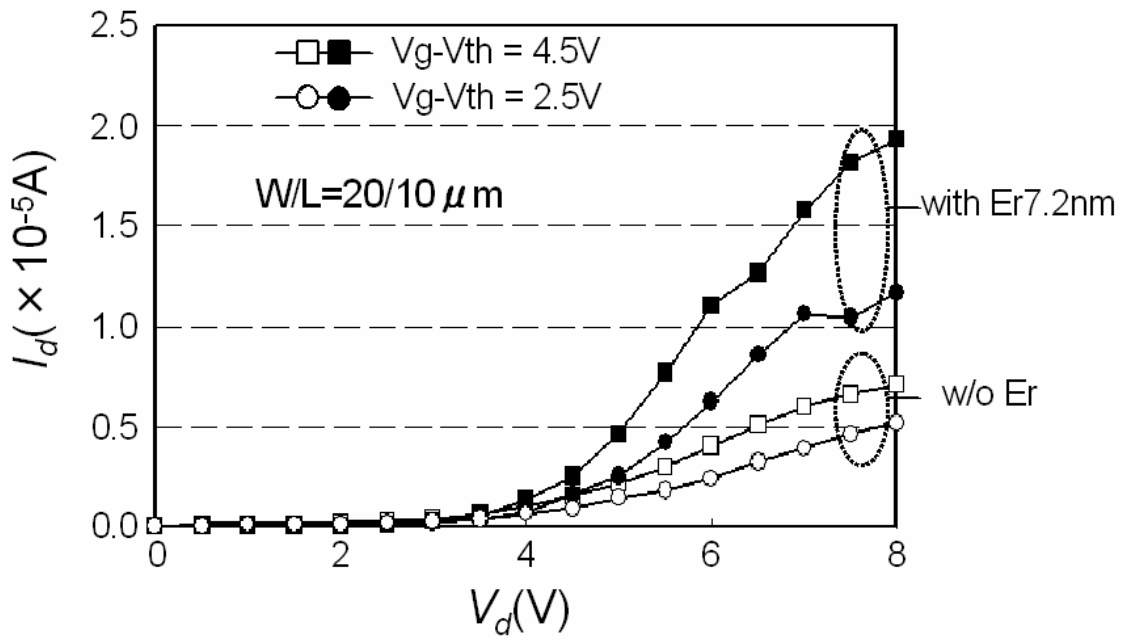


Fig. 5.6 I_d-V_d characteristics of the SOI SB-MOSFETs

Chapter 6
CONCLUSION

6.1 Summary of This Study

We fabricated SB-MOSFETs on SOI substrate by applying novel Schottky barrier height modulation technique of inserting Er interlayer at the Ni/Si interface prior to Ni silicidation. It was found that insertion of Er interlayer lowered Schottky barrier height for electrons while no significant increase in the resistivity was observed compared with pure Ni silicide films by the annealing at temperature in the range from 500 to 750 °C. We confirmed significant increase in drain current for the SOI SB-nMOSFETs with Er interlayer compared with the SOI SB-nMOSFETs without Er interlayer. Our results show that the Er interlayer insertion technique is one of the promising methods for improving electrical characteristics of SB-MOSFETs.

6.2 Future Issues

In this work, we have used Φ_b modulation method for Ni silicide by inserting Er layer to Ni/Si interface and optimized the annealing temperature using the value of resistivity. N-channel Ni Silicide SOI Schottky barrier source/drain MOSFET was fabricated using Er insertion technique and I_d was increased by Er insertion though resistivity was increased. In this work, we supposed that the value of Φ_b was same as Schottky diode and SOI SB-MOSFET. In the SOI SB-MOSFET, we need to consider the value of Φ_b calculated by not schottky diode but SOI SB-MOSFET. Because a silicide depth was very thin and the direction of the current was from silicide to channel. We optimize annealing temperature in the range 500-750℃. We have a room for improvement by optimizing more accurate annealing temperature.

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