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Electrical Characteristics of In$_{0.53}$Ga$_{0.47}$As MOS Device with High-k Gate Dielectrics

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【Chapter 1】

Introduction

1.1. Perspective on CMOS Technology

Recently, Evolution of Information Technology (IT) is remarkable. For example, PC, cell phone and internet which we usually use are essential for our lives. These products are realized by striking progress in ultra-large-scale integration (ULSI) technology. The Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are the basic and fundamental building block of the modern ULSI integrated circuits (ICs). To achieve high performance of ULSI, it is necessary to miniaturize the MOSFET with the scaling method. The miniaturizing is a trend that has been continued for long time in the semiconductor industry. It's considered that the scaling will continue in accordance with Moore's Law using silicon-based technology. This law notes that the device feature size decreases each year and the number of transistors on a LSI doubled every two years. The International Technology Roadmap for Semiconductor (ITRS) [figure1.1] defines how the device parameters are scaled for the next technology node [1.1]. A simple description of miniaturization with scaling factor of κ is shown in Figure 1.2 and Table 1.1. To gain κ times of the device performance, the physical device dimensions are reduced by k times, while the electrical parameters are increased by κ times. After that time, Si-based devices with traditional structure are approaching its fundamental scaling limits. So, using alternative materials are expected to break through the limit of Si-based CMOS. III-V compound semiconductor is one of the most promising candidates for an alternative channel material, due to its high electron mobility.
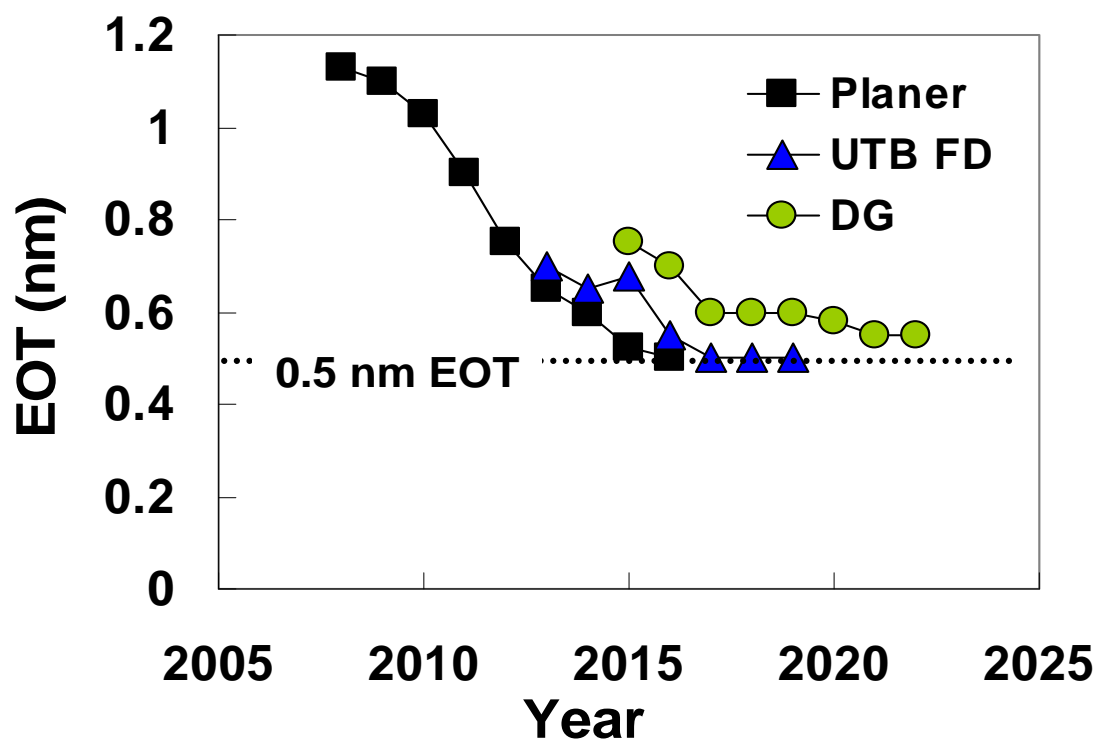
Figure 1.1 EOT scaling road map of various structures MOS transistors (ITRS2008).
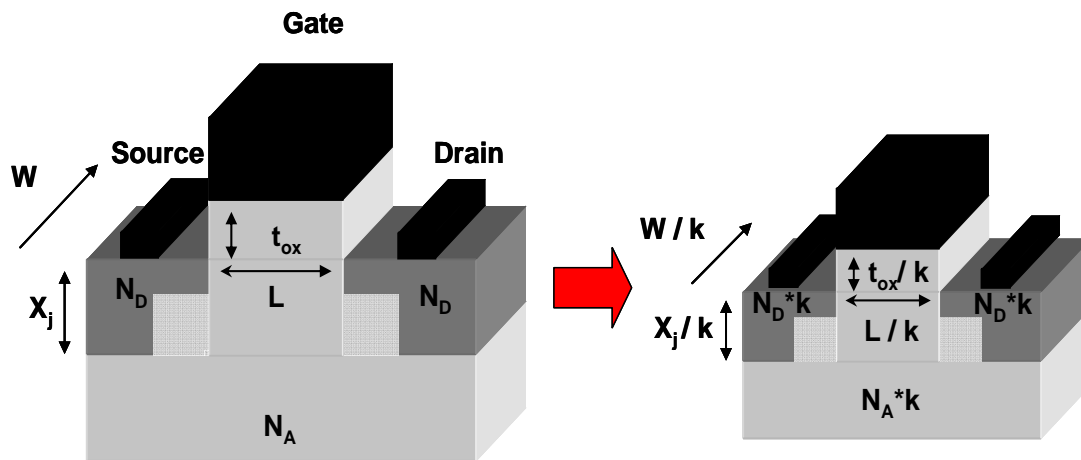
Figure.1.2 Scaling method

Table 1.1 Scaling of MOSFET by a scaling factor of k

Quantity	Before Scaling	After Scaling (k>1)
Channel Length	L	L/k
Channel Width	W	W/k
Device Area	A	A/k^2
Gate Oxide Thickness	t_{ox}	t_{ox}/k
Gate Capacitance per Unit Area	C_{ox}	$C_{ox}*k$
Junction Depth	Xj	Xj/k
Power Supply Voltage	V_{DD}	V_{DD}/k
Threshold Voltage	Vth	Vth/k
Delay Time	t_d	t_d/k
Required Power	$V_{DD}I$	$V_{DD}I/k^2$
Doping Densities	$N_A \quad N_D$	$N_A*k \quad N_D*k$

1.2 Motivation of implementing III-V materials in Si CMOS platform

The increasing demand for high speed and low power device has pushed Si-based transistors to scale down to the limit. III-V compound semiconductors such as InGaAs has higher electron mobility than that of Si, as listed in Table 1.1 [1.1], and are being actively evaluated in research for one of the promising candidate which can enhance the metal-oxide-semiconductor field-effect-transistor (MOSFET) performance. The high electron mobility and velocity may allow a logic device operate much faster but at lower power than modern silicon devices. This is the most important reason that III-V materials have been required as the channel of MOS transistors. Among III-V semiconductor substrates, InGaAs has been used as a channel and barrier layer material and embraced the advantages of higher electron mobility and moderate band gap as compared to Si[1.2-1.4]. However, the lack of highly reliable insulators on InGaAs makes it difficult to form InGaAs MOS device in contrast to Si based CMOS device.[1.5~1.11] Therefore, it is really anticipated to find out the device-quality gate insulator for InGaAs MOS devices.

Table1.2 Electron and hole mobility of semiconductors

	μ_e[cm^2/Vs]	μ_h[cm^2/Vs]
Si	1400	450
Ge	3900	1900
GaAs	8500	400
InP	4600	650
In$_x$Ga$_{1-x}$As	8000〜30000	400〜460

1.3 Requirements in Gate Dielectrics

In CMOS technology, SiO_2 has been used as gate dielectric for more than 30 years. As a gate dielectric, silicon dioxide (SiO2), most widely used in CMOS integrated circuits, has many prominent advantages, including a low interface state density (e.g. D_{it}~ low 10^{10} cm^{-2}eV-1), a good thermal stability in contact with silicon (Si), a large energy band gap and the large energy band offsets in reference to Si. However, recent downsizing has made gate leakage current extremely large. Figure 1.2 shows the relationships between gate leakage current density and EOT (Equivalent Oxide Thickness). Therefore, as substitution of SiO_2, high-k dielectric materials have attracted extensive attention in the last decade due to their great potential for maintaining further down-scaling in equivalent oxide thickness (EOT) with a physically thicker film and a low dielectric leakage current. Figure 1.3 represents the schematic description of differences between the cases using SiO2 and high-k material for gate insulator. Relationship between physical thickness of SiO2 and high-k gate oxide obtained by same gate capacitance

value (C) is written as,

$$C = \frac{\varepsilon_{high-k}}{t_{high-k}} = \frac{\varepsilon_{SiO_2}}{t_{EOT}}$$

where ε_{high-k} is the dielectric constant of high-k materials, t_{high-k} is the physical thickness of high-k gate oxide, ε_{SiO2} is the dielectric constant of $SiO_2(=3.9)$. EOT (Equivalent-Oxide-Thickness) is expressed as,

$$T_{EOT} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} T_{phy}$$
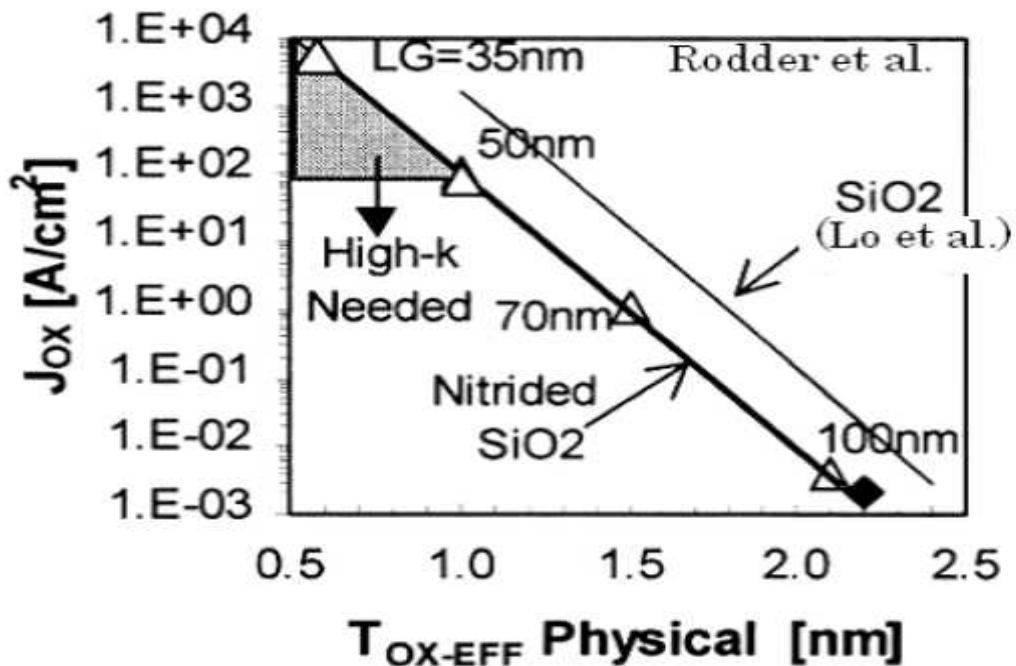
where T_{phy} is the physical thickness of gate oxide.

Figure 1.2 represents the schematic description of differences between the cases using SiO2 and high-k material for gate insulator.
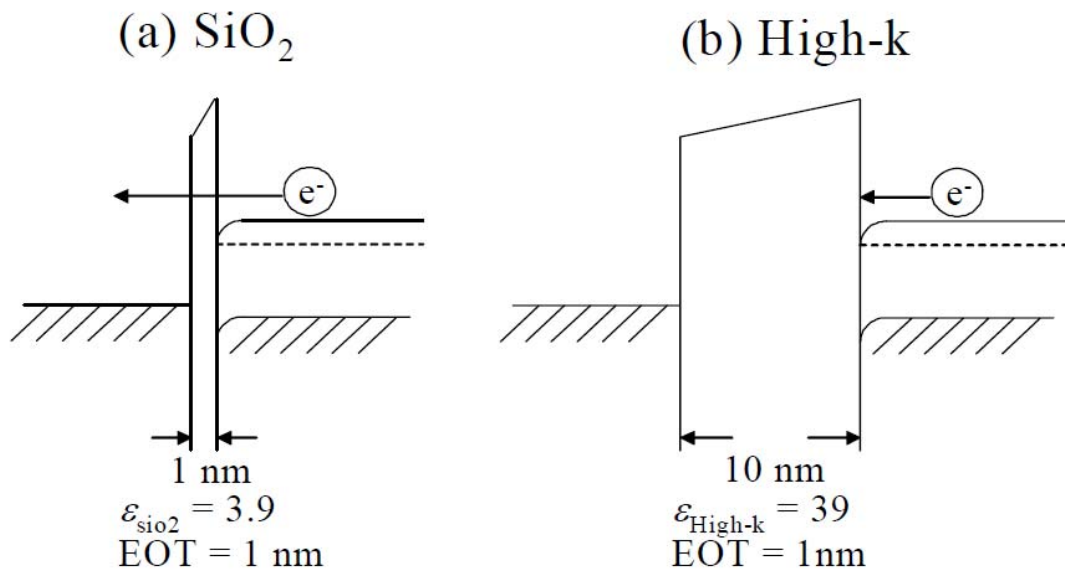
(a) SiO$_2$

(b) High-k

1 nm
$\varepsilon_{sio2} = 3.9$
EOT = 1 nm

10 nm
$\varepsilon_{High\text{-}k} = 39$
EOT = 1nm

Figure 1.3 Schematic description of difference between the cases using (a) SiO$_2$ and (b) High-k for the gate insulator in the MOS structure.

1.3. High-k Gate Materials

The possible candidate of several metal oxides system for the use of gate dielectric materials is shown in white spaces of Table 1.2.

Table 1.2 Candidates for the metal, oxide of which has possibility to be used as high-k gate insulator on periodic table.

Legend:
- ● = Not a solid at 1000 K
- O = Radioactive
- ① = Failed reaction 1: $Si + MO_x \rightarrow M + SiO_2$
- ② = Failed reaction 2: $Si + MO_x \rightarrow MSi_x + SiO_2$
- ⑥ = Failed reaction 6: $Si + MO_x \rightarrow M + MSi_xO_y$

Periodic table (marker in parentheses):

- H(●) ... He(●)
- Li, Be ... B(●), C(●), N(●), O(●), F(●), Ne(●)
- Na(①), Mg ... Al, Si, P(●), S(●), Cl(●), Ar(●)
- K, Ca, Sc, Ti(②), V(①), Cr(①), Mn(①), Fe(①), Co(①), Ni(①), Cu(①), Zn(①), Ga(①), Ge(①), As(●), Se(●), Br(●), Kr(●)
- Rh(●), Sr, Y, Zr, Nb(①), Mo(①), Tc, Ru(①), Rb(①), Pd(①), Ag(●), Cd(①), In(①), Sn(①), Sb(①), Te(①), I(●), Xe(●)
- Cs(●), Ba(⑥), R, Hf, Ta(①), W(①), Re(①), Os(①), Ir(①), Pt(●), Au(●), Hg(●), Tl(●), Pb(①), Bi(①), Po(O), At(O), Rn(O)
- Fr(O), Ra(O), A(O), Rf(O), Ha(O), Sg(O), Ns(O), Hs(O), Mt(O)

R: La, Ce, Pr, Nd, Pm(O), Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu

A: Ac(O), Th(O), Pa(O), U(O), Np(O), Pu(O), Am(O), Cm(O), Bk(O), Cf(O), Es(O), Fm(O), Md(O), No(O), Lr(O)

As shown in Figure 1.4, many papers on high-k materials are submitted in the primary conferences up to 2002. However, from 2003 to now, the candidate of high-k materials have narrowed down.

Hf-based oxide has been considered as one of the most promising candidates because of a high dielectric constant (k ~ 20-25), low bulk trap densities and fixed charges, a large energy band gap (~ 6 eV) and the large band offsets (> 1.5 eV). Actually, Intel announced that the hafnium-based oxide and metal gate electrodes would be put into production for their 45 nm generation in 2007.
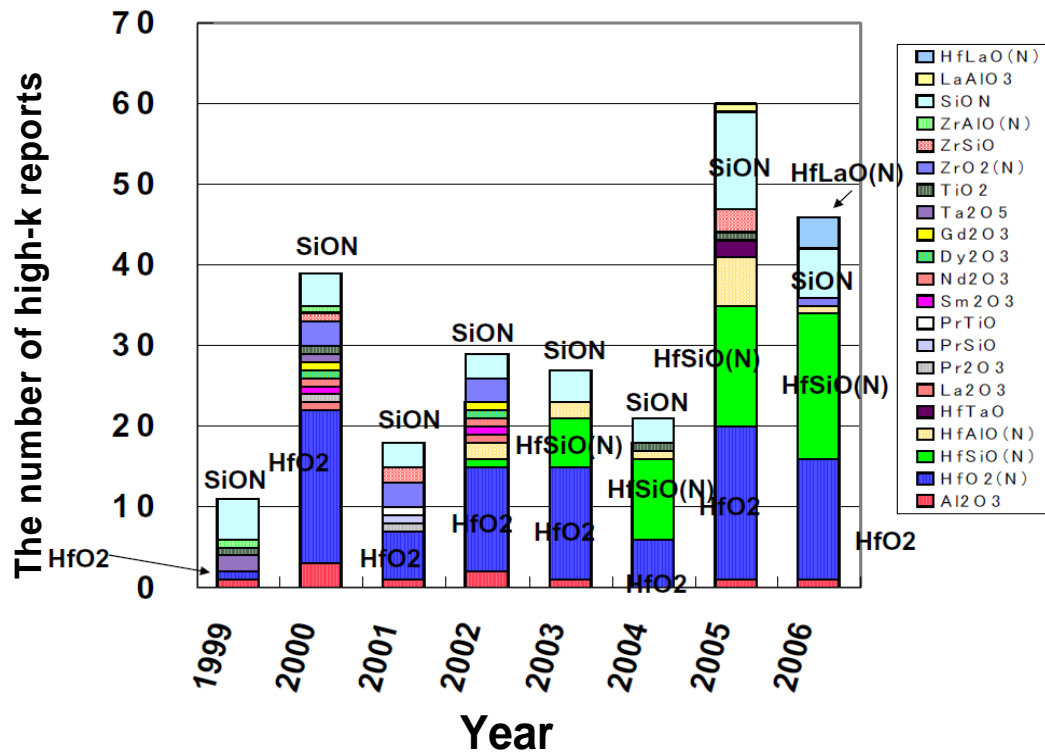
Figure 1.4 Recent trends of high-k reports which had been reported in VLSI symposium and IEDM symposium.

Generally, the interfacial state density of the interface between high-k gate dielectric and semiconductor is not good. A high interfacial state density causes some degradation of electrical characteristics. So, in the case of Si-MOS, SiO_2 which has a low interface state density on Si- substrate is inserted as a interfacial layer.

On the other hand, rare earth oxide (RE) such as La_2O_3 is also one of candidate as a insulator due to high dielectric constant and lower interfacial state density relatively. RE oxides react with Si to form RE-silicate by annealing. RE-silicate layers generally have

dielectric constants more than 8, so that a directly contact structure can be easily achieved with lower interfacial state density and EOT.

However, InGaAs MOS devices with RE-oxide as gate dielectric has not been reported enough.
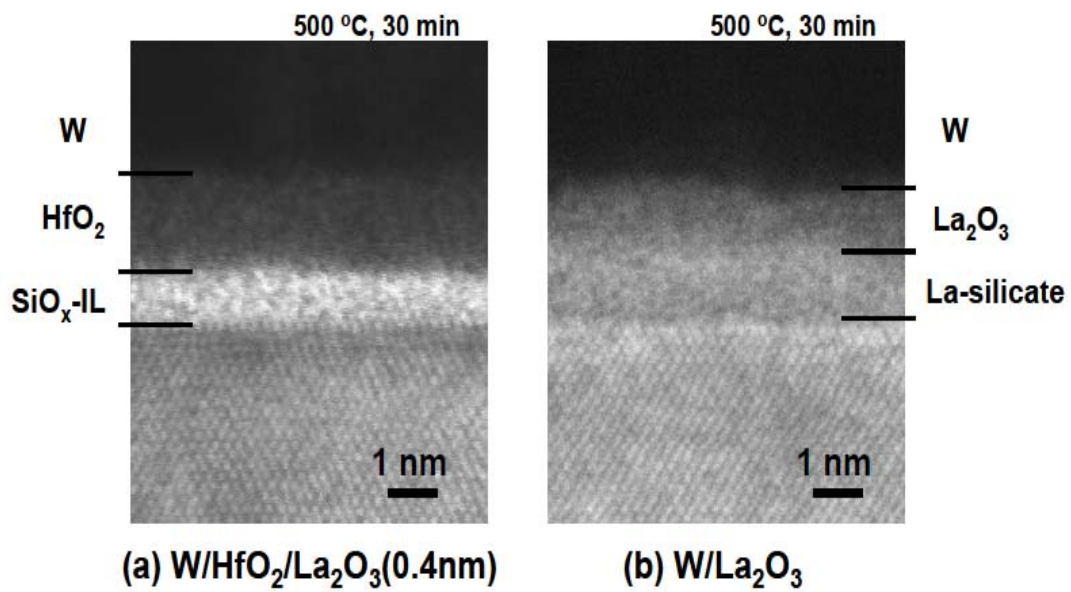

Figure1.5 interfacial reaction of (a) Hf-based MOS structure (b) La_2O_3 MOS structure

1.4. Purpose of this study

InGaAs MOSFET is one of the promising candidates for next generation devices, thanks to its high electron mobility compared to that of Si. To achieve a high performing InGaAs MOSFET with low leakage current, high-k materials with proper interfacial quality should be investigated. In this work, MOS capacitors of $In_{0.53}Ga_{0.47}As$ with high-k materials (HfO2, La_2O_3, PrO_x and CeO_x) which can be attracted for future MOS-devices have been fabricated and the electrical characteristics are measured.

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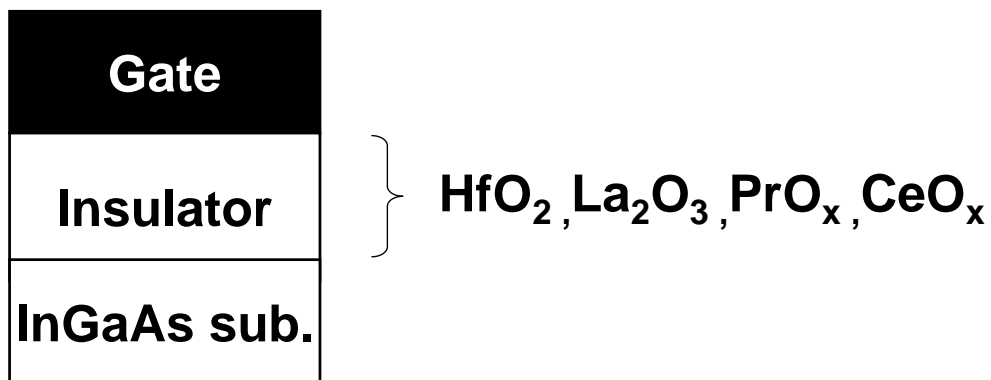| Gate |
|---|
| Insulator |
| InGaAs sub. |

$HfO_2, La_2O_3, PrO_x, CeO_x$

Figure 1.6 InGaAs MOS structure in this study. Various high-k materials were used for insulator

【Chapter 2】

Fabrication and Characterization Method

2.1 Experimental

2.1.1 Fabrication flow for In$_{0.53}$Ga$_{0.47}$As MOS Capacitors with high-k insulator

Figure 2.1 summarizes device fabrication flow of InGaAs MOS capacitor. InGaAs MOS capacitor was fabricated on a n-type In$_{0.53}$Ga$_{0.47}$As substrate, epitaxially grown on a n-type InP substrate. (Density of Si dopant was 5×10^{17} cm^{-3}). On the substrate dipped in HF, high-k gate materials (HfO$_2$,La$_2$O$_3$, PrO$_x$, CeO$_x$) were deposited by electron-beam deposition in an ultra high vacuum at a pressure of 10^{-8} Pa. After high-k deposition, 60 nm-thick tungsten (W) was *in-situ* deposited using sputtering without exposing the wafers to air in order to avoid any moisture or carbon-related contamination absorption. W was patterned by reactive ion etching (RIE) using SF$_6$ chemistry to form gate electrode for MOS capacitors. Wafers were then post-metallization annealed (PMA) using a rapid thermal annealing (RTA) furnace in forming gas (F.G) (N$_2$:H$_2$=97%:3%) ambient at 300, 400, 500℃ respectively. Finally, Al back contacts were formed. The device structure is shown in figure 2.2.
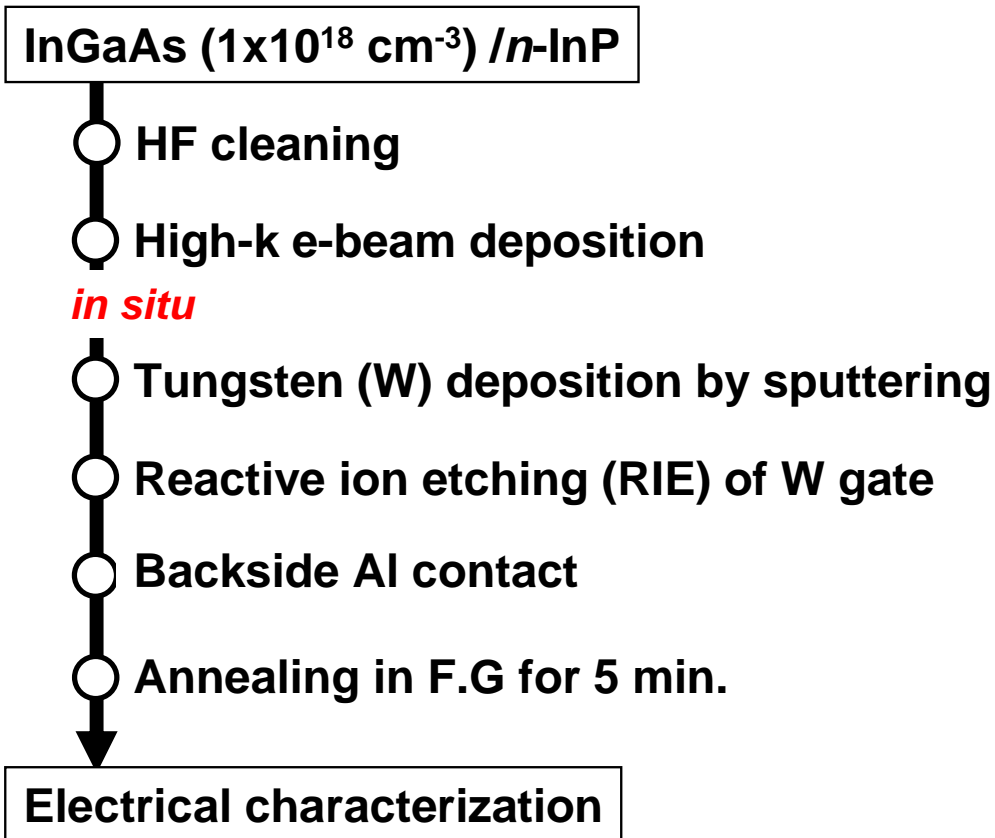
InGaAs (1×10^{18} cm^{-3}) /n-InP

○ **HF cleaning**

○ **High-k e-beam deposition**

in situ

○ **Tungsten (W) deposition by sputtering**

○ **Reactive ion etching (RIE) of W gate**

○ **Backside Al contact**

○ **Annealing in F.G for 5 min.**

Electrical characterization

Figure 2.1 Fabrication process flows of high-k gated MOS capacitors

W (60nm)

High-k

N-In$_{0.53}$Ga$_{0.47}$As

N-InP

Al(50nm)
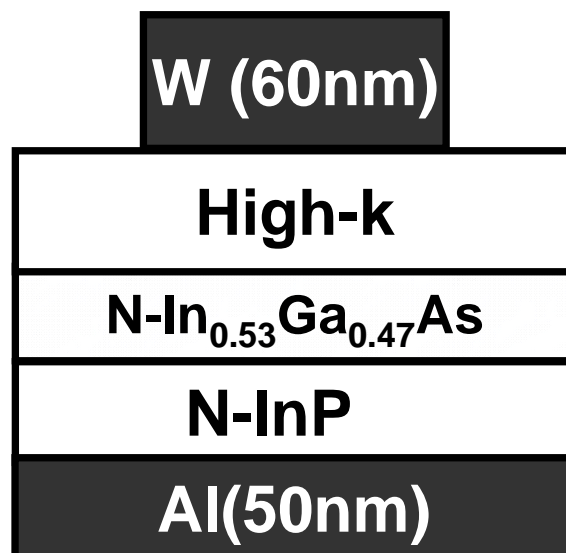
Figure 2.2 Schematic illustration of fabricated MOSCAP of W/high-k/InGaAs

2.1.2 Molecular Beam Epitaxy (MBE)

High-k gate dielectrics were deposited in ultra high vacuum by electron-beam evaporation method. The background pressure in growth chamber reached as high as 10-8 Pa and was approximately 10-7 Pa during deposition. In the chamber, a sintered high-k target, which is evaporation source, is irradiated with electron beam accelerated by 5 kV. The target is heated up. Then ultra thin LaO_x film is deposited on the $In_{0.53}Ga_{0.47}As$-substrate. Physical thickness of the film is monitored with a film thickness counter using crystal oscillator. The temperature of the substrate is controlled by a substrate heater and is measured by a thermocouple.
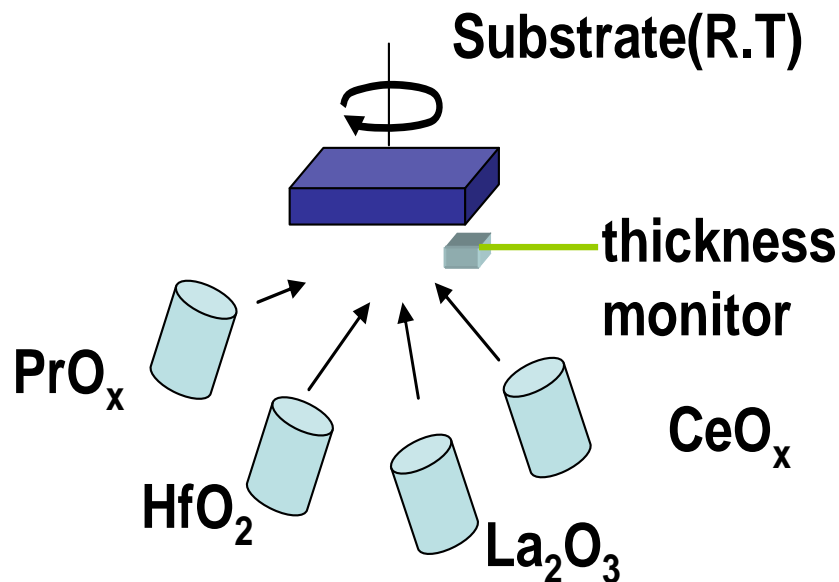

Figure 2.3 Schematic model of molecular beam epitaxy

2.1.3. RF Sputtering

In this experiment, gate metals W was deposited using RF sputtering. The base pressure of sputtering chamber was maintained to be 10^{-7} Pa by TRP and RP (shown in Fig.2.7). In sputtering, Ar was flowed into the chamber and the pressure of which was set to be 10^{-4} Pa, the AC current power was 150W.

2.1.4. Reactive Ion Etching (RIE)

Reactive Ion Etching (RIE) which uses one of chemical reactive plasma to remove materials deposited on wafers was adopted to etch gate electrode in this study. There are two electrodes in vacuum chamber (in figure 2.4). One is usually connected to ground and gas is put into the chamber and exits to the pump, in this study SF_6 and O_2 are used to remove gate W and resist each. And plasma is generated and ion direct for substrate and remove gate electrode and resist chemically.
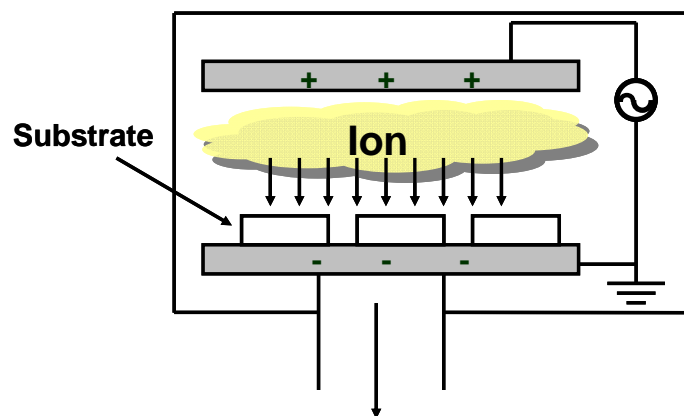
Figure 2.4 Schematic illustration of Reactive Ion Etching (RIE).

2.1.5 Rapid Thermal Annealing (RTA) Method

RTA method was employed for the heat treatments after depositing dielectric films. The annealing process is indispensable to improving defects in dielectric film and at the interface. The samples with gate dielectric were put on silicon subsector and inserted into heat- treating furnace. The ambience in furnace was vacuumed adequately by rotary pump for highly-pure nitrogen or forming gas substitution. And then, nitrogen or forming (in accordance with the purpose) was provided with flow rate of 1.0 l/min and

the samples were annealed at atmospheric pressure. In order to evaluate the electrical or chemical properties, the annealing temperatures ranging from 300-500℃were made an attempt.

2.1.6 Al deposition by vacuum evaporation method

In this study, Al was used for the backside electrode and Al wiring. Al was deposited by vacuum evaporation method. Al source was set on W boat in the chamber. The large current was passed in the W boat and the W boat was heated by the Joule heat. Because the boiling point of Al and the melting point of W are respectively about 2000oC and 3400oC in the atmosphere, the Al source evaporates without the W boat melting. In this way, Al was deposited. The schematic illustration of this deposition is shown in Figure 2.5.
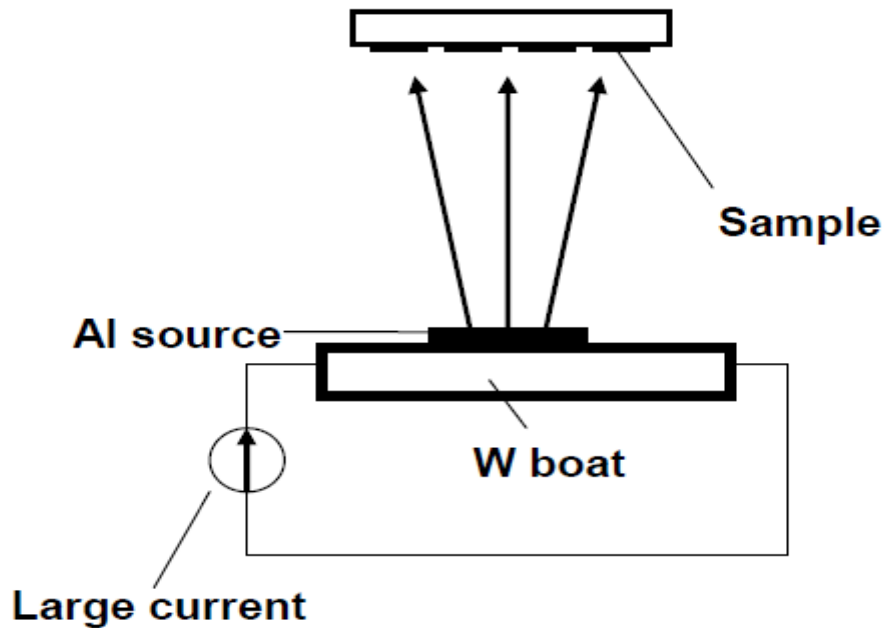
Figure 2.5 the schematic illustration of Al deposition

2.2 Measurement Methods

2.2.1 CV Measurement

C-V characteristic measurements were performed with various frequencies (1kHz ∼ 1MHz) by precision LCR meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in figure 2.6[2.1]. The intrinsic energy level Ei or potential ϕ in the neutral part of device is taken as the zero reference potential. The surface potential ϕs is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \qquad \text{............} \quad (2.1)$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad/units area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitor from the gate, $C = dQ_G / dV_G$, where Q_G and V_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = . (Q_S + Q_{it})$, where Q_S is the semiconductor charge, Q_{it} the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \varphi_s$, where V_{FB} is the flat band voltage, V_{ox} the oxide voltage, and φ_s the surface potential, allowing Eq. (2.1) to be rewritten as

$$C = -\frac{dQ_S + dQ_{it}}{dV_{ox} + d\phi_s} \qquad \text{............} \quad (2.2)$$

The semiconductor charge density Q_S, consists of hole charge density Q_p, space-charge region bulk charge density Q_b, and electron charge density Q_n. With $Q_S = Q_p + Q_b + Q_n$, Eq.(2.2) becomes

$$C = -\frac{1}{\dfrac{dV_{ox}}{dQ_S + dQ_{it}} + \dfrac{d\phi_s}{dQ_P + dQ_b + dQ_n + dQ_{it}}} \qquad \text{............} \quad (2.3)$$

Utilizing the general capacitance definition of Eq. (2.1), Eq. (2.3) becomes

$$C = \frac{1}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_P + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_P + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \qquad \text{............} \quad (2.4)$$

The positive accumulation Qp dominates for negative gate voltages for p-substrate devices. For positive VG, the semiconductor charges are negative. The minus sign in Eq. (2.3) cancels in either case. Eq. (2.4) is represented by the equivalent circuit in figure 2.7 (a). For negative gate voltages, the surface is heavily accumulated and Qp dominates. Cp is very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in figure 2.7 (b) and the overall capacitance is Cox. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = .qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of Cox in series with Cb in parallel with Cit as shown in figure 2.7 (c). In weak inversion Cn begins to appear. For strong inversion, Cn dominates because Qn is very high. If Qn is able to follow the applied ac voltage, the low-frequency equivalent circuit (figure 2.7 (d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in figure 2.7 (e) applies in inversion, with $Cb = Ks \; \varepsilon o / Winv$ with Winv the inversion space-charge region width.
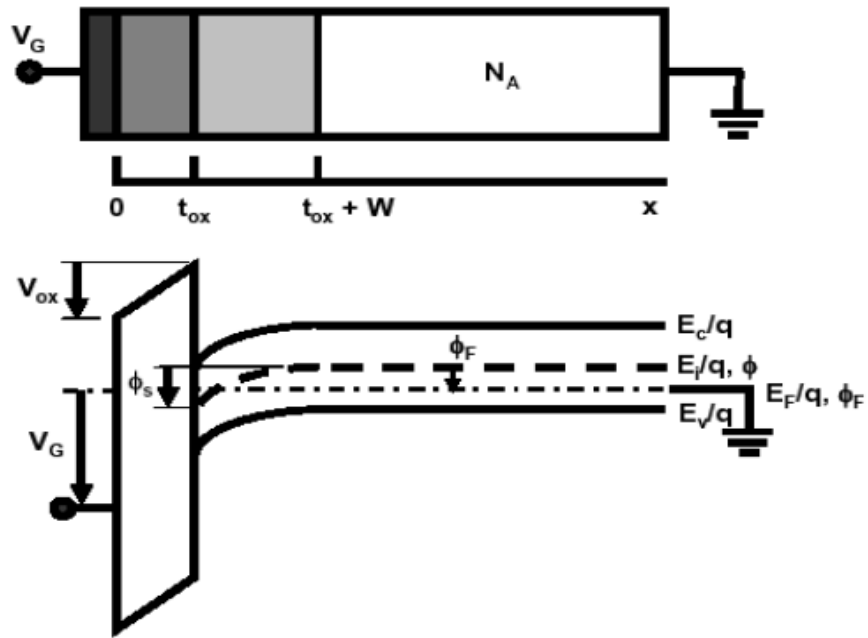
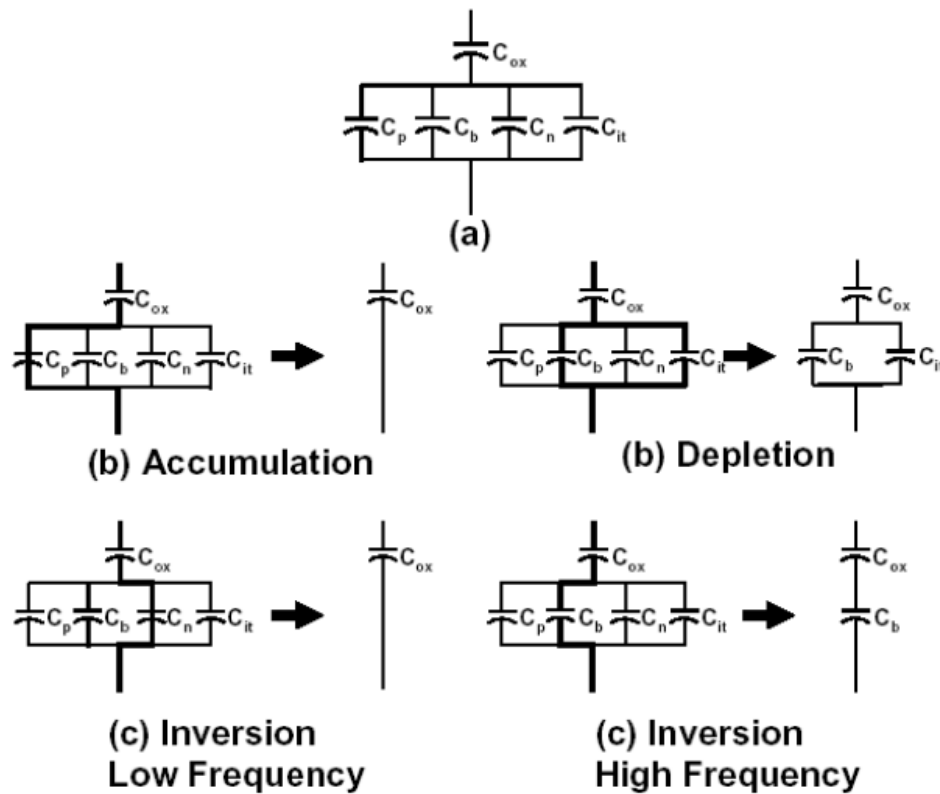Figure 2.6 The energy band diagram of an MOS capacitor on a p-type substrate

Figure 2.7 Capacitances of an MOS capacitor for various bias conditions.

2.5.2. J_g-V measurement

One of the main concepts of replacing the high-k gate dielectrics with SiO_2 is to suppress the gate leakage current. Thus, it is enormously important to measure the gate leakage current-voltage (J-V) characteristics. In addition, the properties of high-k films, such as the barrier height, effective mass, are obtained by analyzing the carrier transport mechanisms from the leakage current. To investigate the voltage and temperature dependence of gate leakage current, it is able to identify the carrier conduction mechanisms experimentally [2.2]. J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

2.5.3. D_{it} measurement ~ conductance method~

The conductance method, proposed by Nicollian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it}. Interface trap densities of 10_9 cm-2eV-1 and lower can be measured. It is also the most complete method, because it yields Dit in the depletion and weak inversion portion of the band gap, the capture cross-sections for majority carriers, and information about surface potential fluctuation. The technique is based on measuring the equivalent parallel conductance G_P of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density. The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in Figure 2.8 (a).
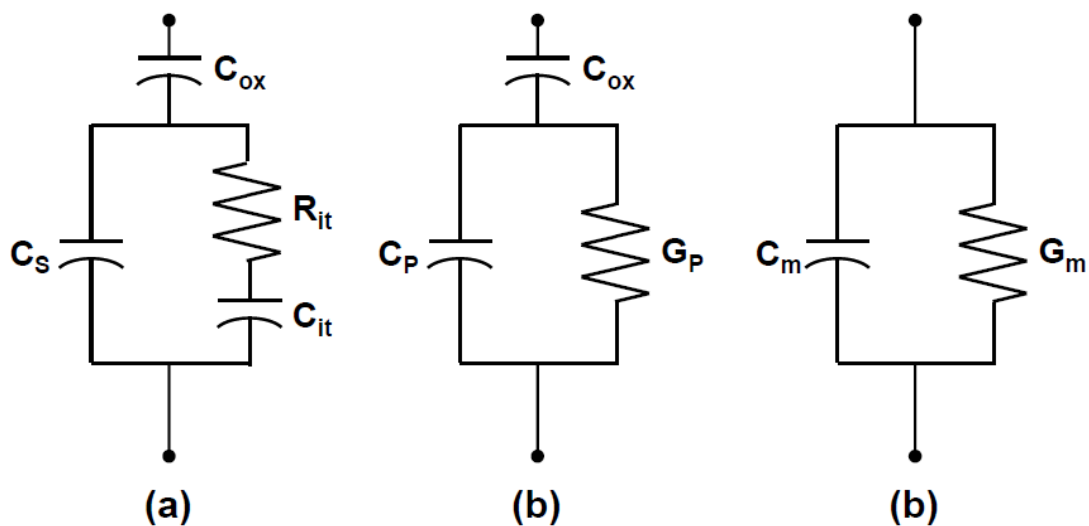
Figure. 2.8 Equivalent circuits for conductance measurement; (a) MOS capacitor with interface trap time constant τ it = RitCit, (b) simplified circuit of (a), (c) measured circuit.

It consists of the oxide capacitance *Cox*, the semiconductor capacitance *CS*, and the interface trao capacitance *Cit*. The capture-emission of carriers by *Dit* is a lossy process, represented by the resistance *Rit*. It is convenient to replace the circuit of Figure 2.8 (a) by that in Figure 2.8 (b), where *Cp* and *Gp* are given by

$$C_P = C_S + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \qquad \text{............} \qquad (2.6)$$

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \qquad \text{............} \qquad (2.7)$$

where *Cit* = q2Dit, ω = $2\pi f$ (*f* = measurement frequency) and τ *it* = *RitCit* . Dividing *Gp* by ω makes Eq. (2.7) symmetrical in $\omega \tau$ *it*. Eq. (2.6) and Eq. (2.7) are for interface traps with a single energy level in the band gap. Interface traps at the SiO2-Si interface, however, are continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by trap located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \qquad \text{............} \qquad (2.8)$$

Equations (2.7) and (2.8) show that the conductance is easier to interpret than the capacitance, because Eq. (2.7) does not require *Cs*. The conductance is measured as a function of frequency and plotted as *Gp*/ω versus ω. *Gp*/ω has a maximum at ω =1τ and at that maximum D_{it} = 2*Gp*/qω. For Eq. (2.8) we find ω ≈ 2 τ and *Dit* = 2.5*Gp*/qω at the maximum. Hence we determine *Dit* from the maximum *Gp*/ω and

determine τ it from ω at the peak conductance location on the ω-axis. Gp/ω versus f plots, calculated according to Eq. (2.7) and (2.8). Experimental Gp/ω versus ω curves are generally broader than predicted by Eq. (6.49), attributed to interface trap time constant dispersion caused by surface potential fluctuations due to non-uniformities in oxide charge and interface traps as well as doping density. Surface potential fluctuations are more pronounced in p-Si than in n-Si. Surface potential fluctuations complicate the analysis of the experimental data. When such fluctuations are taken into account, Eq. (2.8) becomes

$$\frac{G_P}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{it}}{\omega \tau_{it}} \ln\left[1 + (\omega \tau_{it})^2\right] P(U_s)dU_s \quad \text{............} \quad (2.9)$$

where $P(U_s)$ is a probability distribution of the surface potential fluctuation given by

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(U_s - \bar{U}_s)^2}{2\sigma^2}\right) \quad \text{............} \quad (2.10)$$

with S U and σ the normalized mean surface potential and standard deviation, respectively. An approximate expression giving the interface trap density in terms of the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max} \quad \text{............} \quad (2.11)$$

Capacitance meters generally assume the device to consist of the parallel *Cm-Gm* combination in Figure 2.8 (c). A circuit comparison of Figure 2.8 (b) to Figure 2.8 (c) gives *Gp/ω* in terms of the measured capacitance *Cm*, the oxide capacitance, and the measured conductance *Gm* as

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \qquad \ldots\ldots\ldots\ldots \quad (2.12)$$

assuming negligible series resistance. The conductance measurement must be carried out over a wide frequency range. The portion of the band gap probed by conductance measurements is typically from flat band to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50mV or less to prevent harmonics of the signal frequency giving rise to spurious conductance. The conductance depends only on the device area for a given *Dit*. However, a capacitor with thin oxide has a high capacitance relative to the conductance, especially for low *Dit* and the resolution of the capacitance meter is dominates by the out-of-phase capacitive current component. Reducing *Cox* by increasing the oxide thickness helps this measurement problem.

【Chapter 3】

Electrical characteristics of $In_{0.53}Ga_{0.47}As$ MOS capacitors with high-k gate dielectrics

3.1 Introduction

Hf-based oxide is now commercially used in Si CMOS devices. However, HfO_2 on InGaAs exhibits large frequency dispersion, high interfacial state density, and relatively low capacitance. Therefore, new high-k materials suitable for InGaAs MOS device are necessary. RE-oxide such as La_2O_3, which has higher k-value (as shown table 3.1) and lower interfacial state density than that of HfO_2 on Si-MOS, is one of candidate as an insulator for InGaAs MOS. However, InGaAs MOS devices with RE-oxides as gate dielectric have not been reported enough. In this chapter, we investigate electrical property of $In_{0.53}Ga_{0.47}As$ MOS capacitor with RE-oxide and compare with HfO_2 capacitor.

Table 3.1. Dielectric constant and bandgaps of RE oxides

Oxide	k	Eg(eV)
HfO_2	20	5.3
La_2O_3	24	5.5
PrO_x	32	5.5
CeO_x	38	3.2

3.2 Physical analysis ~XPS, TEM-EDX~

The chemical bonding states were analyzed by angle resolved XPS from 90 to 15 degree as shown figure 3.1. From As 3d spectrum, it has been revealed that there are oxidized As in the film.

The intensity ratio of La 3d to oxidized As 3d as well as La 3d to un-oxidized As 3d are shown in this figure. From the weak dependence on take off angle, it can be concluded that As atoms were diffused from the substrate and are uniformly distributed in La_2O_3

layer. The diffusion of As atoms can be one of the reason for explaining the measured large leakage current.
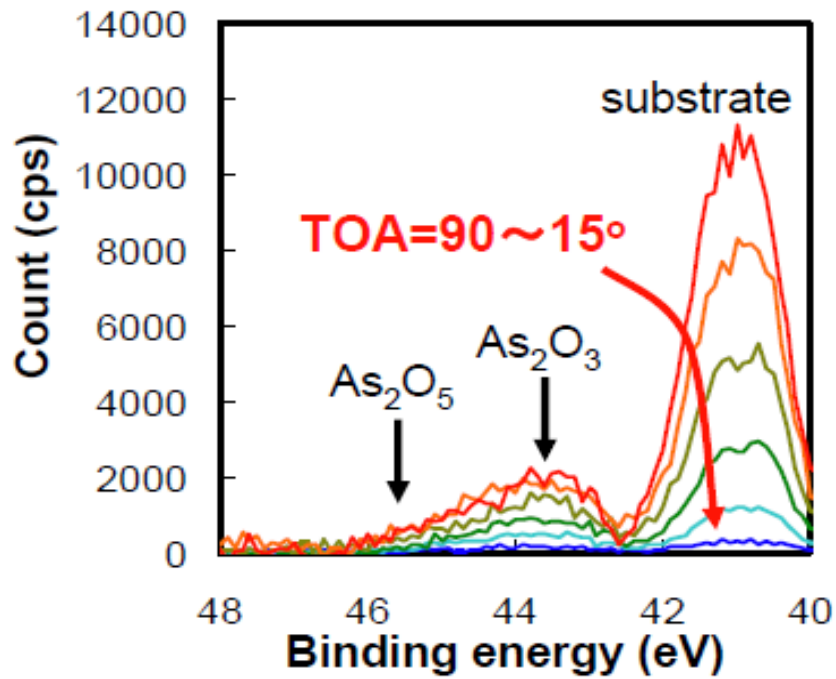
Figure 3.2.1 As 3*d* spectrum of $La_2O_3/In_{0.53}Ga_{0.47}As$
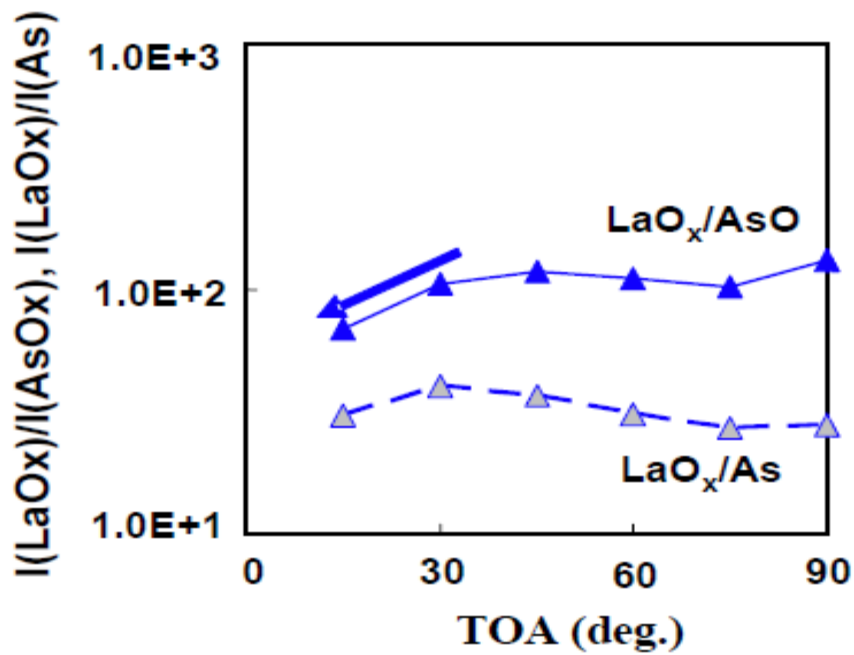
Figure3.2.2 TOA dependent proportion of AsOx and As

We also tried to see the behavior of the atom diffusion from the substrate with Ce-oxide film, which is one of a rare earth oxides same as La_2O_3 and PrO_x. We observed an interfacial layer between Ce-oxide and substrate. From EDX analysis, all the elements from the substrate were detected from Ce-oxide layer.
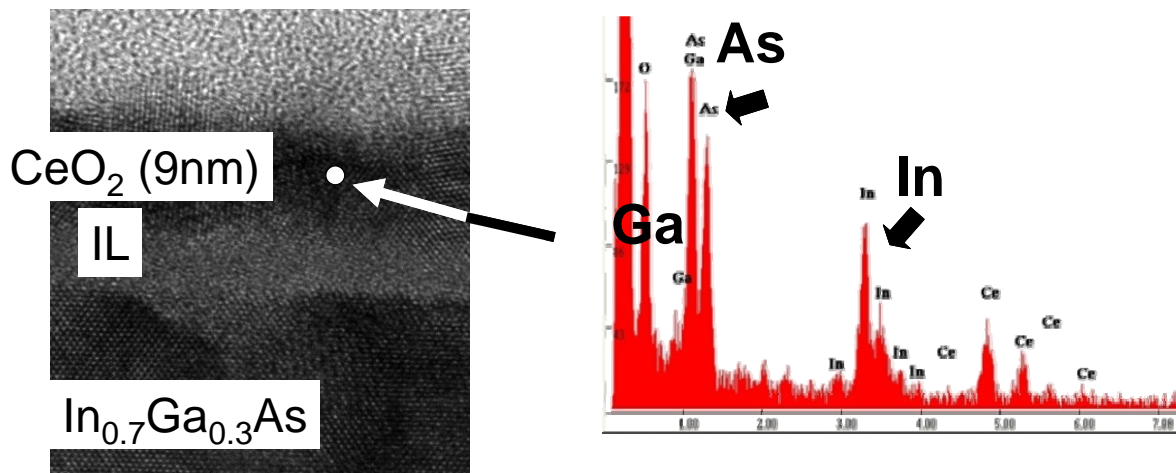
Figure3.2.3 Interface reaction with other rare earth oxides (CeO_x)

Next, figure 3.2.4 shows TEM image of the sample with HfO_2 gate oxide. An interfacial layer, which has bright contrast in the image, between HfO_2 and substrate was observed. From EDX analysis of the HfO_2 layer, no atom from the substrate was observed. Therefore, the diffusion of the atoms from the substrate can be suppressed with the use of HfO_2 layer.
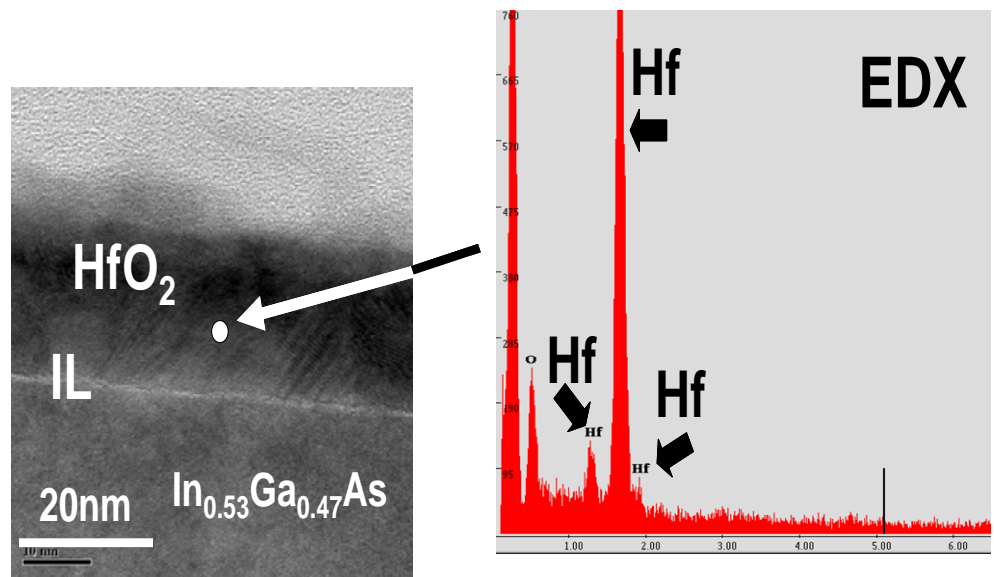
No As was detected in HfO$_2$ layer

Figure 3.2.4 TEM images and EDX analysis of HfO$_2$/In$_{0.53}$Ga$_{0.47}$As

Figure 3.2.5 is the summary of the interfacial reaction model with HfO$_2$ and RE-oxide. After annealing, an interfacial layer is formed for both HfO$_2$ and RE-oxide capacitor. Some of the atoms from the substrate still continue to diffuse into oxide for RE-oxide case. However for HfO$_2$, the diffusion of atoms from the substrate is suppressed. The difference in the diffusion constant of the atoms from substrate may be the important property difference between HfO$_2$ and RE-oxide.
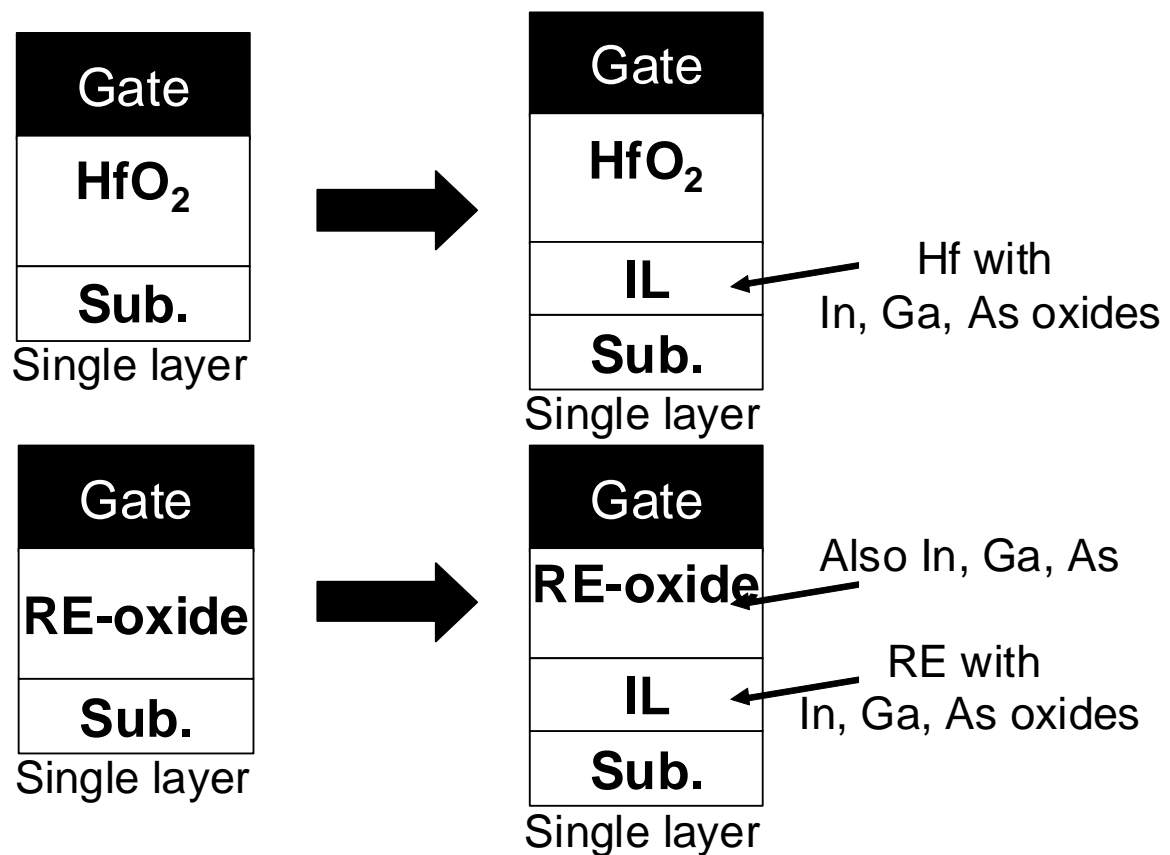
Figure 3.2.5 Interfacial reaction models

3.3 Leakage current density

Figure 3.3.1 and 3.3.2 show J_g-V_g characteristics for four capacitors ; HfO_2 (10nm thick) ,La_2O_3 (12nm thick) , PrO_x and CeO_x single layers with $300\,^oC$ and $500\,^oC$ PMA in F.G ambient for 5min. From these figure, we can see that RE-oxide capacitors show larger leakage current than that of HfO_2. This is why As diffusion from substrate causes large leakage current. On the other hand, in the annealing condition at PMA500 ^oC, Leakage current density of fabricated capacitors increase compared to 300 ^oC. It's also considered that the amount of As diffusion into insulator increase by high temperature

annealing. Meanwhile, larger leakage current of CeO_x than other RE-oxides is attributed that smaller band gap of 3.2eV.
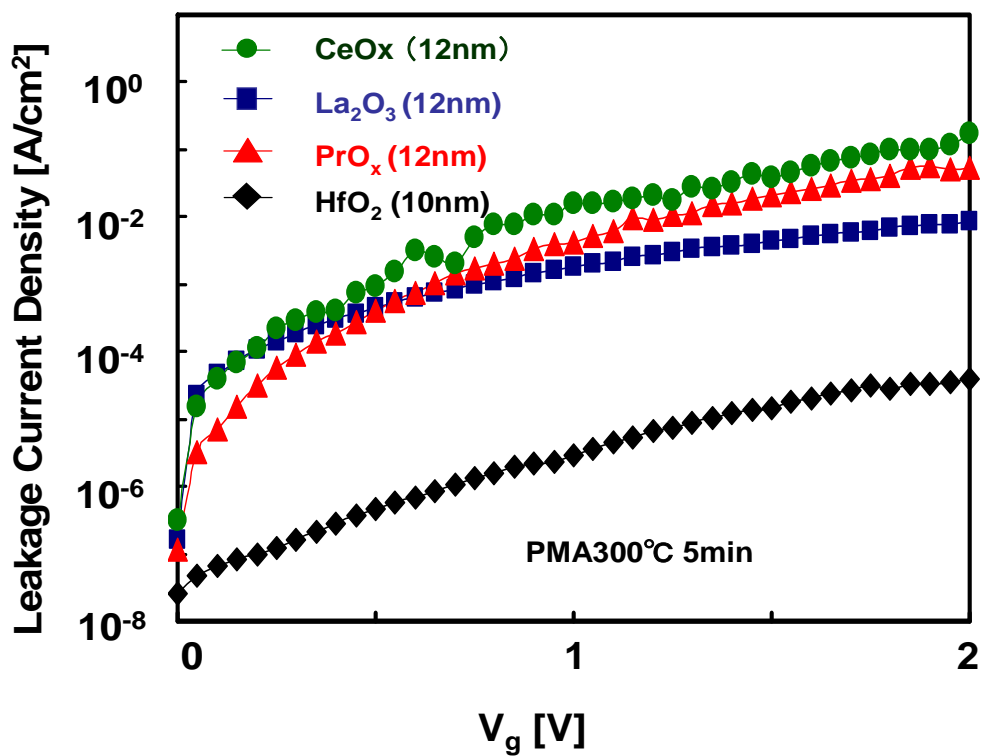
Figure 3.1 J_g-V_g plots of HfO_2, La_2O_3, PrO_x, and CeO_x layer with PMA300℃
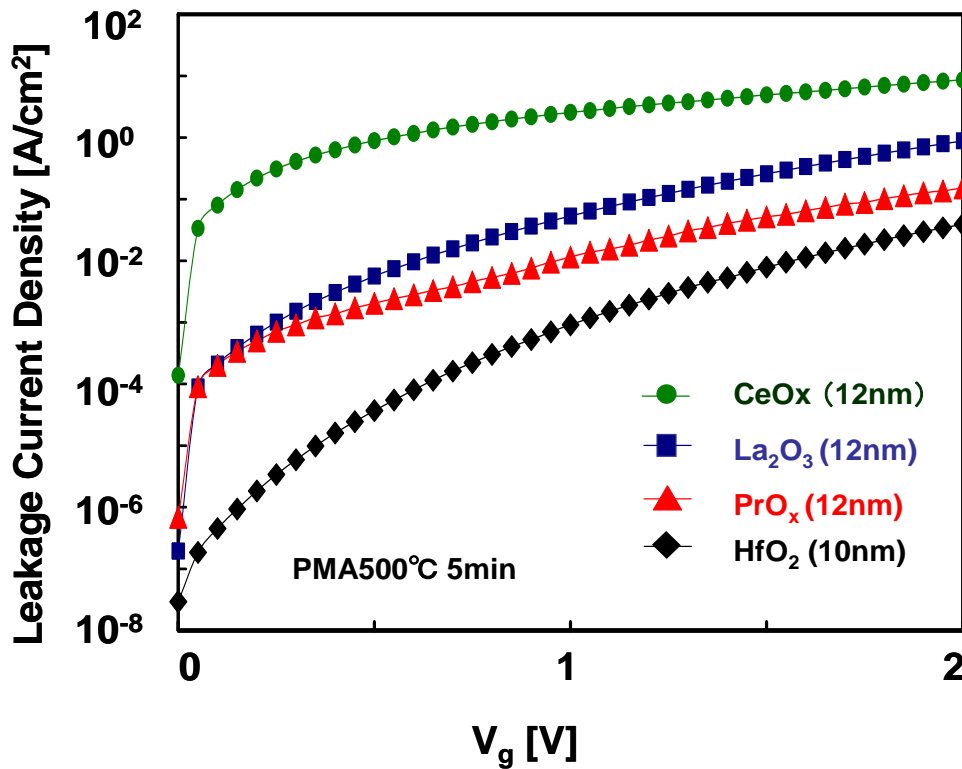
Figure 3.2 J_g-V_g plots of HfO_2, La_2O_3, PrO_x, and CeO_x layer with PMA500℃

3.4 CV Characteristics

Capacitance-Voltage (C-V) measurements are widely used to quantitatively study the MOS structures. There are several important parameters in evaluating high-k dielectrics on novel channel materials, such as hysteresis and frequency dispersion.

Figure 3.4.1~3.4.4 show the C-V characteristics of the fabricated MOS capacitors (HfO_2, La_2O_3, PrO_x, CeO_x) as a function of PMA temperature. PMA 300℃ samples show large C-V hysteresis which indicates the large amount of defects at the high-k oxide/InGaAs interface. On the other hand, as PMA 500℃ samples exhibit very small C-V hysteresis, and the value of accumulation capacitance is drastically decreased with increasing the

annealing temperature. The decrement of capacitance value is attributed that interfacial

layer is grown at 500 $^\circ$C in each oxides.
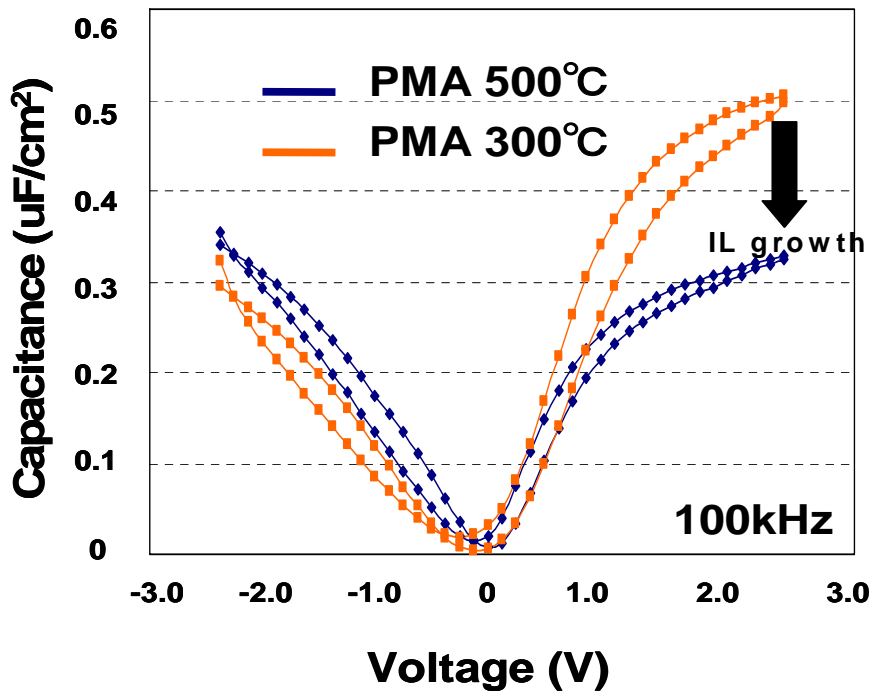
Figure3.4.1 CV characteristics of HfO$_2$ (10nm) capacitor
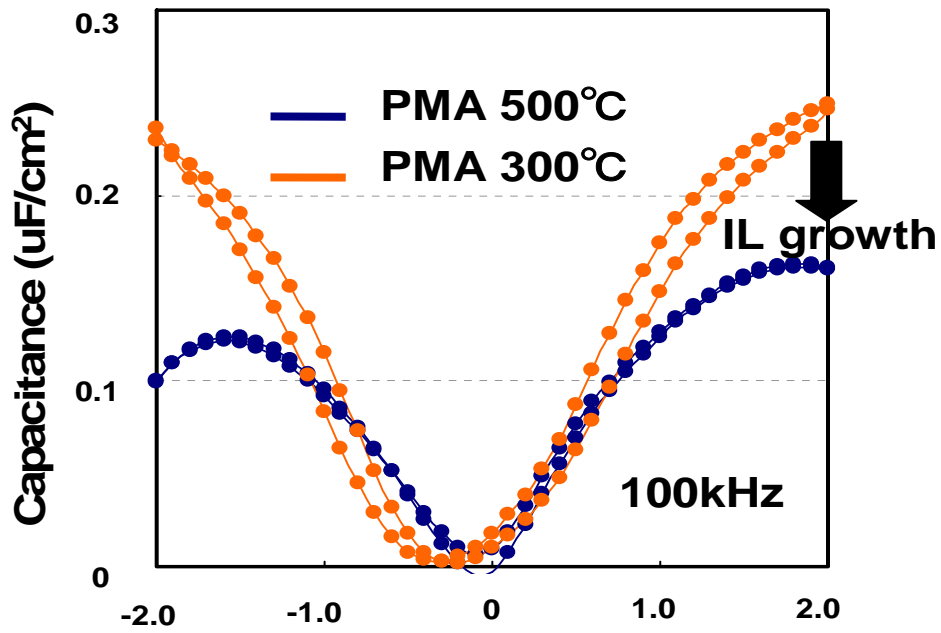
Figure3.4.2 CV characteristics of La$_2$O$_3$ (12nm) capacitor
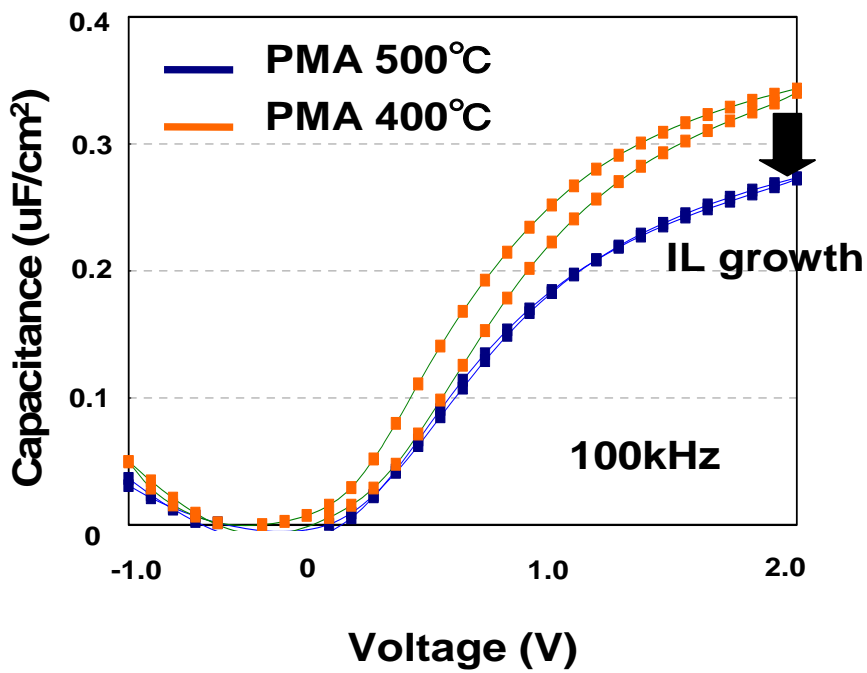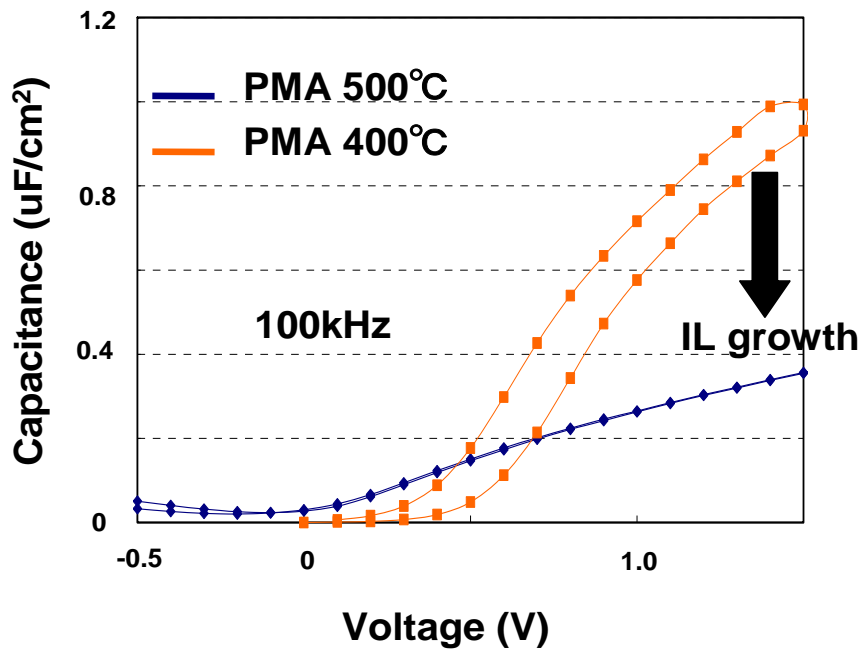

Figure3.4.3 CV characteristics of PrO$_x$ (12nm) capacitor

Figure3.4.4 CV characteristics of CeO_x (12nm) capacitor

3.5 Frequency Dispersion in CV curve

The frequency dispersion on accumulation capacitance is also important issue for high-k dielectrics on III-V MOS device. Figure 3.4.5~3.4.8 show the frequency dispersion of the fabricated MOS capacitors (HfO_2, La_2O_3, PrO_x, CeO_x) at PMA 400 ^{o}C in frequency range 10 kHz to 1 MHz. In the case of low frequency, carriers can react to its ac voltage which indicate high interface state density, were observed.

In CeO_x capacitor, very large frequency dispersion is exhibited large frequency dispersion. The large frequency dispersion suggests their poor interfacial quality of CeO_x on InGaAs. Meanwhile, PrO_x capacitor shows the lowest frequency dispersion in accumulation range among fabricated samples.
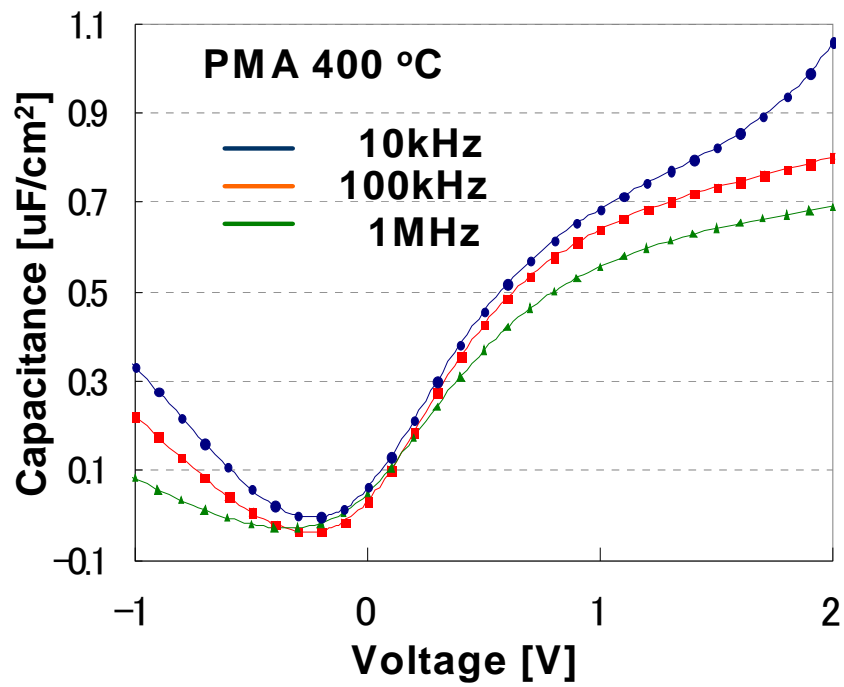
Figure3.4.5 Frequency dispersion in CV curves of HfO_2 capasitor
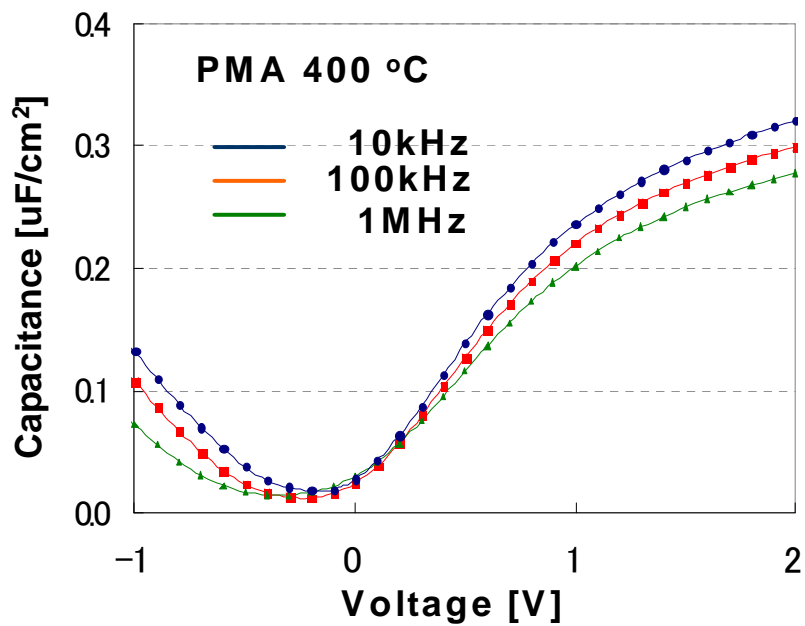
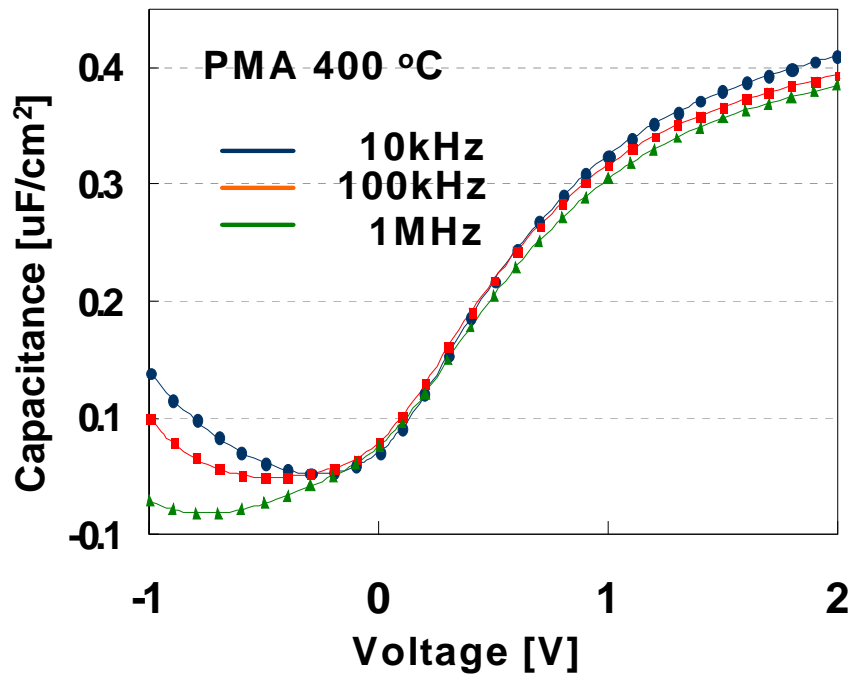Figure3.4.6 Frequency dispersion in CV curves of La_2O_3 capacitor

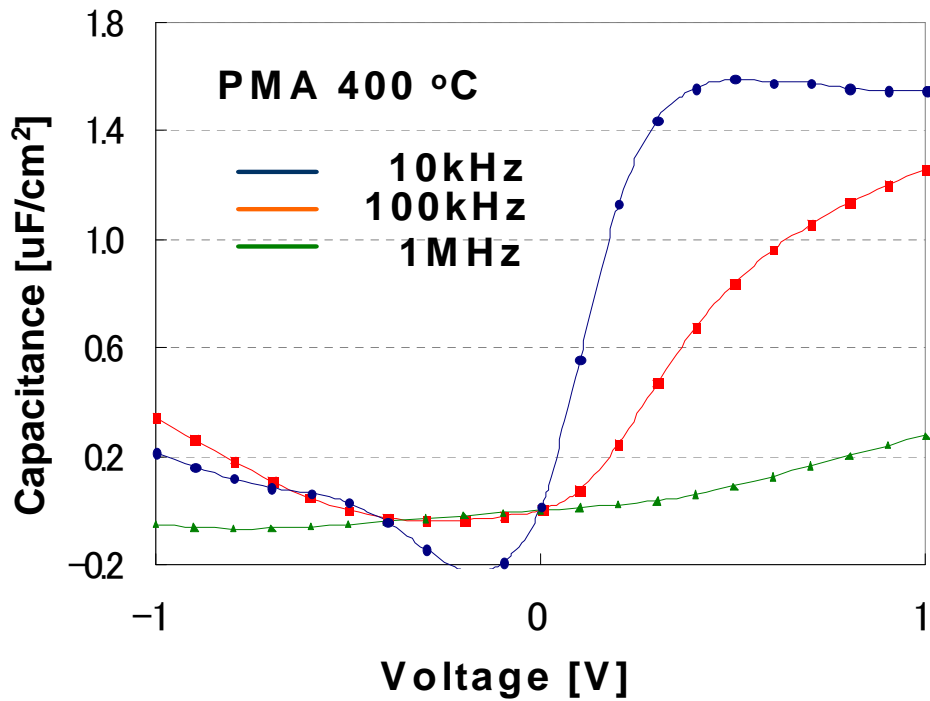Figure3.4.7 Frequency dispersion in CV curves of PrO$_x$ capacitor

Figure3.4.8 Frequency dispersion in CV curves of CeO$_x$ capacitor

3.6 Interfacial State density

The values of D_{it} were extracted by the conductance method. Figure 3.4.9 shows the equivalent circuit of MOS capacitor which is used to extract the interface state density. *Cox* is the capacitance of insulator at accumulation. *Cp* is the interface-trap capacitance, *Gp* is the conductance.
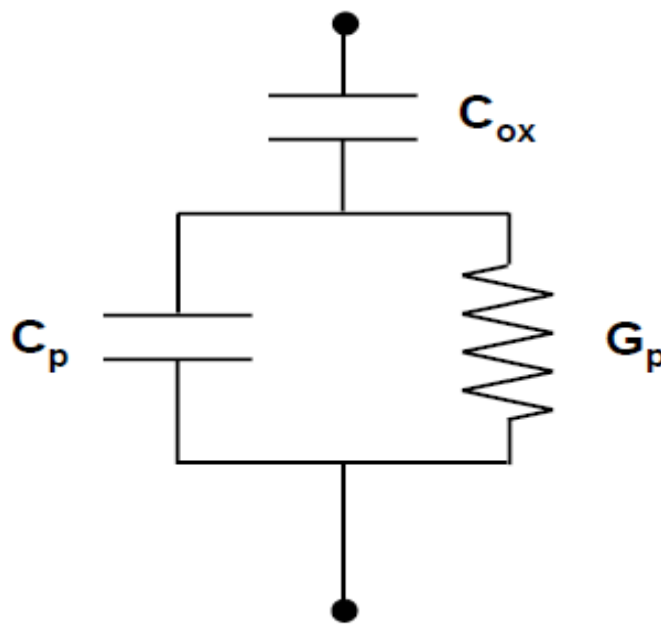

Figure 3.4.9 Equivalent circuit of a MOS capacitor

Figure 3.4.10 shows the interface state density of fabricated MOS capacitors as a function of PMA temperature.

A dependence on PMA temperature is not much observed in La_2O_3 and CeO_x samples. In the case of PrO_x, lower D_{it} of 1.44×10^{12} is shown at PMA temperature 500 °C. However, in HfO_2 sample, the value of interfacial state density gradually increases. It is considered that the interfacial layer (IL) between HfO_2 and InGaAs which has a poor interface quality is grown by high temperature annealing.

These results corresponds to the frequency dispersion of C-V curves as shown in Figure 3.4.5~3.4.8. PrO_x (12nm) capacitor at PMA400°C which was observed few frequency dispersion demonstrates the low interface state density compared to other three samples. On the other hand, HfO_2 and CeO_2 capacitors which was observed large frequency dispersion shows the high interfacial state density of 1.24×10^{13} and 8.09×10^{12} respectively.

From These results, interfacial state density causes large frequency dispersion in CV curve.
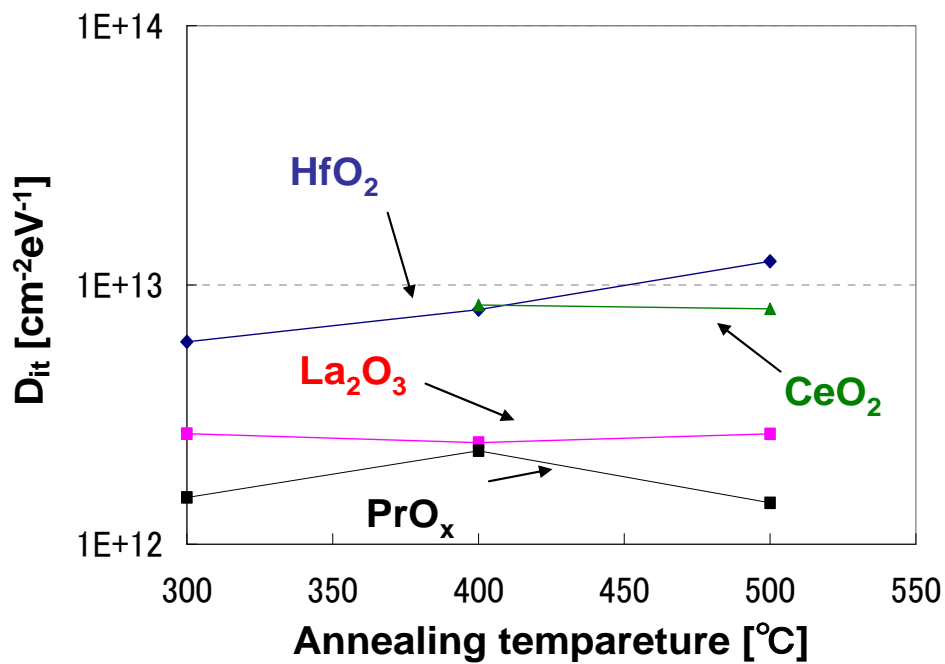
Figure. 3.4.10 D_{it} changes as a function of annealing temperature

【Chapter 4】

Conclusion

4.1 Conclusion of This Study

In this work, we studied the electrical characteristics of InGaAs MOS device with high-k gate dielectrics. RE-oxide capacitors revealed large leakage current compared to HfO_2. it's due to the difference of interfacial reaction between HfO_2 and RE-oxide. After annealing, an interfacial layer is formed for RE-oxide capacitor. Some of the atoms from the substrate diffuse into oxide for RE-oxide case. However for HfO_2, the diffusion of atoms from the substrate is suppressed. The difference may be the important property difference between HfO_2 and RE-oxide.

Next, we showed the CV characteristics of each samples. In the case of low temperature annealing, large hysteresis remained. By PMA 500 ^{o}C, the hysteresis is dramatically reduced in RE-oxide samples. However, CeO_x sample has large frequency dispersion due to its high interfacial state density and higher leakage current compared to other two RE-oxide samples. On the other hand, PrO_x sample exhibited small frequency dispersion, low interfacial state density of 1.64×10^{12} and relatively lower leakage current at PMA500 ^{o}C.

4.2 Recommendation for future work

In this study, we mainly focused CV characteristics, leakage current and interfacial state density for RE-oxide. PrO_x capacitor shows lower D_{it} compared to HfO_2 which is one of candidate as insulator for InGaAs MOS device. However, interfacial state density is still high. Therefore, further effort is needed. For example, it is necessary to find the optimal conditions of deposition temperature, annealing ambient, annealing temperature and passivation before high-k deposition. I think these optimizing is the key to obstacle

many problems of insulator on InGaAs MOS such as high interfacial state density.

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