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A Study on Ni Silicide contact for Si Nanowire FET

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Chapter 1

Introduction

1.1 Background of This Study

Nowadays, CMOS Large Scale Integrated circuits (LSIs), are really indispensable components for our human society. Needless to say, but almost all the human activities, such as living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc. proceed without the help of the CMOS LSI operation. For example, all the bank activities immediately stop without CMOS computation. Cellular phones do not exist without CMOS technology. Also, it should not be forgotten that CMOS semiconductor industry is one of big driving force of world economy, which is not limited to semiconductor fields but also includes many different kinds industries of materials, equipments, and software's required for the integrated circuits.

The continuous progress of CMOS technologies in terms of high-performance operation and low power consumption have been and will be very important because of the following three reasons.

At first, under the rapid progress of aging population and falling birth rate, we need to accelerate the replacement of some of the human jobs by intelligent machines – such as humanoid for elderly-care, for example. For the penetration of such intelligent robots to the daily family use, much higher intelligence and much lower power consumption than those of today are required. Therefore the development of CMOS integrated circuits with much more high performance and low power consumption are indispensable.

Secondly, our society is now facing the global warming. The reduction of the CO_2 gas release is a critically urgent issue for the earth. Continuous progress of CMOS technologies contributes to the 'cooling of the earth' in two ways. One is a direct contribution to the power reduction for IT (Information Technology) devices. Explosive increase of energy consumption at office and home are demanded to be suppressed by so called 'Green IT' procedure. This can be done by the development of low power and high performance CMOS devices used in data centers, routers and terminals, together with the highly efficient DC power feeding technology. Another contribution of the CMOS technology is the total power consumption reduction in social facilities such as entire city transportation traffic system, individual car operation system. This could be realized through the optimum power saving control of the operation by intelligent CMOS processors.

Thirdly, continuous progress of CMOS technology is critically important from the semiconductor industry point of view, as well as from the global economical point of view. The scaling of logic devices from 65nm to 45nm node and further has boosted the performance with the same and even smaller power consumption. The scaling of memory devices from 40nm to 30nm generation realized higher density in a chip, leading to the bit cost reduction. As a whole, the scaling has made products in new generation more attractive than the previousones. In case if there is no more progress in the CMOS technologies, semiconductor industry will face a disaster, and hence, the world economy will be in a crisis.

As mentions above, it is well known that the progress of CMOS LSI has been accomplished by the downsizing of MOSFETs. In the past, there were many downsizing limits predicted already from the 0.8 micron-meter generation since 1970's.

It was fortunate, however, that those limits were proven not to be true by the fabrication of smaller dimension MOSFETs and confirmation of their excellent electric characteristics. However, it has been predicted by most of the engineers now, that the downsizing would reach its limit probably about the gate length of 5 nm around the year of 2020. 2020 is not too far, but there is no sufficiently clear image for the world after CMOS reaches its scaling limit.

1.2 Ultimate CMOS downsizing

Why it is expected that about 5 nm is the limit of the downsizing? There are four main reasons; A) Difficulty on off-current suppression, B) Difficulty on increase in on-current, C) Difficulty on decrease in gate capacitance, D) Production and development cost increase.

A. Difficulty on off-current suppression

With decrease in gate length, off-current – the subthreshold and direct-tunneling leakage currents between source and drain – becomes significant at the gate length of 5~3 nm. From the consideration of the integration of huge number of MOSFETs in a chip, and resulted huge entire off-leakage current, probably, around 5 nm could be regarded as the limit of the gate length reduction. It might be even 10 nm or 3 nm, depending on the number of MOSFET integrations. Below 3 nm, the direct-tunneling leakage current increases very significantly and it is almost impossible to suppress the off-leakage current.

B. Difficulty on increase of on-current

Already the conduction of the drain current enters in the semi-ballistic region and thus, no significant increase of the drain saturated current or on-current is expected by reducing the gate length below 5 nm. Also, increase in source/drain resistance of small geometry MOSFETs tends to suppress the on-current.

C. Difficulty on increase of MOSFETs speed

One of the scaling merits is to reduce the gate capacitance, C_g, because the switching

time of MOSFETs is defined by C_gV_{dd}/I_d, where I_d is the drain on-current and V_{dd} is power voltage. However, C_g will not decrease in proportion to the gate length because of gate electrode sidewall capacitance component and that of drain/source-to-gate electrode overlap. These capacitance components are very difficult to be reduced because the gate electrode thickness and source/drain areas are very difficult to be further reduced.

D. Production and development cost increase

It is expected that the structure and manufacturing process of such small dimension MOSFETs with huge number of integration on a chip becomes very complicated and the development and production cost of the CMOS LSI would become to expensive to retain the profit for the production.

E. Possible solution after that

It is not sure exactly at what gate length and exactly at what year, the downsizing of MOSFETs reach its limit, but most of the engineers are expected that it would be happen around at the gate length of 5 nm and around in the year of 2020, although it could be 10 nm in 2015 or 3 nm in 2030.

Then, what will be the world after we reached the limitation. Unfortunately, at this moment, there are no candidates among the so-called ‘beyond CMOS’ or ‘Post Si’ new devices, which are believed to really replace CMOS transistors used for the products of highly integrated circuits within 20 years. Our opinion is that we need to still continue CMOS based transistors with ‘More Moore’ approach with combining that of ‘More than Moore.’ Then, what is ‘More Moore’ approach after we reached the downsizing

limit or with no more decrease in gate length? Because the number of the transistors in a chip is limited by the power consumption, we could continue the 'More Moore' law for certain period by replacing current CMOS transistors by nanowire or nanotube MOSFETs with which the suppression of off-leakage current and increase of on-current under low voltage could be realized because of its nature such as quasi-one-dimensional conduction, multi- quantum channel per wire/tube and high-density integration of wire/tube in multi-layers. Figure 1.1 shows our roadmap for wire and tube MOSFETs after 2020.

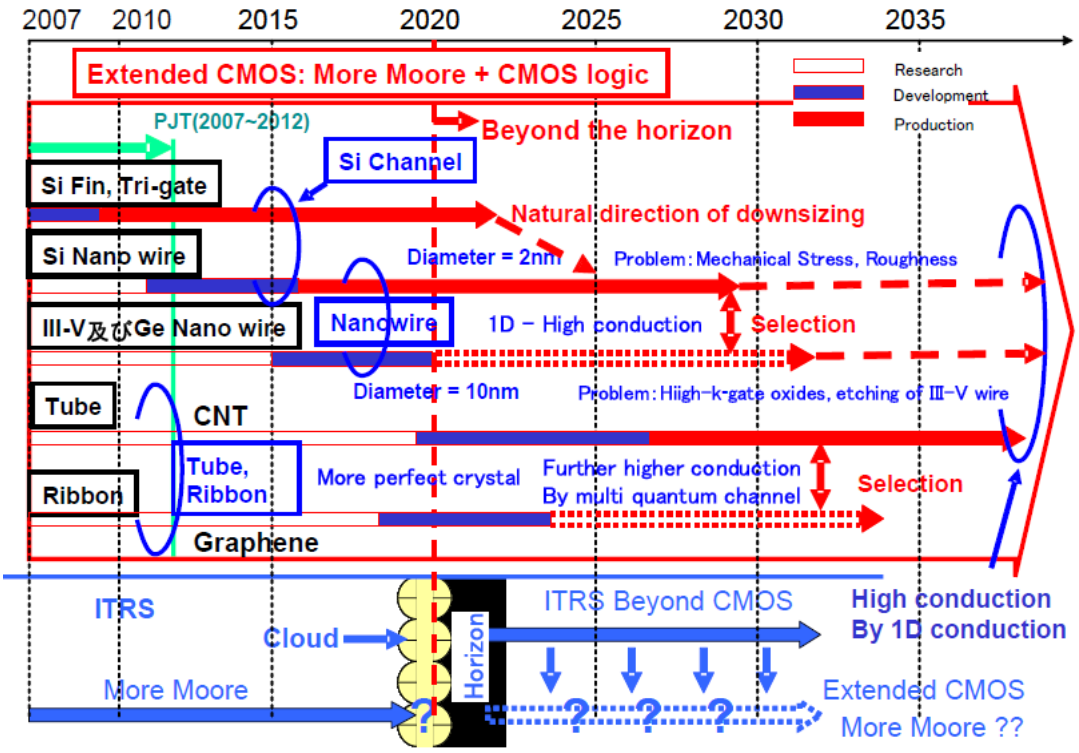


Figure 1.1 Rordmap for wire and tube.

1.3 Silicon Nanowire Field Effect Transistor

Si nanowire FET is considered as one of the promising candidates for further extending the device downsizing, owing to its gate-all-around (GAA) structure which enables better gate control capability than planar transistors [1-2]. Figure 1.2 shows schematic image of GAA structure. Therefore, high I_{on}/I_{off} ratio can be achieved. Figure 1.3 shows comparison of the requirement to the bulk Si, the ultra-thin body fully depleted (UTB FD) SOI and the double-gate (DG) MOSFET in 2008 in ITRS2008 with previously reported data on Si nanowire FET fabricated using CMOS compatible processes [3-9]. Si naowire FETs have already been obtained higher I_{on}/I_{off} ratio than any planer transistors.

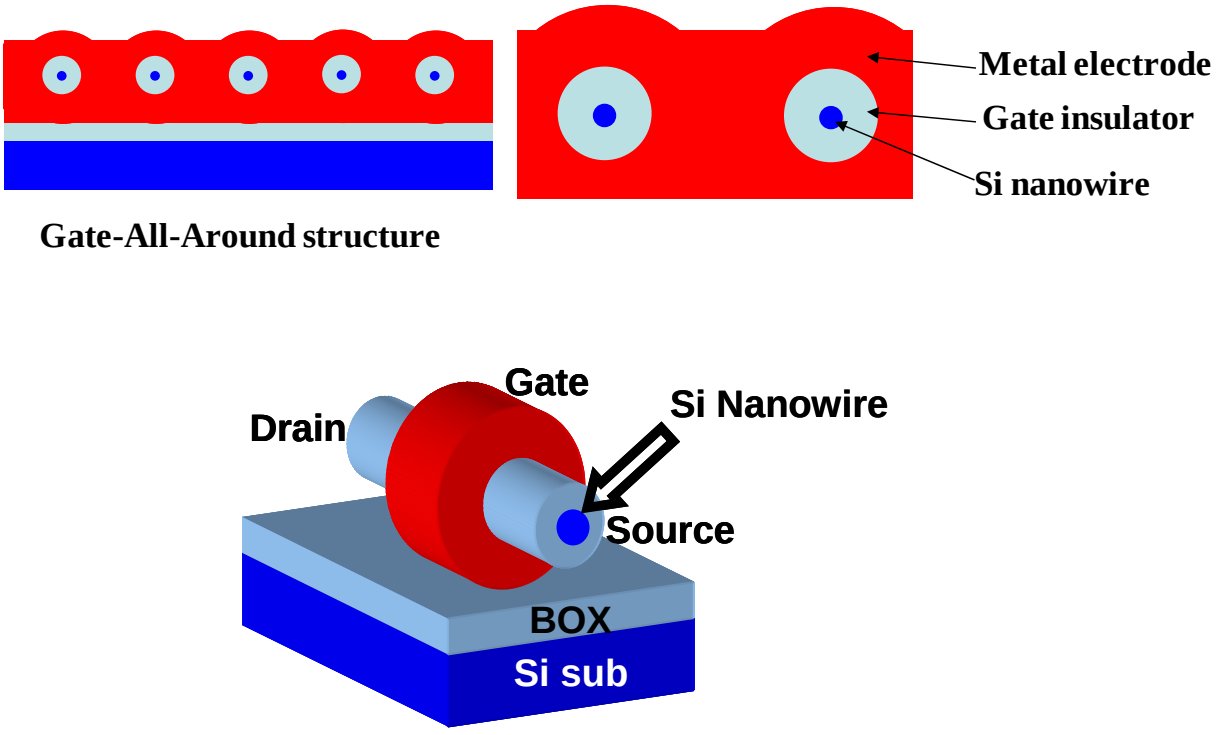


Figure 1.2 Schematic of GAA structure.

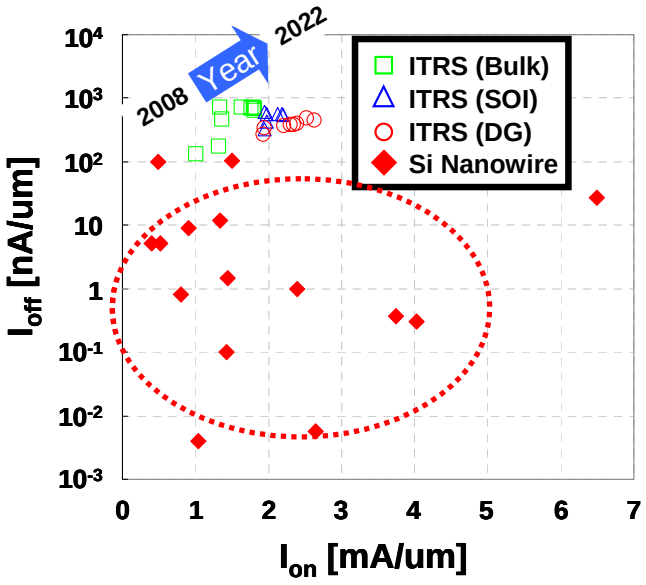


Figure 1.3 Comparison of the requirement to the bulk Si, UTB FD SOI and DG MOSFET in 2008 in ITRS2008 with previously reported data on Si nanowire FET fabricated using CMOS compatible processes.

Si nanowire FET has been fabricated by several techniques including, Si fins are patterned by lithography and etching followed by the oxidation (Figure 1.4 (a) shows Top-down method) or Methods using CVD, MBE and other processes to grow Si nanowire with better controllability of the size of the wire (Figure 1.4 (b) shows Bottom-up method) [10-11].

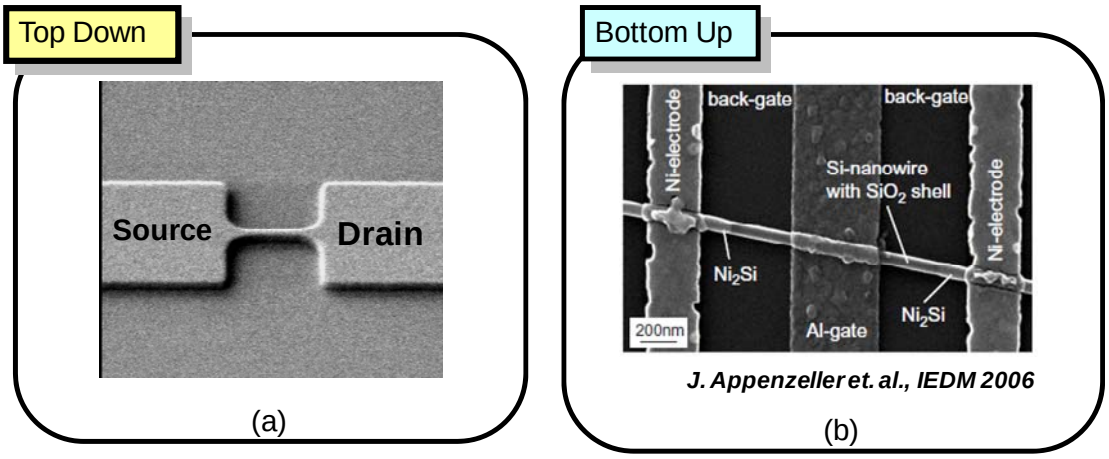


Figure 1.4 Fabrication methods of Si nanowire FET, (a)Top-down,(b)Bottom-up.

The electrical characteristics of Si nanowire FET are not yet completely understood should be clarified. Fabrication guideline for the shape control of Si nanowire must be facilitated the interface characteristic of the insulator on it, the geometry intolerances and surface roughness created by the Top-down processing, the strain, influence the transistor characteristic (mobility and threshold). In addition, another concern on Si nanowire FET is the increase in parasitic resistance at source and drain region, which eventually reduces the on-state current. Therefore, in this thesis, source-drain silicidation process of Si nanowire is investigated especially in term of its structural effect on the silicidation mechanism. For the study, Ni silicide was used because this material is currently used in the LSI production.

Refernces

[1] S. D. Suk *et al., IEDM Tech Dig.*, p. 717, 2005.

[2] S. D. Suk *et al., IEDM Tech Dig.*, p. 1, 2006.

[3] N.Singh et al., *IEDM*, p.547, 2006

[4] Y. Tian et al, IEDM, p.845, 2007

[5] K. H. Yeo et al., IEDM, p.539, 2006

[6] H. Lee et al., VLSI Tech. Symp., p.58, 2006

[7] W. W. Fang et al., *IEEE EDL*, vol. 28, no.3, p.211, 2007

[8] C. Dupre et al, IEEE, p749, 2008

[9] International Technology Roadmap for Semiconductor (ITRS), 2008 up data

[10] J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, and S. Guha , *Technical Digest of IEDM*, pp. 555 (2006).

[11] J. T. Sheu, S. P. Yeh, C. H. Lien, and S. T. Tsai, *Japanese Journal of Applied Physics*, Vol.45 , No.4B, pp. 3686-3689 (2006).

[12] R. Mukai, S. Ozawa and H. Yagi. *Thin Solid Film* 270 (1995)567

[13] H. Jeon, C. A. Sukow, J. W. Honeycutt, G. A. Rozgonyi and R. J. Nemanich. *J. Appl. phys.* **71** (1992) 4269

[15] F. Deng and R. A. Johonson. *J. Appl. Phys.* **81** (1997) 8047

[16] Toyota Morimoto, Tatsuya Ohguro, Hisayo Sasaki Momose , Toshihiko Iinuma, Iwao Kunishima, Kyouichi Suguro, Ichiro Katakabe, Hiroomi Nakajima, Masakatsu Tsuchiaki, Misuki Ono, Yasuhiro Katsumata, and Hiroshi Iwai, *IEEE TRANSACTIONS ON ELECTRON DEVICE*, VOL.42, NO.5 (1995)

Chapter 2

Fabrication and Characterization Method

2.1 Experimental Procedure

2.1.1 Si Substrate Cleaning Process

At first, high quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25^{o}C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩcm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the Si substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The first step, which use a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4: H_2O_2=4:1), was performed to remove any organic material and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:99). Then the cleaned wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber to deposit as soon as it was dried by air gun.

2.1.2 Oxidation Furnace

Thermal oxidation is accomplished by using an oxidation furnace (or diffusion furnace, since oxidation is basically a diffusion process involving oxidant species), which provides the heat needed to elevate the oxidizing ambient temperature. A furnace typically consists of: 1) a cabinet; 2) a heating system; 3) a temperature measurement and control system; 4) fused quartz process tubes where the wafers undergo oxidation; 5) a system which transfers process gases into and out of the process tubes; and 6) a loading station used for loading (or unloading) wafers into (or from) the process tubes.

The heating system usually consists of several heating coils that control the temperature of the furnace tubes. The wafers are placed in quartz glassware known as boats, which are supported by fused silica paddles inside the process tube. A boat can support many wafers. The oxidizing agent (oxygen or steam) then enters the process tube through its source end, subsequently diffusing to the wafers surface where the oxidation occurs. In this study, Figure 2.1 shows a photo of Oxidation Furnace.

Depending on oxidant species used (O_2 or H_2O), the thermal oxidation of SiO_2 may either be in the form of dry oxidation (wherein the oxidant is O_2) or wet oxidation (wherein the oxidant is H_2O). The reactions for dry and wet oxidation are governed by the following equations:

1) for dry oxidation: $Si\ (solid) + O_2\ (vapor) \rightarrow SiO_2\ (solid)$; and

2) for wet oxidation: $Si\ (solid) + 2H_2O\ (vapor) \rightarrow SiO_2\ (solid) + 2H_2\ (vapor)$.

Figure 2.2 shows the thermal oxidation rate using bulk P-Si substrate and SOI substrate which has 51 nm thick SOI, 137.8 nm thick BOX layer. The figure indicate

that SiO_2 thickness increases and residual SOI thickness decreases as increasing oxidation time.

Figure 2.1 Oxidation furnace.

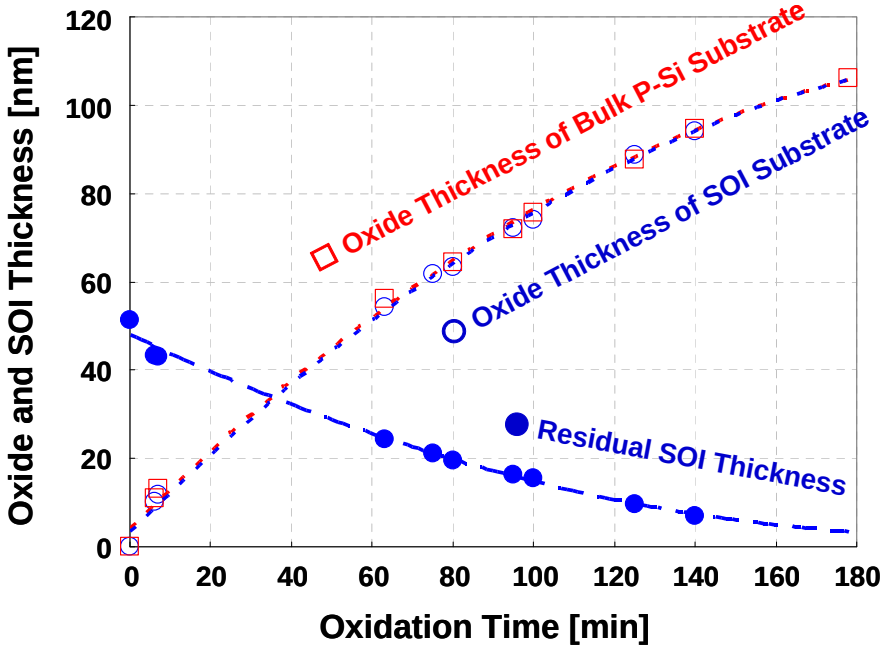


Figure 2.2 Oxide rate of dry oxidation.

2.1.3 Photolithography

The process flow and a photo of the photolithography apparatus used throughout this study are shown in Figure.2.3. Electrical hotplate is used for the baking purposes. The spin-coated photoresist layer was exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light with the wavelength of 405 nm. MJB4 of Karl Suss contact-type mask aligner shown in Figure.2.3 was used for the photolithography process. The exposure duration was set to 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.). The wafers were dipped into the solvent for 2 minute and baked at 130 ˚C for 5 minutes.

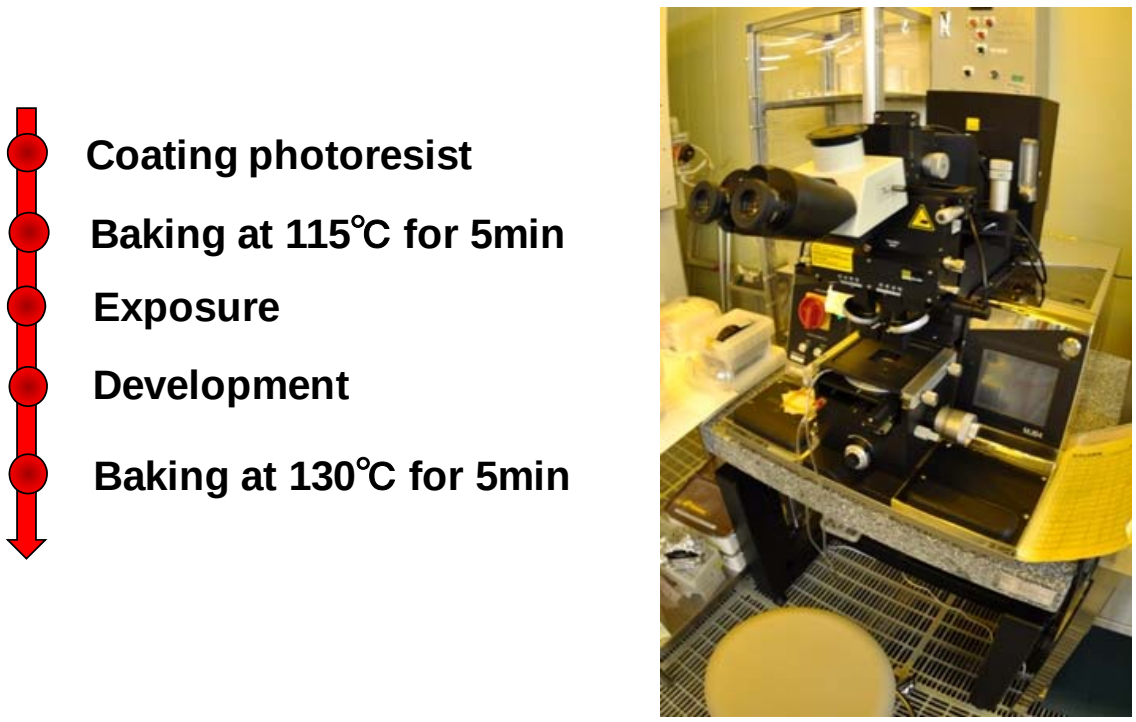


Figure 2.3 The process flow and the photo of photolithography apparatus.

2.1.4 UHV-Sputtering System

After cleaned by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive layer.) and Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. A high voltage across a low-pressure gas (usually argon at about 5 mTorr) is applied to create a "plasma," which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the "target," composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to the substrate surface.

An UHV-sputtering system is used for thin film formations of electronic devices, for experiments of GMR, and for creating new high temperature superconductors materials. In this study, UHV Multi Target Sputtering System ES-350SU shown Figure 2.5 was used. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. For other details, Table 2.1 is attached for reference.

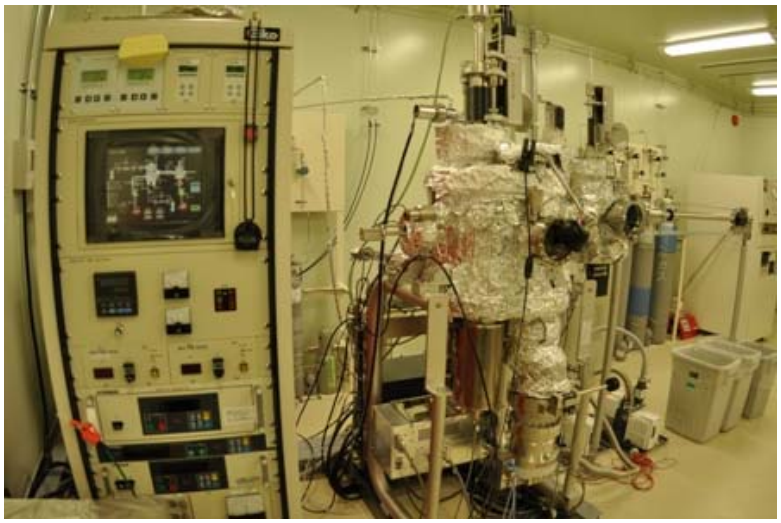


Figure 2.4 Photo of UHV Multi Target Sputtering System ES-350SU.

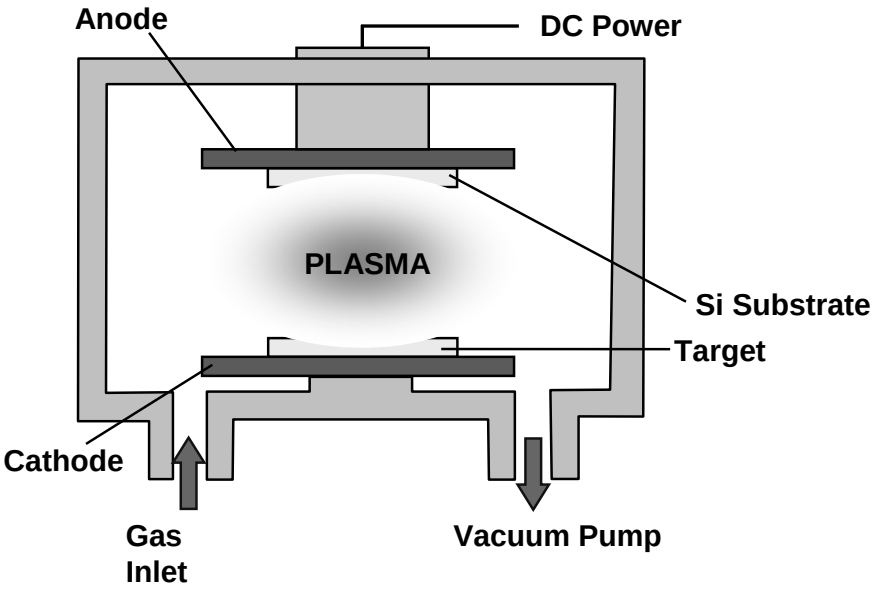


Figure 2.5 Structure of UHV sputtering system.

Growth chamber	1. Ultimate pressure	1.5 x 10^{-6}Pa
	2. Substrate size	2 inch in diameter
	3. Heating temperature	600ºC
	4. Heater type	Lamp type heater
	5. Target	3 inch x 5 pieces (motor-driven)
Load lock chamber	6. Vacuum pumps	TMP 500L/sec and RP 250L/min
	7.Ultimate pressure	6.6 x 10^{-5}Pa
	8. Vacuum pumps	TMP60L/sec and RP90L/min
	9. Substrate holder with cooling function / Substrate holder with heating function /Cleaning function / Radical beam source	

Table 2.1 Specifications for UHV Multi Target Sputtering System ES-350S.

2.1.5 Infrared Annealing Furnace

After formation in the UHV sputtering system, thin films of Ni/Si, Ni/M/Si, or M/Ni/Si were transferred to annealing furnace to perform thermal process. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation is QHC-P610CP (ULVAC RIKO Co. Ltd). Figure 2.6 is the photo of the infrared annealing furnace, whose schematic illustration was shown in Figure 2.7. The annealing was performed by six infrared lamps surrounding the sample stage made of carbon coated by SiC. The heating temperature was controlled by thermocouple feedback.

Figure 2.6 Photo of infrared annealing furnace.

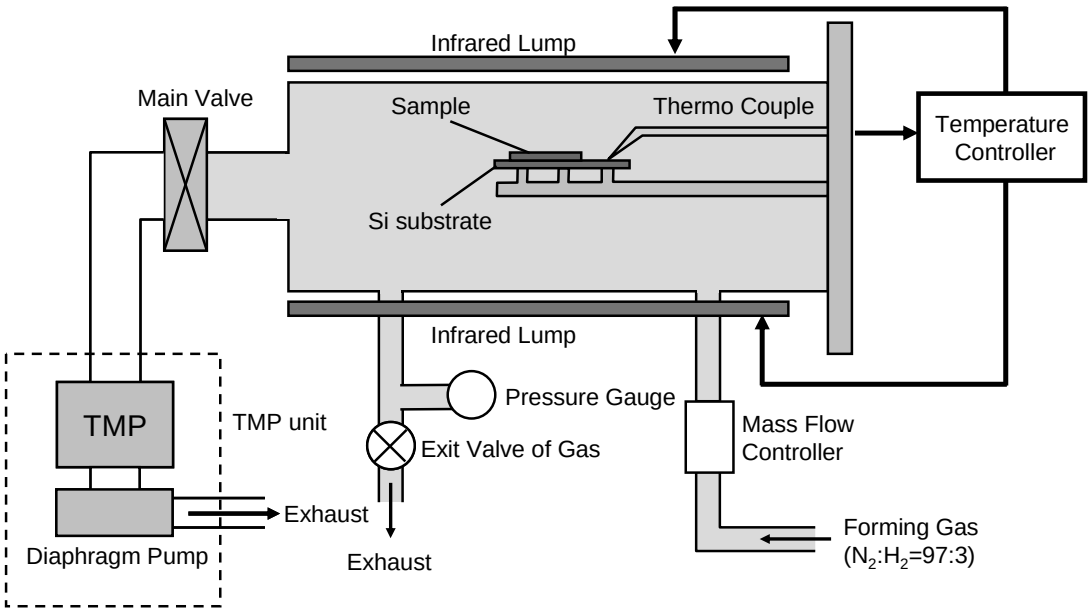


Figure 2.7 Schematic image of infrared annealing furnace.

2.2 Measurement Methods

2.2.1 Scanning Electron Microscope (SEM)

Figure.2.9 shows Scanning Electron Microscope (SEM) system. The equipment is S-4800 (HITACHI High-Technologies Corporation). The ‘Virtual Source’ at the top represents the electron gun, producing a stream of monochromatic electrons. The stream is condensed by the first condenser lens. This lens is used to both form the beam and limit the amount of current in the beam. It works in conjunction with the condenser aperture to eliminate the high-angle electrons into a thin, tight, coherent beam. A user selectable objective aperture further eliminates high-angle electrons from the beam. A set of coils then scan or sweep the beam in a grid fashion and make the beam dwell on points for a period of time determined by the scan speed. The final lens, the Objective, focuses the scanning beam onto the part of the specimen desired. When the beam strikes the sample, interactions occur inside the sample and are detected with various instruments interactions. Before the beam moves to its next dwell point these instruments count the number of interactions and display a pixel on a CRT whose intensity is determined by this number. This process is repeated until the grid scan is finished and then repeated, the entire pattern can be scanned 30 times per second.

Figure 2.8 Photograph of SEM equipment.

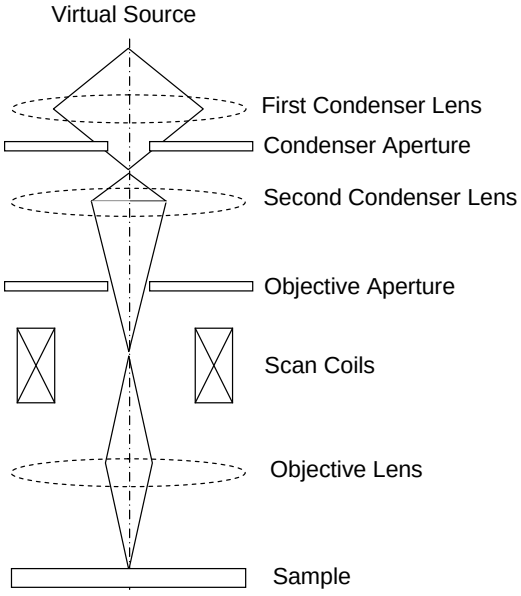


Figure 2.9 Schematic drawings of SEM equipment.

2.2.2 Transmission Electron Microscope (TEM)

Cross-section TEM image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Figure.2.10 shows TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording of the image is performed by direct exposure on exclusive films for electron microscope use located below the fluorescent screen.

Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 to 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 to 0.3 nm at 200 kV.

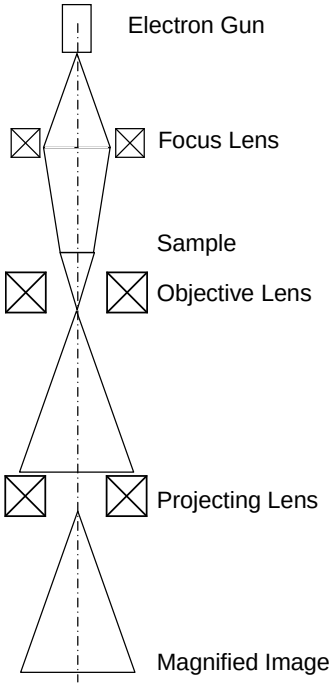


Figure 2.10 Schematic drawings of TEM equipment.

2.2.4 Auger Electron Spectroscopy (AES)

Auger electron emission is initiated by the creation of an ion with an inner shell vacancy. Auger electrons are emitted in the relaxation of the excited ion. In this process an electron from a higher lying energy level fills the inner shell vacancy with the simultaneous emission of an Auger electron. This simultaneous two electron coulombic rearrangement results in final state with two vacancies. Auger electron emission is one of two relaxation mechanisms possible in an excited ion. The other is x-ray fluorescence, in which a photon is emitted.

The two relaxation processes for an excited ion are shown in the energy level diagrams of figure 2.11. Note that all energies are referenced to the Fermi level Ef, which corresponds to zero binding energy. In these diagrams the initial vacancy occurs in the K shell. The incident particle is any particle that ionizes the K shell. Hence, Auger emission will result from bombardment of a sample with electrons, x-rays, or ions. However, dedicated Auger instruments typically employ electron irradiation since electron beams can be focused to very small diagram.

Both Auger electron emission and photoelectron emission occur as a consequence of the x-ray irradiation used in X-ray Photoelectron Spectroscopy (XPS) also known as Electron Spectroscopy for Chemical Analysis (ESCA). In XPS, low energy x-ray, such as the Mg or Al Kα, impinge on a sample and cause the emission by Auger electron emission, since x-ray fluorescence is a minor process in this energy range (up to ~1500eV).

The sum of the total Auger yield and the fluorescence yield is unity, since an excited ion can relax by either Auger electron emission or x-ray emission. Auger electron emission is the more probable decay mechanism for low energy transitions, i.e., for low

atomic number elements with initial vacancy in the K shell and for all elements with initial vacancies in the L or M shells. By choosing an appropriate Auger transition, all elements (except H and He) can be detected with high sensitivity. Auger transitions are typically labeled by the energy levels of the electrons involved, using x-ray spectroscopy nomenclature. The first label corresponds to the energy level of the initial core hole. The second and third labels refer to the initial energy levels of the two electrons involved in the Auger transition. Thus the Auger transition shown in Figure is a $KL_{II}L_{III}$ transition, or simply KLL transition [1].

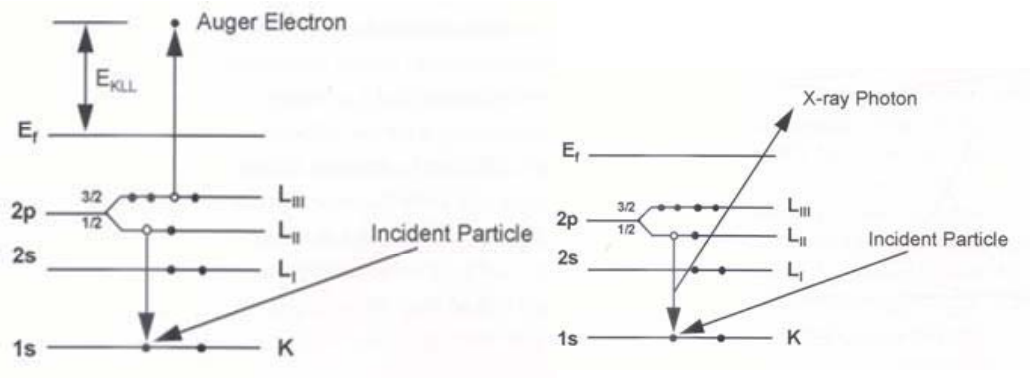


Fig. 2.11 Schematic diagrams of Auger electron emission and x-ray fluorescence. The incident particle causes the ejection of a K shell electron [1].

AES is a very useful analytical method to evaluate the elemental depth profile compositions of regions of several tens of nanometers in the near surface layer of a sample [2]. The equipment is PHI 700 (ULVAC-PHI, INC.).

References

[1] Handbook of Auger Electron Spectroscopy Third Edition.

[2] N. Urushihara et al, *J. Vac. Sci. Technol*. A 26(2008) 668-672.

Chapter 3

Nickel Silicidation of Si Nanowire and The Encroachment Phenomenon

3.1 Introduction

3.1.1 The Reason for the Silicidation of Source and Drain regions

In MOSFET fabrication, Silicide often has been used for the materials of source/drain regions and gate electrodes. There are many kinds of metals (Ni, Ti, Co, Mo, W, Pt and so on…) for silicides. Especially, Ni-, Co-, and Ti- silicides with low resistivities have been studied for a long time. Though $TiSi_2$ was used in sub-micron era, it has relatively large sheet resistance when the line width becomes thin. Therefore, Ni and Co-silicides are used in 100 nm- or smaller generations. Although $CoSi_2$ has very good electrical properties, its high Si consumption and junction spiking problems limit its application to deep sub-micrometer devices [1]. The study on Ni silicide started to become an active research area in the 1970's and the silicide technology in MOSFET fabrication process since 1980's [2-4].

3.1.2 Resistance in Self-Aligned Silicide Technologies

Both R_{sh} and R_{co} are greatly reduced in advanced CMOS technology with self-aligned silicide. R_{sh} of the source-drain diffusionresion region is simply,

$$R_{sh} = \rho_{sd} \frac{S}{W} \qquad (3.1)$$

,where W is the device width, S is spacing between the gate edge and the contact. The

sheet resistance is of the order of 50-500 Ω/□ for the source drain without silicide.

As shown schematically in Fig.3.1, a highly conductive (≈ 2-10 Ω/□) silicide film is formed on all the gate and source-drain surfaces separated by dielectric spacers by the self-aligned process. Since the sheet resistivity of silicide is 1-2 orders of magnitude lower than that of the source-drain, the silicide layer practically shunts all the currents, and the significant contribution to R_{sh} is from the nonsilicided region under the spacer. This technology is virtually regarded as the method which reduces the length S to 0.01-0.02 μm. $R_{sh}W$ should be no more than 50 Ω-μm in sub-micron MOSFETs. At the same time, R_{co} between the source-drain and silicide is also reduced, since now the metal/semiconductor contact area can be enlarged to the entire diffusion area. So it is one of the most important issues to enhance the on-current, especially for Nanowire MOSFETs in which the volume source and drain region is limited as mentioned below.

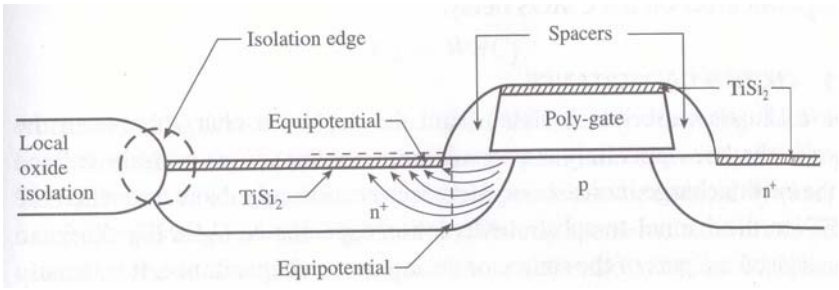


Figure 3.1 Shematic diagram of an- n-channel MOSFET fabricated with self-aligned $TiSi_2$, showing the current flow pattern between the channel and the silicide [5].

3.1.3 Source-Drain Series Resistance

As the current flows from the channel to the terminal contact, there is a voltage drop in the source and drain regions due to the finite silicon resistivity and metal contact

resistance. In a long–channel device, the source-drain parasitic resistance is negligible compared with the channel resistance. In short-channel device, however, the source-drain series resistance can be an appreciable fraction of the channel resistance and can therefore cause significant current degradation. Resistance on the source side is particularly troublesome, as it degrades the gate drive as well.

3.1.4 Ni Silicidation on Bulk Si

This section describes about Ni silicidation on bulk Si. Ni silicides are formed in variety formation, which are NiSi, Ni_2Si, $NiSi_2$, Ni_3Si, $Ni_{31}Si_{12}$ and Ni_3Si_2. Fundamental data about Ni silicides are shown in table 3.1 [9-10]. The data indicate that NiSi has the lowest resistivity, and the Ni to Si ratio is rather large for the formation of NiSi.

Phase	Resistivity (μΩcm)	Activation Energy E_a (eV)	Density (g/cm3)	$T_{silicide}/T_{Ni}$	Silicon consumed/ T_{Ni}
Ni	7-10	-	8.91	1	0
Ni_3Si	80-90	-	7.87	1.31	0.61
$Ni_{31}Si_{12}$	90-150	-	7.56	1.40	0.71
Ni_2Si	24-30	1.5	7.51	1.47	0.91
Ni_3Si_2	60-70	-	6.71	1.75	1.22
NiSi	10.5-18	1.4	5.97	2.20	1.83
$NiSi_2$	34-50	-	4.80	3.61	3.66
Si	Dopant dependent	-	2.33	-	-

Table 3.1 Fundamental data of Ni silicide.

3.1.5 Ni Silicidation on Bulk Si and The Encroachment Phenomenon

For Si Nanowire, the parasitic resistance becomes very large as the volume source and drain is limited. Therefore, silicidation with precise control of the length of Ni silicide in the Nanowire is important to obtain high on-current. But the control of Ni silicide has a problem which is called encroachment [6-8]. Figure 3.2 shows an X-TEM image of Ni silicide encroachment of <110>/Si (110) nMOSFET [8]. In this figure, Ni silicide encroachment penetrates into the channel region.

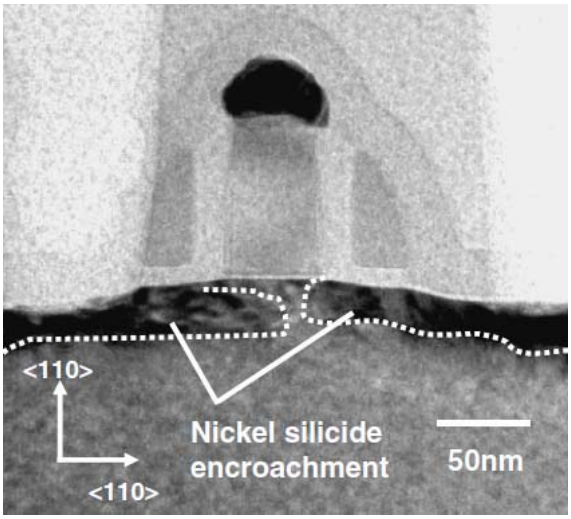


Figure 3.2 X-TEM image of Ni silicide encroachment of <110>/Si (110) nMOSFET [8].

The encroachment of Ni silicide in Si Nanowire makes the control of the channel length of transistor difficult. Also due to the parasitic overlap capacitance, the degradation of the transistor speed will become an issue. In addition, if p-n junction is located under or next to the silicide region, severe leakage current increase would be predicted.

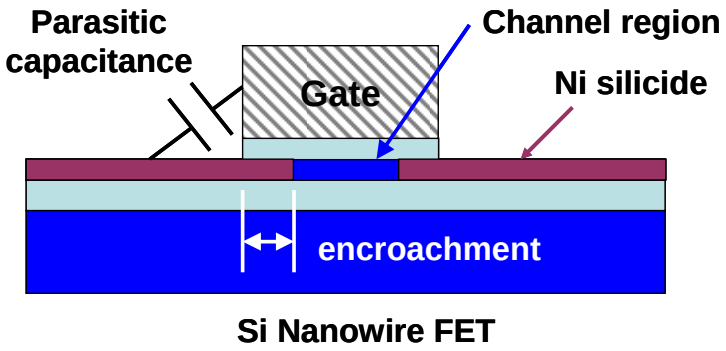


Figure 3.2 A Schematic figure of Si Nanowire FET using Ni silicide Source/Drain.

3.2 Experimental

We utilized top-down fabrication process of Si nanowires and investigated Ni silicidation phenomenon by the reaction of nanowires and Ni films. Figure 3.2 shows the experimental procedure. Si nanowires have been fabricated by lithography, dry etching and thermal oxidation. Conditions of the thermal oxidation are varied depending on the SOI thickness. For example, it was at 1000 ^{o}C for 45min for 30-nm-thick SOI. Oxide around Si Nanowire was partially removed by buffered HF solution. 6-nm-thick Ni film was deposited on exposed Si Nanowire by magnetron sputtering in an Ar ambient. Rapid Thermal Annealing (RTA) at various temperatures ranging from 350 ^{o}C to 600 ^{o}C was performed in forming gas (F.G) (N_2:H_2=97%:3%) ambient. Unreacted Ni film was removed by SPM (mixed H_2SO_4 and H_2O_2) solution. Ni silicide encroachment into Si Nanowire was observed by SEM and the encroachment length was measured.

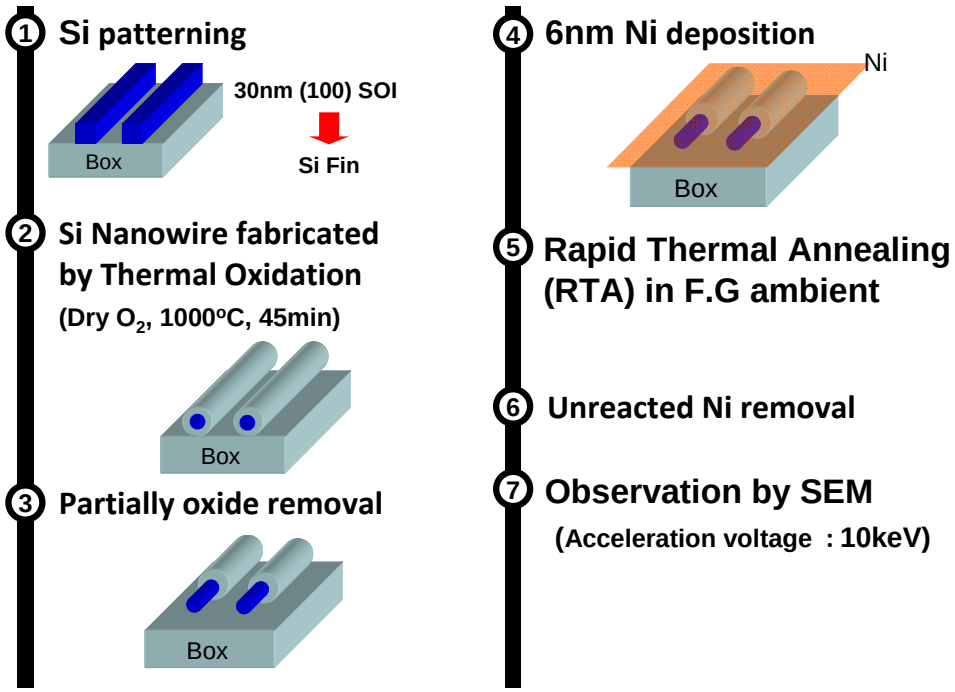
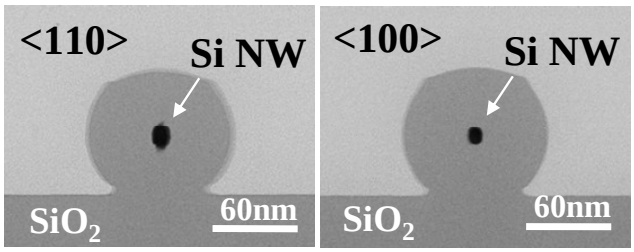


Figure 3.2 Fabrication process flow.

3.3 Results and Discussion

3.3.1 TEM Images of Si Nanowire

Figure 3.3 shows the cross-section TEM views of <110> and <100> Si Nanowire formed by thermal oxidation of 61-nm-thick (100) SOI substrate at 1100 ^{o}C for 30 min. The starting Si fin width was 40.8 nm in this case.



cross-section 17nm x 12nm **cross-section 12nm x 8nm**

Figure 3.3 <110> and <100> Si Nanowire formed by the thermal oxidation of (100) SOI substrate with the thickness of 61nm at 1100^{o}C for 30min.

3.3.2 SEM and TEM Images of Ni Silicide Contact for Si Nanowire

The reaction of Ni and Si take place at thermal treatment. Due to the diffusion of Ni atoms into Si Nanowire, Ni silicide starts to form inside the Si Nanowire, encroachment of Ni silicide occurs. Figures 3.4 shows schematic figures of the encroachment of Ni silicide Si Nanowire. The length of encroachment is a function of annealing time and temperature.

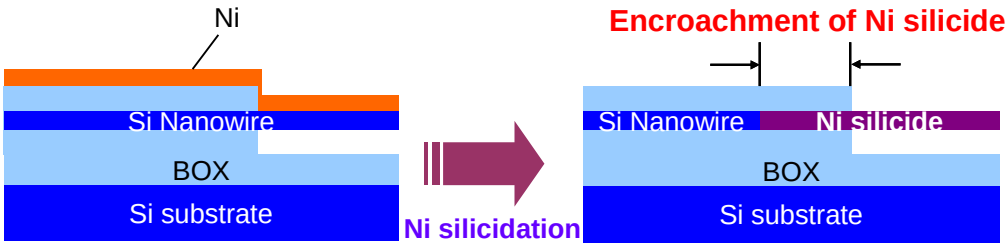


Figure 3.4 Schematic figures of encroachment of Ni Silicide Si Nanowire.

Figure 3.5 shows SEM and TEM images of Ni silicide contact for Si Nanowire. Si Nanowire with a diameter of 30 nm was covered with a SiO_2 of 50 nm. The Ni silicide Nanowire is formed from the edge of the Si Nanowire. A brighter contrast of the Nanowire near the oxide edge indicates the formation of Ni silicide in this region. The figure on the right hand side shows the plane TEM image of the formed Ni silicide in the Si Nanowire. A darker contrast in the Nanowire also indicates the encroachment of Ni silicide into the Si Nanowire. Here, we can see that there is no volume expansion due to the incorporation of Ni in the Si Nanowire. And also Ni silicide and Si nanowires are smoothly connected.

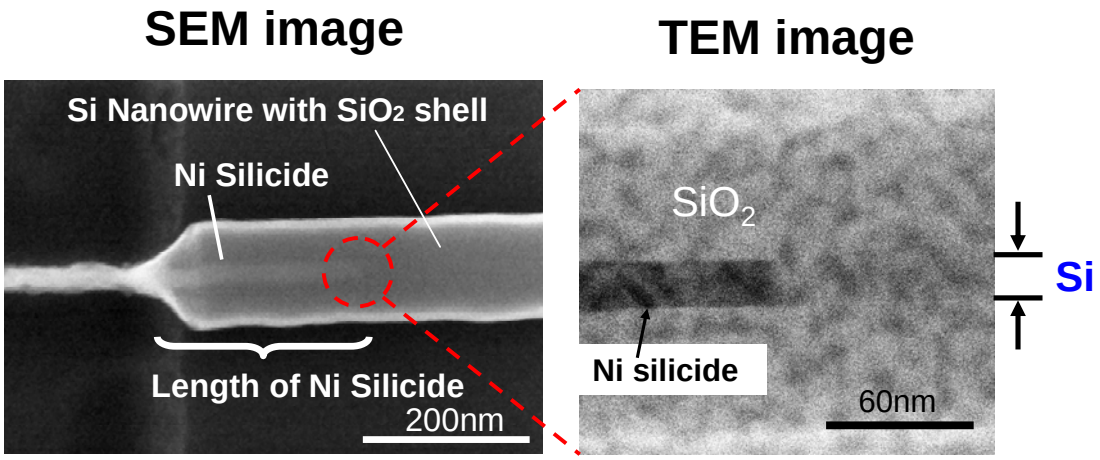


Figure 3.5 SEM and TEM images of Ni Silicide of Si Nanowire.

3.3.3 EDX Analyses of Ni Silicide Si Nanowire

The SEM photograph in Figure 3.6 (a) shows the typical shape of Ni silicide formed by the reaction between Ni layer and Si Nanowire. The Nanowire width W_{nw} was 23 nm in this case. It is observed that there is a bright portion (II) surrounded by SiO_2 adjacent to bright area (I), which was the former Si area exposed with buffered HF solution and reacted with Ni layer. Figure 3.6 (b) shows EDX spectra at four points (I) ~ (IV) indicated in SEM images. The EDX point measurement at point (I) indicates Ni existence. As in point (I), Ni existence was confirmed at point (II). No Ni peaks were detected at points (III) and (IV). We defined the encroachment length λ of Ni silicide as the length of portion (II) from the edge of exposed Nanowire.

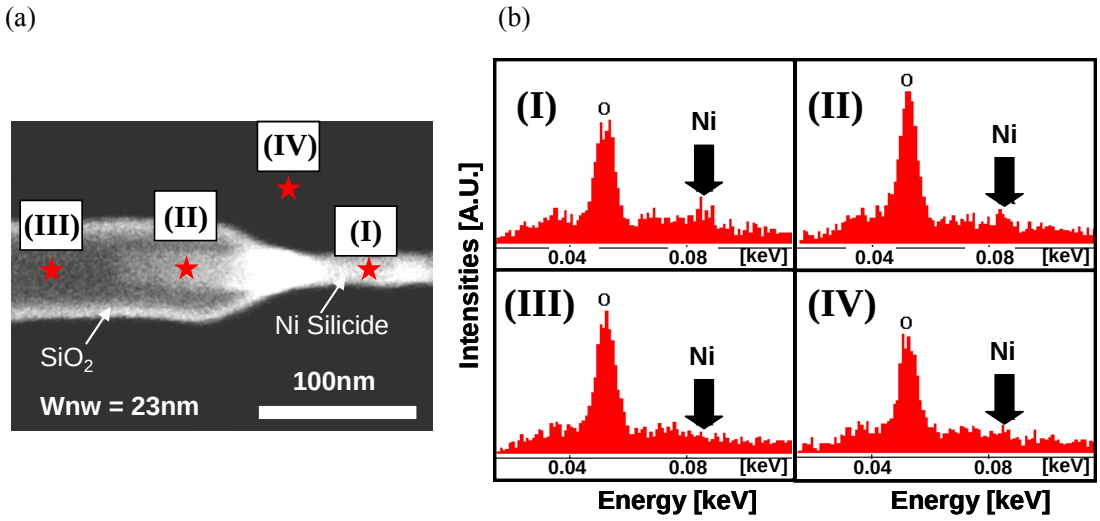


Figure 3.6 (a) Typical shapes of Ni silicide formed by the reaction between Ni layer and Si Nanowire. The Nanowire width W_{nw} was 23nm in this case. (b) EDX spectra at four points (I) ~ (IV) indicated in SEM images.

3.3.4 Auger Electron Spectroscopy (AES) Analyses of Ni Silicide Si Nanowire

The composition of the formed Ni silicide was analyzed by Auger electron microscope. The Si Nanowire width is around 23 nm. The annealing was done at 600 ^{o}C for 30 sec for this sample, which results in a 2.4 μm of Ni silicide encroachment. By separating the oxide and the un-oxidized spectra in Si, we obtained a Si and Ni ratio of 1 to 2 as shown in figure 3.7. Therefore, Ni_2Si is formed in the Si Nanowire. Also, this ratio seems to be constant within the formed Ni silicide. At a temperature of 600 ^{o}C, generally Ni-mono silicide is formed for the reaction of bulk Si and Ni. However, Ni-rich phase was formed for silicidation with Si Nanowire. This fact indicates the difference between bulk and Si Nanowire.

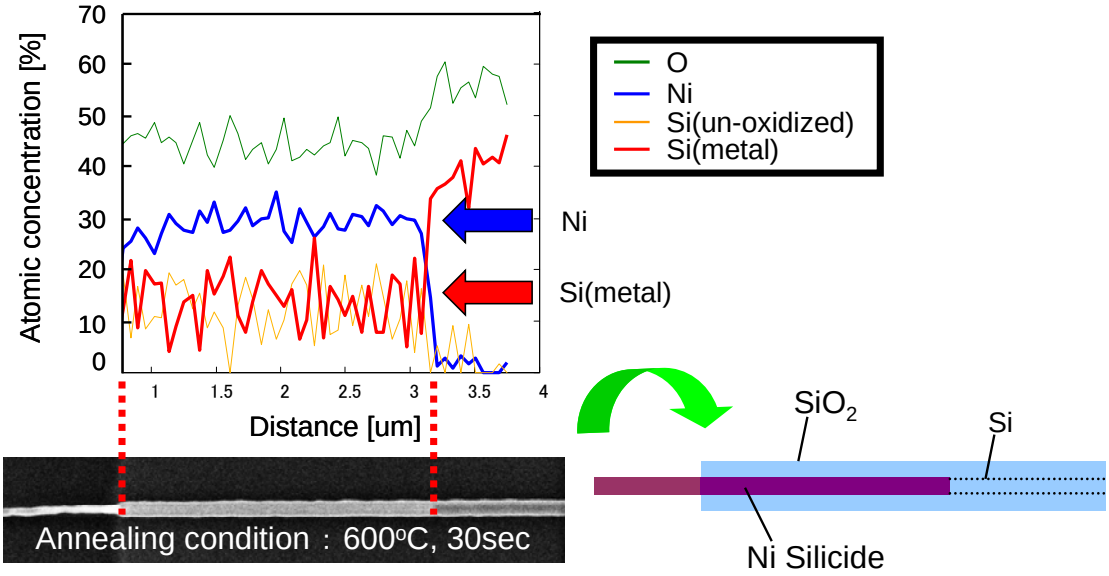


Figure 3.7 Auger Electron Spectroscopy (AES) Analyses of Ni Silicide Si Nanowire.

3.3.5 Annealing Time and Temperature Dependence of Ni Silicidation for Si Nanowire

Figure 3.8 shows the time dependence of the encroachment length λ of Ni silicide formed by RTA at 400 °C. Note that the length was plotted as a function of square-root of time in this figure. The linear relationship of these plots indicates that this encroachment phenomenon is governed by the diffusion law such as,

$$\lambda \propto A\sqrt{t} \qquad (1)$$

, where A is the slope of the plot. This figure also indicated that the increase in the reaction Nanowire width W_{nw} leads to the increase in the slope of the plot.

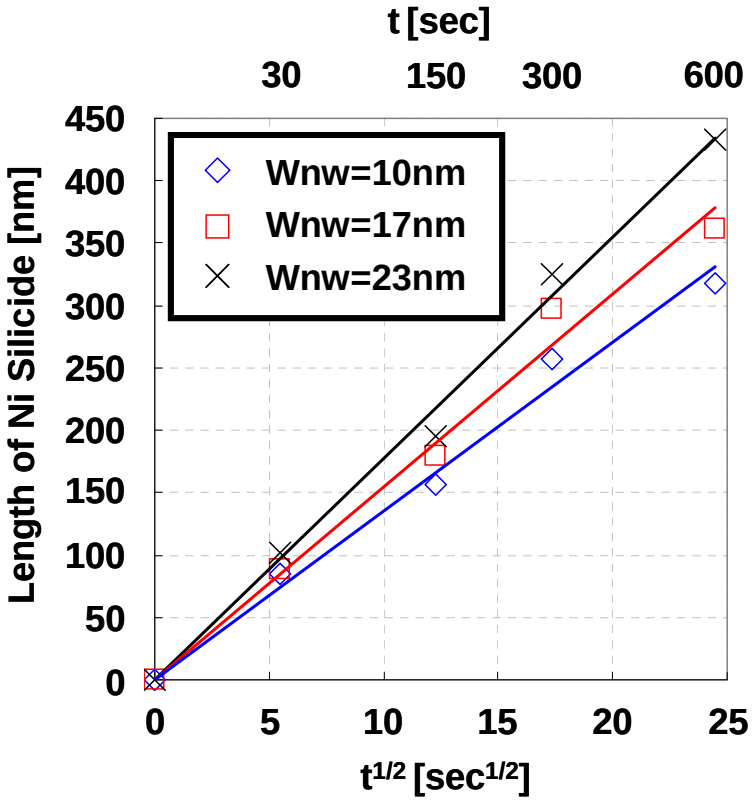


Figure 3.8 Time dependence of the encroachment length of Ni silicide λ. Silicides are formed at 400 ^{o}C using 30-nm-thick (100) SOI substrate.

Figure 3.9 shows the temperature dependence of the encroachment length of Ni silicide λ, taking the Nanowire width W_{nw} as the parameter. This figure indicates similar exponential dependence of encroachment length on temperature for all Nanowire width experimented. No clear facet was observed at the interface at Ni silicide and residual Si nanowire for both orientations [11].

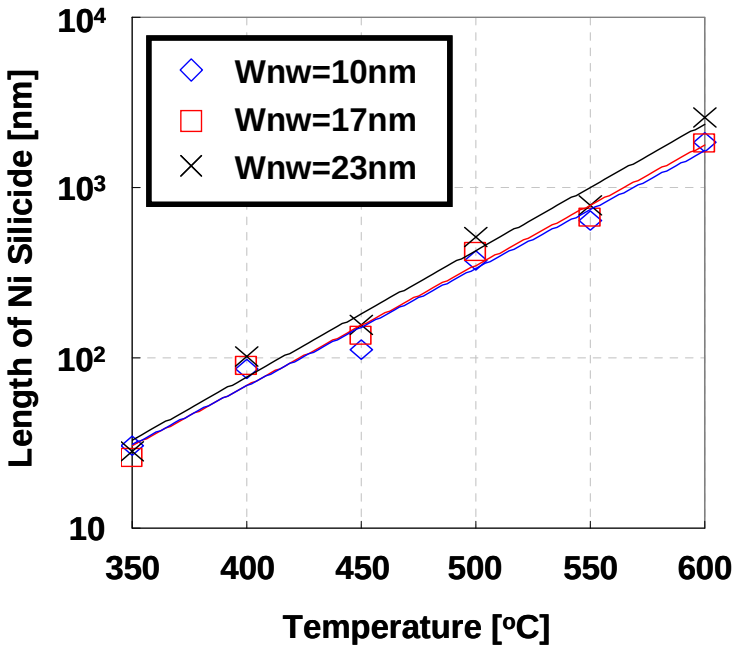


Figure 3.9 Temperature dependence of the encroachment length of Ni silicide λ for various Nanowire widths W_{nw}.

Figure 3.10 shows Arrhenius plots of 'A' in equation (1). The results in difference from Nanowire width W_{nw} using orientation <110> nanowires of 30-nm-thick (100) SOI substrate. Calculated activation energy (E_a) of W_{nw} = 10, 17 and 23 nm were 1.48 eV, 1.52 eV and 1.60 eV, respectively. The activation energy of NiSi and Ni_2Si were reported 1.4 eV and 1.5 eV in bulk Si, respectively. The activation energy obtained in Si nanowire is close to that with Ni_2Si (shown on Table 3.1). Therefore, it can be speculated that the formation of Ni silicide in the Si nanowire is Ni_2Si silicide.

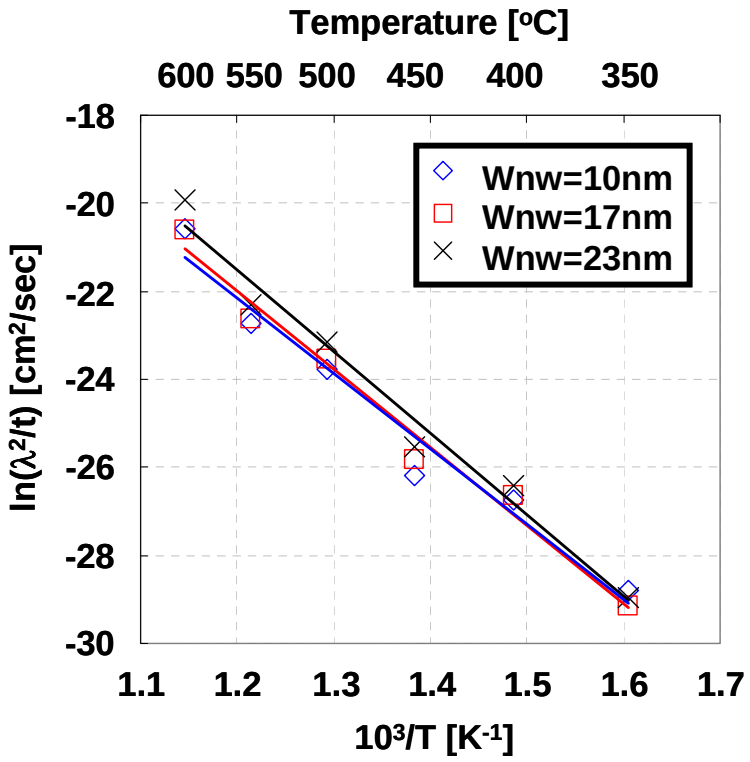


Figure 3.10 Arrhenius plots of nanowires when W_{nw} compared using 30-nm- thick (100) SOI substrate.

3.4 Conclusions of this section

This section indicates fundamental experiments analyses of Ni silicide in Si nanowire. Si nanowires were fabricated by lithography, dry etching and thermal oxidation. In this experiment, Si nanowire were formed by thermal oxidation of 30-nm-thick (100) SOI substrate at 1000 ^{o}C for 45 min in dry O_2 ambient, by changing diameters Si nanowires were varied from 10 nm to 30 nm. Oxide around Si nanowire was partially removed by buffered HF solution. In order to react Si nanowires with Ni film, 6-nm-thick Ni film was deposited on partially exposed Si nanowire by magnetron sputtering in an Ar ambient. Rapid Thermal Annealing (RTA) at various temperatures ranging from 350 ^{o}C to 600 ^{o}C was performed in forming gas (F.G) (N_2:H_2=97%:3%) ambient. Unreacted Ni film was removed by SPM (mixed H_2SO4 and H_2O_2) solution. And Ni silicide encroachment into Si nanowire was observed by SEM and the encroachment length was measured.

Ni silicide encroachment into Si nanowire was observed by SEM and TEM images. The junction of Si nanowire and Ni silicide encroachment are smoothly connected. Thanks to the oxide around Si Nanowire, no volume expansion was observed in Ni silicide encroachment.

The EDX point measurement indicated Ni existence in Ni silicide encroachment. AES analyses of Ni silicide encroachment indicated the formation of Ni silicide into Si nanowire is Ni_2Si from atomic concentration. In this case, diameter of Si nanowire is 23 nm and annealing condition is at 600 ^{o}C for 30sec.

AES analysis was performed for a sample of Ni silicide with 23nm of W_{nw}, which was annealed at 600 ^{o}C for 30 sec in silicidation processes. In this sample, atoms ratio of Ni to Si is 2 to 1. Therefore, it was concluded that Ni_2Si is formed on Si nanowire in

this condition.

RTA processes proceeding Ni silicide encroachment were performed at various annealing time ranging from 30 sec to 600 sec and temperature from 350 ^{o}C to 600 ^{o}C in order to investigate the mechanism of the phenomenon. Encroachment length of Ni silicide is proportional to the square-root of annealing time. This time dependence indicates this encroachment phenomenon is governed by the diffusion law. Arrhenius plots were obtained by temperature dependence. Calculated activation energies (E_a) of W_{nw} = 10, 17 and 23 nm were 1.48, 1.52, 1.60 eV, respectively. The activation energy obtained in Si nanowire is close to that with Ni_2Si. This result almost conforms to AES analysis. It is considered that Ni silicidation for Si nanowire is similar to that for thin film SOI.

References

[1] P. S. Lee, K. L. Pey, D. Mangelinck, J. Ding, D. Z. Chi and L. Chan. *IEEE Electron Device Lett*. **22** (2001) 568.

[2] K. N. Tu et al., *J. Appl. Phys.* **54** (1983), p. 758.

[3] T. Morimoto et al., *IEEE Trans. Electron Devices* **42** (1995) 915.

[4] K. N. Tu et al., *Thin Solid Films*, **25**, 403, (1975).

[5] Yuan Taur and Tak H Ning., *Fundamentals of MODERN VLSI DEVICES*. Cambridge University Press (1998), Chap 5.2.

[6] J. Seger et al., *Appl. Phys. Lett.* **86**, 253507 (2005).

[7] B. Imbert et al., Microelectron. Eng. In Press, Corrected Proof, Available online 14 June 2009.

[8] T. Yamaguchi et al., *Jpn. J. Appl. Phys.* **48** (2009) 066513.

[9] S. P. Murarka, *SILICIDES FOR VLSI APPLICATIONS.* Academic Press, New York, 1983, Chap.5.

[10] L. J. Chen, *Silicide Technology for Integrated Circuits.* The IEE, London, 2004. Chap. 5.

[11] N. Mise et al., *IEEE Trans. Electron Devices*, **55**, No. 5, p. 1244, MAY (2008).

CHAPTER 4

Suppression of The Encroachment Phenomenon in Ni Silicide Formation

4.1 Introduction

In order to apply the silicidation to source/drain region of Si nanowire FET, it is very important to suppress encroachment length of silicide. If the encroachment proceeds, effective gate length is reduced in uncontrollable. If the phenomena are excessive, channel region during source and drain would be short-circuited. For fabrication of Si nanowire FET of 20nm generation, suppression the length of Ni siliside of approximately 10 nm is necessary. It is considered that there are several solutions to suppress the encroachment length of Ni silicide formed in Si nanowire.

4.1.1 Two Step Annealing

It is considered that two step annealing process is one of the encroachment suppressing method for Ni silicide formation on Si nanowire. For years, two step annealing process has been studied for self-aligned silicide (Salicide) processes of narrow line gate electrode as well as source/drain electrode in order to control the silicide phase [1]. The narrow line width effect appears less than 100 nm using single step annealing in bulk MOSFET. An increase in sheet resistance is observed, which is shown Figure 4.1.1 [2].

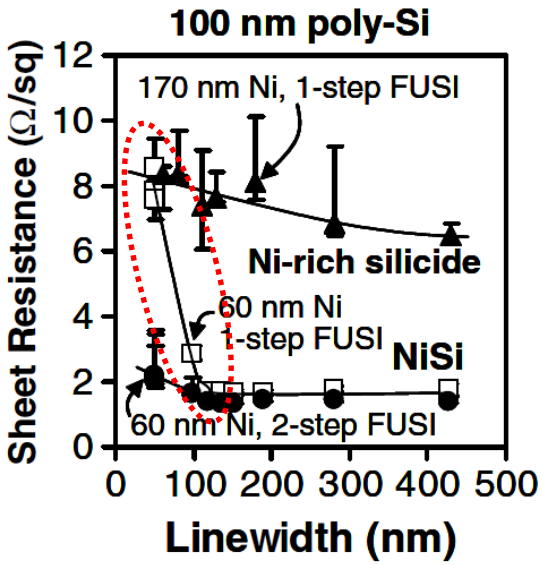


Figure 4.1.1 Line width dependences in sheet resistance.

Two step annealing process has four steps, which is different from single step annealing process. First, Ni films are deposited on Si substrate. Second, first annealing process is performed at lower temperature to formed Ni-rich silicide or incomplete silicide. Third, unreacted Ni is removed by SPM. Thanks to the Ni removal, two step annealing processes can control the amount of Ni diffusion atoms. Fourth, secondary annealing process is performed at high temperature to change the silicide to a phase with lower resistivity.

In Si nanowire, two step annealing processes are believed to be effective for suppression encroachment of silicide by control the diffusion of Ni atoms.

4.1.2 The Effect of N Incorporation in Ni for Silicidation

The effect of N atom incorporation into Ni film on the silicidation was previously evaluated [3]. If Ni films are deposited by sputtering in Ar and N_2 gas mixture ambient, the condition forms nitrogen (N) doped Ni film. N-doping in Ni films is effective to formation of $NiSi_2$ crystalline phase. Silicide processes using Ni and N-doped Ni films are shown in figure 4.1.2 with the comparison to the conventional Ni silicide formation. When N-doped Ni films are used, poly-crystalline and epitaxial $NiSi_2$ films is formed by annealing at 500°C. In general, the annealing temperature at 500°C forms NiSi phase and the annealing temperature higher than 800°C is required for $NiSi_2$ formation. As figure 4.1.2 (a) shows, NiSi films grown from Ni film without N-doping is promoted by the fast diffusion of Ni atoms via grain boundary. Figure 4.1.2 (b) shows epitaxial $NiSi_2$ grows through uniform lattice diffusion by the assistance nitrogen in Ni film. The growth rate is very slow and the technique, therefore it is considered to be useful for the suppression of the encroachment phenomenon at the source and drain silicidation in Si nanowire FET.

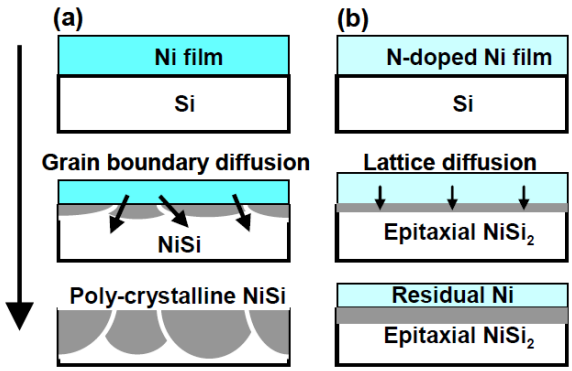


Figure 4.1.2 Models explaining the different growth behavior of NiSi and epitaxial $NiSi_2$ films [3].

4.2 Experimental

4.2.1 Two Step Annealing Process

For some samples, two step silicidation processes was performed. Schematic figures are depicted for the single step and the two step annealing processes in Figure 4.2.1. The first annealing of the two step process was performed at 300 ^{o}C for 30 sec, followed by the unreacted Ni removal by SPM solution and the second annealing at 400 ^{o}C for 30 sec. The annealing processes were performed in a F.G ambient.

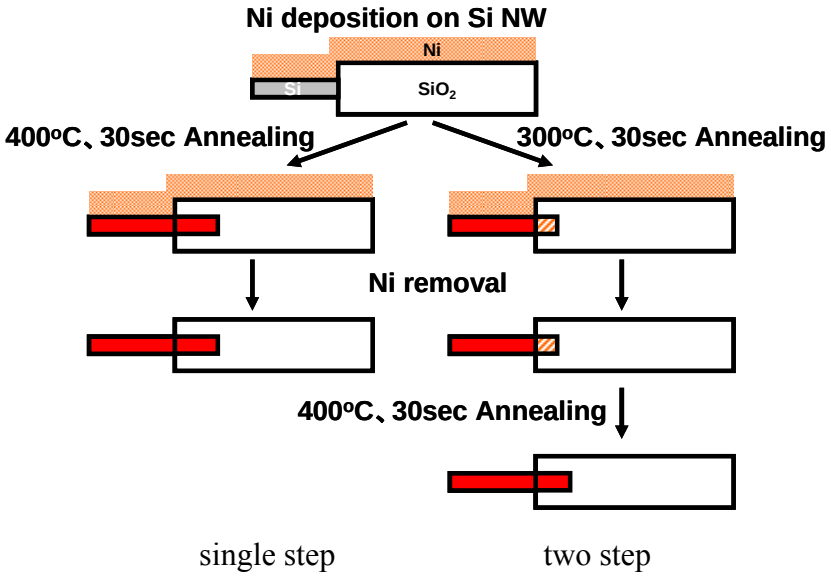


Figure 4.2.1 Schematic illustration of single step and two step annealing processes.

4.2.2 N Incorporation in Ni for Silicidation

Nitrogen incorporation in Ni is performed by sputtering of Ni film in Ar and N_2 gas mixture ambient. Nitrogen is doped in Ni by this process. Process flow is same as previously-shown by figure 3.2. In this experimental, Ni sputtering is performed by RF power of 150 W. The ratio of Ar to N_2 is 7 sccm to 7 sccm. Therefore, we obtain N-doped Ni film by sputtering in Ar and N_2 gas mixture.

4.3 Results and Discussion

4.3.1 Suppression of length of Ni silicide by two step annealing

Figures 4.3.1 show SEM images of Ni Silicide formed from Si nanowire. Figure 4.3.1 (a) is the result of single step annealing process in which Ni silicide formation was performed at 400 ^{o}C for 30 sec, while Figure 4.3.1 (b) is the result for the two step annealing process, in which the first annealing was performed at 300 ^{o}C for 30 sec, followed by the residual Ni removal and the second annealing at 400 ^{o}C for 30 sec. These two pictures indicate that the encroachment length λ of Ni silicide is dramatically reduced by two step annealing process, compared from that by the single step annealing process. This is thought that two step annealing process have advantageous in fabrication process of Si nanowire MOSFET.

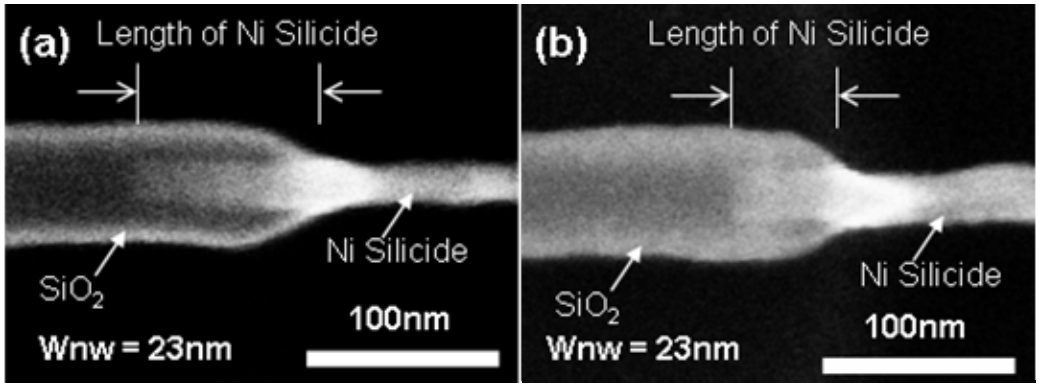


Figure 4.3.1 SEM images of Ni silicide formed by two different processes: (a) single step annealing process at 400 ^{o}C for 30 sec. (b) two step annealing process which consists of the first step annealing at 300 ^{o}C for 30 sec, followed by the residual Ni removal and the second step annealing at 400 ^{o}C for 30 sec.

Figure 4.3.2 shows the encroachment length of Ni silicide as a function of nanowire width. In this figure, results of single step annealing process and two step annealing process are compared. The error bar indicates the standard deviation of the encroachment length $1\sigma_{\lambda}$ by measurement samples of same twenty samples. This figure says that the encroachment length of Ni silicide on two step annealing process becomes shorter than that on single step annealing process for all nanowire width experimented. There exists a slight increase in the encroachment length for both silicidation processes when nanowire width increases.

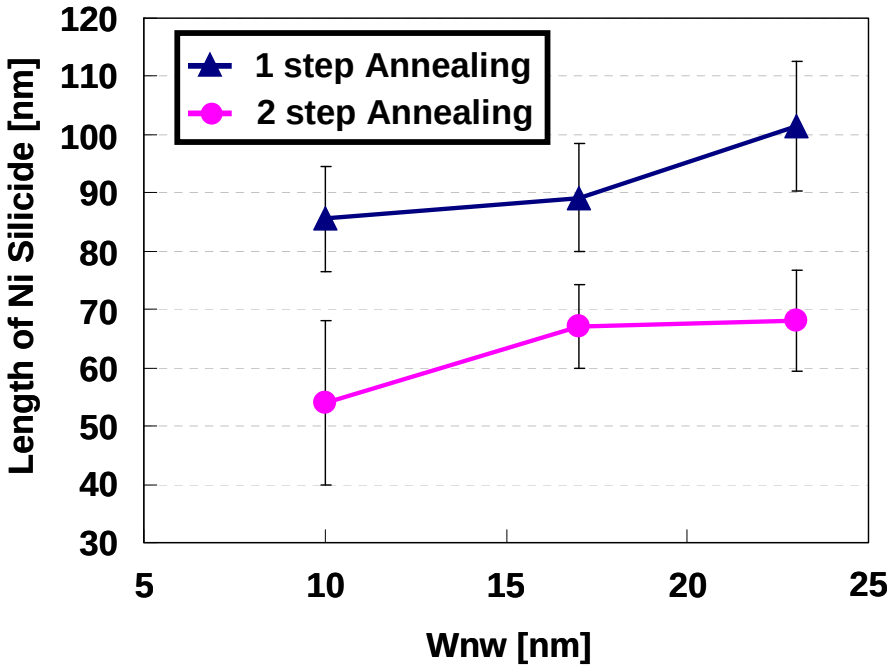


Figure 4.3.2 Encroachment length of Ni silicide on single step and two step processes.

Figures 4.3.3 show SEM images of Ni silicide (a) just after the first annealing process at 300 ^{o}C for 30 sec and residual Ni removal and (b) after the second annealing at 400 ^{o}C for 30 sec. Ni silicide encroachment was less than the detection limit of this observation just after the low temperature first annealing, but the encroachment took place at the second annealing. This may be due to the transformation from Ni rich silicide phase to Si rich silicide change during the second phase. These results show that, in order to alleviate the encroachment phenomena, amount of Ni atoms diffused into nanowire at high temperature annealing should be minimized.

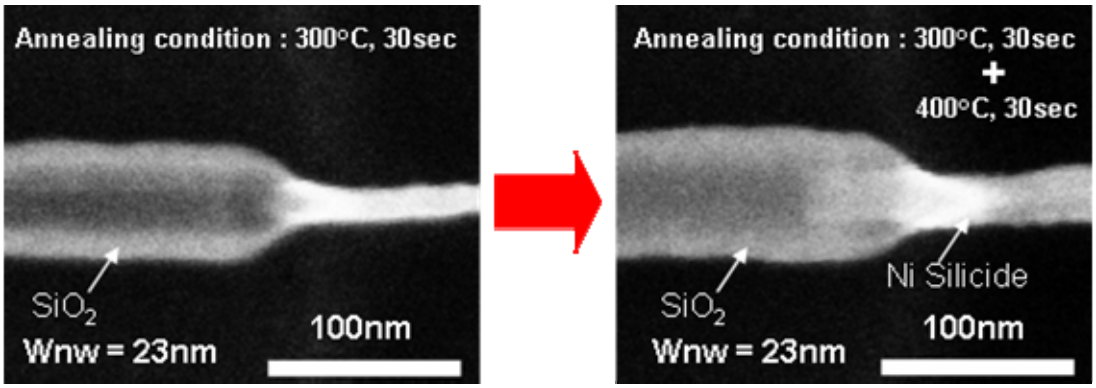


Figure 4.3.3 SEM images of Ni silicide (a) just after the first annealing process at 300 ^{o}C for 30 sec and residual Ni removal and (b) after the second annealing at 400 ^{o}C for 30 sec.

Figure 4.3.4 shows the annealing time dependence on the length of Ni silicide. For two step annealing process, only the second annealing time was changed. It should be mentioned that horizontal axis is $t^{1/2}$. With the use of the conventional single step annealing, the length of Ni silicide increases with annealing time as shown in the red line. The fact that experimented data fit to $L_{\lambda} = A\sqrt{t}$ line indicates that the diffusion

of the constituent species governs the phenomena for the conventional single step as well as early stage of two step annealing. However, with two step annealing process, the length of Ni silicide can be well suppressed as shown in the blue line. The reason can be considered as the difference in the supply of Ni atoms. With conventional process, there are plenty of metal Ni atoms at the surface compared to the volume of Si nanowire. So that Ni diffuses fast into Si nanowire. On the other hand, since the unreacted Ni was removed after the first annealing step, the diffusion of Ni is limited and this leads to the suppressed supply of Ni atoms.

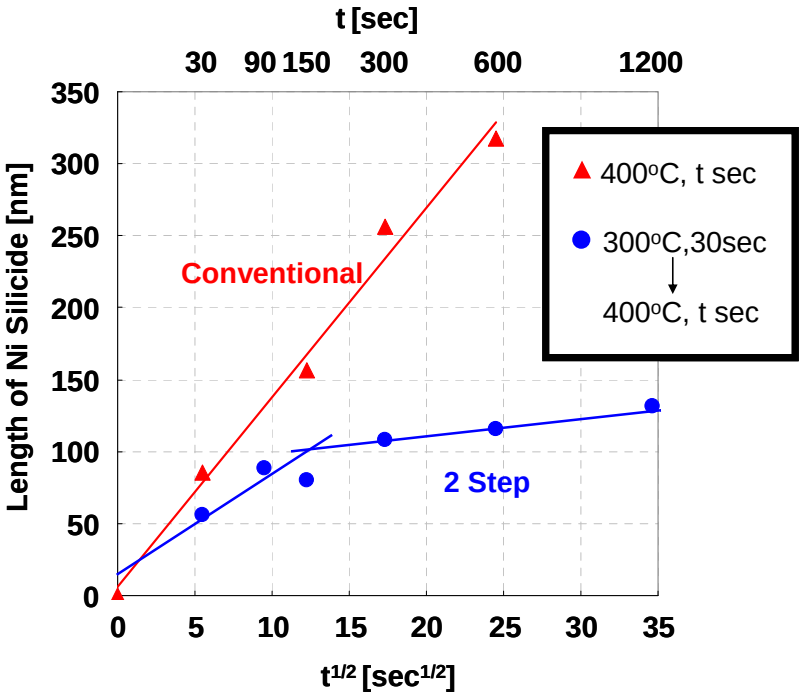


Figure 4.3.4 The annealing time dependences of two step annealing on the length of Ni silicide. The second annealing time was changed.

4.3.2 The Effect of N Incorporation in Ni for Silicidation

Figure 4.3.5 shows comparison of two different processes on Ni deposition with or without N_2 gas. The upper blue broken line indicates encroachment length of Ni silicide at 400°C, 30 sec annealing, formed from Ni deposited in Ar gas ambient. Another red broken line indicates encroachment length of Ni silicide at 400°C, 30sec annealing, formed from Ni deposited in Ar and N_2 mixture gas ambient. In case of Ni deposition with N_2 gas, the encroachment length of Ni silicide at same annealing conditions is reduced for all W_{nw} experimented. The suppression effect of Ni deposition with N_2 gas almost equals to two step annealing processes.

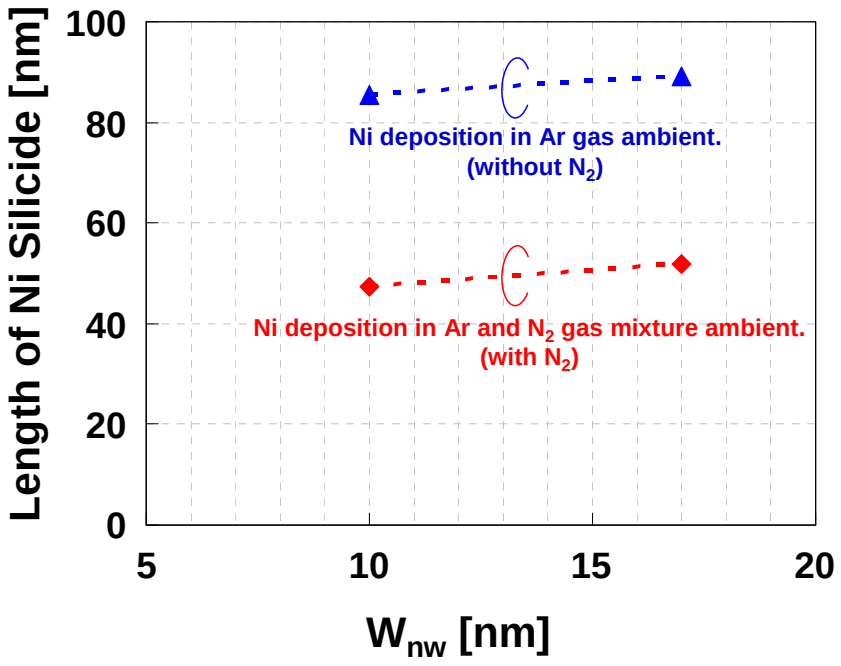


Figure 4.3.5 Encroachment length of Ni silicide on two different Ni deposition processes.

4.4 Conclusions of this section

This section indicates suppression methods of encroachment Ni silicide in Si nanowire.

We confirmed suppressing effect of the two step annealing process. The two step annealing process, in which the first annealing was performed at 300 ^{o}C for 30 sec, followed by the residual Ni removal and the second annealing at 400 ^{o}C for 30 sec. The two step annealing process suppresses the encroachment length of Ni silicide. In this annealing condition, the encroachment length of Ni silicide became shorter from 86 nm of single step annealing process to 54 nm of two step annealing process. Calculated length of encroachment Ni silicide after first step annealing of two step annealing process is 14 nm. At first step annealing of two step annealing process, it was considered Ni-rich silicide was formed by low annealing temperature. Thanks to the unreacted Ni removal after first step annealing, the diffusion of Ni atoms decreased. Therefore, the encroachment of Ni silicide in Si nanowire was suppressed by two step annealing process. It is considered that Ni atoms were supplied in Si nanowire covered with oxide from the Ni-rich silicide in Si nanowire after the first annealing.

Time dependence at second step annealing in two step annealing process indicates effect of two step annealing process. Since the unreacted Ni was removed after the first annealing step, the diffusion of Ni is limited and this leads to the suppressed supply of Ni atoms.

Ni deposition with or without N_2 gas were performed to suppress the encroachment length of Ni silicide. The ambient ratio of Ar to N_2 is 7 sccm to 7 sccm. It is considered the mixture ambient of Ar and N2 forms N-doped Ni and retard the silicide reaction at

RTA. The suppression effect of Ni deposition with N_2 gas almost equals to two step annealing process.

References

[1] J. A. Kittl et al., *Microelectron. Eng*. **70** (2003) 158.

[2] J. A. Kittl et al., *Microelectron. Eng*. **83** (2006) 2117.

[3] S. Migita et al., *Solid State Devices and Materials*, (2008) 686.

Chapter 5

Conclusions of This Study

5.1 Fabrication of Si nanowire

Si nanowires were fabricated by lithography, dry etching and thermal oxidation. In this experiment, Si Nanowire formed by thermal oxidation of 30-nm-thick (100) SOI substrate at 1000 ^{o}C for 45 min in dry O_2 ambient. Around from 10 nm to 30 nm of diameters Si nanowires were formed by thermal oxidation.

5.2 Ni silicidation in Si nanowire by single step annealing processes

Ni silicide encroachment into Si nanowire was observed by SEM and TEM images. The junction of Si nanowire and Ni silicide encroachment are smoothly connected. Thanks to the oxide around Si Nanowire, no volume expansion was observed in Ni silicide encroachment.

AES analysis was performed for a sample of Ni silicide with 23 nm of W_{nw}, which was annealed at 600 ^{o}C for 30 sec in silicidation processes. In this sample, atoms ratio of Ni to Si is 2 to 1. Therefore, Ni_2Si is formed on Si nanowire in this condition.

RTA processes proceeding Ni silicide encroachment were performed at various annealing time and temperature ranging from 30 sec to 600 sec and from 350 ^{o}C to 600 ^{o}C. Encroachment length of Ni silicide is proportional to the square-root of annealing time. This time dependence indicates this encroachment phenomenon is governed by the diffusion law. Arrhenius plots were obtained by temperature dependence. Calculated activation energies (E_a) of W_{nw} = 10, 17 and 23 nm were 1.48, 1.52, 1.60 eV,

respectively. The activation energy obtained in Si nanowire is close to that with Ni_2Si formation on bulk silicon. This result almost conforms to AES analysis. It is considered that Ni silicidation for Si nanowire is similar to that for thin film SOI. These results are first report about details of Ni silicide encroachment in thin Si nanowire.

5.3 Suppression methods of encroachment Ni silicide in Si nanowire

The encroachment phenomenon is problematic in Si nanowire MOSFETs in term of a few aspects. In this study, there are two solution of suppressing encroachment length of Ni silicide in Si nanowire. The first solution is two step annealing process, and second one is N-doped Ni deposition.

The two step annealing process, in which the first annealing was performed at 300 ^oC for 30 sec, followed by the residual Ni removal and the second annealing at 400 ^oC for 30 sec. The two step annealing process suppresses the encroachment length of Ni silicide. In this case, the encroachment length of Ni silicide became shorter from 86 nm of single step annealing processes to 54 nm of two step annealing process.

At first step annealing of two step annealing process, it was considered Ni-rich silicide was formed by low annealing temperature. Thanks to the unreacted Ni removal after first step annealing, the diffusion of Ni atoms during high temperature the second annealing considerably decrease. Therefore, encroachment Ni silicide in Si nanowire was suppressed by two step annealing processes. Smaller encroachment occurs even for the two process. It is considered that Ni atoms were supplied in Si nanowire covered with oxide from the Ni-rich silicide in Si nanowire after the first annealing.

Also, Ni deposition with or without N_2 gas were performed to suppress the encroachment length of Ni silicide. The ambient ratio of Ar to N_2 is 7 sccm to 7 sccm. It

is considered the mixture ambient of Ar and N2 forms N-doped Ni and retard the silicide reaction of RTA. The suppression effect of Ni deposition with N_2 gas almost equals to two step annealing process. These processes are useful for fabrication of Si nanowire FET.

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