Fabrication of SB-MOSFETs on SOI Substrate Using Ni Silicide Containing Er Interlayer

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SB-MOSFETs were fabricated on SOI substrates by applying novel Schottky barrier height modulation technique of Er interlayer insertion at the interface of Ni/Si prior to Ni silicidation process. It was found that Er interlayer insertion lowered Schottky barrier height for electrons while no significant increase of the resistivity in the Er interlayer inserted films compare to pure Ni silicide films in the annealing temperature range of 500-750 ^{o}C. Effects of Er insertion to the transistor characteristics of SOI SB-MOSFETs are also discussed.

Introduction

Schottky barrier source/drain MOSFET (SB-MOSFET) is one of the promising candidates for next generation highly miniaturized CMOS devices, thanks to its shallow junction depth with lower sheet resistance and lower process temperature [1-2]. However, high schottky barrier height (Φ_b) decreases the drive current of SB-MOSFETs [3-4]. Er silicide has been proposed for n-channel SB-MOSFETs (SB-nMOSFETs) because of very low Φ_b of 0.27-0.36 eV for electrons [5]. However, mid-gap materials such as NiSi are also promising for the SB-MOSFETs by employing the Φ_b modulation techniques [3]. In previous works, Φ_b of Ni silicide was modulated by inserting an Er interlayer at the Ni/Si interface before silicidation. [6] In this work, we applied this technique to SB-nMOSFETs fabrication on SOI and discussed Er insertion effect.

Experimental

Figure 1 shows fabrication process of the sample for measuring sheet resistance of the (NiEr)Si layer. The SOI wafers with 100-nm-thick p-type SOI layer were used as substrates. The wafers were cleaned in a mixed solution of H_2SO_4 and H_2O_2 followed by a chemical oxide removal by diluted HF. 55-nm-thick or 200-nm−thick Ni film was deposited onto the substrates. And Er interlayer with various thickness was inserted at interface between the 55-nm-thick Ni and Si . Silicidation was performed in N_2 at various temperatures for 1 minute. The un-reacted metal was removed by SPM. Finally, sheet resistance of samples were measured by the four terminals method.

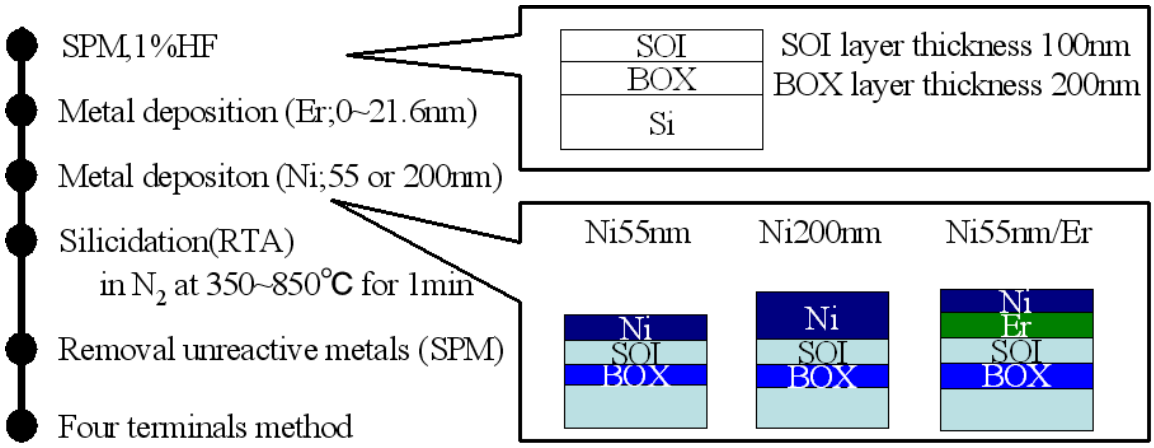

Figure 1. Fabrication process of samples for measuring sheet resistance.

Figure 2 shows fabrication process of Schottky diode. The diode was formed on SiO_2 isolated p-type bulk (100) Si wafers. Er and Ni films were deposited subsequently on the substrates by sputtering. The layered structures of Ni/Er/Si consisting of 55-nm-thick Ni layer and Er layer of 0~21.6-nm-thick were formed. The samples were then annealed in N_2 at temperatures of 500~750°C for 1 min. The un-reacted metal was removed by SPM. The backside Al-contact was finally formed. The Schottky barrier heights of the fabricated diodes were evaluated from current voltage (*I-V*) characteristics.

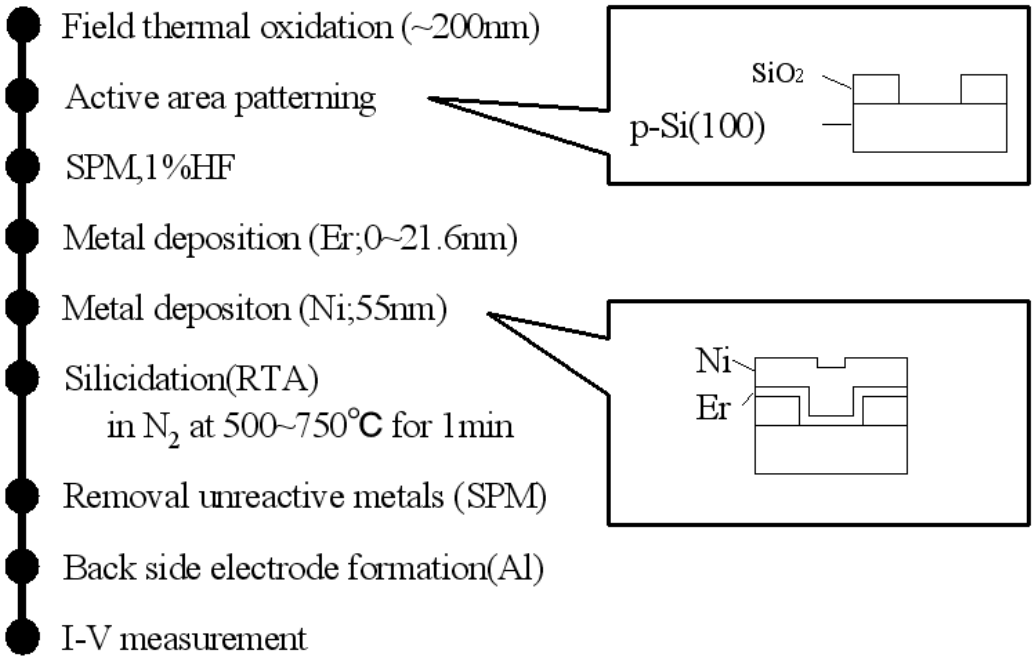

Figure 2. Fabrication process of Schottky diode.

Figure 3 shows fabrication process of SOI SB-nMOSFET. The MOSFET was formed on the SOI wafers with a 100-nm-thick p-type SOI layer and a 200-nm-thick BOX layer. The SOI layer was patterned by dry etching a and SiO_2 layer was formed on the SOI layer by sputtering. After removing the SiO2 layer on the source/drain region, 55-nm−thick Ni films with and without 7.2-nm-thick Er interlayer were deposited. Silicidation was performed in N_2 at 600°C for 1 minute. The un-reacted metal was removed by SPM. The backside Al gate electrode was finally formed.

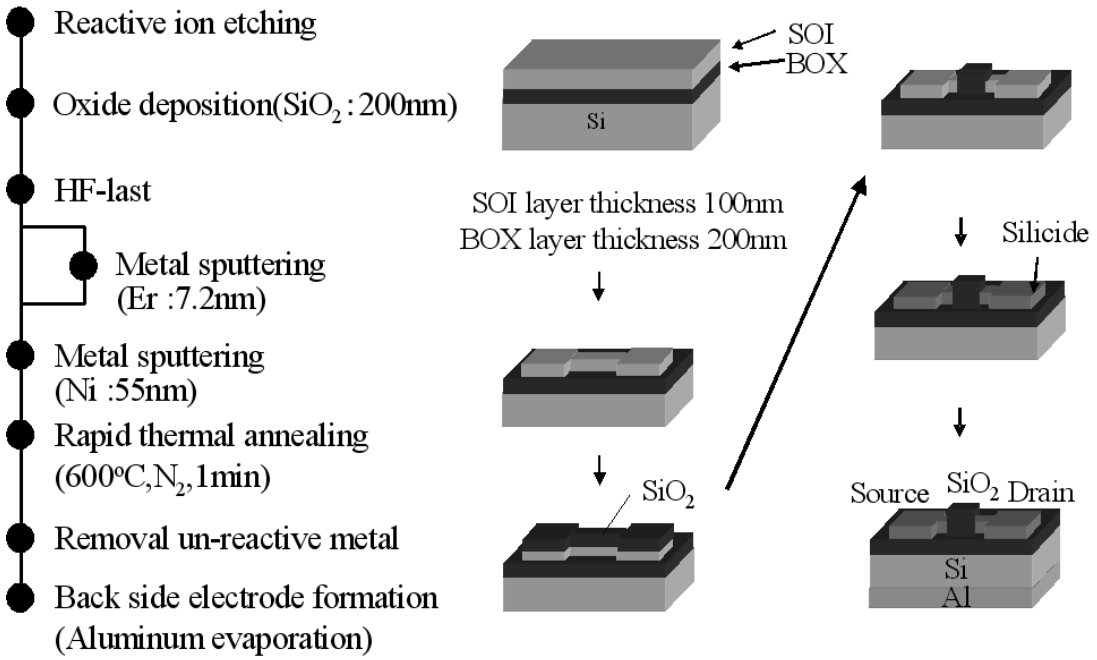

Figure.3 Fabrication process of SOI SB-nMOSFET.

Results and Discussion

First, we measured sheet resistance of two samples described in Fig. 1. In these two sampels Ni layer having the thickness of 55nm and 200nm was deposited on the SOI substrate, respectively. Figure 4 shows resistivity of the NiSi layer evaluated from sheet resistance measured. The same resistivity was obtained for both the Ni thickness of 55nm and 200nm. According to the reference, resistivity of NiSi, as indicated by a red line, is 14 $\mu\Omega \cdot$cm. [7]. At the annealing temperatures in the range from 450 to 850 °C, the resistivity obtained for two samples were close to that obtained for NiSi, indicating the formation of NiSi by silicidation at the temperatures of 450-850 °C.

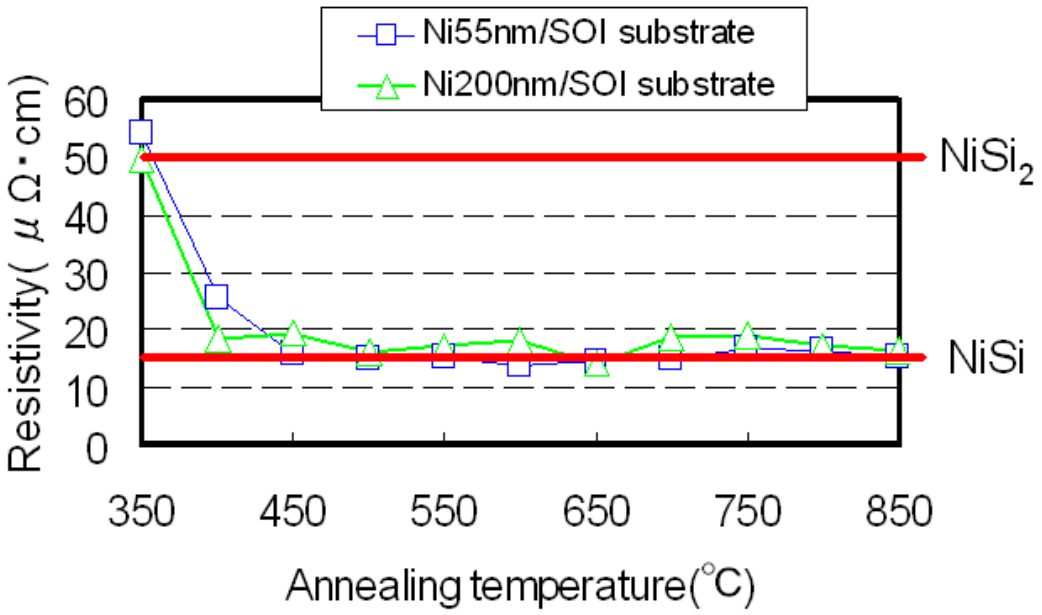

Figure 4. Resistivity of Ni-Si films on insulator as a function of annealing temperature.

Figure 5 shows the resistivity of the sample with an Er interlayer with various thickness at the Ni/Si interface. The resistivity was slightly increased by inserting the Er interlayer. The resistivities of samples which inserted Er interlayer than annealing temperature 750°C significantly increased that indicates poor thermal stability. In particular when the Er thickness increased, the degradation became pronounced. Figure 5 also show that the annealing temperatures lower than 500°C were not enough to form NiSi in the samples inserted with Er interlayer. So in this structures, the optimum range of annealing temperature was 500-750 °C.

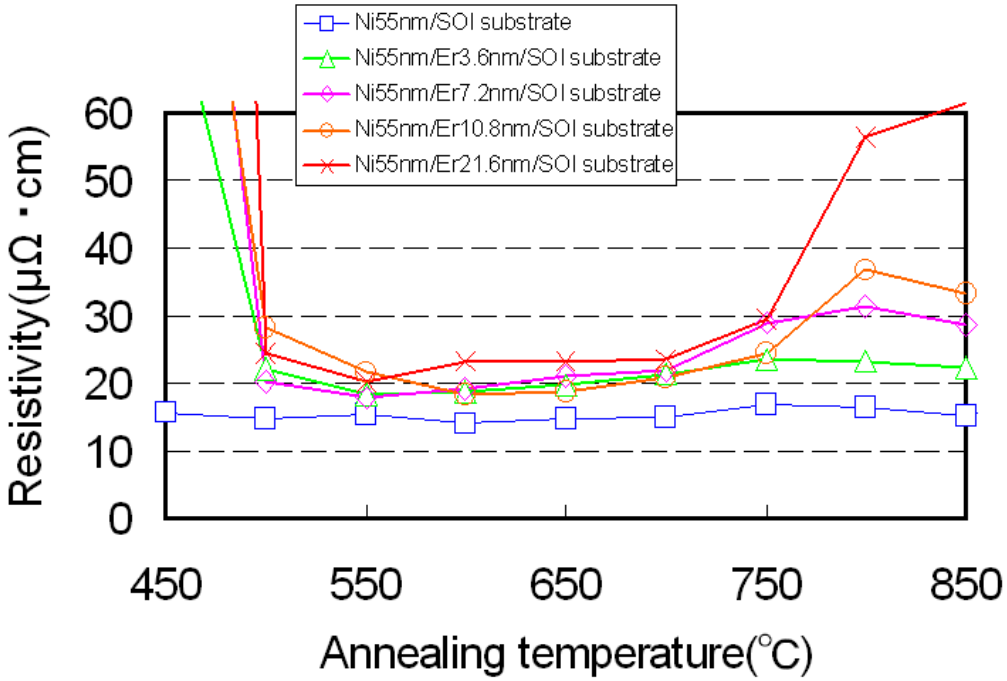

Figure 5. Resistivity of Ni silicide formed on SOI structures with or without Er versus annealing temperature.

Next, we characterized the Schottky barrier diodes as described in Fig. 2. Figure 6 shows Schottky barrier height (Φ_b) for holes on the bulk p-Si substrate. The Φ_b for holes increased by inserting Er. This means that the Φ_b for electrons was lowered by the insertion of Er interlayer. The largest increase by 0.146eV in Φ_b for holes was observed for sample inserted with 21.6-nm-thick Er interlayer at 750°C. The modulation of Φ_b by 0.06eV was observed for sample inserted with 7.2-nm-thick Er interlayer at 600 °C compared with that of the samples without Er interlayer. In contrast, the sample inserted with 21.6-nm-thick Er was modulated only 0.01eV comparing to with 7.2-nm-thick Er. Therefore, the optimum thickness of Er interlayer might be around 7.2nm if the thermal stability of the Ni silicide films is also considered.

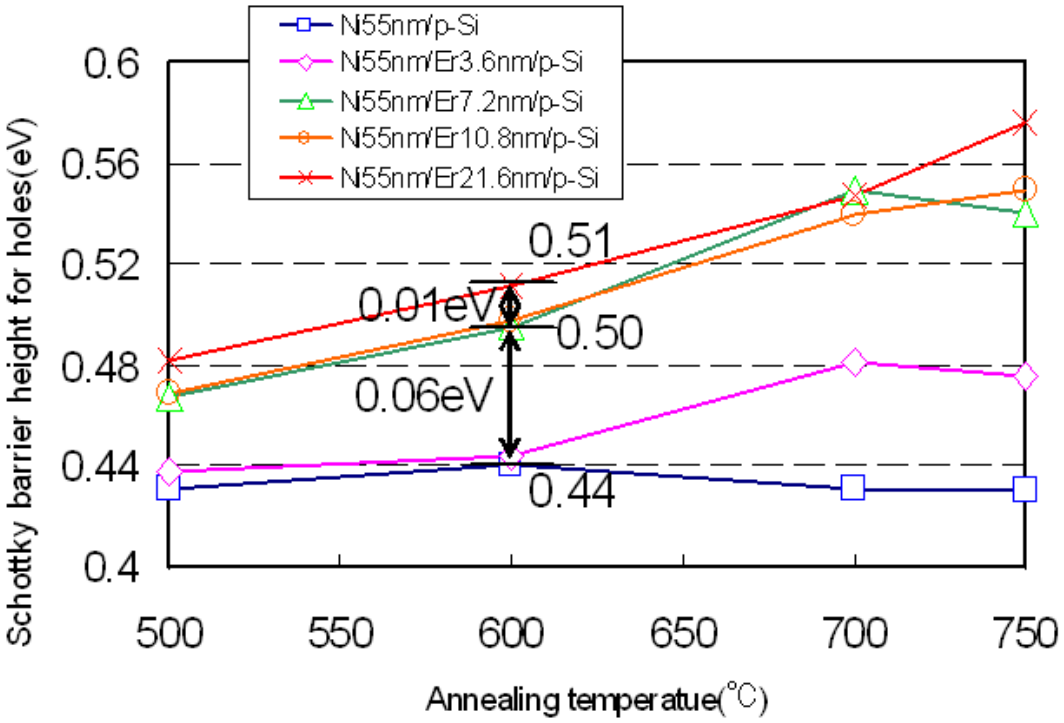

Figure 6. Schottky barrier height of Ni/p-Si and Ni/Er/p-Si versus annealing temperature range 500-750 °C.

Finally, we fabricated the SB-nMOSFETs on SOI using Er contained Ni silicide. 7.2-nm-thick Er interlayer was inserted at the Ni/SOI interface and the silicidation was carried out at the annealing temperatures of 600 °C. Figure 7 shows I_d-V_d characteristics of SOI SB-nMOSFET formed by inserting Er interlayer. We confirmed FET operation of the SOI SB-nMOSFETs. Figure 8 shows I_d-V_g characteristics of SOI SB-nMOSFET. Drain current in the device significantly increased compared with the reference device of pure Ni silicide S/D SB-nMOSFET without Er interlayer. This can be understood as the effect of Er interlayer on the lowering of Φ_b for electron.

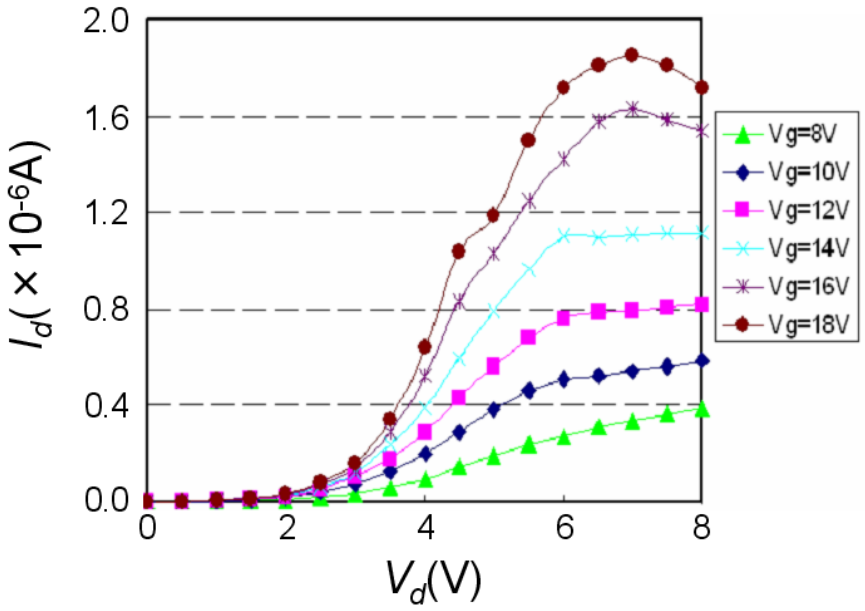

Figure 7. I_d-V_d characteristics of SOI SB-nMOSFET.

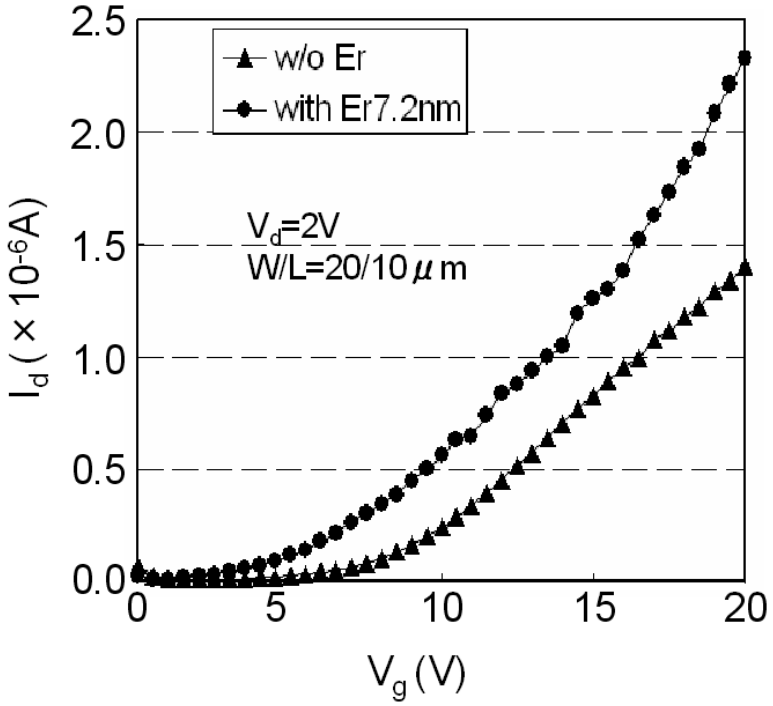

Figure 8. I_d-V_g characteristics of SOI SB-nMOSFET.

Conclusion

We fabricated SB-MOSFETs on SOI substrate by applying novel Schottky barrier height modulation technique of inserting Er interlayer at the Ni/Si interface prior to Ni silicidation. It was found that insertion of Er interlayer lowered Schottky barrier height for electrons while no significant increase in the resistivity was observed compared with pure Ni silicide films by the annealing at temperature in the range from 500 to 750 ^{o}C. We confirmed significant increase in drain current for the SOI SB-nMOSFETs with Er interlayer compared with the SOI SB-nMOSFETs without Er interlayer. Our results show that the Er interlayer insertion technique is one of the promising method for improving electrical characteristics of SB-MOSFETs.

Acknowledgments

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