Electrical Characterization of W/HfO_2 MOSFETs with La_2O_3 Incorporation

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Electrical characterization of HfO_2 MOSFETs with La_2O_3 in corporation has been conducted. A shift in threshold voltage to negative direction had been observed with La_2O_3 incorporation. Moreover, g_m and subthreshold slope have been improved with La_2O_3. 1/f noise measurement has revealed that HfO_2 gated MOSFET with incorporating La_2O_3 layer reduces the noise level .

Introduction

Hf-based-oxides have been used to replace SiO_2 gate insulator for advanced CMOS technologies. Recently, La_2O_3, one of rare earth oxides, has attracted much attention as it has wide bandgap of 5.5ev and high dielectric constant of 24 with fairly nice interface property**.** Also, La_2O_3 has been used to control the threshold voltage to negative direction **[1]**

In this paper, we investigated the effect of La_2O_3 incorporation underneath HfO_2 layer on electrical properties of MOSFETs .

Device fabrication and characterization

HfO_2 gated N-channel MOSFET (W/L=50μm/2.5μm) with La_2O_3 incorporation was fabricated on a p-Si (100) with LOCOS isolation. The source and drain were pre-formed prior to the high-k deposition. No interfacial layer was intentionally formed before high-k deposition. 2-nm-thickness of HfO_2 and La_2O_3 with thickness of 4nm were deposited by e-beam evaporation in an ultra high vacuum chamber. Tungsten metal electrode was deposited on top of the high-ks by sputtering. The device structure is shown in fig 1(a). Annealing temperature was performed in forming gas ambient at 500 ^oC for 30 min.

In the same way, a MOSFET with 4-nm-thick-HfO_2 was fabricated as a reference. The equivalent oxide thickness of the MOSFET were 1.6 nm.

The process flow is summarized in fig 1(b) The electrical characteristics of the fabricated high-k gated MOSFETs were measured using Agilent4156C semiconductor parameter analyzer. 1/f noise measurements[2]. were carried out with a Agilent HP89410A vector signal analyzer.

(a) (b)

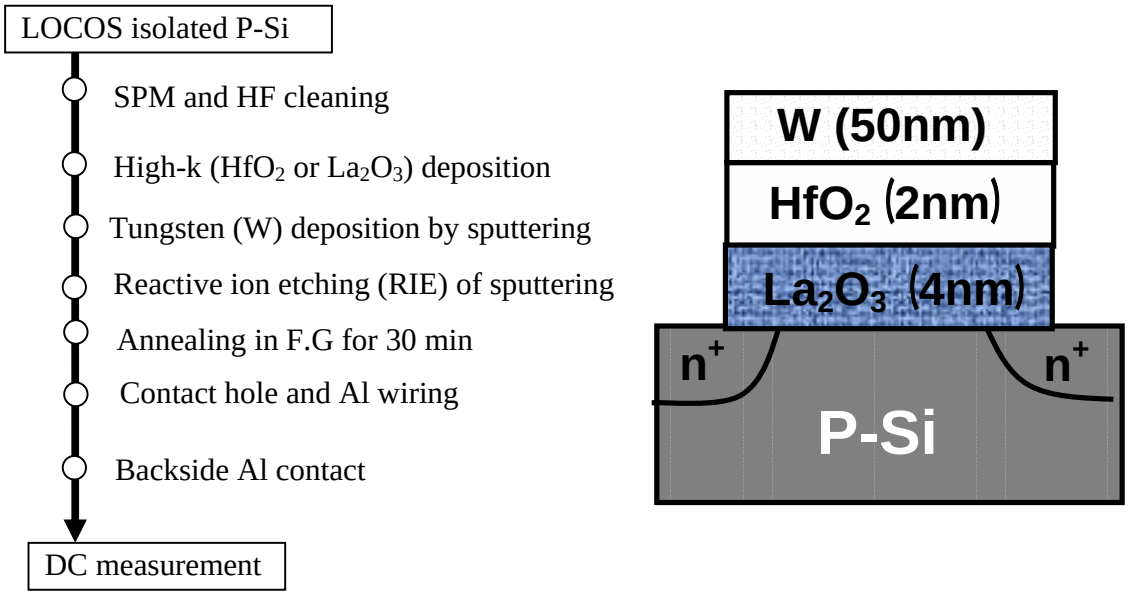
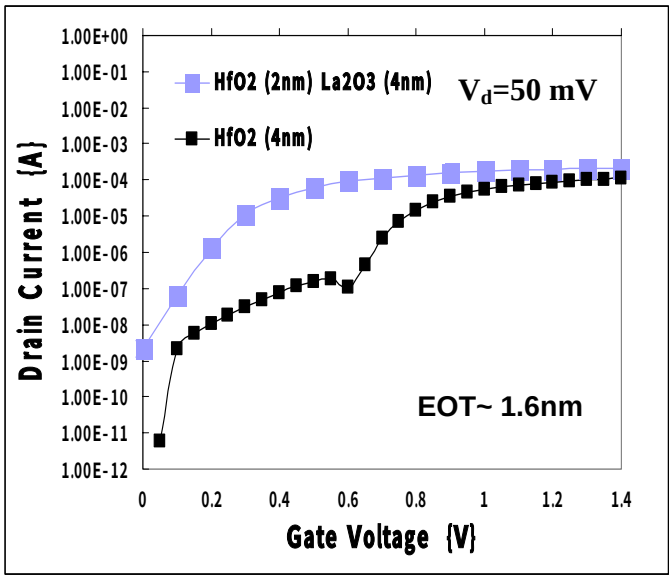


Figure 1. (a) Fabrication process flow of high-k gated n-MOSFET (b) Structure of fabricated MOSFET

Result and Discussion

I_d-V_g of the fabricated MOSFETs are shown in fig 2. The threshold voltage was shifted to negative direction by 0.45V with La_2O_3 incorporation.

(a) (b)



	Vth (V)	SS (mV/dec.)
HfO_2 (4nm)	0.68	94.6
Hf (2nm) La (4nm)	0.23	71.8

Figure 2. (a) I_d-V_g characteristics (b) parameter of these MOSFETs

Subthreshold swing (SS) of 94.6 mV/dec was improved to 71.8 mV/dec. with the incorporation of La_2O_3 presumably owing to better interfacial property.

The effective electron mobility (μ_{eff}) of the fabricated MOSFET is evaluated by split CV method [3].Figure 4 shows the calculated μ_{eff} also with HfO_2 and La_2O_3 MOSFETs that have the same EOT of 1.6 nm. The peak mobility was improved from 150 to 200 cm^2/Vs by incorporating La_2O_3 underneath HfO_2 layer.

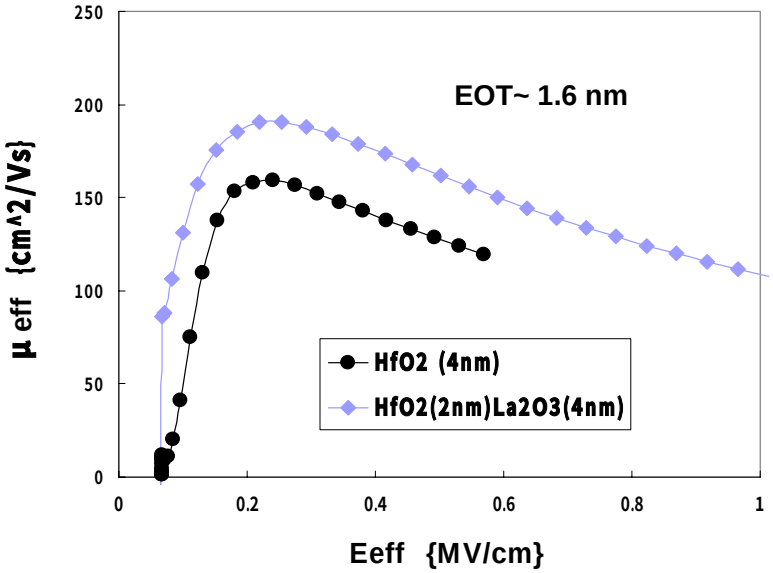


Figure 4. Effective electron mobility of La_2O_3 incorporated HfO_2 MOSFET. Samples are same EOT of 1.6 nm.

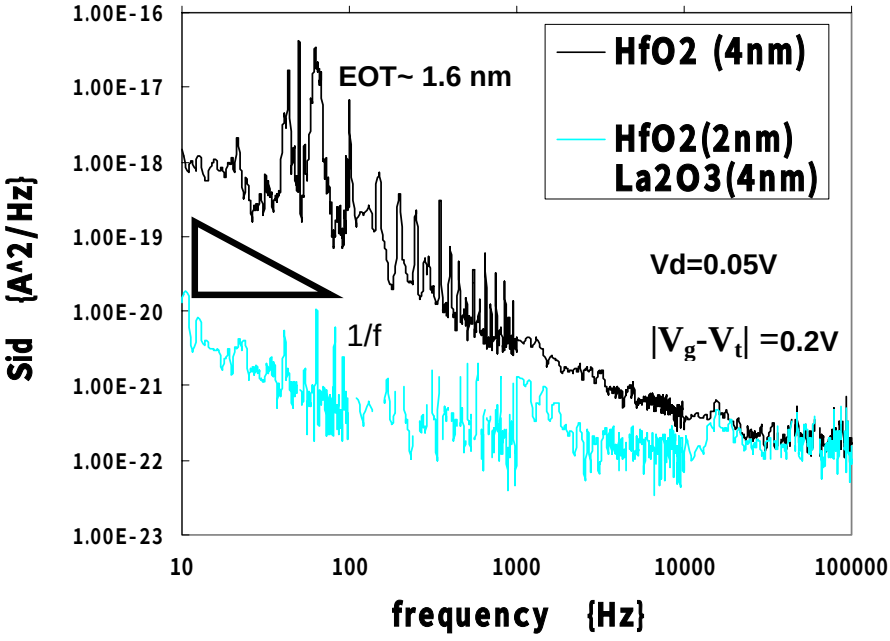


Figure.5 Drain Current Noise vs frequency at V_d=0.05V and $|V_g-V_t|$=0.2V

Figure 5. shows the drain current noise (S_{id}) characteristics of the devices at V_d=0.05V and $|V_g-V_t|$=0.2V for n-MOSFETs with W/HfO_2(4nm) /Si and W/La_2O_3(4nm) HfO_2(2nm)/Si In this figure, Sid of the MOSFET incorporated 4nm thickness of La_2O_3 was found to be lower than W/HfO_2(4nm) /Si. Noise level found to be reduced by incorporating La_2O_3 underneath HfO_2 layer.

Conclusions

By incorporating La_2O_3 under HfO_2 layer, a shift in threshold voltage to negative direction was observed. Moreover, the characterization of MOSFET was improved and the peak mobility was improved from 150 to 200 cm^2/Vs. HfO_2 gated MOSFET with incorporating La_2O_3 layer showed lower 1/f noise characteristics.

References

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