

I-V Characteristics of SOI MOSFETs in Ballistic Mode

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Abstract

$I - V$ characteristics of ultra-thin SOI MOSFETs operating in ballistic transport mode is given. It is derived with the similar guiding principle as is used in quantum point contact. The obtained result is independent of channel length, and is expressed with elementary parameters without depending on ambiguous carrier mobility. It shows triode and pentode operational modes as is the normal MOSFET. Saturation current, when carriers are degenerate, is independent of temperature and is proportional to carrier density to the 1.5-th power.

1 Introduction

Recently, ultrasmall size MOSFETs of less than $0.1 \mu\text{m}$ have been extensively investigated[1],[2] with regards to device size limitation or velocity overshoot in MOSFETs. This paper reports the zero-th order evaluation of SOI MOSFETs $I - V$ characteristics in ballistic mode. Ultrasmall MOSFETs in bulk Si is usually requested by scaling law to have high dose substrate, which necessarily leads to the electron mobility degradation as well as junction leakage increase. SOI MOSFETs are regarded as a promising candidate of ultrasmall device because it can provide an intrinsic (non-doped) channel free of impurity scattering. Phonon scattering is dominant if operated at room temperature. But ultrasmall MOSFETs may inevitably be operated at low temperatures if the improvement of subthreshold characteristics is necessary. Large portion of carrier scattering may be well suppressed in these intrinsic channel devices at low temperatures. A detailed Monte Carlo simulation of ultrasmall SOI MOSFETs[3] also suggests the possibility of ballistic transport. With these points in view, we have discussed the ballistic operation of intrinsic channel SOI MOSFETs at low temperatures.

2 Analysis

Fig.1 shows the assumed device structure, a very thin SOI film MOSFET, where the channel region is of intrinsic Si.

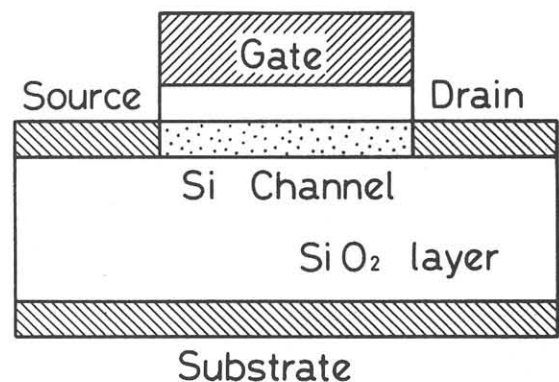


Fig.1 Thin film SOI MOSFET structure.

The potential energy distribution along the channel, assigned at the conduction band energy minimum, is schematically shown in Fig.2. It usually has a maximum point near source edge. The source region has degenerate carriers and feeds them to channel. If the source and the drain region are ideal reservoirs, the fed carriers are in thermal equilibrium. All carriers that pass this maximum point reach drain without being scattered back if the wave reflection at the drain edge is neglected. The drain current is decided by the number of carriers that rush through the maximum point per unit time, irrespective to the carrier velocity distribution in the channel past this point. The cross section of channel region at the potential maximum is schematically shown in Fig.3, where y and z show the channel width and the channel depth direction, respectively. Electronic state at this point consist of a num-

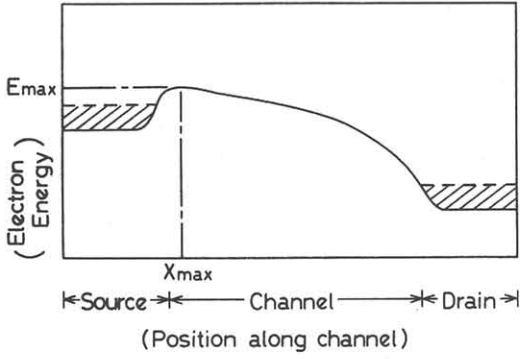


Fig.2 Electronic energy distribution along the channel. It is defined as that of conduction band energy minimum.

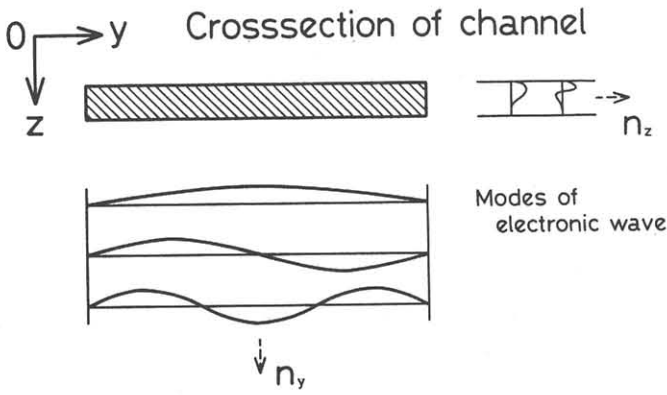


Fig.3 Electronic states in the channel form subbands and are specified with Quantum numbers n_y and n_z .

ber of one-dimensional subbands propagating in x -direction along the channel, each specified by a pair of quantum numbers n_y and n_z showing the wave modes along the y and z direction. The electronic current consists of subband components, each of which is the product of carrier group velocity, density of states and an occupancy probability factor expressed with the Fermi distribution function all integrated over electron energy. The product of group velocity and density of states gives a constant as in Landauer's formula. Summation Over subbands consist of those over n_y , n_z and also contributing valleys. The summation over n_y is substituted for integration over energy when the channel width is not excessively small. The current is evaluated as,

$$I = W \frac{\sqrt{2}q(kT)^{3/2}}{\pi^2 \hbar^2} \sum_v \sum_{n_z} \sqrt{m_y} \left\{ F \left(\frac{\phi_{FS} - E_{n_z}}{kT} \right) - F \left(\frac{\phi_{FS} - E_{n_z} - qV_D}{kT} \right) \right\} \quad (1)$$

$$F(u) = \int_0^\infty \frac{\sqrt{y}}{1 + e^{(y-u)}} dy \quad (2)$$

W is the channel width, m_y is the effective mass in y direction and $(\phi_{FS} - E_{n_z})$ is the energy difference between the source Fermi level and the energy level associated with n_z . $F(u)$ is the Fermi-Dirac integral. Contribution from evanescent modes is neglected. Charge of mobile carriers $|Q|$ at the potential maximum is also evaluated in a similar way. It consists of two components each summed up over subbands; one is from electrons moving from source to drain and distributed with source Fermi level and the other from those moving from drain to source and distributed with drain Fermi level. $|Q|$ is evaluated as,

$$|Q| = \frac{qkT}{2\pi\hbar^2} \sum_v \sum_{n_z} \sqrt{m_x m_y} \ln \left\{ 1 + \exp \left(\frac{\phi_{FS} - E_{n_z}}{kT} \right) \right\} \times \left\{ 1 + \exp \left(\frac{\phi_{FS} - E_{n_z} - qV_D}{kT} \right) \right\} \quad (3)$$

In strong inversion condition, $|Q|$ is expressed with the usual threshold voltage approximation as,

$$|Q| = C_{eff}(V_G - V_T) \quad (4)$$

where, C_{eff} is the effective capacitance, and V_G and V_T are respectively the gate voltage and the threshold voltage. The validity of this expression should be examined under a very small MOFET environment and low temperature condition. The above expression can be derived by an approximation around the potential maximum, with the capacitance expression

$$C_{eff} = \left(\frac{t_{ox}}{\epsilon_{ox}} + \frac{\langle z \rangle}{2\epsilon_s} \right)^{-1} \quad (5)$$

where t_{ox} is the oxide thickness, ϵ_{ox} and ϵ_s are dielectric constants associated with oxide and Si, and $\langle z \rangle$ is the average spacing between the MOS interface and the center of charge distribution.

As for summations over valley and n_z in Eqs.(1) and (3), for (100) interface, the dominant contribution comes from two lowest levels belonging to two heavy mass valleys. We can substitute these summations for a multiplication factor M_v giving the effective number of contributing valleys and levels, at the same time setting E_{n_z} at the lowest level. Fraction of population in lowest level is supposed to be around 0.8 [4] at 77K in heavily inverted MOS junction, and we put $M_v = 2(1 + 0.2/0.8) = 2.5$.

Combining Eqs.(1),(2),(3) and (4), we get the closed expression of I in term of terminal voltages V_G and V_D .

$$I = W \frac{\sqrt{2q}(kT)^{3/2}}{\pi^2 \hbar^2} M_v \sqrt{m_t} \{F(u) - F(u - v_d)\} \quad (6)$$

$$v_d = \frac{qV_D}{kT} \quad \rho = \frac{2\pi \hbar^2 C_{eff}(V_G - V_T)}{qkTm_tM_v}$$

$u = \ln\{\sqrt{(1 + e^{v_d})^2 + 4e^{v_d}(e^\rho - 1)} - (1 + e^{v_d})\} - \ln 2$
 where, m_t is the electron transverse effective mass.

3 Result and Discussion

We can depict some points characteristic to ballistic operation. The current does not depend on channel length L . It is expressed with elementary parameters like q , \hbar , T , effective mass, etc, and is independent on carrier mobility.

Examples of the evaluated $I - V$ characteristics are illustrated in Figs.4 and 5. Note that the current saturation characteristics are naturally derived in accordance with the conventional MOSFET. This is because V_D dependence is due to the current component flowing from drain to source expressed by the second term in $\{ \}$ of Eq.(1), which becomes negligibly small as the Fermi level of drain goes far below the potential maximum in the channel. In heavily inverted condition ($\rho \geq 1$), function $F(u)$ can be approximated by an analytical expression,

$$F(u) = \frac{2}{3}u^{3/2} \quad (7)$$

and the saturation current is evaluated as

$$I = \frac{8}{3}W \frac{\hbar \{C_{eff}(V_G - V_T)\}^{3/2}}{m_t \sqrt{q\pi M_v}} \quad (8)$$

This value is independent of temperature because carriers are degenerate. It is proportional to carrier density to the 1.5-th power. This is compared with the case of normal MOSFET where it is proportional to the square of carrier density, and the case of velocity saturated MOSFET where it is directly proportional to carrier density.

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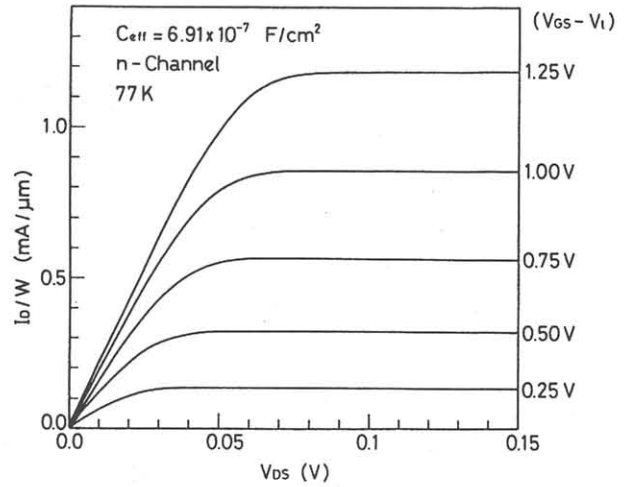


Fig.4 Calculated $I_D - V_D$ characteristics of a unit width n-channel ballistic SOI MOSFET at 77K. C_{eff} corresponds to effective 5nm oxide thickness.

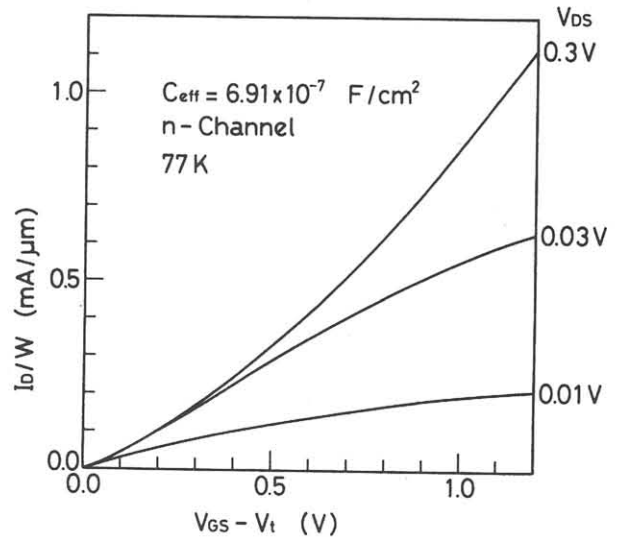


Fig.5 $I_D - V_G$ characteristics of the device of Fig.4. $V_G = 0.3V$ is in the region of current saturation.

References

- [1] G.A.Sai-Halasz et al.:IEEE Electron Device Lett.,EDL-9,pp.464(1988).
- [2] T.Hashimoto et al.:Ext.Abs. Int.Conf.Solid State Devices and Materials,pp.490(1992).
- [3] D.J.Frank et al.:IEDM Tech.Dig.,IEDM 92-553(1992).
- [4] F.Stern:Phys.Rev.B.,vol.5,pp.4891(1972).