

Effect of Ultrathin Si Passivation Layer for La₂O₃/Ge MOS structure

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Germanium (Ge) has drawn lots of attention for alternative channel materials of metal-oxide-semiconductor field-effect transistor (MOSFET) thanks to its high carrier mobility. The technology generation using Ge channel will require very small equivalent oxide thickness (EOT). Therefore, high dielectric constant (high-k) materials are considered as gate dielectric of Ge MOS devices. Among many high-k materials, La₂O₃, one of the rare earth oxides, is more attractive compared with other high-k materials in terms of high dielectric constant and large band-gap [1]. On the other hand, it seems difficult to achieve satisfactory property in direct formation of high-k on Ge substrate, and better characteristics have been obtained with passivation layer such as GeON, Ge₃N₄ and Si on Ge substrate [2-4]. In this work, we studied the effects of ultrathin Si passivation layer on Ge substrate in La₂O₃/Ge MOS structure.

Chemically cleaned n-type Ge(100) wafers were transferred into an ultrahigh-vacuum (UHV) chamber (~10⁻⁸ Pa) and annealed at 500°C to remove the Ge oxide completely. After that, ultrathin Si layer and La₂O₃ films were deposited by electron-beam evaporation under pressure of ~1×10⁻⁶ Pa. Tungsten (W) films were deposited *in situ* to avoid moisture absorption of La₂O₃ from air. Gate-electrode patterns were defined by lithography and reactive ion etching (RIE) using SF₆ chemistry. Then, the post-metallization annealing (PMA) was carried out using a rapid thermal annealing (RTA) furnace.

Figure 1 shows C-V characteristics of W/La₂O₃/Ge MOS capacitors with or without Si passivation layer on Ge substrate. The initial thickness of Si passivation layer without PMA is about 1.5 nm as can be seen in Fig. 2. As shown in Fig. 1, the amount of hysteresis on C-V curve significantly decreased with Si passivation layer of 1.5nm. In the La₂O₃/Ge stack, a large amount of hysteresis is considered to be caused by the growth of a Ge sub-oxide layer [5]. Therefore, the suppression of Ge sub-oxide growth by the Si layer over 1nm would reduce the hysteresis of La₂O₃/Ge system, as is indicated in Fig. 3. Figure 4 shows PMA-temperature dependence of (a) hysteresis and (b) capacitance equivalent thickness (CET) for W/La₂O₃/Ge structures with or without a Si layer. The results for the same layers on a Si substrate are also shown as references. The sample with a Si layer on a Ge substrate exhibited almost the same characteristics as those of the reference sample using a Si substrate. Hysteresis reduction and CET increment by 500 °C PMA in La₂O₃/Si structures are considered to be due to the formation of an interfacial La-silicate layer [6].

The effect of ultrathin Si passivation layer on Ge MOS characteristics with La₂O₃ gate dielectric has been examined. C-V hysteresis has been significantly reduced by inserting an ultrathin Si passivation layer due to suppression of Ge sub-oxide growth and formation of the La-silicate layer.

Reference

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[5] J. Song et al., Microelec. Eng., **84**, 2336 (2007). [6] K. Tachi et. al., ECS Trans., **3**, 425 (2006).

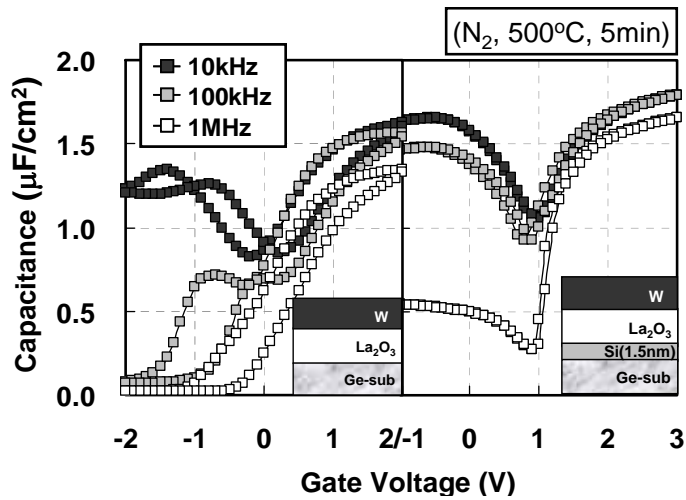


Figure 1. C-V characteristics of W/La₂O₃/Ge MOS capacitors with or without Si passivation layer on Ge substrate.

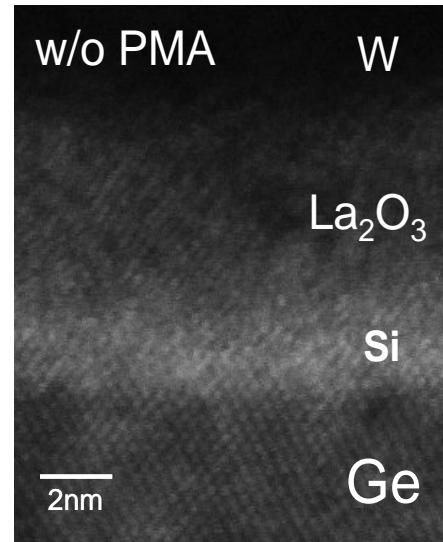


Figure 2. Cross-sectional TEM image of the capacitor with 1.5-nm-thick Si passivation layer obtained for as-deposited condition.

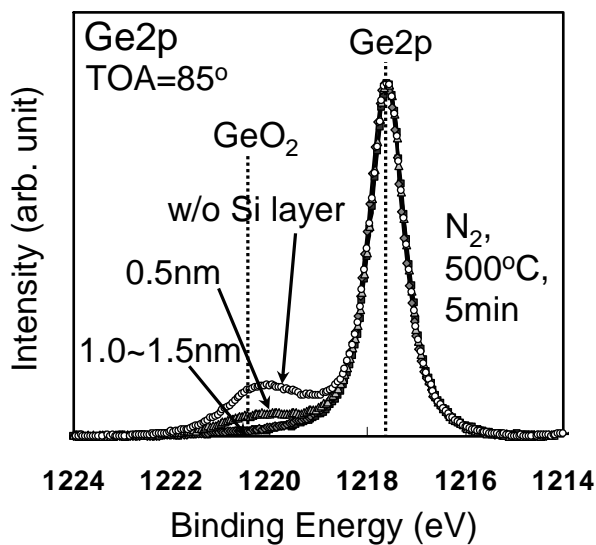


Figure 3. Ge2p spectra of XPS measurement in La₂O₃/Ge system with Si passivation layer of 0-1.5 nm. PMA was performed in N₂ at 500°C for 5minutes.

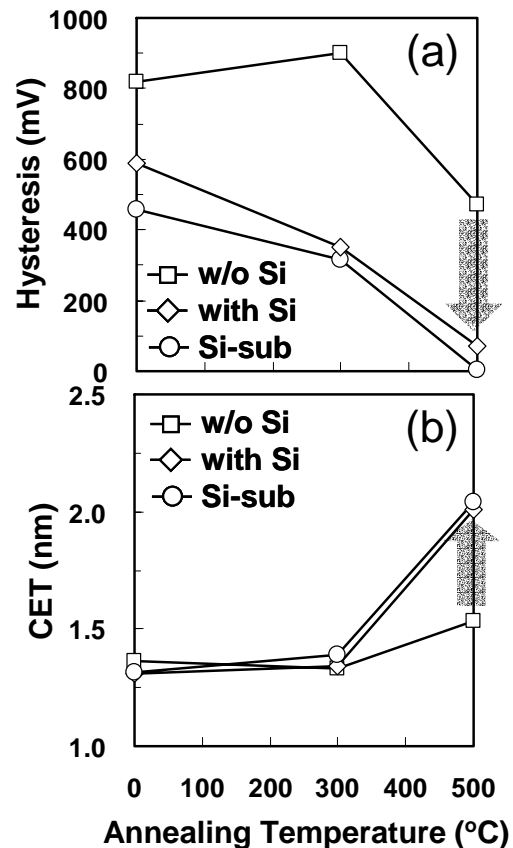


Figure 4. PMA temperature dependence of (a) hysteresis and (b) CET of W/La₂O₃/Ge structures with or without Si layer. Those of W/La₂O₃/Si structure are also shown.