Evaluation of Channel Potential Profile of Si Nanowire Field Effect Transistor

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Abstract

Electrical potential profile of Si nanowire (NW) FET was experimentally characterized using four-terminal measurement transistor. Obtained electrical potential profile is similar to that of bulk planar MOSFET, which indicates that this transistor is a promising methodology for determination of the electrical potential profile of Si NW FET.

Introduction

Operation of the MOSFET is determined by its lateral electrical potential profile of electrons and holes transported in its channel. The electrical potential profile of planar bulk MOSFET is obtained by theoretical calculation [1] and schematically illustrated [2]. On the other hand, electrical potential profile of Si nanowire (NW) FET can be thought to be different from the planar bulk MOSFET, which originates in difference between 2DEG and quasi-1D structure. In order to obtain the potential of Si NW FET, a four-terminal measurement transistor was designed and fabricated.

Device Fabrication [3]

A schematic fabrication process is shown in figure 1. 300mm – diameter SOI wafer, whose thickness of SOI layer and BOX layer is 61nm and 145nm, respectively. A Si fin patterns are formed through lithography and dry etching process, followed by sacrificial oxidation in 1000 ^{o}C for one hour in dry oxygen ambient. Then sacrificial oxide was partially removed by wet etching process (fig. 2). Poly-Si / SiO_2 gate stack was formed and gate electrode was patterned (fig. 3). After SiN sidewall formation, Ni SALICIDE process was conducted to reduce parasitic resistance of source/drain region.

Results and Discussion [4]

During I_dV_g measurement, applied voltage of terminal 1 and 2 were measured using Agilent 4156C semiconductor parameter analyzer. Based on the model (figs. 5 and 6), the electrical potential profile, in this case a quasi-Fermi potential of electron, is determined. (figs. 7 and 8) This result coincides well with bulk planar MOSFET because cross-sectional dimensions of NW in this work is large not enough for appearance of quantum-mechanical effects.

Conclusion

The electrical potential profile of Si NW FET is obtained experimentally, which assure this methodology is effective for analysis of electrical potential profile of FET.

Reference

[1] R. Troutman, *IEEE Trans. Electron Devices.*, (1979) 461.
[2] S. M. Sze, K. Ng, Physics of Semiconductor Devices 3rd edition, Wiley-Interscience, 2007.
[3] S. Sato, et. al., ESSDERC 2009 Technical Digests of Papers, *to be published.*
[4] S. Sato, et. al., JSAP Spring Meeting 2009 (1a-V-5).

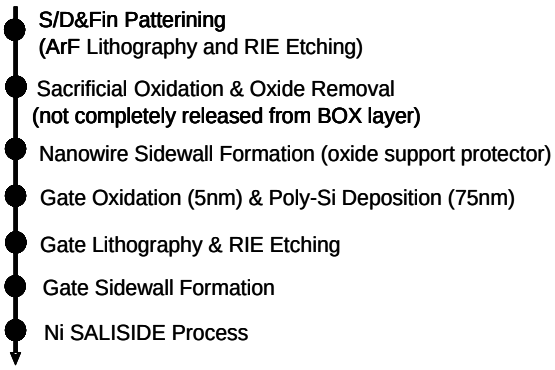

Figure 1. Schematic process flow of Si NW FET

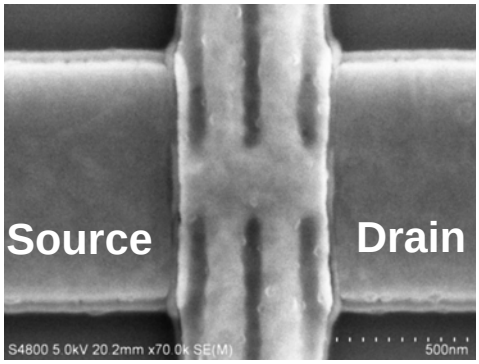

Figure 3. A SEM image after gate pattering and SALICIDE.

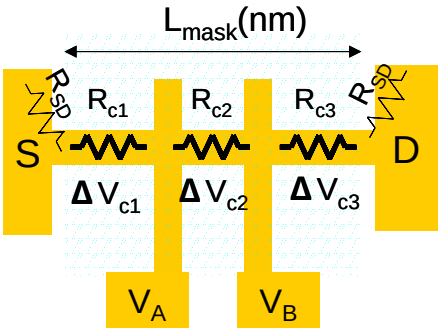

Figure 5. Analysis model of four-terminal measurement transistor.

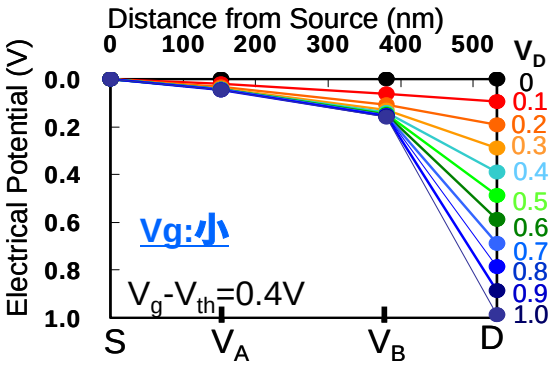

Figure 7. Obtained potential profile at low V_g.

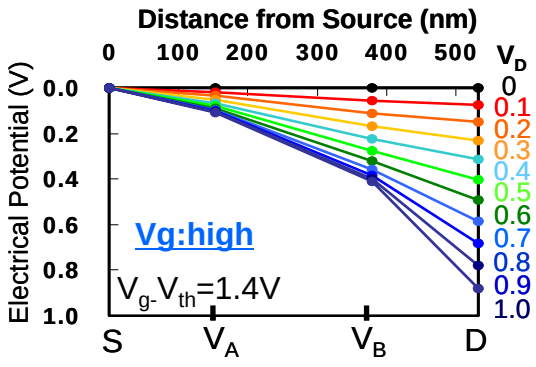

Figure 8. Obtained potential profile at high V_g.

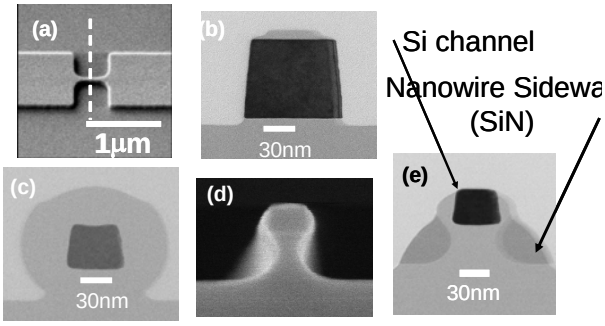

Figure 2. SEM images of (a) patterned fin and XTEM images of (b) Si fin, (c) fin after sacrificial oxidation, (d) after oxide removal and (e) nanowire sidewall formation.

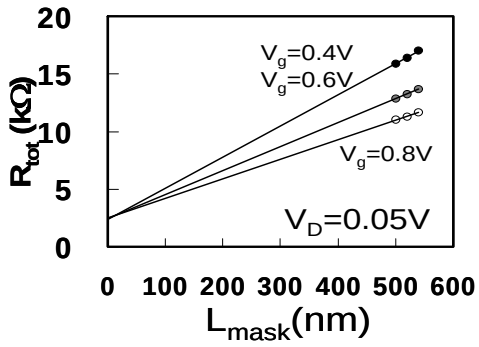

Figure 4. Parasitic resistance extraction by standard method. (R_{SD}=0.7kΩ)

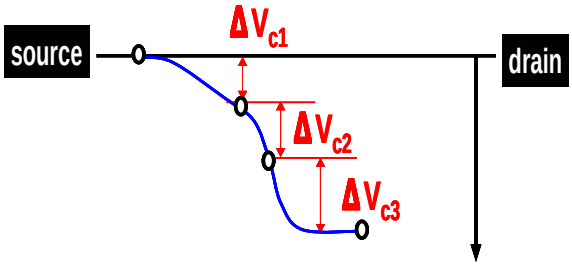

Figure 6. Potential profile model of Si NW FET in this work.