Experimental Investigation of V_{FB} shift and Effective Mobility in La_2O_3 MOS Devices

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1. Introduction

Integration of Metal gate with High-k gate dielectrics is crucial to improve the performance of CMOSFET. Although SiO_x-based interfacial layer is typically inserted or regrown to suppress the performance degradation in MOSFETs with Hf-based gate dielectrics [1], there exists a limitation for further scaling. It is required that high-k gate dielectrics should be directly in contact with Si substrate without any SiO_x interfacial layer [2]. We focus on La_2O_3 as a gate dielectric to achieve a structure without any SiO_x interfacial layer, and La-Silicate layer is formed after annealing instead of SiO_x interfacial layer [3]. In this paper, we experimentally clarified the issue of La_2O_3 gate dielectrics.

2. Experiment

La_2O_3 was deposited on a HF-last n-Si wafer ($N_{sub} = 3x10^{15}$ cm^{-3}) for MOS-Capacitor and source and drain pre-formed p-Si wafer ($N_{sub} = 3x10^{16}$ cm^{-3}). Metal gate electrode was formed by RF sputtering without breaking ultra-high vacuum to avoid any contamination. The samples were post-metallization annealed in forming gas ambient (H_2:N_2=3%:97%) for 30min. Al was deposited on the source/drain region and back side of the substrate as a contact. Effective mobility was measured by Split-CV method [4]. The interface state density was measured by charge pumping method [5].

3. Results and Discussion

It was reported that V_{FB}/V_{TH} of High-k gate MOS devices vary considerably in that of conventional Poly-Si/SiO_2 structure [6]. Thus, it is indispensable to understand the V_{FB} shift in La_2O_3 gate capacitor. **Fig.1** shows the EOT-V_{FB} plots of La_2O_3 MOS-Capacitor with different metal gates and compares the V_{FB} of SiO_2 MOS-Capacitors. Effective work function (EFW) can be estimated form intercept of EOT-V_{FB} plots [6]. Comparing to the SiO_2 MOS-Capacitors, reduction of EFW on La_2O_3 gate dielectrics is clearly observed. Our group reported the presence of potential shift at La_2O_3/Si interface by XPS measurement and the amount of potential shift is about -0.46V [7]. As the V_{FB} shift attributed to the fixed charge in La_2O_3 corresponds to about -0.1V, the reduction of EFW of W/La_2O_3 is mainly due to the potential shift at La_2O_3/Si interface. In the case of TaSi gate, the EFW is dramatically reduced comparing to the SiO_2 MOS-Capacitors. It is reported that the potential shift at Si-based gate and High-k interface only occur [6]. **Fig.2** shows the schematics of potential shift in metal and Si-based gates. These potential shifts at both top and bottom interface well coincide with other previous report [6]. Thus, we must consider the influence of potential shift when adjusting the V_{TH} of La_2O_3 gate MOS devices. Effective mobility is one of the most important factors for MOSFET performance. Therefore, to understand what extent fixed charges in the High-k dielectrics or high interface state density at High-k/Si interface affect to the effective mobility is crucially important. **Fig.3** shows the EOT-V_{FB} plots of W/La_2O_3 MOS-Capacitor with various annealing temperature and change of slope can be observed. The slope of EOT-V_{FB} plots represents the fixed charges in dielectrics and steep slope correspond to large amount of fixed charges in dielectrics. The slope is converted from positive to negative after high temperature annealing. **Fig.4** shows the XPS Si 1s spectrum as a function of annealing temperature. Increase of La-silicate can be observed after high temperature annealing. Thus, it seems that increase of La-silicate plays a role to generate the positive fixed charges. Co-existent of both positive and negative charges in La_2O_3 dielectrics makes it difficult to estimate the amount of fixed charges because V_{FB} shift contain the influence of both positive and negative charges. **Fig. 5** shows the effective mobility as a function of EOT. **Fig. 6** shows the charge pumping measurement as a function of annealing temperature. Although fixed charges or interface states are small in high-temperature annealed devices, effective mobility is almost identical. Moreover, effective mobility reduced with decreasing the EOT, which implies that the metal/high-k top interface affects the mobility reduction [8].

4. Conclusion

We experimentally investigate the electrical characteristics with La_2O_3 gate MOS devices. The reduction of EWF can be explained by potential shift and quantitatively coincide with XPS measurement. We also show the difficulty of accurate estimation of fixed charges in La_2O_3 gate dielectrics. Continuous investigation is required for understanding the mobility degradation.

Reference

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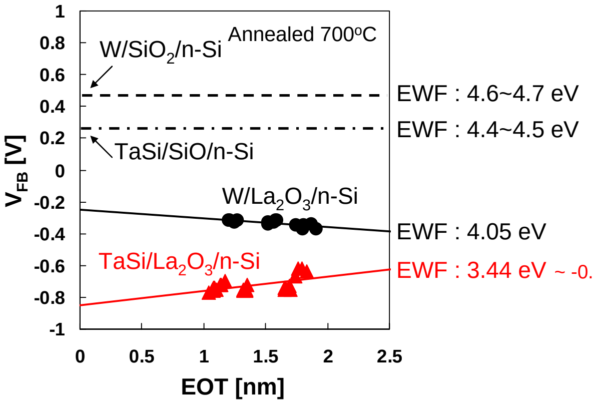

Fig.1 EOT-V_{FB} plots with different metal gates.

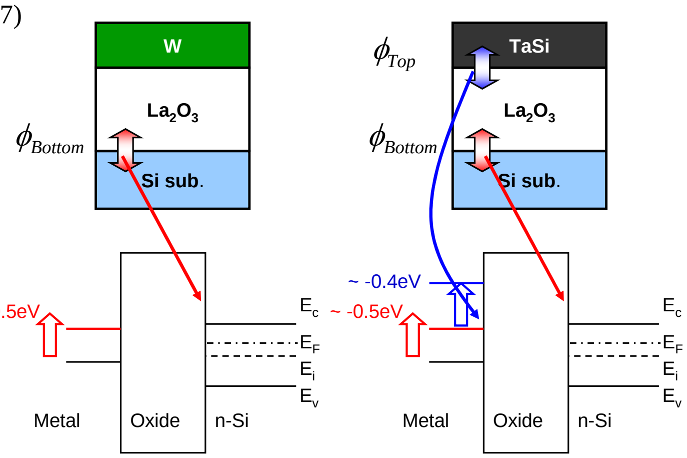

Fig.2 Schematics of potential shift.

Potential shift is incorporated in effective work function.

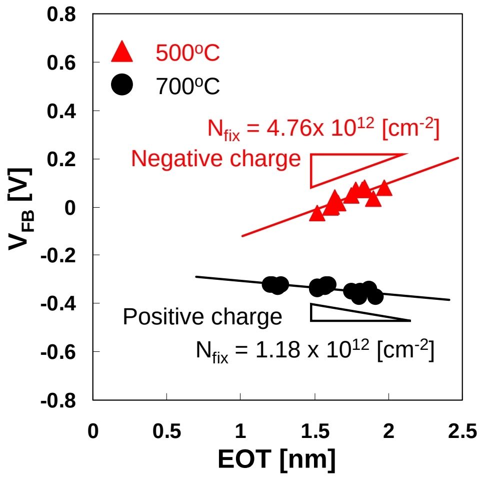

Fig.3 EOT-V_{FB} plots as a function of annealing temperature.

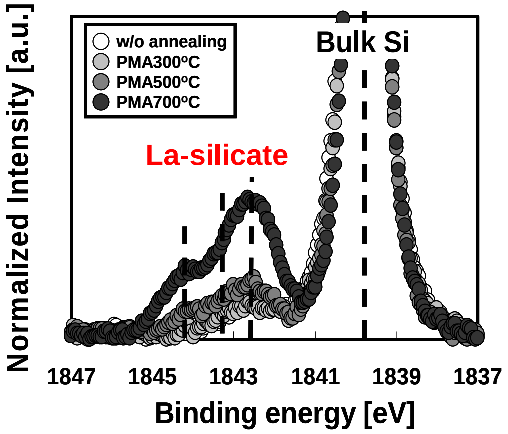

Fig.4 XPS Si1s spectrum.

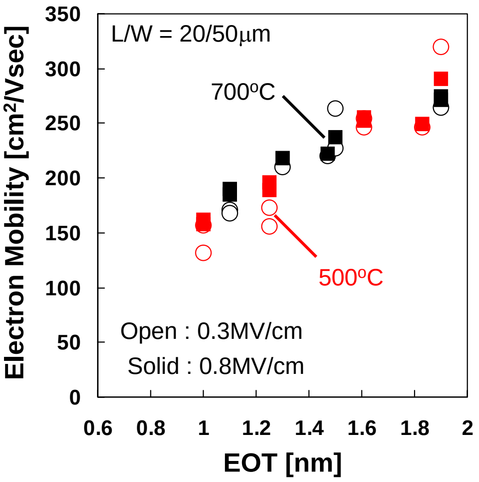

Fig.5 Effective mobility as a function of EOT.

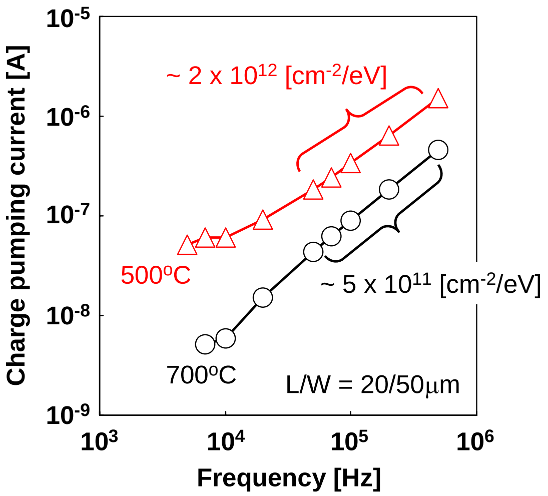

Fig.6 Charge pumping measurement.