Miniaturization and future prospects of Si devices

Hiroshi Iwai
Frontier Research Center, Tokyo Institute of Technology
4259, Nagatsuta, Midori-ku, Yokohama 226-8502, Japan

The down-scaling of MOSFETs has been the most important and effective way for achieving the high performance and low power consumption for LSIs, and thus, the shrinking trends of the MOSFETs has been kept for many years by all means in spite of so many past pessimistic predictions for the downsizing limit. In fact, the downsizing limit of the gate length was thought to 1 um in 1970's, however, now, the limit is believed to be about 5 nm, or 0.005 um. One of the current bottlenecks for the downsizing is the thinning of the gate oxides, and this can be solved by the introduction of new materials. In 2007, Intel introduced HfO_2 based high-k gate insulator for thinning the equivalent gate oxide thickness (EOT) to 1 nm. However, HfO_2 based high-k requires an SiO_2-rich thin interfacial layer on the Si substrate in order to maintain the good electrical characteristics of MOSFETs, and thus, the quest for further new materials, such as rare earth oxides, are important to realize the direct contact between the high-k and Si substrate (Fig.1). In the ITRS roadmap, the EOT has been believed to reach its limit at 0.5 nm (Fig.2). Recently, however, we have demonstrated that good MOSFETs operation at EOT=0.37 nm with the merit of current drive increase [1] (Fig.3). This is just an example of the breakthrough for the downsizing limit, and future bottlenecks will be solved by introduction of various new materials into Si-MOSFETs as well as new structures such as 3D.

The MOSFET downsizing will encounter its downsizing limit sometime in 2020-2030 around the gate length of 5 nm [2]. Probably we will have 6 more generation until then. Two types of MOSFET technologies have been recently recognized as the emerging device technologies which will replace current planer bulk CMOS [3]. They are the Si-nanowire FET and the alternative channel (such as GaAs and Ge) FET (Figs.4 and 5). They are quite different from the current planar type Si CMOS devices, in terms of structure and material, respectively. Considering the compatibility with current Si CMOS process technologies, Si-nanowire FETs will be introduce first and then, alternative channel will be next. However, both of the Si-nanowire and alternative channel will be keys for future solution for the downsizing as well as the rare earth high-technologies.

Ref: [1] K. Kakushima et al., IWDTF 2008,
[2] H. Iwai, IWJT 2008
[3] H. Iwai, INFOS 2009

This work was partially supported by NEDO and JST

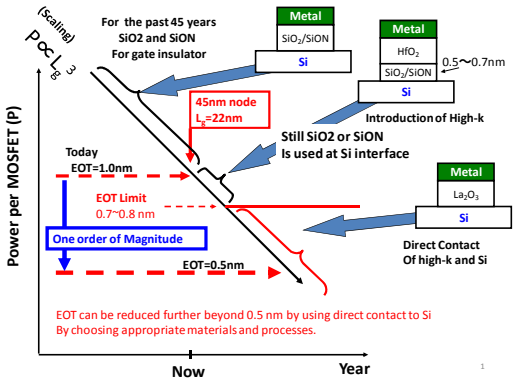


Fig.1 High-k technology scheme beyond EOT=0.5 nm

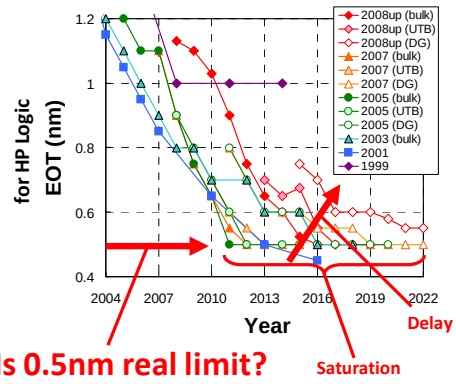


Fig.2 ITRS predictions for EOT

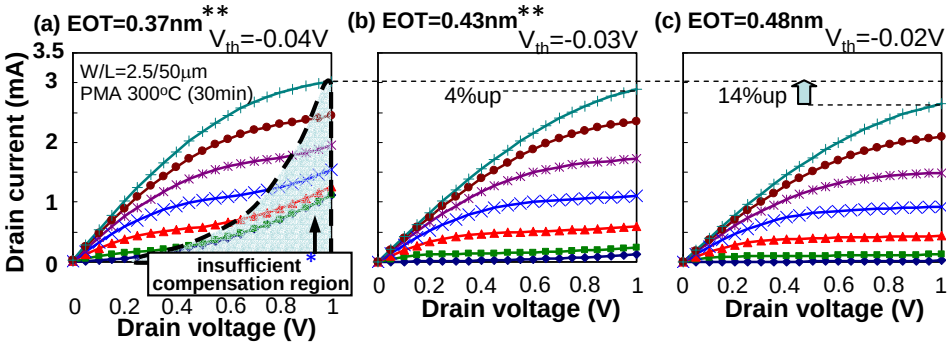


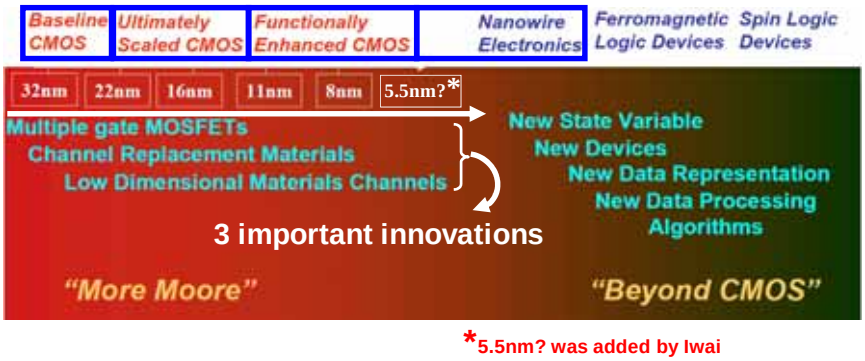
Fig.3 La_2O_3 High-k MOSFETs beyond EOT=0.5 nm

-Two candidates have emerged for R & D

1. Si-Nanowire MOSFETs

2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.



*5.5nm? was added by Iwai

Fig.4 Two key technologies towards the downsizing limit in 20 years

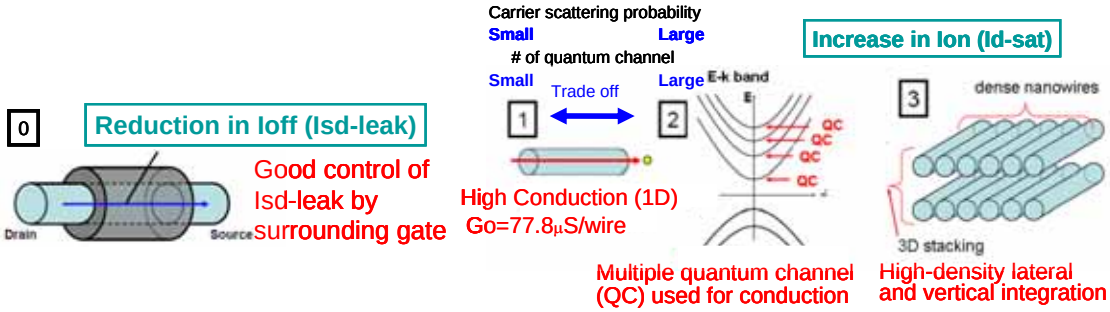


Fig.5 Merits of Si nanowire FET