A Study of Schottky Barrier Height Modulation of NiSi by Interlayer Insertion and Its Application to SOI SB-MOSFETs

W.Hosoda[1] K.Ozawa[1] K.Kakushima[2] P.Ahmet[1] K.tsutsui [2] A.Nishiyama[2] N.Sugii[2] K.Natori[1] T.Hattori[1] and H.Iwai [1]FRC Tokyo Institute of Technology[1],
4259-S2-20, Nagatsuta-cho, Midori-ku, Yokohama 226-8503, Japan
Tel: +81-45-924-5847 Fax: +81-45-924-5846 IGSSE, Tokyo Institute of Technology[2],

ABSTRACT

We investigated the modulation of Schottky barrier height (Φ_b) by inserting Er layer between Si (100) substrate and Ni layer before the silicidation annealing. Φ_b for electrons of NiSi was decreased by inserting an Er layer. We applied the technology to SOI SB-MOSFET and confirmed increasing drain current by using barrier height modulation.

INTRODUCTION

The Schottky barrier source/drain MOSFET (SB-MOSFET) is one of the promising candidates for next generation devices, thanks to its shallow junction depth with lower electrode resistance and process temperature [1-2]. However, the high barrier height (Φ_b) severely limits the drive current of SB-MOSFETs [3-4]. The Er silicide has been proposed for SB-NMOS because of very low Φ_b of 0.27-0.36 eV for electrons [5]. However, the reports of middle gap materials such as NiSi also showed the great possibility of these materials for applications of the SB-MOSFET by employing the Φ_b modulation techniques [3].In this work, we investigated Φ_b modulation of Ni silicide by inserting an Er interlayer at the Ni/Si interface before silicidation, and applied the technique to n-cannel SOI SB-MOSFETs fabrications.

EXPERIMENTAL DETAILS

Schottky diode was formed on SiO_2 isolated and p-type bulk (100) Si wafers. The patterned wafers were cleaned in mixed solution of H_2SO_4 and H_2O_2 followed by chemical oxide removal by diluted HF. Pure metals of Er and Ni were deposited subsequently on to the substrates by DC sputtering in Ar gas at a pressure of 5.5×10^{-1} Pa. The layered structures of Ni/Er/Si consisting of 12-nm-thick Ni layer and Er layer of various thicknesses ranging from 3.6 to 12 nm were deposited. The samples were annealed in forming gas (3% H_2 + 97% N_2) at various temperatures from 400^{o}C to 700^{o}C for 1 min. After the removal of un-reacted metals by chemical etching, Al back contacts were formed. A fabrication process of n-channel back gate type SOI SB-MOSFETs is shown in Fig. 2. 200-nm-thick BOX layer and 100-nm-thick SOI layer pre-formed p-Si substrates were used in this work. Active regions were patterned by lithography and reactive ion etching. Channel regions were covered with 100-nm-thick thermal-oxide layer formed by Dry oxidation in O_2 at 1100^{o}C for 30min. Then, 12nm-Ni/7.2nm-Er layers or 12nm-Ni layers were deposited and annealed at 600^{o}C for 1 minute. After the un-reacted metals were etched, an Al back contact was formed. Finally, annealing in FG at 420^{o}C for 30 minutes was carried out.

RESULTS

The Φ_b values evaluated from the *I-V* corves in the forward bias region are plotted as a function of the Er thickness as shown in Fig. 1. It was found that the insertion of 12-nm-thick Er followed by annealing at 500^{o}C increased the Φ_b for holes by 0.18eV. It means Φ_b for electrons was lowered. Fig. 3 shows I_d-V_d characteristics of the fabricated n-channel Ni silicide SOI SB-MOSFETs**.** I_d was increased about 60% in the case of Er insertion. As stated above, the Φ_b value for electrons was lowered, so the drain current increased.

CONCLUSION

The Φ_b modulation of Ni silicide on Si by the Er interlayer was investigated. We found that the Φ_b for electrons was lowed by 0.18eV, by using this technique. We used the technology to SOI SB-MOSFETs and confirmed increasing of the drain current.

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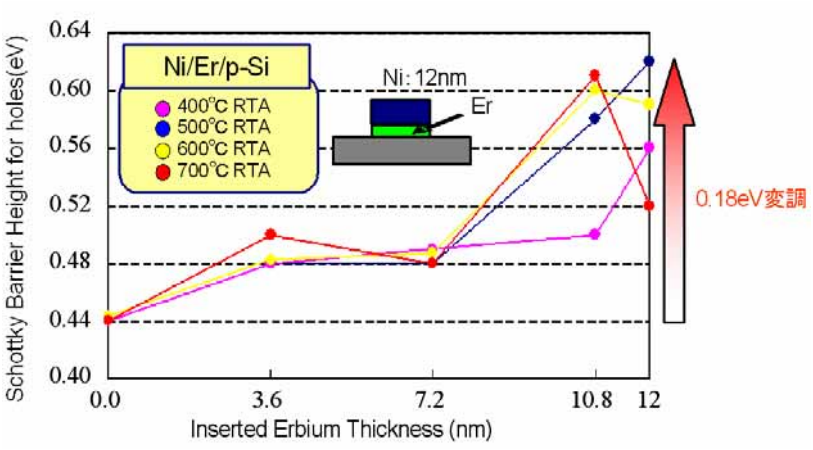

Fig. 1 Schottky barrier height for holes depending on thickness of Er interlayer after rapid thermal annealing at various temperatures.

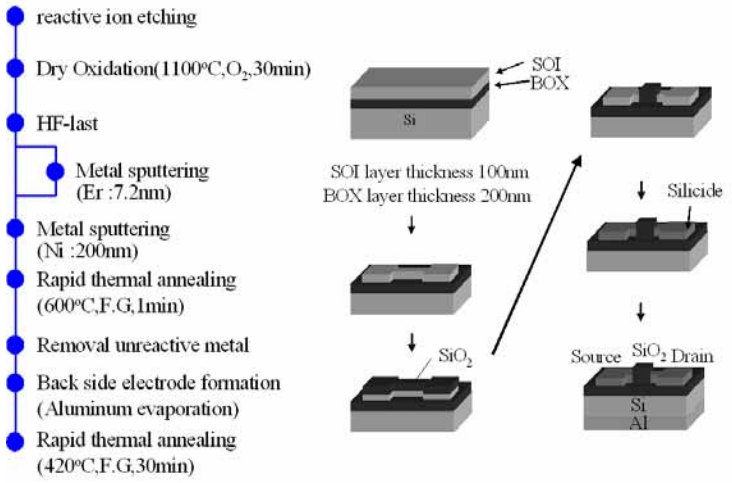

Fig. 2 Fabrication process of back gate type N-ch. SOI SB-MOSFETs.

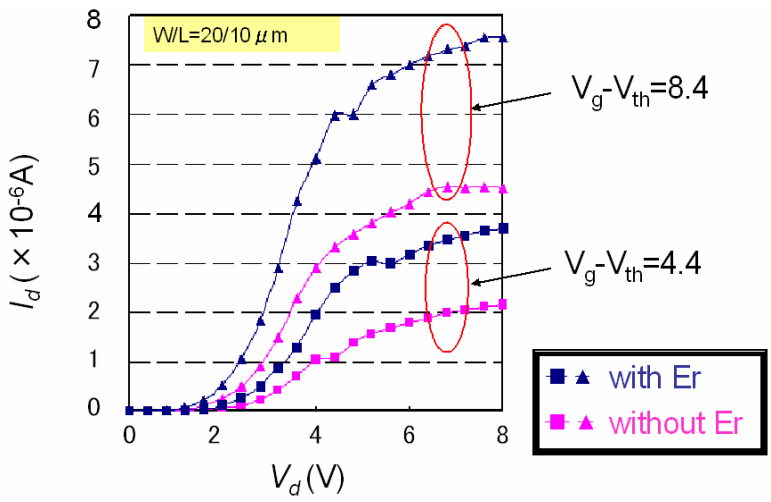

Fig.3 I_d-V_d characteristics of the N-ch. SOI SB-MOSFETs**.**